# Fred Owens

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## EDUCATION

**Purdue University, West Lafayette, IN** **2020**
**Bachelor of Science, Computer Engineering** **GPA: 3.77**

- Relevant coursework: Microprocessor Systems and Interfacing, Advanced C Programming, Computer Architecture, Data Structures, Operating Systems, Object-Oriented Programming, ASIC Design, Artificial Intelligence

## SKILLS

- C, C++, Python, Java
- STM32, STM32Cube, Eclipse, ARM Cortex M-0, MIPS, RTOS
- Git, Linux, Unix, Bash, Tcl, Excel, MATLAB
- USB, UART, SPI, I2C, GPIO, JTAG

## EXPERIENCE

**STEM Teacher** **Sep 2021-Present**
C2 Education Cupertino, CA

- Instructed high-achieving high school/college students on AP Physics, AP Calculus, C Programming, and Java in a fast-paced 3:1 setting
- Increased SAT scores of high school students by identifying and teaching math weaknesses

**Digital Design Engineer** **June 2020-Aug 2021**
Texas Instruments Santa Clara, CA

- Developed object-oriented SystemVerilog test benches for design verification of two ~17 million transistor FPD-Link IV deserializers used in automotive display systems
- Designed, coordinated design reviews for, and implemented Finite-State-Machine in SystemVerilog to achieve backwards compatibility with legacy chips already in the field
- Coordinated register map code and documentation across analog and digital teams
- Led and coordinated Clock-Domain-Crossing checks, debug, and sign-off for chip tape-outs
- Updated tape-out signoff flow to new Cadence tools, and trained colleagues on their use
- Developed python and tcl scripts to automate repetitive work
- Used version control software to maintain code consistency across a large codebase

**Digital Design Engineer Intern** **May 2019-Aug 2019**
Texas Instruments Federal Way, WA

- Developed python scripts and GUIs for TICS Pro, an applications software used for end-user device register programming of phase-locked loops and clocking devices
- Designed SystemVerilog test benches for design verification of digital phase-lock loops

**Industrial Automation Intern** **May 2018-July 2018**
Glenmount Global Solutions Portage, IN

- Converted outdated ladder logic for use in updated PLCs (Programmable Logic Controllers)

## PROJECTS

**March Madness Bracket Optimizer (C/Python)**

- Programmed STM32F0 microcontroller to calculate optimal final four picks for given pool

**Maze-Solving Logic Game (C)**

- Used STM32F0 with bare-metal ADC, DAC, GPIO, and SPI drivers to play maze-solving game

**Pipelined MIPS Processor with Caches (SystemVerilog)**

- Designed and verified pipelined MIPS processor in SystemVerilog from scratch