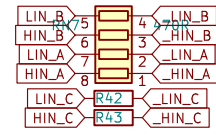
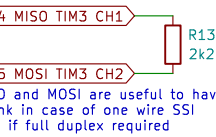
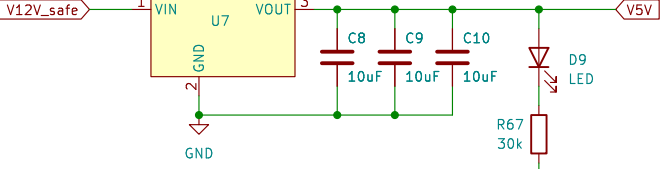
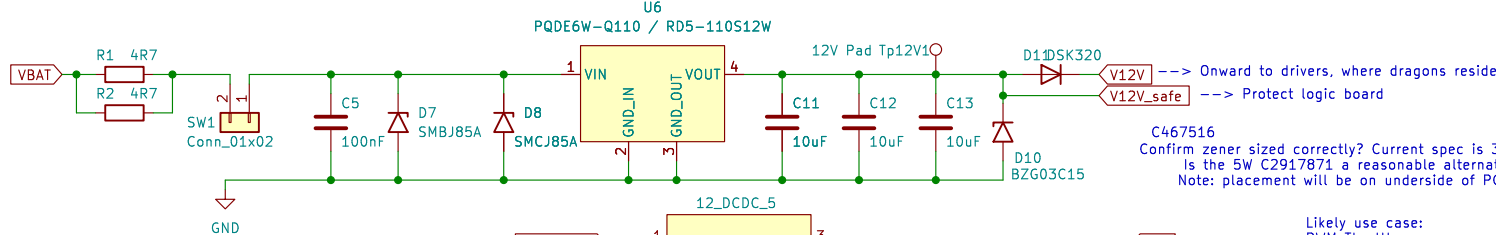
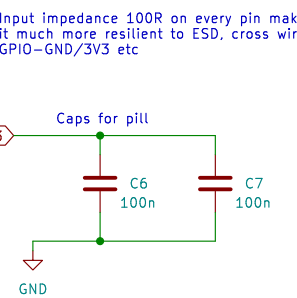
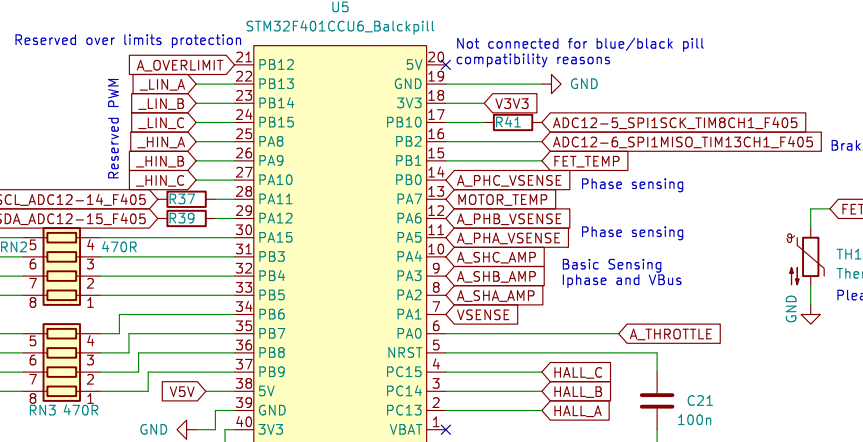


Footprint for CUI isolated module for up to 160V operation.
Only allows 500mA.
HiLink HLK-10D11012
CUI PQDE6W-Q110

Or anything that exceeds your battery voltage and gives 12V out



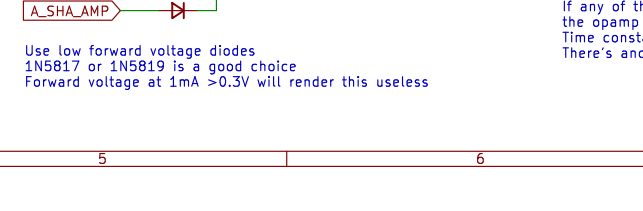
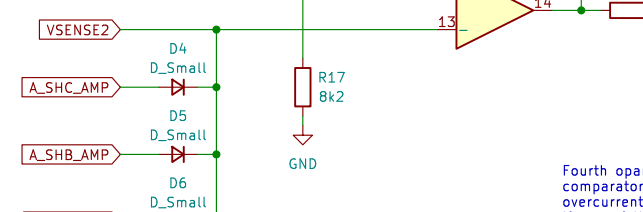
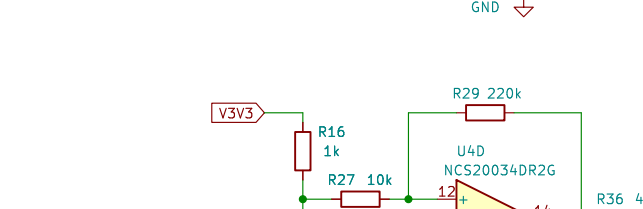
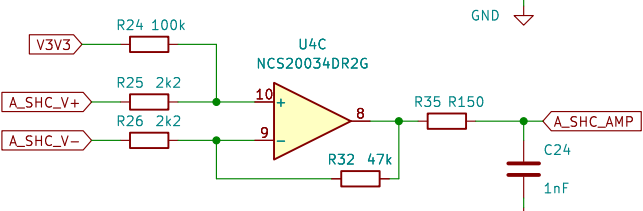
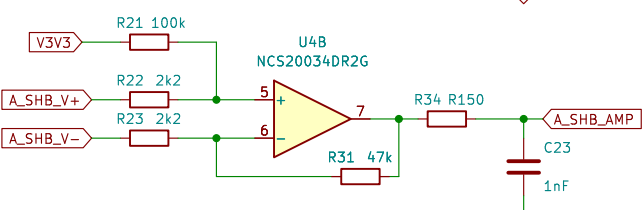
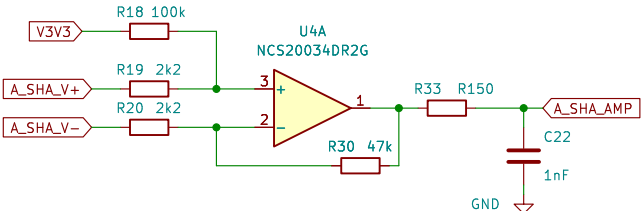
The "Pill" is chosen as a generic STM32 module that should allow easy compatibility with multiple firmwares:
VESC with GD32F303CG pill (Netzpfuscher mod, note C6)
VESC with STM32F405 pill (Dwhite) (github.com/davidmalony/F405_pill)
EBICS with F103 Bluepill (Stancecoke)
SmartESC V3 (Casalino)
SmartESC V2 (Netzpfuscher/Koxx3)
MESC with F401 Blackpill (MxlemmingFOC)
STM32 Motor Control Workbench (F401, F103)
Maybe others?
Pills are simply boards with an MCU, a regulator, USB and Boot0 button.



MP2-DFN PUNCHLIST:

Clean / uninterrupted VBus and GND layers
Restructured vbat and gnd buses for copper bus bars
Restructured phase buses
Differential lines for shunt resistors
Heatsink mounting holes
Different lines for (DRVH with HB) (DRV + GND)
MOSFETS changed to DFNW format (NVMTC4D3N15MC)
Added gate to source 4.7nF capacitors (CGS1-18)
Protective 470 ohm resistors (RN7) between the drivers and PWM pill pins
Phase sense caps (C29, C30, C33) set to 10nF for 10kHz range filtering
Added zener diode (D10) protection between gate drivers and 12/5 DCDC
Rearranged mosfet driver area to fit 12/5 DCDC
Larger distance between edge and all copper fills
Added on board thermister
Restructured ceramic caps, added radial caps
Manual review of all parts / values / footprints in comparison to BOM
Removed many test points to conserve space; pins can be soldered to FETs for testing.

Opamp is a standard SOIC14 pinout. There are many that will fit. However, certain characteristics are needed:
GBP (GBW) gain Bandwidth Product > 4MHz
Rail to rail output
No phase inversion with exceeded limits
Input includes lower rail
Options are plentiful, preferred:
NCS20034 (NCS20074 might work)
TLV824
Current sensing ultimately defines the performance of your FOC algorithm, don't skimp on this part.
Using the wrong opamp can cause nasty failures like phase inverted currents, saturated outputs...

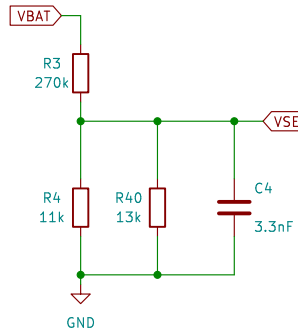
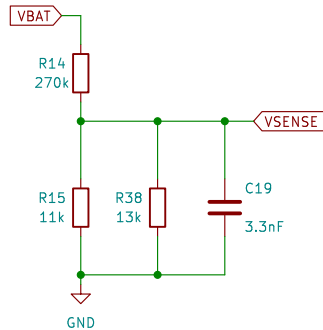


Fourth opamp used as overcurrent and voltage comparator to protect against shoot through, overcurrent + overvoltage in MCU crash.
If any of the opamps outputs exceeds 3v3/8/2/(8.2+9.2) + diode forward voltage, the opamp will pull low, which pulls PB12 low, triggering the STM32 hardware BRK.
Time constant approximately 0.47us
There's another 0.47us LFP on the F405 pill! That is not the case for Bluepill or Blackpill

Use low forward voltage diodes
1N5817 or 1N5819 is a good choice
Forward voltage at 1mA >0.3V will render this useless

R38 and R40 values for Vsense dividers – for different power stage Voltages.

Since the we're going with the NVMTC4D3N15MC MOSFETs, Vsense will be for 150V:
150V max 30s lipo, overvoltage cutoff at 137V) – 13k (LCSC C22797)
100V max 20s lipo, overvoltage cutoff at 92.6V) – 47k (LCSC C25819)
80V max 16s lipo, overvoltage cutoff at 75.6V) – Do not fit at all!



Notes on power stage design:

Pulldowns optional, most gate drivers pull down the FETs when UVLO
MOS should have good Ciss/Crss ratio
Ciss/Crss>Vbat minimises the chance of parasitic turn-on.
Target gate time constant <200ns:
RG = 15R(1uF) + 15R (ext) + 3R33/3 (gate driver)
Ciss = 11.4nF
RC = 11.4nF x 16.9R = 192.66ns

