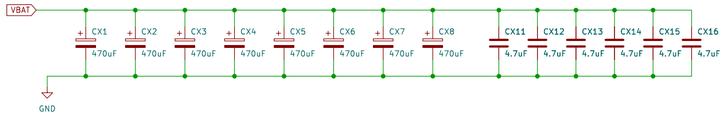
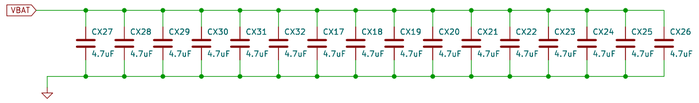
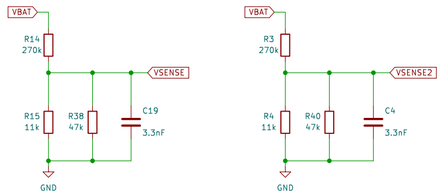




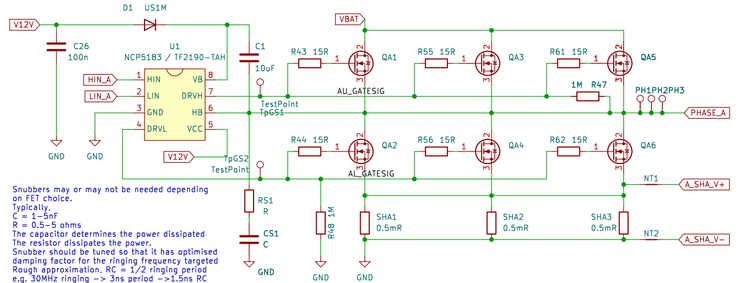
R3B and R40 values for Vsense dividers – for different power stage Voltages.

80V power stage (max 16s lipo, overvoltage cutoff at 75.6V) – Do not fit at all!
100V power stage (max 20s lipo, overvoltage cutoff at 92.6V) – 47k (LCSC C25819)
150V power stage (max 30s lipo, overvoltage cutoff at 137V) – 13k (LCSC C22797)



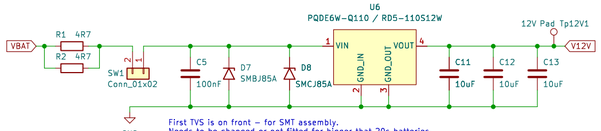
Notes on power stage design:

Pulldowns optional, most gate drivers pull down the FETs when UVLO
MOS should have good Ciss/Crss ratio
Ciss/Crss>Vbat minimises the chance of parasitic turn-on.
Target gate time constant ~200ns:
RG = 1R8(fet) + 15R (ext) + 3R33/3 (gate driver)
Ciss = 11.4nF
RC = 11.4nF x 16.9R = 192.66ns

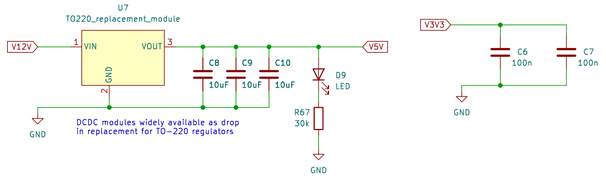


Snubbers may or may not be needed depending on FET choice.
Typically,
C = 1–5nF
R = 0.5–5 ohms
The capacitor determines the power dissipated
The resistor dissipates the power.
Snubber should be tuned so that it has optimised damping factor for the ringing frequency targeted
Rough approximation. RC = 1/2 ringing period
e.g. 30MHz ringing -> 3ns period -> 1.5ns RC
2nF 1ohm is a good starting point
Highest damping factor usually where Csnub ~= Coss MOS

Footprint for CUI isolated module for up to 160V operation.
Only allows 500mA.
HiLink HLK-10D11012
CUI PQDE6W-Q110
Or anything that exceeds your battery voltage and gives 12V out



First TVS is on front – for SMT assembly.
Needs to be changed or not fitted for bigger that 20s batteries.
Optionally a 20..47uF cap can be used which together with R1 and R2
creates a sort of LPF protecting the DCDC from high frequency noise/spikes.
Second TVS on the back – for hand soldering, in case a different / bigger one is wished.

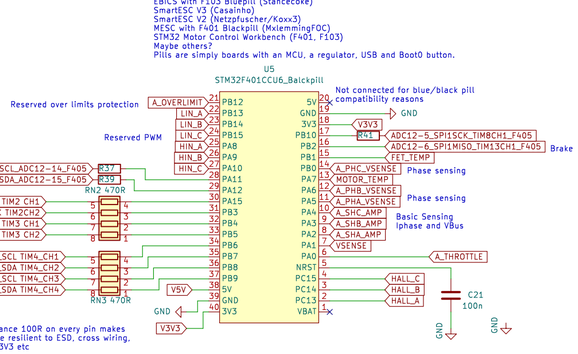


DCDC modules widely available as drop in replacement for TO-220 regulators

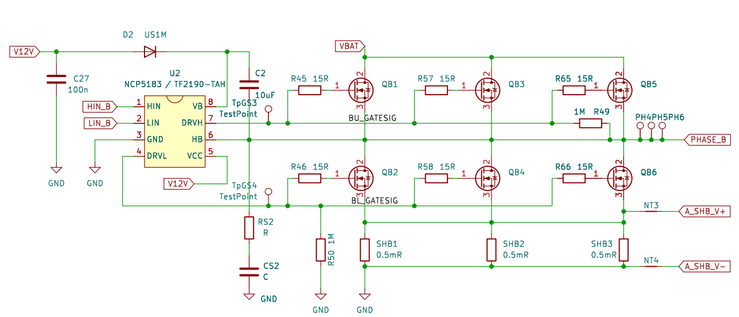
PB4 MISO TIM3 CH1
PB5 MOSI TIM3 CH2
R13 2k2

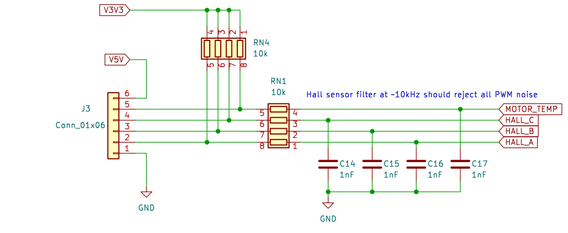
MISO and MOSI are useful to have a link in case of one wire SSI
DNP if full duplex required

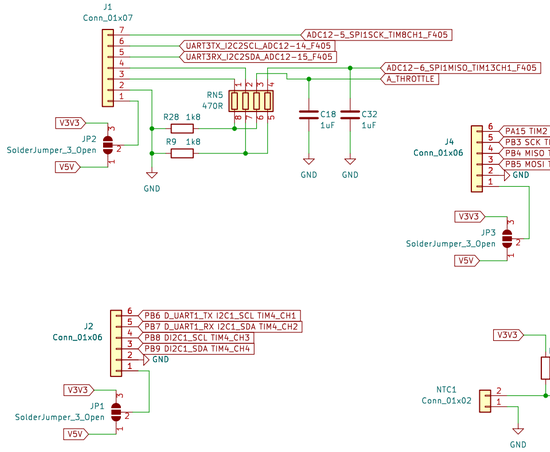
The "Pill" is chosen as a generic STM32 module that should allow easy compatibility with multiple firmwares:
VESC with GD32F303CG pill (Netzpfuscher mod, note CG)
VESC with STM32F405 pill (Owhite) (github.com/davidmolony/F405_pill)
EBICS with F103 Bluepill (Stancecoke)
SmartESC V3 (Casainho)
SmartESC V2 (Netzpfuscher/Koxx3)
MESC with F401 Blackpill (MxlemmingFOC)
STM32 Motor Control Workbench (F401, F103)
Maybe others?
Pills are simply boards with an MCU, a regulator, USB and Boot0 button.

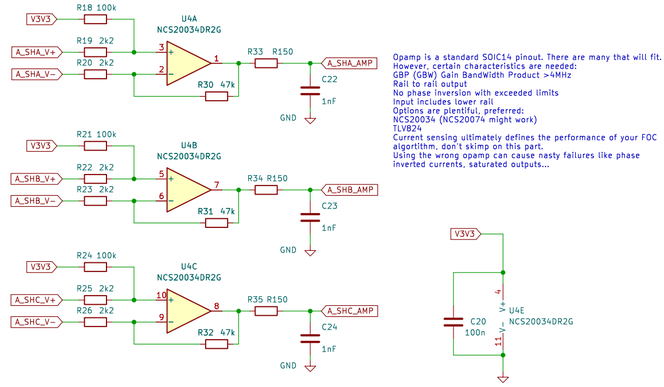


Input impedance 100R on every pin makes it much more resilient to ESD, cross wiring.
GPIO-GND/3V3 etc

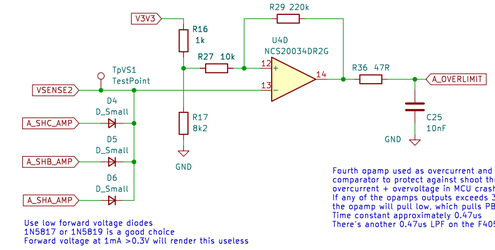






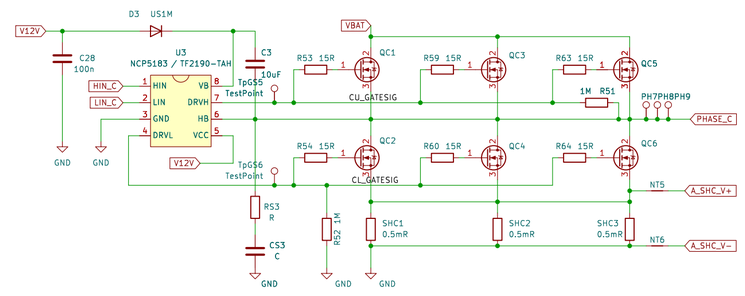


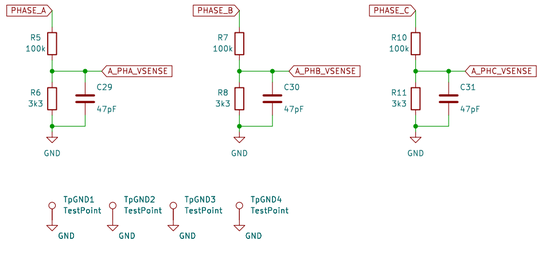
Opamp is a standard SOIC14 pinout. There are many that will fit.
However, certain characteristics are needed:
GBP (GBW) Gain BandWidth Product >4MHz
Rail to rail output
No phase inversion with exceeded limits
Input includes lower rail
Options are plentiful, preferred:
NCS20034 (NCS20074 might work)
TLV824
Current sensing ultimately defines the performance of your FOC algorithm, don't skimp on this part.
Using the wrong opamp can cause nasty failures like phase inverted currents, saturated outputs...



Use low forward voltage diodes
1N5817 or 1N5819 is a good choice
Forward voltage at 1mA >0.3V will render this useless

Fourth opamp used as overcurrent and voltage comparator to protect against shoot through, overcurrent + overvoltage in MCU crash
If any of the opamps outputs exceeds 3v3x8/2/(8.2+9.2) + diode forward voltage, the opamp will pull low, which pulls PB12 low, triggering the STM32 hardware BRK
Time constant approximately 0.47us
There's another 0.47us LPF on the F405 pill! That is not the case for Bluepill or Blackpill





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