15/2/24

Proton Beam Therapy

Proton range. Beam in right location H+V

Radio Therapy <1mm

Range QA

UCL Bits

Scintilator

like bread. Brightest beam spot.

Ti DDC 232 170μS conver.

→ Hamamatsu S12915 photodiodes.

Nexys Vidyo

FMC Daughter Card → USB-C or Ribbon.

9-12V input

Eurocircuits

Clean power supply.

Reduce

Glh102

Opal Kelly

2 * Sysygy Standard

→ Carrier QSE-020

ZMOD → Peripheral QTE-020

RevC

FMC replaced by a → ZMod ←

to USB-C connector

[2.5mm DC Jack.]

TABLE OF CONTENTS

SHEET NO.	SHEET NAME	BLOCK NAME
1	TABLE OF CONTENT	pc065b_fibv2_toplevel
2	POWER	pc065b_fibv2_toplevel
3	FMC_CONNECTOR	pc065b_fibv2_toplevel
4	SFP_CONNECTORS	pc065b_fibv2_toplevel
5	SFP_INTERFACES_0:3	pc065b_fibv2_toplevel
6	SFP_INTERFACES_4:7	pc065b_fibv2_toplevel
7	CLOCK	pc065b_fibv2_toplevel
8	MUX AND CDR	pc065b_fibv2_toplevel
9	I2C LEVEL TRANSLATORS	pc065b_fibv2_toplevel
10	LEVEL TRANSLATORS	pc065b_fibv2_toplevel
11	CONNECTORS	pc065b_fibv2_toplevel
12	EEPROM	pc065b_fibv2_toplevel
13	page13	pc065b_fibv2_toplevel
14	page1	sfp_module
15	page1	sfp_module

TABLE OF CONTENTS

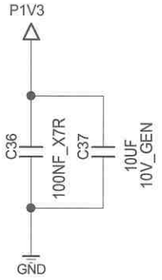
SHEET NO.	SHEET NAME	BLOCK NAME
16	page1	sfp_module
17	page1	sfp_module
18	BUFFER 1:2	diff_buff_1to2
19	BUFFER 1:2	diff_buff_1to2
20	BUFFER 1:2	diff_buff_1to2
21	BUFFER 1:2	diff_buff_1to2
22	page1	sfp_module
23	page1	sfp_module
24	page1	sfp_module
25	page1	sfp_module
26	BUFFER 1:2	diff_buff_1to2
27	I2C LEVEL TRANSLATOR	i2c_level_translate
28	I2C LEVEL TRANSLATOR	i2c_level_translate
29	I2C LEVEL TRANSLATOR	i2c_level_translate
30	I2C LEVEL TRANSLATOR	i2c_level_translate

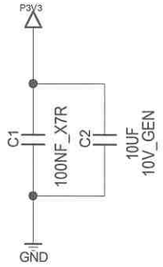
TABLE OF CONTENTS

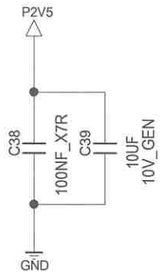
SHEET NO.	SHEET NAME	BLOCK NAME
31	I2C LEVEL TRANSLATOR	i2c_level_translate
32	I2C LEVEL TRANSLATOR	i2c_level_translate
33	I2C LEVEL TRANSLATOR	i2c_level_translate
34	I2C LEVEL TRANSLATOR	i2c_level_translate
35	I2C LEVEL TRANSLATOR	i2c_level_translate
36	AB	fmc_hpc_generic
37	CDGH	fmc_hpc_generic
38	EFJK	fmc_hpc_generic

I2C ADDRESSES
EEPROM 0X50 (ALTERNATIVE: 0X51)
CDR 0X60 (ALTERNATIVE: 0X40)
CLOCK 0X68 (0X69, 0X6A, 0X6B)
EXPANDER 0X74
EXPANDER 0X75

PROJECT:	pc065b_fibv2_toplevel		
PARTICLE PHYSICS UNIVERSITY OF BRISTOL H. H. WILLS PHYSICS LABORATORY TYNDALL AVENUE, BS8 1TL BRISTOL, UK	REVISION: 2	DATE MODIFIED: 14/05/2020	
	DESIGNED BY: P. Baesso	SIZE: A3	PAGE: 1 / 38
	TABLE OF CONTENT		

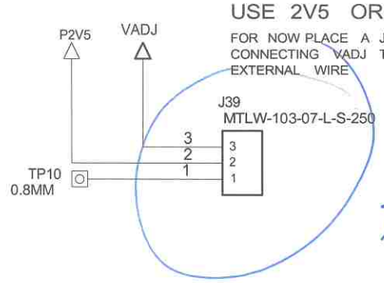






USE 2V5 OR VADJ FOR TRANSLATORS?

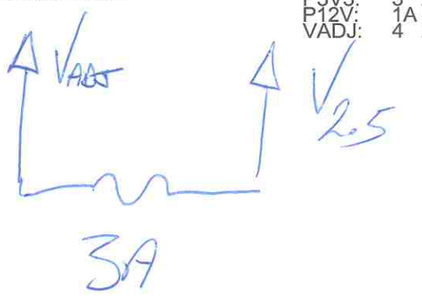
FOR NOW PLACE A JUMPER+TP TO ALLOW CONNECTING VADJ TO P2V5 OR USING EXTERNAL WIRE



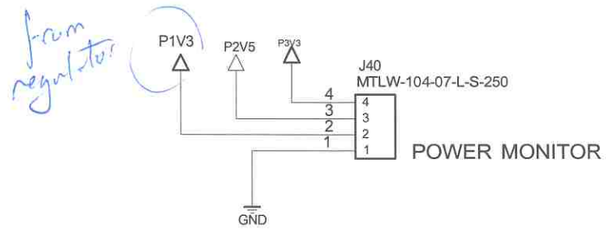
#10

#9

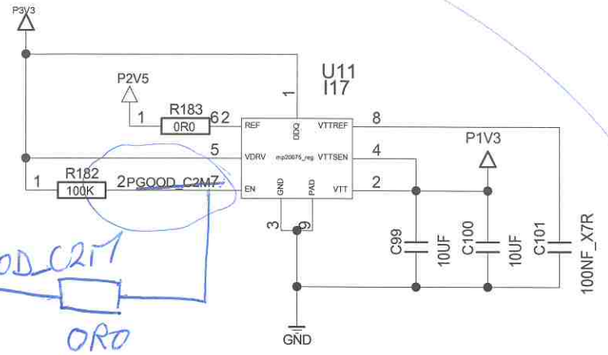
MAX CURRENTS PER RAILS
P3V3: 3 A
P12V: 1A
VADJ: 4 A



from regulator



POWER MONITOR

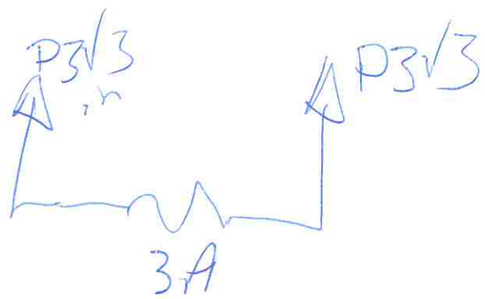


PGOOD_C2M7

0R0

DNF

#2



0603

1.6 x 0.8mm 3A SMT

RS 692-5003

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PARTICLE PHYSICS UNIVERSITY OF BRISTOL H. H. WILLS PHYSICS LABORATORY TYNDALL AVENUE, BS8 1TL BRISTOL, UK	REVISION: 2	DATE MODIFIED: 14/05/2020	
	DESIGNED BY: P. Baesso	SIZE: A3	PAGE: 2 / 38
	POWER		

IO FMC_LA_P<0..33>

IO FMC_LA_N<0..33>

remove IN CDR_D_P\BASE 0

0 CDR_D_N\BASE IN remove

OUT TD_FFD_P<0..7>\BASE

0 2
1 4
2 7
3 11
4 15
5 19
6 21
7 24

TD_FFD_N<0..7>\BASE OUT

2 0
4 1
7 2
11 3
15 4
19 5
21 6
24 7

IN RD_FPGA_P<0..3>\BASE

0 3
1 28
2 30
3 8

RD_FPGA_N<0..3>\BASE IN

3 0
28 1
30 2
8 3

<RD_FPGA_{N/P}<7..0>

IO SFP_I2C_SDA_CVCC<0..7>\BASE

0 6
1 12
2 10
3 31
4 14
5 9
6 18
7 33

SFP_I2C_SCL_CVCC<0..7>\BASE OUT

6 0
12 1
10 2
31 3
14 4
9 5
18 6
33 7

OUT MUX_SEL_CVCC<0..2>\BASE

0 27
1 1
2 27

remove

1 RST_I2C_B_CVCC\BASE OUT

fanout input select
2.5V

no CDR on more -> no clock

IN REC_CLK_FPGA_P 0
IN CLK_MAIN_P<8> 1

output clocking

CLK_M2C_P<0..1>

IN REC_CLK_FPGA_N 0
IN CLK_MAIN_N<8> 1

CLK_M2C_N<0..1>

from carrier to fanout.

OUT CLK_IN_P<1> 0
OUT CLK_IN_N<1> 0

CLK_BIDIR_P<0..1>
CLK_BIDIR_N<0..1>

CLK_DIR
WHEN 3.3: C2M
WHEN GND: M2C

P3V3
R33 10K
R58 XX
CLK_DIR
GND

R30 0R0 2PRSNT_L
GND

DNF #7

R184 0R0
R185 0R0
GND

I2C_SDA_CVCC IO
I2C_SCL_CVCC OUT

FMC_HPC_GENERIC

PG_M2C
PG_C2M PGOOD_C2M OUT
LA_P<0..33>
LA_N<0..33>
HA_P<0..23>
HA_N<0..23>
HB_P<0..21>
HB_N<0..21>
GBTCLK_M2C_P<0..1>
GBTCLK_M2C_N<0..1>
DP_C2M_P<0..9>
DP_C2M_N<0..9>
DP_M2C_P<0..9>
DP_M2C_N<0..9>
CLK_M2C_P<0..1>
CLK_M2C_N<0..1>
CLK_BIDIR_P<0..1>
CLK_BIDIR_N<0..1>
CLK_DIR
VIO_B_M2C
VREF_A_M2C
VREF_B_M2C
PRSNT_M2C_L
TCK TDI TDO TMS TRST_L SCL SDA GA0 GA1

I1

encapsulator en discrete encapsulator

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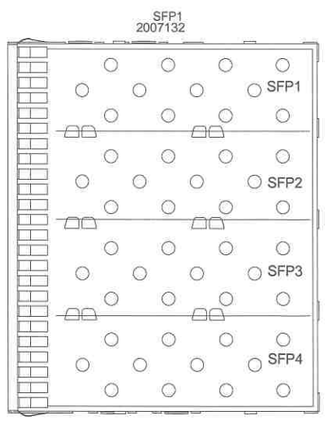
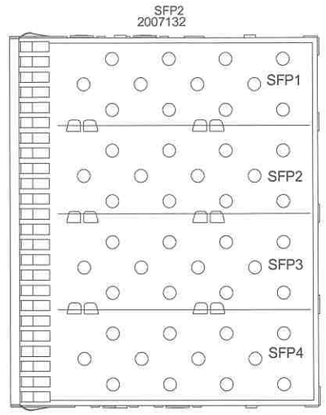
	DESIGNED BY: P. Baesso	SIZE: A3	PAGE: 3 / 38
	FMC_CONNECTOR		

1X4 SFP+ CAGE

USE 2110069-1 FOR LIGHTPIPES

USE 2007132-1 FOR NO LIGHTGUIDES





colinear
cn75als
cn75als ✓
cn74lv ✓
cn74tiac ✓
encmos
cn pld ✓
cnvlsi

bus connect ✓
mem ✓
pld ✓
cnspecial ✓
standards ✓
switches

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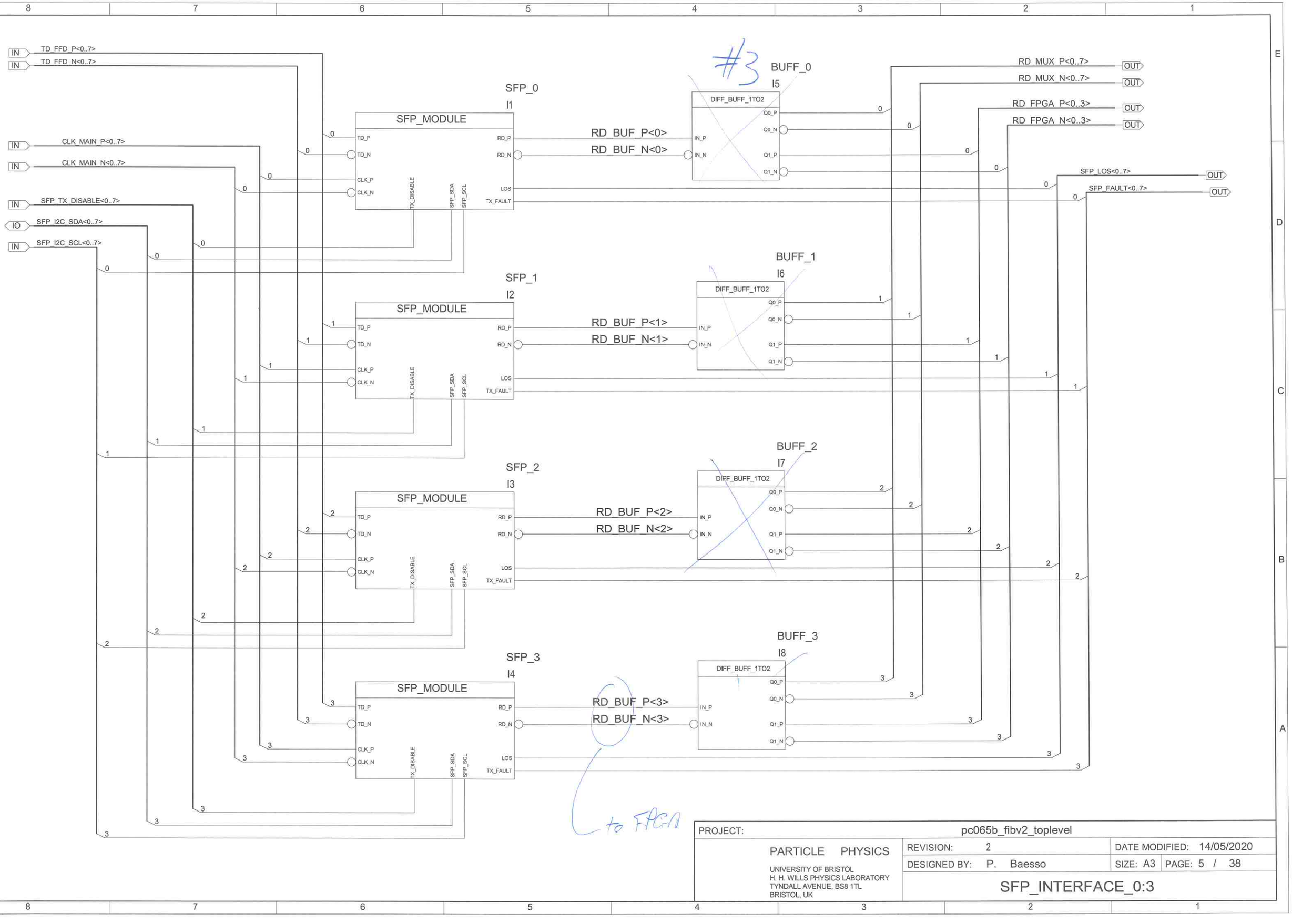
	DESIGNED BY: P. Baesso	SIZE: A3	PAGE: 4 / 38
	SFP_CONNECTORS		



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PARTICLE PHYSICS UNIVERSITY OF BRISTOL H. H. WILLS PHYSICS LABORATORY TYNDALL AVENUE, BS8 1TL BRISTOL, UK	REVISION: 2	DATE MODIFIED: 14/05/2020	
	DESIGNED BY: P. Baesso	SIZE: A3	PAGE: 5 / 38
	SFP_INTERFACE_0:3		

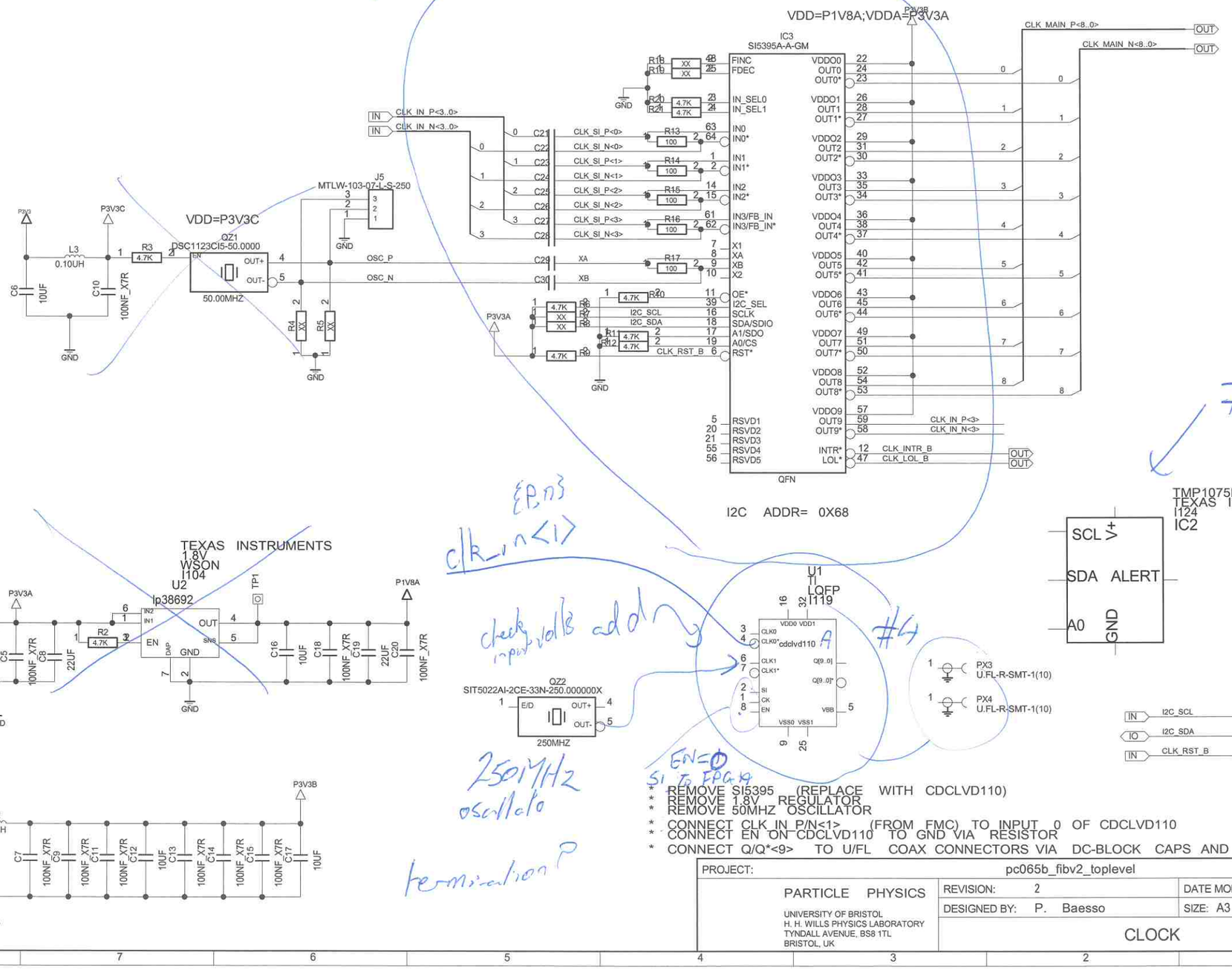
IN TD_FFD_P<0..7>
IN TD_FFD_N<0..7>
IN CLK_MAIN_P<0..7>
IN CLK_MAIN_N<0..7>
IN SFP_TX_DISABLE<0..7>
IO SFP_I2C_SDA<0..7>
IN SFP_I2C_SCL<0..7>

SFP_4
I47
SFP_5
I45
SFP_6
I35
SFP_7
I13

SFP_MODULE
TD_P
TD_N
CLK_P
CLK_N
TX_DISABLE
SFP_SDA
SFP_SCL
RD_P
RD_N
LOS
TX_FAULT

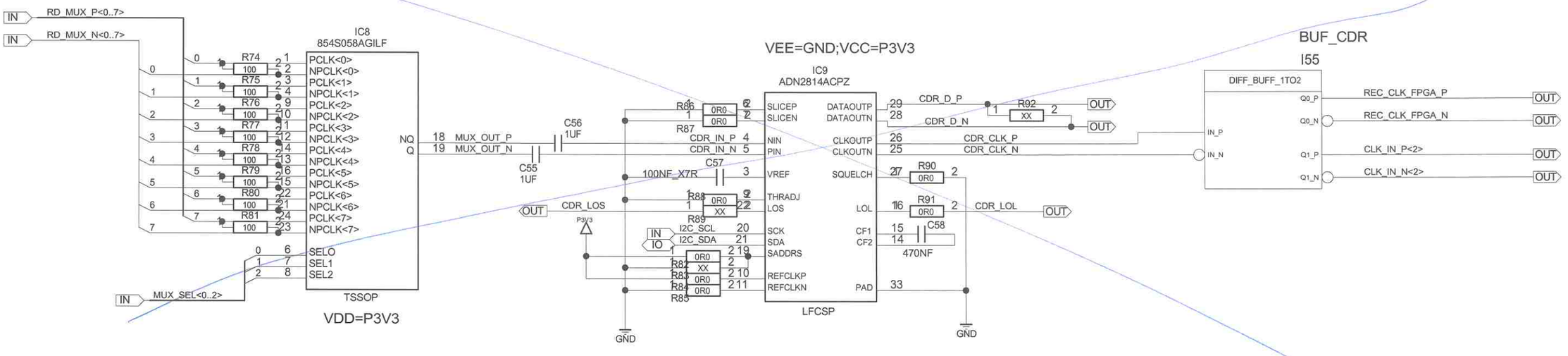
OUT RD_MUX_P<0..7>
OUT RD_MUX_N<0..7>
to FPGA, not Mux
OUT SFP_LOS<0..7>
OUT SFP_FAULT<0..7>

PROJECT:	pc065b_fibv2_toplevel		
PARTICLE PHYSICS UNIVERSITY OF BRISTOL H. H. WILLS PHYSICS LABORATORY TYNDALL AVENUE, BS8 1TL BRISTOL, UK	REVISION: 2	DATE MODIFIED: 14/05/2020	
	DESIGNED BY: P. Baesso	SIZE: A3	PAGE: 6 / 38
	SFP_INTERFACE_4:7		


VDD=P1V8A;VDDA=P3V3A
IC3
SI5395A-A-GM
VDD=P3V3C
QZ1
DSC1123CI5-50.0000
50.00MHZ
MTLW-103-07-L-S-250
J5
CLK_IN_P<3..0>
CLK_IN_N<3..0>
CLK_SI_P<0>
CLK_SI_N<0>
CLK_SI_P<1>
CLK_SI_N<1>
CLK_SI_P<2>
CLK_SI_N<2>
CLK_SI_P<3>
CLK_SI_N<3>
OSC_P
OSC_N
I2C_SCL
I2C_SDA
CLK_RST_B
CLK_MAIN_P<8..0>
CLK_MAIN_N<8..0>
CLK_IN_P<3>
CLK_IN_N<3>
CLK_INTR_B
CLK_LOL_B
QFN
I2C ADDR= 0X68
TMP1075NDRLR
TEXAS INSTRUMENTS
I124
IC2
SCL
SDA
ALERT
A0
GND
V+
TEXAS INSTRUMENTS
1.8V
WSON
I104
U2
lp38692
U1
TI
LQFP
I119
QZ2
SIT5022AI-2CE-33N-250.000000X
250MHZ
PX3
U.FL-R-SMT-1(10)
PX4
U.FL-R-SMT-1(10)
* REMOVE SI5395 (REPLACE WITH CDCLVD110)
* REMOVE 1.8V REGULATOR
* REMOVE 50MHZ OSCILLATOR
* CONNECT CLK_IN_P/N<1> (FROM FMC) TO INPUT 0 OF CDCLVD110
* CONNECT EN ON CDCLVD110 TO GND VIA RESISTOR
* CONNECT Q/Q*<9> TO U/FL COAX CONNECTORS VIA DC-BLOCK CAPS AND 10:1 DIVIDER TO GIVE 100-OHM TERM WHEN NOT CONNECTED
PROJECT: pc065b_fibv2_toplevel
PARTICLE PHYSICS
UNIVERSITY OF BRISTOL
H. H. WILLS PHYSICS LABORATORY
TYNDALL AVENUE, BS8 1TL
BRISTOL, UK
REVISION: 2
DESIGNED BY: P. Baesso
DATE MODIFIED: 14/05/2020
SIZE: A3 PAGE: 7 / 38
CLOCK

NOTE:
CDR ADN2814 HAS A SIMILAR PINOUT TO ADN2805
THE SCHEMATIC ALLOWS TO SWAP BETWEEN THE TWO
DIFFERENT PINS ARE 6, 7, 9, 22

#3



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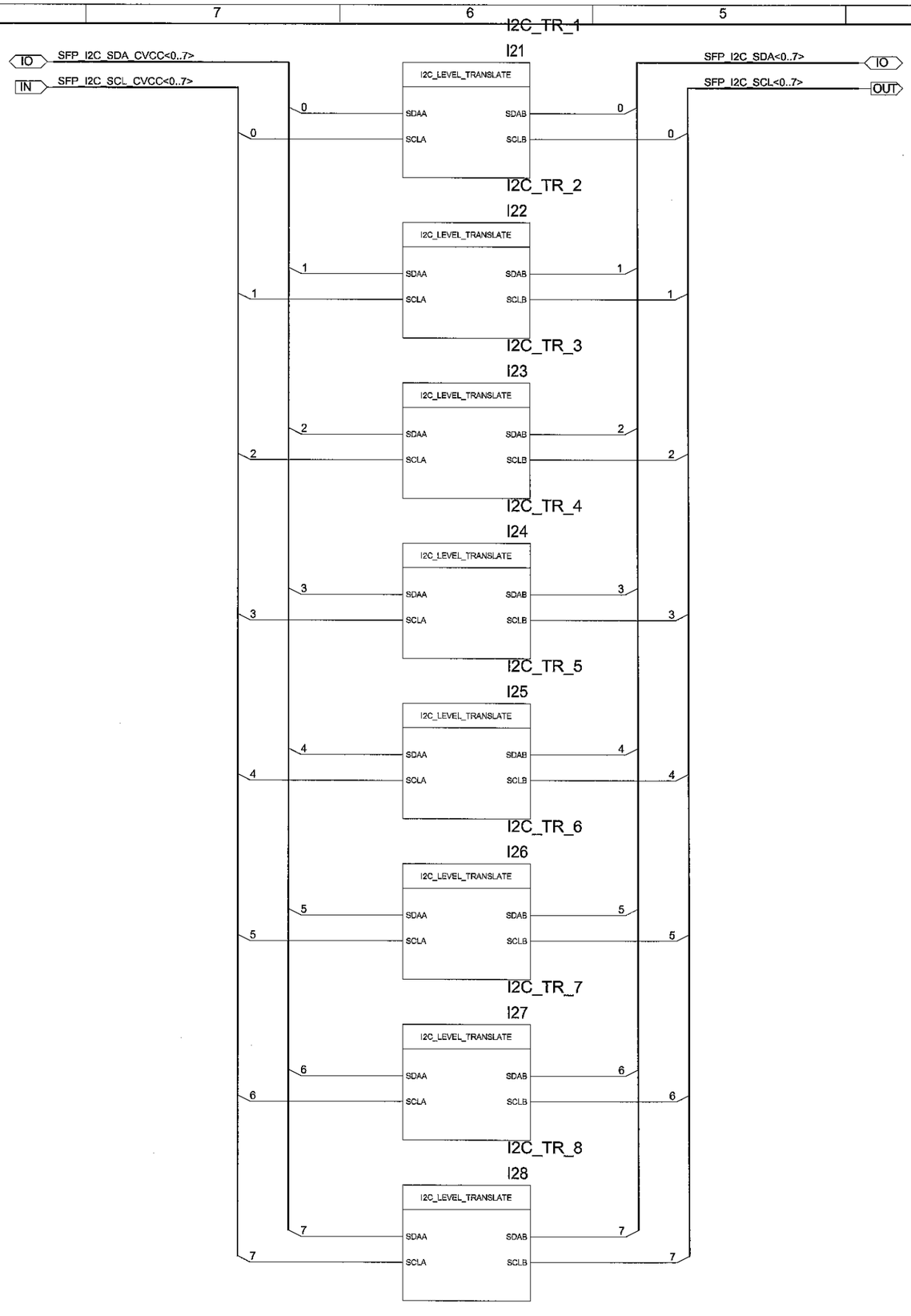
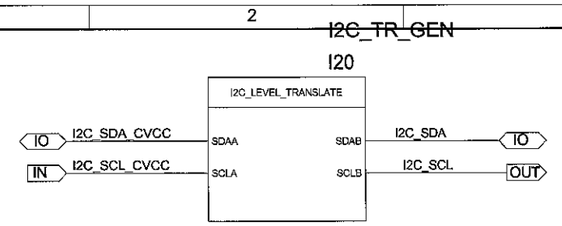
	DESIGNED BY: P. Baesso	SIZE: A3	PAGE: 8 / 38
	MUX AND CDR		





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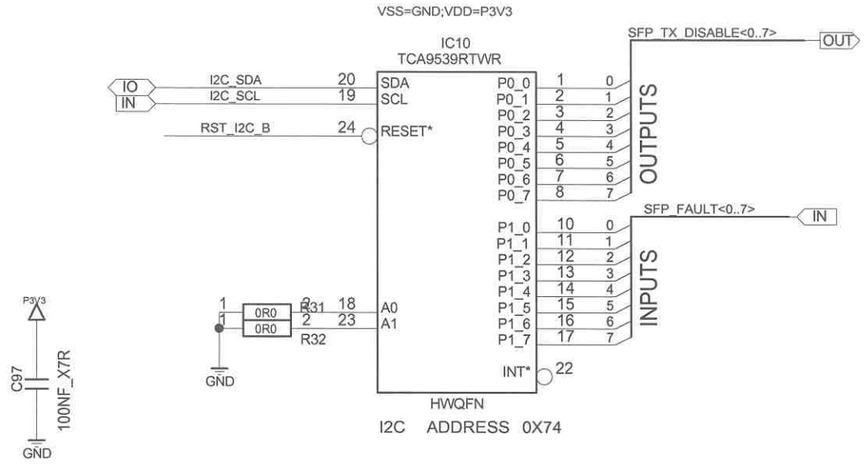
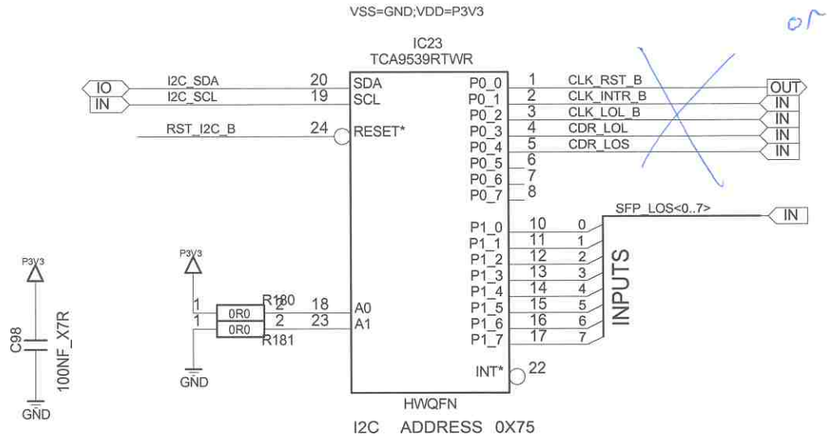
	DESIGNED BY: P. Baesso	SIZE: A3	PAGE: 9 / 38
	I2C LEVEL TRANSLATORS		





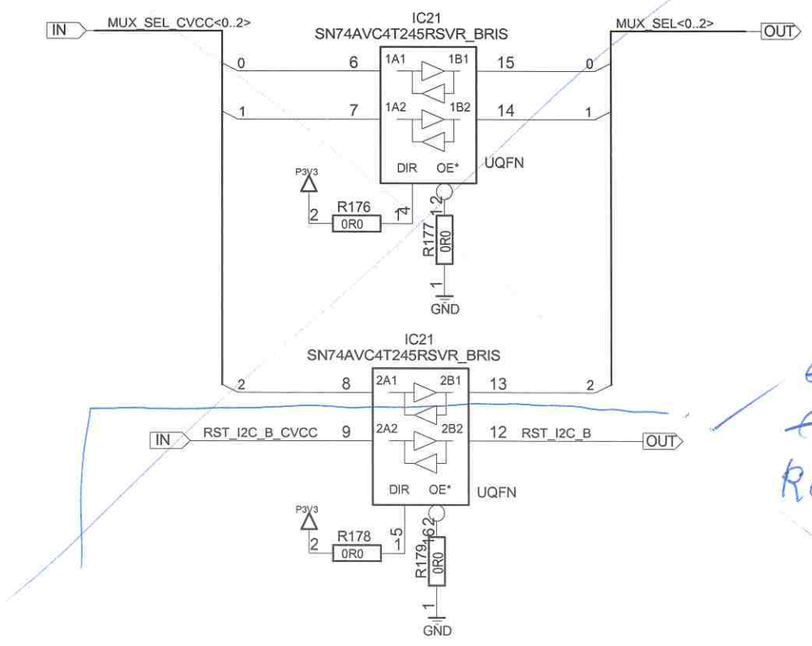
or reuse one pin as fanout input select?

Celfanl = clk from carrier

CHECK PINOUT AND FOOTPRINT!

DIR LOW: B >>> A
DIR HIGH: A >> B

VCCA=P2V5;VCCB=P3V3



check. ~~can~~ RST_I2C Keep be removed

PROJECT:	pc065b_fibv2_toplevel		
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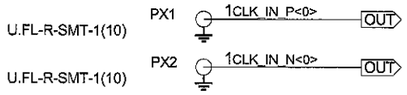
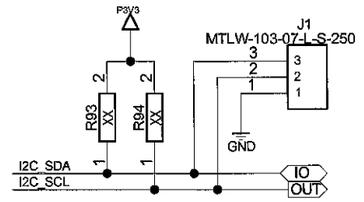
	DESIGNED BY: P. Baesso	SIZE: A3	PAGE: 10 / 38
	LEVEL TRANSLATORS		





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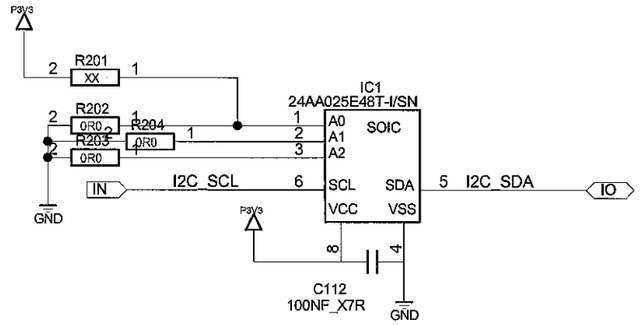
	DESIGNED BY: P. Baesso	SIZE: A3	PAGE: 11 / 38
	CONNECTORS		

NBSG53AMNG IS AT END OF LIFE. DO NOT USE
ALTERNATIVES:
NB7V52MMNG
SY55852U
MAX9381EUA+

ADN2814ACPZ IS NO LONGER AVAILABLE



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	DESIGNED BY: P. Baesso	SIZE: A3	PAGE: 12 / 38
	EEPROM		

PROJECT:	pc065b_fibv2_toplevel
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	DATE MODIFIED: 14/05/2020
	DESIGNED BY: P. Baesso
	SIZE: A3 PAGE: 13 / 38
	TITLE