Property of CERN - For Internal Use Only – External Distribution Prohibited

MicroTCA®

PICMG® Specification MTCA.4

Revision 1.0

MicroTCA Enhancements for Rear I/O and Precision Timing

August 22, 2011

PICMG®

Open Modular Computing Specifications

µTCA®

Contents

Figures

Tables

This page intentionally left blank

1 Introduction

1.1 Objectives

The purpose of this document is to define an Advanced Mezzanine Card (AMC) and a corresponding μRTM module set for rear I/O along with an appropriate MicroTCA shelf. The document also contains a section on precision timing that was driven by needs in the physics accelerator control and experiment data collection electronics. The committee feels that although originally driven by the physics research community this specification has much wider general use.

1.1.1 Reference documents

The publications cited in this section are relevant to this specification. Most of the specifications referred to are subject to periodic and independent updates, and are the responsibility of their respective organizations. The reader is advised to check carefully the version or revision of the referenced specification that is to be used in conjunction with this document.

1.1.2 Reference specifications

All documents may be obtained from their respective organizations.

Document	Organization	Contact information
PICMG 3.0 R3.0	PICMG	www.picmg.org
PICMG AMC.0 R2.0	PICMG	www.picmg.org
PICMG IRTM.0 R1.0	PICMG	www.picmg.org
PICMG IRTM.1 R1.0	PICMG	www.picmg.org
PICMG MTCA.0 R1.0	PICMG	www.picmg.org
PICMG MTCA.1 R1.0	PICMG	www.picmg.org
IPMI v2.0 R1.0	Intel, HP, NEC, Dell	

1.2 Contributors

The following companies and institutions contributed to the creation of this document:

Agilent Technologies	Institute of High Energy Physics (IHEP)	SLAC National Accelerator Laboratory
Arroyo Technology Consultants	Instrumentation Technologies ITECH	TEWS Technologies
D-TACQ Solutions	Intel	TE Connectivity
DESY	IPFN	Ulticom
Elma Electronic	N.A.T.	
Extrusion Tech (XTech)	National Instruments	
Fermi National Accelerator Laboratory	Pentair Technical Products	
Foxconn Electronics	Performance Technologies	
GE Intelligent Platforms	Positronic Industries	

1.3 Special word usage

In this specification the following key words (in **bold** text) will be used:

may: Indicates flexibility of choice with no implied preference.

should: Indicates flexibility of choice with a strongly preferred implementation. The use of **should not** (in **bold** text) indicates a flexibility of choice with a strong preference that the choice or implementation should be prohibited.

shall: Indicates a mandatory requirement. Designers **shall** implement such mandatory requirements to ensure interchangeability and to claim conformance with this specification. The use of **shall not** (in **bold** text) indicates an action or implementation that is prohibited.

Note: When not in bold text, the words “may,” “should,” and “shall” are being used in the traditional sense; that is, they do not adhere to the strict meanings described above.

1.4 Name and logo usage

This is the MicroTCA logo:

μTCA®

The blue color used for the “μ” is PANTONE 293 CVC.

The PCI Industrial Computer Manufacturers Group's policies regarding the use of its logos and trademarks are as follows:

Permission to use the PICMG organization logo is automatically granted to designated members only as stipulated on the most recent *Membership Privileges* document (available on the Web at www.picmg.org), during the period of time for which their membership dues are paid. Non-members of PICMG must not use the PICMG organization logo.

The PICMG organization logo must be printed in black or in color as shown in the files available for download from the members' side of the Web site. Logos with or without the “Open Modular Computing Specifications” banner can be used. Nothing may be added to or deleted from the PICMG logo.

Manufacturers' distributors and sales representatives may use the MicroTCA® logo (but not the PICMG organization logo) in promoting products sold under the name of the manufacturer.

The use of MicroTCA logos is a privilege granted by the PICMG organization to companies who have purchased the relevant specifications (or acquired them as a member benefit) and who believe their products comply with these specifications. Use of the logos by either members or non-members implies such compliance. PICMG may revoke permission to use logos if they are misused.

The PICMG name and logo are registered trademarks of PICMG. Registered trademarks must be followed by the ® symbol, and the following statement must appear in all published literature and advertising material in which the logo appears:

PICMG and the PICMG logo are registered trademarks of the PCI Industrial Computer Manufacturers Group.

The MicroTCA name and logo are registered trademarks of PICMG. Registered trademarks must be followed by the ® symbol, and the following statement must appear in all published literature and advertising material in which the logo appears:

The MicroTCA name and logo are trademarks of the PCI Industrial Computer Manufacturers Group.

1.5 Signal naming conventions

All signals are active high unless denoted by a trailing # symbol. Differential signals are denoted by a trailing + (positive) or – (negative) symbol.

1.6 Intellectual property

The Consortium draws attention to the fact that it is claimed that compliance with this specification may involve the use of a patent claim(s) ("IPR") concerning connector mechanicals given in Appendix A. The Consortium takes no position concerning the evidence, validity, or scope of this IPR.

The holder of this IPR has assured the Consortium that it is willing to license or sublicense all such IPR to those licensees (Members and non-Members alike) desiring to implement this specification. The statement of the holder of this IPR to such effect has been filed with the Consortium.

Attention is also drawn to the possibility that some of the elements of this specification may be the subject of IPR other than those identified below. The Consortium shall not be responsible for identifying any or all such IPR.

THIS SPECIFICATION IS BEING OFFERED WITHOUT ANY WARRANTY WHATSOEVER, AND IN PARTICULAR, ANY WARRANTY OF NON-INFRINGEMENT IS EXPRESSLY DISCLAIMED. ANY USE OF THIS SPECIFICATION SHALL BE MADE ENTIRELY AT THE IMPLEMENTER'S OWN RISK, AND NEITHER THE CONSORTIUM, NOR ANY OF ITS MEMBERS OR SUBMITTERS, SHALL HAVE ANY LIABILITY WHATSOEVER TO ANY IMPLEMENTER OR THIRD PARTY FOR ANY DAMAGES OF ANY NATURE WHATSOEVER, DIRECTLY OR INDIRECTLY, ARISING FROM THE USE OF THIS SPECIFICATION.

No representation is made as to the availability of any license rights for use of any IPR inherent in this specification for any purpose other than to implement this specification.

Necessary Claims (referring to mandatory or recommended features):

ERNI Electronics GmbH, Seestraße 9, D-73099 Adelberg Germany
US Patent 6,899,566
European Patent W02003/065511

Tyco Electronics Corporation, c/o The Whittaker LLC, 4550 New Linden Hill Road, Suite 140, Wilmington DE 19808
US Patent 6,899,566
CN Patent ZL03807091.x
DE Patent 60314228.1
FR and GB Patents 1470618
JP Patent 4236585

Unnecessary Claims (referring to optional features or non-normative elements):

Elma Electronic Inc., 44350 Grimmer Blvd, Fremont, CA 94538
US Provisional Patents: 61/461,194

Emerson Network Power, 1050 Dearborn Drive, Columbus, OH 43085
US Patent: 7,957,138
US Provisional Patents: 2010/0216389, 2010/0216390

Third Party Disclosures (Note that third party IPR submissions do not contain any claim of willingness to license the IPR):

Intel Corporation, 5200 NE Elam Young Parkway. MS: JF2-98, Hillsboro, OR 97124
US Patent: 6,912,129

Refer to PICMG IPR Policies and Procedures and the company owner of the patent for terms and conditions of usage.

PICMG makes no judgment as to the validity of these claims or the licensing terms offered by the claimants.

1.7 Acronyms and definitions

The following terms and acronyms are used in specific ways throughout this document.

µRTM	The Micro Rear Transition Module that mates with an associated AMC Module. It is the analog of the RTM in ATCA.
RP##	Designator for the pin connector (male contacts) in the µRTM and also the µRTM alignment/key
Airflow Filler	An airflow impedance matching module used when a module is not present to prevent excessive cooling air from shunting around empty slots.

1.8 Revision history

Date	Revision	Changes
August 22, 2011	R1.0	Initial Revision

2 Mechanical

2.1 Tolerances

¶ 1 A Root Sum Squared (RSS) tolerance was applied to all mechanical interfaces and test dimensions following ISO 1101 standards.

2.2 AMC Module

2.2.1 Printed Circuit Board

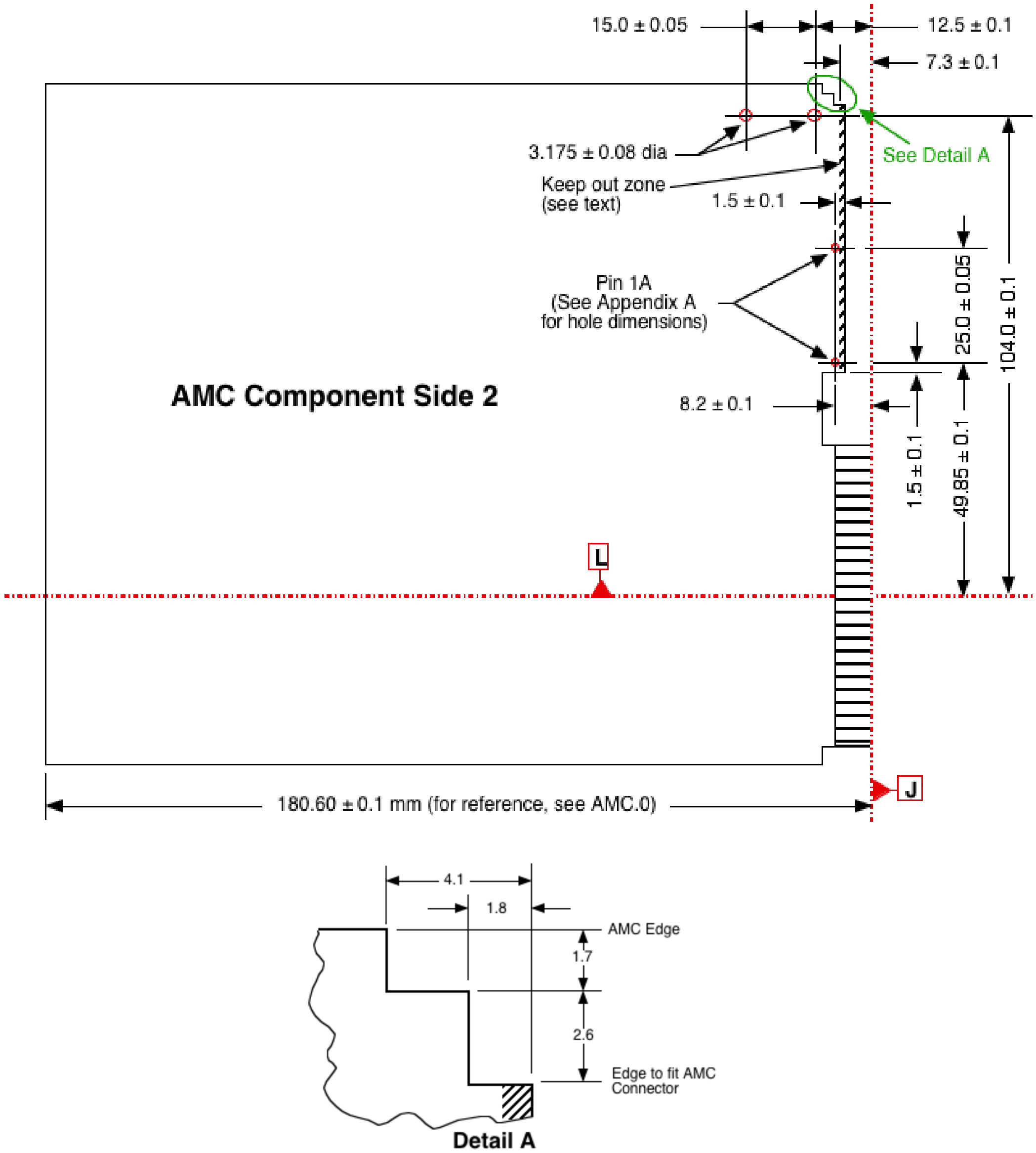


Figure 2-1: AMC Dimensions

Note: Figure 2-1 shows pin 1A locations for Zone 3 ADF connectors.

REQ 2-1: The outline of the AMC with ADF connectors **shall** follow AMC.0 R2.0, Section 2.2.1.2 except as noted in Figure 2-1.

REQ 2-2 Implementations using other connectors **may** have different positions for Pin 1 and different Zone 3 PCB edge details than those shown in Figure 2-1.

¶ 2 Unless otherwise noted, all dimensions conform to AMC.0 R2.0. Note that although the AMC outline is similar to AMC.0, Figure 2-5 the profile in the Zone 3 area is different. The profile in that area was specified for the case when there were two backplanes in a two-tier subrack. The outline insured that the PCB missed the upper backplane AMC connector. Since that area is now specified for attachment to a μRTM the old outline dimensions have been changed. The reference 42.5 is now 48.35, 107.5 is now 110.05 maximum and the setback from Datum J that was 7.5 is now 6.7. The old outline was the start of another edge card connector but with the fingers removed and cut short.

REQ 2-3: The inside and outside PCB corners in the Zone 3 area **shall** follow AMC.0 R2.0, Section 2.2.2, Figure 2-12 (Inside corners to be R1 and outside corners to be R0.5).

¶ 3 Detail A allows AMCs without Zone 3 connectors and the Guide/Key block to be inserted in shelves or carriers that have an AMC connector in the Zone 3, Connector 1 area (see MTCA.0 R1.0, Figure 2-100). The removal of PCB material in the notch area (detail A) will result in the Guide/Key block overhanging the PCB by about 0.5 mm. One should be aware that some of the AMCs original functionality could be lost in such a configuration.

REQ 2-4: To be compatible with subracks and carriers that have the AMC connector in the Zone 3, Connector 1 area, other components **shall not** be in the keep out zone shown in Figure 2-1.

REQ 2-5: The AMC board **shall** implement the ESD strip as detailed in AMC.0, Section 2.2.1.4.

2.2.2 Zone 3 Keying and Alignment

¶ 4 The keying mechanism used by modules adds protection from potentially damaging voltages being applied at the Zone 3 interface. In some cases system considerations may not allow gating of the voltages on the μRTM to the Zone 3 connector possibly resulting in damage to circuitry on the front board.

¶ 5 The alignment mechanism adjusts the front and rear modules so the Zone 3 connectors are positioned for mating.

REQ 2-6: The AMC Modules that mate with μRTM Modules **shall** implement female key/alignment mechanics as specified in Appendix B-2.

2.2.2.1 Key Orientation

Table 2-1: Key Orientation

N	A = Orientation in Degrees
1	0
2	45
3	90
4	135
5	180
6	225
7	270
8	315

¶ 6 The Orientation details can be found in Appendix B-3.

REQ 2-7: N = 0 **should** be used for test fixtures or in cases where only alignment is necessary.

2.2.2.2 Module Keying when using ADF Connectors

REQ 2-8: AMC Modules using ADF connectors **shall** use the key definitions as described in Table 2-2.

Table 2-2: Data Connector Voltage Level Keying

N	Data Signal in Volts
1	LVDS
2	0 – ±1
3	>±1 – ±3.3
4	>±3.3 – ±10
5	>±10
6	Reserved
7	Reserved
8	Reserved

2.2.2.3 Module Keying when not using ADF Connectors

REQ 2-9: Key definitions for AMC Modules and µRTMs that use connectors other than ADF connectors in Zone 3 **shall** be defined by the Module designer.

2.2.3 Connectors

2.2.3.1 Zone 1

REQ 2-10: The front board **should** use an add-on plug connector instead of edge card fingers.

¶ 7 The use of the add-on plug connector is similar to that specified for the MCH in MTCA.0 R1.0, Section 2.11.4. The versions of these connectors that have only Tongue 1 can be used here. These connectors have tighter tolerances and better overall mechanical properties than that obtainable with edge fingers. In addition the tight constraint on the PCB thickness is relaxed.

2.2.3.2 Zone 3 Connectors

¶ 8 The AMC Module uses connectors in the Zone 3 area to connect to the µRTM. The following sections provide details on how to use specific connectors in Zone 3. Table 2-3 lists the necessary signals to be provided at the AMC and µRTM interface.

Table 2-3: Power/Management Connections for AMC/µRTM Interface

Name	Description	Name	Description
µRTM_PWR	+12 Volts (nom)	GND	Ground
µRTM_PS#	µRTM Present	µRTM_MP	+3.3 Volts (nom)
µRTM_SDA	I^2C Data	µRTM_SCL	I^2C Clock
µRTM_TCK	Optional JTAG TCK	µRTM_TDI	Optional JTAG TDI
µRTM_TDO	Optional JTAG TDO	µRTM_TMS	Optional JTAG TMS

REQ 2-11: An ADF connector in J30 **shall** have a Short Pin in position J30-C1 for µRTM_PS#.

¶ 9 The ADF connector Short Pin is defined in Appendix A.

REQ 2-12: Implementation of JTAG **shall** be optional (TDI, TDO, TMS, TCK in Table 2-5).

REQ 2-13: If JTAG is implemented on the Front AMC and the µRTM is not present the AMC **should** short the TDI and TDO lines that go to/from the µRTM on the AMC.

¶ 10 The AMC can use the µRTM_PS# line to activate the TDI to TDO connection to the µRTM.

REQ 2-14: If a µRTM that does not implement JTAG is associated with an AMC that implements JTAG the µRTM **shall** connect the TDO and TDI pins on the Zone 3 connector.

REQ 2-15: When both a µRTM and AMC that implement JTAG are connected the µRTM **shall** be included in the AMCs JTAG signal chain.

REQ 2-16: If an AMC that does not implement JTAG is connected to a µRTM that does the user **should** make sure that the µRTM JTAG signals are in a state that will not cause unintended JTAG operations.

2.2.3.2.1 Zone 3 ADF Connectors

REQ 2-17: Front boards **may** use ADF connectors in Zone 3 for connection to the µRTM.

REQ 2-18: Front boards designed with Zone 3 ADF connectors **shall** comply with the requirements of this section.

REQ 2-19: Front Board ADF receptacle connectors J30 and J31 **shall** be as defined in Appendix A.

REQ 2-20: The 20 pair ADF connector **may** be used on Mid-size and Full-size Modules.

REQ 2-21: The 30 pair ADF connector **may** be used on Mid-size and Full-size Modules.

REQ 2-22: The 40 pair ADF connector **may** be used on Full-size Modules.

Table 2-4: ADF Connector Compatibility Table

	Compact	Mid-size	Full-size
ADF 20 Pair	no	yes	yes
ADF 30 Pair	no	yes	yes
ADF 40 Pair	no	no	yes

¶ 11 Columns E, F, G, H, GndF and GndH are not available in the 20 pair version and therefore JTAG cannot be implemented. Columns G, H and GndH are not available in the 30 pair version. The 20 and 30 pair ADF connectors are detailed in Appendix A. The 40 pair ADF male is detailed in PICMG 3.0 R3.0 and the female in PICMG 3.8. (See Table 2-5 and Table 2-6.)

REQ 2-23: The ADF J30/RP30 connector **shall** have data, power and system management functions assigned to pins as shown in Table 2-5.

REQ 2-24: ADF connector J31 **may** be populated to afford extra data connectivity

¶ 12 Table 2-5 has the pin assignments for the J30/RP30 connectors. J31/RP31 are entirely user-defined (see Table 2-6). Both tables are for the 20, 30 and 40 pair ADF connectors.

REQ 2-25: Functions in rows 1 and 2 that are not used as shown **shall** be left unconnected

Table 2-5: J30/RP30 Pin Assignments

Col→ Row↓	GndH	H	G	GndF	F	E	GndD	D	C	GndB	B	A
10	GNDH10	H10	G10	GNDF10	F10	E10	GNDD10	D10	C10	GNDB10	B10	A10
9	GNDH9	H9	G9	GNDF9	F9	E9	GNDD9	D9	C9	GNDB9	B9	A9
8	GNDH8	H8	G8	GNDF8	F8	E8	GNDD8	D8	C8	GNDB8	B8	A8
7	GNDH7	H7	G7	GNDF7	F7	E7	GNDD7	D7	C7	GNDB7	B7	A7
6	GNDH6	H6	G6	GNDF6	F6	E6	GNDD6	D6	C6	GNDB6	B6	A6
5	GNDH5	H5	G5	GNDF5	F5	E5	GNDD5	D5	C5	GNDB5	B5	A5
4	GNDH4	H4	G4	GNDF4	F4	E4	GNDD4	D4	C4	GNDB4	B4	A4
3	GNDH3	H3	G3	GNDF3	F3	E3	GNDD3	D3	C3	GNDB3	B3	A3
2	GNDH2	H2	G2	GNDF2	TMS	TDI	GNDD2	SCL	MP	GNDB2	PWRB2	PWRA2
1	GNDH1	H1	G1	GNDF1	TDO	TCK	GNDD1	SDA	PS#	GNDB1	PWRB1	PWRA1
							20 Pair ADF Connector					
				30 Pair ADF Connector								
	40 Pair ADF Connector											

Notes: 1. The connector name prefix has been omitted in this table for readability. The JTAG, management and power pins have the µRTM_ prefix omitted in the table.

2. PS# is a short pin for last mate and first break.

3. JTAG is not available on 20 pair connector.

¶ 13 Connector designation and row/column number name the signal contacts. For example: J30-A5 would be the pin in the J30 connector, column A and row 5. Ground contacts are by row number and column where the column designator is the same as the adjacent signal column. RP31-GNDF6 would be the designator for connector RP31 grounds pin in ground column F row 6. For signals pins that have specific use the designator uses that signal name, *i.e.* J30-MP or RP30-PWRB2.

REQ 2-26: Each pair A/B, C/D, E/F and G/H **may** be used as a differential pair or as two individual single-ended signals.

REQ 2-27: If used as a differential signal pair A, C, E and G **shall** be assigned as positive/+ and B, D, F and H as negative/- signals.

¶ 14 The ground contacts, GNDx(n) of a row are connected together within the ADF connector. Unless referring to a specific ground pin in a connector this document uses the generic term GND. Note that in 20 pair ADF connectors only A, B, GndB, C, D, and GndD are in the connector. For the 30 pair ADF connectors A, B, GndB, C, D, GndD, E, F and Gnd F are in the connector.

REQ 2-28: All pins named 'GND' **shall not** be used for signals.

REQ 2-29: In the case of analog signals these GND contacts **may** be connected to a separate "analog ground" to control signal fidelity.

Table 2-6: J31/RP31 Pin Assignments

Col→ Row↓	GndH	H	G	GndF	F	E	GndD	D	C	GndB	B	A
10	GNDH10	H10	G10	GNDF10	F10	E10	GNDD10	D10	C10	GNDB10	B10	A10
9	GNDH9	H9	G9	GNDF9	F9	E9	GNDD9	D9	C9	GNDB9	B9	A9
8	GNDH8	H8	G8	GNDF8	F8	E8	GNDD8	D8	C8	GNDB8	B8	A8
7	GNDH7	H7	G7	GNDF7	F7	E7	GNDD7	D7	C7	GNDB7	B7	A7
6	GNDH6	H6	G6	GNDF6	F6	E6	GNDD6	D6	C6	GNDB6	B6	A6
5	GNDH5	H5	G5	GNDF5	F5	E5	GNDD5	D5	C5	GNDB5	B5	A5
4	GNDH4	H4	G4	GNDF4	F4	E4	GNDD4	D4	C4	GNDB4	B4	A4
3	GNDH3	H3	G3	GNDF3	F3	E3	GNDD3	D3	C3	GNDB3	B3	A3
2	GNDH2	H2	G2	GNDF2	F2	E2	GNDD2	D2	C2	GNDB2	B2	A2
1	GNDH1	H1	G1	GNDF1	F1	E1	GNDD1	D1	C1	GNDB1	B1	A1
							20 Pair ADF Connector					
				30 Pair ADF Connector								
	40 Pair ADF Connector											

Note: The connector name prefix has been omitted in this table for readability.

¶ 15: The 40 pair ADF connectors are defined in PICMG 3.0 R1.0 (receptacle) and PICMG 3.8 R1.0 (pin). The 20 and 30 pair ADF connectors are defined in this document.

2.2.3.2.2 Zone 3 Non ADF Connectors and Zone 3 Interface Repository

REQ 2-30: Front AMCs **may** use connectors other than ADF connectors in Zone 3.

REQ 2-31 Front AMC designers that use connectors other than ADF connectors in Zone 3 **should** submit a µRTM Zone 3 Interface repository entry to PICMG.

REQ 2-32: µRTM Zone 3 Interface repository entries **shall** specify what connectors are used in Zone 3 by the Front AMC.

REQ 2-33: µRTM Zone 3 Interface repository entries **shall** include mechanical drawings with Zone 3 connector locations for the Front AMC.

REQ 2-34: µRTM Zone 3 Interface repository entries **shall** specify the key/guide position used by the Front AMC.

REQ 2-35: µRTM Zone 3 Interface repository entries **shall** specify the Front AMC's Zone 3 connector pinout for the required management functions listed in Table 2-3.

¶ 16 µRTM_PS# in Table 2-3 is a short pin (see Section 2.2.3.2) and that last-mate/first-break function is necessary in a non-ADF connector for proper management operation.

REQ 2-36: µRTM Zone 3 Interface repository entries **shall** specify the electrical characteristics of other Zone 3 connector pins for the Front AMC.

2.2.4 AMC Face Plate

REQ 2-37: AMC Modules **shall** have a faceplate, including the latch and retention device, as specified in MicroTCA.1 R1.0, Section 2.5.

¶ 17 See also PICMG Rugged MicroTCA.1 R1.0, Appendix B for implementations of the retention device.

2.2.5 AMC Mid-size Module Component Envelope

¶ 18 The AMC Modules in this specification have the component envelope similar to that shown in AMC.0 R2.0, Figure 2-15 except as modified in Figure 2-2 below. This outline eliminates the stair stepping and makes the Mid-size Module outline similar to the Compact and Full-size Module outlines.

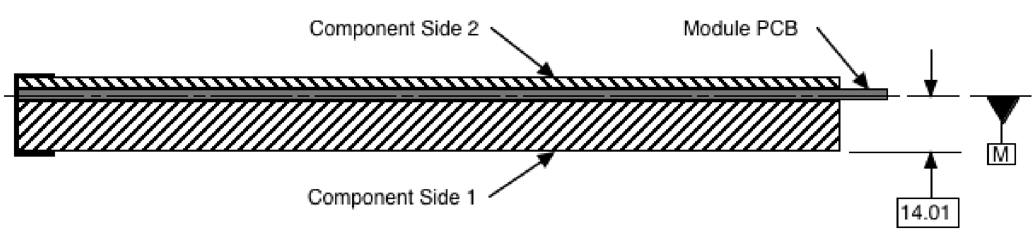


Figure 2-2: AMC Component Outline

2.2.6 AMC Test Dimensions

¶ 19 The test dimension for the depth of the assembly is the same as that in PICMG Rugged MicroTCA.1 R1.0. The projection of the Zone 3 ADF connector mating face beyond Datum J is an added dimension. The test dimensions from Datum L are to the edge of the ADF connector housing.

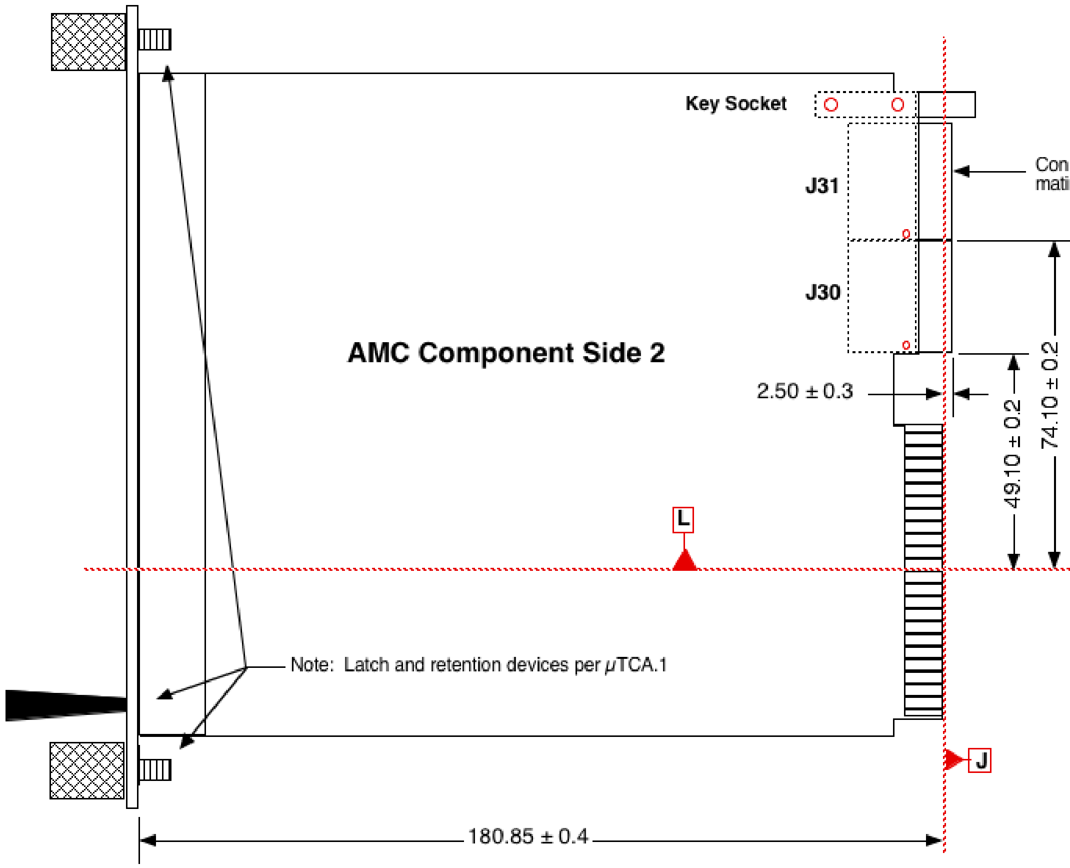


Figure 2-3: AMC Module Test Dimensions

2.3 µRTM Module

¶ 20 Construction of the µRTM is similar to the AMC in AMC.0 R2.0.

REQ 2-38: The panel and other hardware **shall** be rotated 180° about an axis perpendicular to the PCB so as to be compatible with existing hardware.

¶ 21 The 180º rotation places the latch in the upper left of the µRTM Module. Other hardware is similarly repositioned. All drawings are shown from side two of the PCB.

2.3.1 Printed Circuit Board

¶ 22 The µRTM is similar to the AMC front board in size. Figure 2-4 shows the board outline and the location of Zone 3 ADF connectors and the male alignment/key pin. As in the AMC specification there are reserved areas for hot swap switch, faceplate mounting hardware, and ESD zone along the top and bottom edge.

REQ 2-39 The PCB outline and pin 1 locations in Figure 2-4 **shall** be for µRTMs using ADF connectors.

REQ 2-40: Implementations using other connectors **may** have different positions for Pin 1 and different Zone 3 PCB edge details than those shown in Figure 2-4.

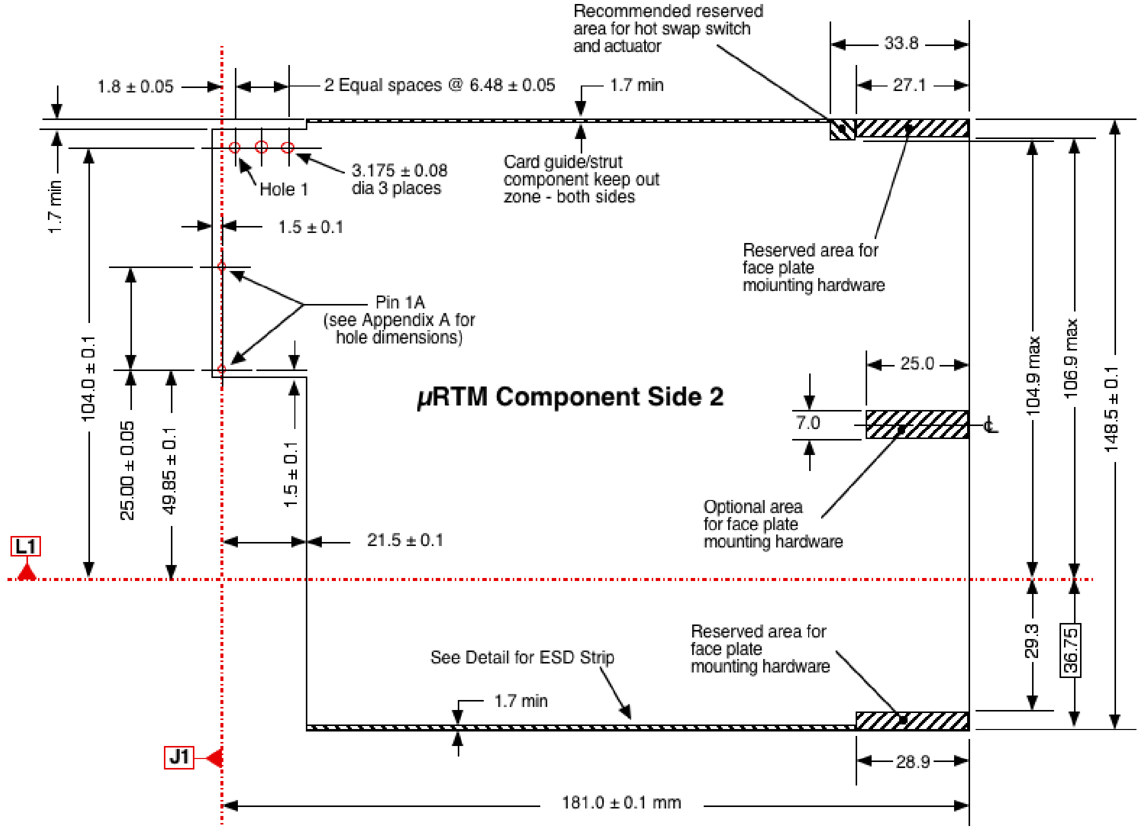


Figure 2-4: µRTM PCB Dimensions

Note: Datum L1 is collinear with Datum L in Figure 2-1 and Datum J1 is parallel to Datum J in Figure 2-1.

¶ 23 Dimensions for keep out and for mounting hardware are similar to AMC.0 R2.0, Figure 2-5 except for rotation of pattern from lower (upper) left to upper (lower) right.

¶ 24 The ESD strip shown in Figure 2-5 is similar to that specified in AMC.0, Section 2.2.1.4. The ESD segments are located only on component side 2 of the µRTM. The difference is that the strip is at the bottom of the µRTM rather than at the top as for the AMC Module.

REQ 2-41: The µRTM **shall** have ESD protection as shown in Figure 2-5.

¶ 25 Figure 2-5 shows the general dimension of the ESD strip on the lower part of the µRTM. Other dimensions of the PCB are in Figure 2-4. Segments 1, 2 and 3 are similar to those in AMC.0, Figure 2-8. More ESD data can be obtained from AMC.0, Section 2.2.1.4 and Section 4.4.

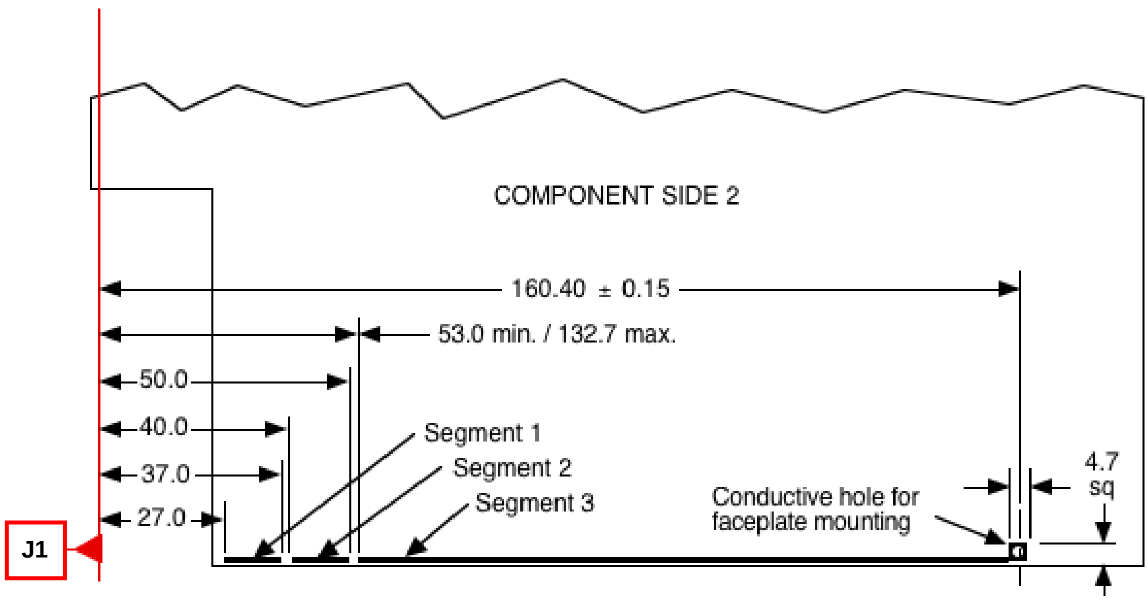


Figure 2-5: µRTM ESD Strip Dimensions

2.3.2 Zone 3 Keying

¶ 26 See this document Section 2.2.2 and Appendix B for other Key Information.

REQ 2-42: The µRTM Modules that mate with AMC Modules **shall** implement the male key/alignment mechanics as specified in Appendix B-1.

2.3.3 Zone 3 Connectors

2.3.3.1 ADF Connectors

REQ 2-43: The µRTMs **shall** position the Zone 3 ADF connector(s) according to the pin 1 location for each connector as shown in Figure 2-4.

REQ 2-44: The mounting hole pattern on the µRTM **shall** be as shown in Appendix A.

2.3.3.2 Non ADF Connectors and Zone 3 Interface Repository

REQ 2-45: µRTMs **may** use connectors other than ADF connectors in Zone 3.

REQ 2-46: µRTM designers that use connectors other than ADF connectors in Zone 3 **should** submit a µRTM Zone 3 Interface repository entry to PICMG.

REQ 2-47: µRTM Zone 3 Interface repository entries **shall** specify what connectors are used in Zone 3 by the µRTM.

REQ 2-48: µRTM Zone 3 Interface repository entries **shall** include mechanical drawings with Zone 3 connector locations for the µRTM.

REQ 2-49: µRTM Zone 3 Interface repository entries **shall** specify the key/guide position used by the µRTM.

REQ 2-50: µRTM Zone 3 Interface repository entries **shall** specify the µRTMs Zone 3 connector pinout for the required management functions listed in Table 2-3.

REQ 2-51: µRTM Zone 3 Interface repository entries **shall** specify the electrical characteristics of other Zone 3 connector pins for the µRTM.

2.3.4 µRTM Face Plate

REQ 2-52: µRTM Modules **shall** have a faceplate, including the latch and retention device, as specified in MicroTCA.1 R1.0, Section 2.5.

¶ 27 See also PICMG Rugged MicroTCA.1 R1.0, Appendix B for implementations of the retention device. The hardware is the same as for the AMC.0 R2.0, however, the mounting is reversed top to bottom. Figure 2-6 shows the reversed mounting for the LEDs and handle. Bar code and vendor label area is the same as shown in AMC.0 R2.0, Figure 2-20.

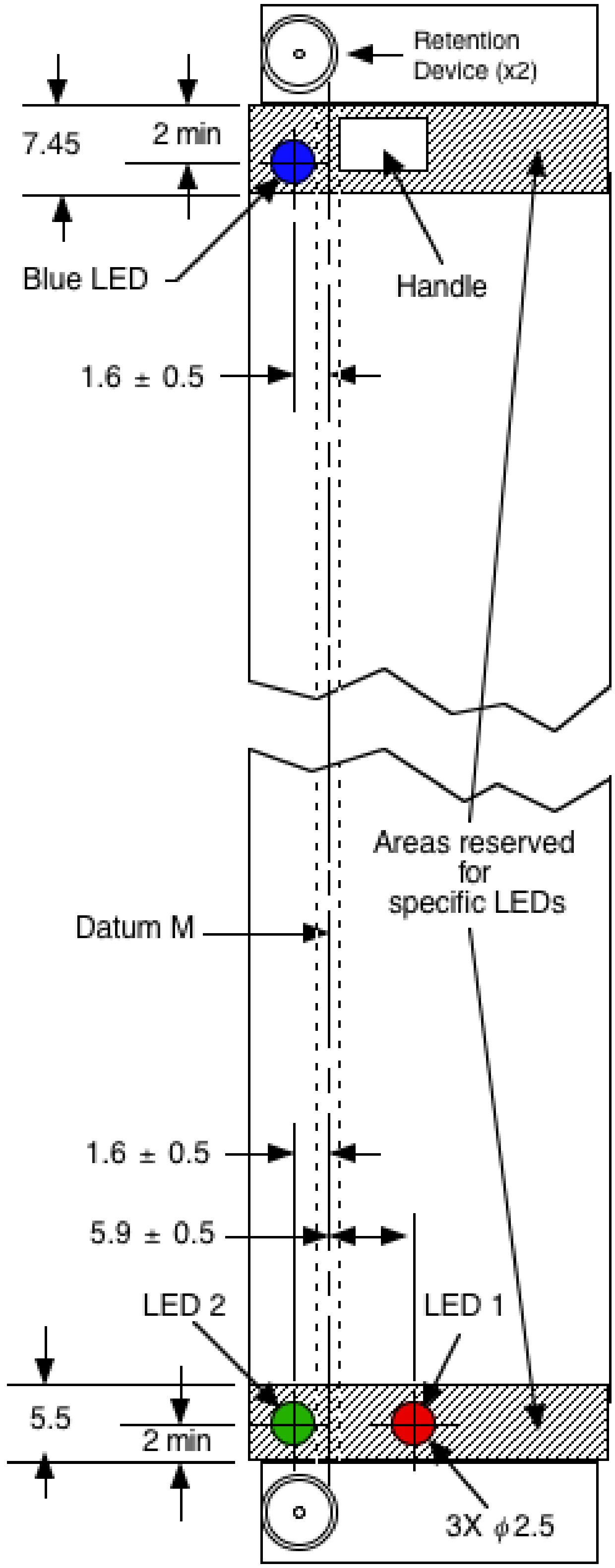


Figure 2-6: µRTM Face Plate

Note: the color of LED1 and LED2 can vary per AMC.0 R2.0, Section 2.2.4.1.

2.3.5 µRTM Module Component Envelope

REQ 2-53: µRTM modules **shall** use the same component height outline as AMC.0 R2.0, Figure 2-14, Figure 2-16 and Figure 2-15 as modified by Figure 2-2 in this document.

¶ 28 The Figures cited in REQ 2-53 do not include the ADF connector outlines. The connector outlines can be determined from PICMG 3.0 R1.0, PICMG 3.8 R1.0 and this document Appendix A as appropriate for the use.

¶ 29 The male ADF connector plastic housing extends beyond the Module panel by a nominal 0.33 mm on component Side 2. Since there is no metallic contact possible this overhang has been deemed by the committee to be acceptable.

2.3.6 µRTM Test Dimensions

REQ 2-54: µRTMs that implement ADF connectors **shall** meet the test dimensions in Figure 2-7.

¶ 30 Test dimensions from Datum L1 are to the edge of the ADF connector housing.

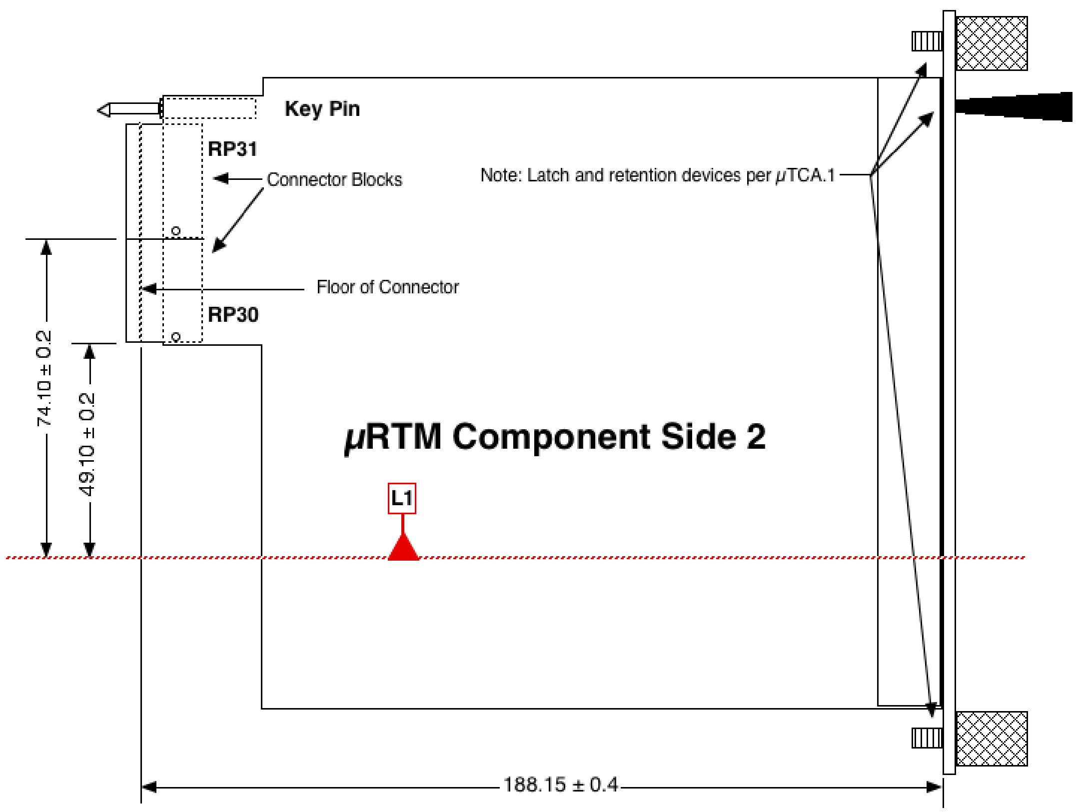


Figure 2-7: µRTM Module Test Dimensions

2.4 MicroTCA Subrack

¶ 31 In the broadest sense one can think of the MicroTCA Subrack as two subracks mated back-to-back. Obviously there is more to the subrack but this gives the user a way of viewing this section of the document.

2.4.1 Subrack Dimensions

¶ 32 Subrack specifications follow the MTCA.0 R1.0 specification. The AMC Modules and the front part of the subrack are fully compatible with the Double Modules of this specification. The rear of the subrack accommodates μRTM Modules specified in this document.

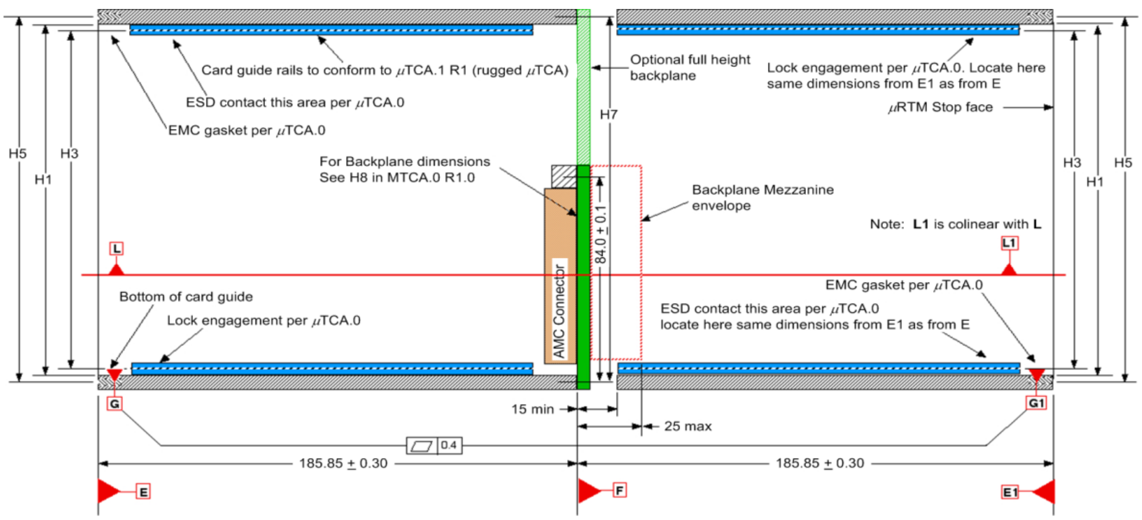


Figure 2-8: Side view of Subrack

Note: For missing dimensions see MTCA.0, Section 2.

REQ 2-55: Figure 2-8 side view drawing **shall** serve as the basis for designing the MicroTCA subrack.

REQ 2-56: Other manifestations of the subrack such as Pico, half width rack mounted, *etc* **shall** conform to the dimensions of Figure 2-8.

¶ 33 Subracks that have the modules mounted horizontally rather than vertically have certain constraints imposed by the module retention requirements. Such Subracks are not described in this document and may prove difficult to manufacture.

REQ 2-57: The backplane printed circuit board thickness **should** be 5 mm.

¶ 34 The height of the backplane is detailed in MTCA.0 R1, Table 2-10. The distance from L or L1 to the top of the backplane is one half of H8 for the single width entry in Table 2-10 when the AMC connects directly to the μRTM. The top support bar is included in the maximum backplane height for the single width case.

2.4.2 Insertion of Front and Rear Boards

REQ 2-58: When initially configuring modules in the MicroTCA subrack the following sequence **shall** be followed:

1. Insert the Front AMC Module of the AMC/µRTM pair
2. Fasten the retention device on the AMC panel to the subrack
3. Insert µRTM
4. Fasten the retention device on the µRTM panel to the subrack

¶ 35 After the initial configuration sequence specified in REQ 2-58, the removal and reinsertion of either the AMC Module or the µRTM Module will not require this sequence to be repeated.

REQ 2-59: If both the AMC and µRTM are removed then the insertion sequence in REQ 2-58 **shall** be repeated.

2.4.3 Subrack Test Dimensions

REQ 2-60: Subracks that conform to this specification **shall** meet the test dimensions in Figure 2-9.

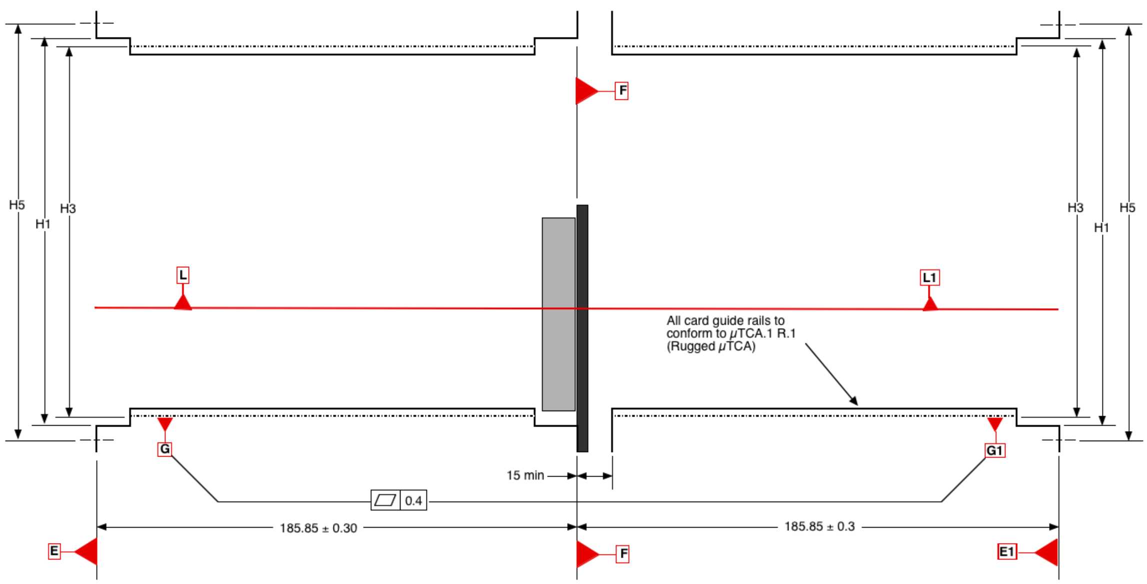


Figure 2-9: Test Dimensions for Subrack

¶ 36 Datum's L and L1 are collinear. For location of Datum L see MTCA.0, R1.0, Figure 2-29. The dimensions H1, H3 and H5 are defined in MTCA.0, R1.0, Section 2.7.1.

2.4.4 Subrack Cooling

Section 5.2 contains diagrams of airflow balancing modules that can be used when dealing with temporary, permanent or empty slots. The airflow requirements are also in Section 5.2.

2.4.5 Module sizes for subracks

¶ 37 Subracks can be constructed for any module size (Compact, Mid-size, or Full-size) or mixture of various sizes. Mid-size Modules can fit either the 2 or 3 row ADF connector in Zone 3. Full-size Modules can fit the 2, 3 or 4 row ADF connectors into Zone 3.

REQ 2-61: Modules without Zone 3 connectors, if used, **shall** have a µRTM Filler Module inserted in the rear of these units to block air flowing between the front and rear of the subrack.

¶ 38 It should be noted that there could be a slight interference between the adjacent modules gasket and the connector when inserting either the AMC or the µRTM. This interference only occurs as the inserted module passes the adjacent front panel and does not impact the other hardware on either board. This has not been deemed to be a problem (see Section 2.3.5).

2.4.6 Zone 3 Backplane

¶ 39 The subrack and AMC Module with ADF connectors are defined such that a backplane could be mounted in Zone 3 without modifying the AMC Module. The ADF connectors on the AMC Module would mate correctly with the vertical male ADF backplane connector. If a µRTM were also used with the Zone 3 backplane it would have to be modified.

¶ 40 MicroTCA.4 does not detail either the backplane or the µRTM that would be compatible with such a backplane.

This page intentionally left blank

3 Management

3.1 Overview

¶ 41 MicroTCA.4 systems extend the functionality of the MicroTCA.0 specification. This section defines the hardware platform management extensions required by MicroTCA.4 systems. The requirements from AMC.0 and MicroTCA.0 apply to MicroTCA.4 systems unless explicitly superseded by this specification.

3.2 µRTM Management Hardware

¶ 42 AMCs designed for MicroTCA.4 systems support a µRTM via Zone 3 connectors (see Section 2.1.3.2 and Section 2.3.3). The µRTM is managed by the MMC of the front AMC board. In order to detect a mismatched µRTM, a standardized management interface between the AMC and the µRTM is required.

¶ 43 The management interface between the AMC and the µRTM includes the following:

- Ground (GND)
- µRTM-PS#
- Management Power (µRTM-MP)
- I^2C bus
- Payload Power (µRTM-PWR)

¶ 44 In addition to the signals through the Zone 3 Interface, there are additional circuitry requirements for the AMC and the µRTM.

¶ 45 Figure 3-1 shows an example block diagram of the basic AMC and µRTM management circuitry.

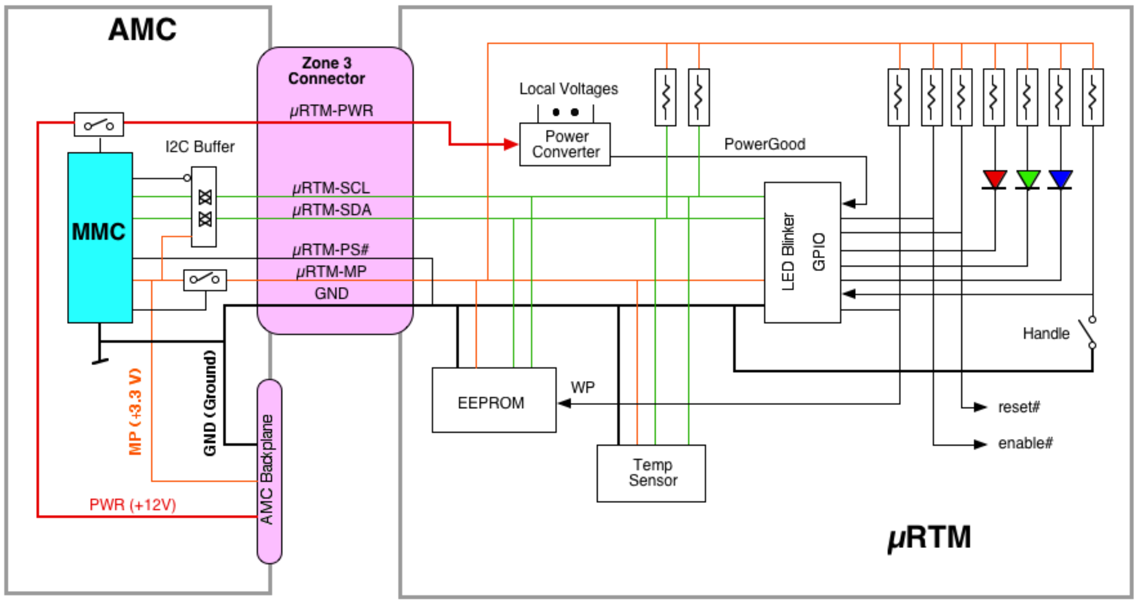


Figure 3-1: Example AMC/µRTM Management Block Diagram

3.2.1 µRTM-PS#

¶ 46 The µRTM-PS# signal is used to detect the presence of a µRTM.

REQ 3-1: The Front AMC **shall** pull-up µRTM-PS# to management power.

REQ 3-2: The µRTM **shall** connect µRTM-PS# to ground.

REQ 3-3: The Front AMC's MMC **shall** monitor the µRTM-PS# signal.

REQ 3-4: If the Zone 3 connectors do not guarantee µRTM-PS# to be a last mate contact, the MMC design **should** take precautions to ensure the µRTM is fully mated before considering the µRTM as present.

¶ 47 The precautions in REQ 3-4 about the lack of a short pin are design specific and are beyond the scope of this specification.

3.2.2 Management Power

¶ 48 Management Power (MP) is delivered to the µRTM through the Front AMC.

REQ 3-5: The Front AMC's MMC **should** gate MP to the µRTM.

3.2.3 I^{2}C Bus

REQ 3-6; The MMC **shall** provide an I^{2}C bus for connection to devices on the µRTM.

REQ 3-7: The AMC **should** provide a bi-directional buffer such as an LTC4307 or equivalent powered by MP to isolate the µRTM I^{2}C bus from the AMC's I^{2}C bus.

REQ 3-8: The µRTM **shall** provide an AT24C32A compatible serial EEPROM that contains the Platform Management FRU information of the µRTM.

REQ 3-9: This EEPROM **shall** be connected to the Front AMC MMC's I^{2}C port.

REQ 3-10: The address of the EEPROM **shall** be 50h.

REQ 3-11: If a larger SEEPROM is needed, devices up to 24C512 **may** be used, as they are software compatible with the 24C32.

¶ 49 Although SMBus is very similar to I^{2}C, there are minor differences. Some SMBus devices might appear to work, but might occasionally cause errors. I^{2}C compatibility is required.

3.2.4 Hot Swap Handle

¶ 50 A Hot Swap ejector handle switch is used to notify the MMC when the µRTM can proceed from Hot Swap state M1 to M2 during an insertion and from Hot Swap state M4 to M5 during an extraction. Because incompatible µRTMs do not proceed beyond the M1 state, a standardized interface for reading the hot swap ejector handle state is not needed.

REQ 3-12: The µRTM **shall** provide a Hot Swap ejector handle switch readable by a compatible AMC's MMC.

3.2.5 µRTM LEDs

¶ 51 Like an AMC, the µRTM provides a Blue Hot Swap LED, LED1 and optionally LED2.

REQ 3-13: The µRTM **shall** provide a Blue Hot Swap LED as defined in AMC.0.

REQ 3-14: The Blue Hot Swap LED **shall** be powered from MP.

REQ 3-15: The Blue Hot Swap LED **shall** power up in the on state.

REQ 3-16: The Blue Hot Swap LED **shall** be controllable by a compatible AMC's MMC.

REQ 3-17: The µRTM **shall** provide LED1 as defined by AMC.0.

REQ 3-18: LED1 **shall** be controllable by a compatible AMC's MMC.

REQ 3-19: The µRTM **should** provide LED2 as defined by AMC.0.

REQ 3-20: LED2, if implemented, **shall** be controllable by a compatible AMC's MMC.

¶ 52 The hardware interface between the AMC's MMC and the µRTM's LEDs is not defined in this specification. A design can choose to use dedicated pins in the Zone 3 interface or can provide an I^2C-based interface. It should be noted, however, that many MMC firmware implementations cannot generate steady blink rates for LEDs connected to I^2C-based GPIO devices. It is recommended that I^2C-based designs use LED blinker devices rather than simple GPIO to drive the LEDs.

REQ 3-21: µRTMs that control the LEDs via I^2C **should** use LED drivers with programmable blink rate and duty cycle.

3.2.6 Payload Power

¶ 53 Payload power is delivered to the µRTM through the Front AMC.

REQ 3-22: The Front AMC's MMC **shall** gate Payload Power to the µRTM.

REQ 3-23: The MMC **shall** only enable Payload Power to the µRTM as defined in Section3.5.

¶ 54 Payload Power is delivered to the µRTM as PWR (nominally 12V) minus a small voltage drop due to the PWR switching on the AMC (see Section 4.2.2).

REQ 3-24: If a µRTM requires other voltages, the µRTM **shall** provide any necessary voltage conversion circuitry.

3.2.7 µRTM Reset

¶ 55 Some µRTM designs require a reset signal. This can be implemented using a dedicated Zone 3 pin, an I^2C-based implementation, or some other design-specific mechanism.

3.2.8 Zone 3 Interface Enable

¶ 56 Many µRTM designs require a Zone 3 interface enable signal. This enable signal can be implemented using a dedicated Zone 3 pin, an I^2C-based implementation, or some other design-specific mechanism.

3.2.9 µRTM Temperature Sensor

REQ 3-25: The µRTM **shall** provide at least one temperature sensor readable by the Front AMC's MMC.

REQ 3-26: The temperature sensor **should** monitor the most temperature critical component on the µRTM.

REQ 3-27: The temperature sensor **may** be connected to the I^2C bus or **may** be connected using user I/O.

¶ 57 Information on Sensor Types and Data Conversion can be found in IPMIv2.0. The user is cautioned to check for IPMI addenda, errata and revisions as posted.

3.3 FRU Device IDs

¶ 58 The AMC.0 specification requires AMCs to implement a single FRU device ID of 0. Because the µRTM needs to be managed as an independent FRU, this specification requires the MMC to implement two specific FRU device IDs.

REQ 3-28: The MMC **shall** implement FRU Device ID 0 to represent the Front AMC.

REQ 3-29: In MicroTCA.4 environments, the MMC **shall** implement FRU Device ID 1 to represent its µRTM.

REQ 3-30: In response to a Get PICMG Properties command, the MMC **shall** report a *Max FRU Device ID* of 1.

REQ 3-31: The MMC **shall** provide a FRU Device Locator record in its SDRs for the µRTM.

REQ 3-32: This FRU Device Locator record **shall** report the µRTM as having an Entity ID of PICMG Rear Transition Module (COh).

REQ 3-33: The MMC **shall** implement the Get Device Locator Record ID command as defined in the AMC.0 specification.

REQ 3-34: The Carrier Manager **shall** map each AMC's FRU Device ID 0 (Front AMC) to Carrier Manager relative FRU Device IDs 5-39 as defined in MicroTCA.0.

REQ 3-35: The Carrier Manager **shall** map each AMC's FRU Device ID 1 (µRTM) to Carrier Manager relative FRU Device IDs 90-124.

3.4 MicroTCA Carrier Information

¶ 59 The MicroTCA Carrier Information record includes a list of Slot Entries for each FRU in the MicroTCA Carrier. Each Slot Entry specifies the Site Type and Site Number as well as physical location coordinates.

REQ 3-36: Slot Entries corresponding to µRTMs **shall** have their *Site Type* field set to a value of 09h (Rear Transition Module as defined in the PICMG 3.0 R1.0 specification).

REQ 3-37: Slot Entries corresponding to µRTMs **shall** have their *Site Number, Origin X, and Origin Y* fields set to the same values as the respective fields in the associated Front AMC's Slot Entry.

¶ 60 This means that the Origin X and Origin Y fields are relative to the lower left corner when viewed from the front of the Carrier and are relative to the lower right corner when viewed from the rear of the Carrier.

3.5 Operational State Management

¶ 61 Hot swap of µRTMs is handled very similarly to hot swap of AMCs. The Front AMC's MMC implements two Module Hot Swap sensors, one for the Front AMC and one for the µRTM. The Carrier Manager implements FRU Hot Swap sensors for each Front AMC and each µRTM. Additionally, the Carrier Manager maps FRU IDs to the µRTMs, maps sensors to µRTM sensors, *etc*.

¶ 62 The following sections provide more details about operational state management for µRTMs.

3.5.1 Typical µRTM Insertion Process

¶ 63 The following sequence is recommended when inserting a µRTM in a system.

1) The µRTM is inserted and µRTM-PS# is asserted.
2) When the MMC detects µRTM-PS# asserted by the µRTM, it enables µRTM-MP to the µRTM and the µRTM's management circuitry is powered.
3) The µRTM's Blue LED defaults to On.
4) The MMC enables the Module Hot Swap sensor associated with the µRTM, and generates a Module Hot Swap sensor (µRTM Present) event.
5) The Carrier Manager changes the Hot Swap state for the µRTM from M0 to M1.

6) The MMC performs a compatibility check as described in Section 1 and generates a Module Hot Swap sensor (µRTM Compatible or µRTM Incompatible) event.

7) If the µRTM was determined to be incompatible with the Front AMC, the insertion process is complete and the µRTM is left in the M1 state. If the µRTM was determined to be compatible with the Front AMC, the insertion process continues.

8) The user closes the µRTM hot swap handle.

9) When the MMC detects the µRTM's hot swap handle is closed, it generates a Module Hot Swap sensor (Handle Closed) event from the Module Hot Swap sensor associated with the µRTM.

10) The Carrier Manager changes the Hot Swap state for the µRTM from M1 to M2 and sends a Set FRU LED (Blue LED Long Blink) command to the MMC for FRU ID 1.

11) The MMC sets the µRTM's Blue LED to long blink.

12) The MMC enables the remaining sensors associated with the µRTM.

13) The Carrier Manager creates local sensors that map to each sensor associated with the µRTM.

14) The Carrier Manager, Shelf Manager or System Manager sends a Set FRU Activation (Activate) command to the Carrier Manager.

15) The Carrier Manager changes the Hot Swap state for the µRTM from M2 to M3.

16) The Carrier Manager sends a Set Power Level (Level=1) command to the MMC for FRU ID 1.

17) The MMC enables payload power to the µRTM.

18) The Carrier Manager changes the Hot Swap state for the µRTM from M3 to M4.

19) The MMC enables the µRTM and AMC Zone 3 Interfaces.

20) The Carrier Manager sends a Set FRU LED (Blue LED Off) command to the MMC for FRU ID 1.

21) The MMC turns off the µRTM's Blue LED.

3.5.2 Typical µRTM Extraction Process

¶ 64 The following sequence is recommended when removing a µRTM from a system.

1) The user opens the µRTM hot swap handle
2) When the MMC detects the µRTM's hot swap handle is open, it generates a Module Hot Swap sensor (Handle Open) event from the Module Hot Swap sensor associated with the µRTM.
3) The Carrier Manager changes the Hot Swap state for the µRTM from M4 to M5 and sends a Set FRU LED (Blue LED Short Blink) command to the MMC for FRU ID 1.
4) The MMC sets the Blue LED to short blink.
5) The System Manager, Shelf Manager or Carrier Manager sends a Set FRU Activation (Deactivate) command to the Carrier Manager
6) The Carrier Manager changes the Hot Swap state for the µRTM from M5 to M6 and sends the FRU Control (Quiesce) command to the MMC for FRU ID 1.
7) The MMC takes any design specific action to quiesce the Zone 3 Interface. Refer to Section 1 for more details.
8) The MMC disables the µRTM and AMC Zone 3 Interfaces and generates a Module Hot Swap sensor (Quiesced) event from the Module Hot Swap sensor associated with the µRTM.
9) The Carrier Manager sends a Set Power Level (Level=0) command to the MMC for FRU ID 1.
10) The MMC disables payload power to the µRTM.
11) The Carrier Manager changes the Hot Swap state from M6 to M1, and sends a Set FRU LED (Blue LED On) command to the MMC for FRU ID 1.
12) The MMC turns on the µRTM's Blue LED.
13) The user extracts the µRTM.
14) When the MMC detects µRTM-PS# is de-asserted, the MMC disables all the sensors associated with the µRTM except the Module Hot Swap sensor, disables the µRTM's MP, generates a Module Hot Swap sensor (µRTM Absent) event, and then disables the Module Hot Swap sensor associated with the µRTM.
15) The Carrier Manager changes the Hot Swap state for the µRTM from M1 to M0 and deletes all local sensors associated with the µRTM.

3.5.3 FRU Hot Swap and Module Hot Swap Sensors

¶ 65 The Carrier Manager manages the hot swap state for µRTMs similarly to how it manages the hot swap state for AMCs.

REQ 3-38: The Carrier Manager **shall** implement a FRU Hot Swap sensor as defined in the PICMG 3.0 R1.0 specification for each µRTM.

¶ 66 µRTMs are hosted by the MMC on the Front AMC.

REQ 3-39: The MMC **shall** implement a Module Hot Swap sensor for the µRTM in addition to the Module Hot Swap sensor for the AMC.

REQ 3-40: The Module Hot Swap sensor associated with the µRTM **shall** generate events as defined in Table 3-1.

REQ 3-41: The Module Hot Swap sensor associated with the µRTM **shall** respond to Get Sensor Reading commands as defined in Table 3-2.

Table 3-1: Module Hot Swap Event Message

Data Type	Byte	Data Field
Request Data	1	*Event Message Rev* = 04h (IPMI specification)
Request Data	2	*Sensor Type* – F2h (Module Hot Swap)
Request Data	3	*Sensor Number* = xxh (Implementation specific)
Request Data	4	*Event Direction (bit 7)* = 0b (Assertion) Event Type [6:0] = 6Fh (Generic Availability)
Request Data	5	Event Data 1 [7:4] = 00h (unspecified Event Data 2 and 3) [3:0] = Current Event 0 = Module Handle Closed 1 = Module Handle Opened 2 = Quiesced 3 = Backend Power Failure 4 = Backend Power Shut Down 5 = µRTM Present[1] 6 = µRTM Absent[1] 7 = µRTM Compatible[1] 8 = µRTM Incompatible[1] 9-Fh = Reserved
Request Data	6	*Event Data 2* = FFh or not present
Request Data	7	*Event Data 3* = FFh or not present
Response Data	1	*Completion Code*

Note 1: Only applicable to Module Hot Swap sensors associated with µRTMs or Module Hot Swap sensors associated with other module types, write as 0b and ignore on read.

Table 3-2: Get Sensor Reading (Module Hot Swap sensor)

Data Type	Byte	Data Field
Request Data	1	*Sensor Number* (FFh = reserved)
Response Data	1	*Completion Code*
Response Data	2	*Sensor Reading* [7:0] Not Used. Write as 00h.
Response Data	3	*Standard IPMI byte* (See "Get Sensor Reading" in the IPMI specification): [7] – 0b = All Event Messages disabled from this sensor [6] – 0b = Sensor scanning disabled [5] – 1b = Initial update in progress. This bit is set to indicate that a "Re-Arm Sensor Events" or "Set Event Receiver" command has been used to request an update of the sensor status, and that update has not occurred yet. Software should use this bit to avoid getting an incorrect status while the first sensor update is in progress. This bit is only required if it is possible for the MMC to receive and process a "Get Sensor Reading" or "Get Sensor Event Status" command for the sensor before the update has completed. This is most likely to be the case for sensors, such as fan RPM sensors, that may require seconds to accumulate the first reading after a re-arm. [4:0] Reserved. Ignore on read.
Response Data	4	*Current State Mask* [7] – 1b = µRTM Compatible[1] [6] – 1b = µRTM Absent[1] [5] – 1b = µRTM Present[1] [4] – 1b = Backend Power Shut Down [3] – 1b = Backend Power Failure [2] – 1b = Quiesced [1] – 1b = Module Handle Opened [0] – 1b = Module Handle Closed
Response Data	(5)[2]	[7] – Reserved. Write as 1b. Ignore on read. [6:1] – Reserved. Write as 0b. Ignore on read. [0] – 1b = µRTM Incompatible[1]

Note 1: Only applicable to Module Hot Swap sensors associated with µRTMs. For Module Hot Swap sensors associated with other module types, write as 0b and ignore on read.

Note 2: Required for Module Hot Swap sensors associated with µRTMs. This is optional for all other module types.

REQ 3-42: The Front AMC's MMC **shall** enable and disable the Module Hot Swap sensor associated with the μRTM as defined in Section 3.5.6.

REQ 3-43: When the MMC detects that the μRTM is present, after enabling the Module Hot Swap sensor associated with the μRTM, the MMC **shall** generate a Module Hot Swap (μRTM Present) event from the Module Hot Swap sensor associated with the μRTM.

REQ 3-44: When the MMC detects that the μRTM is no longer present, before disabling the Module Hot Swap sensor associated with the μRTM, the MMC **shall** generate a Module Hot Swap (μRTM Absent) event from the Module Hot Swap sensor associated with the μRTM.

REQ 3-45: The MMC **shall** support μRTM Compatible and μRTM Incompatible states and events as defined in Section 3.5.5.

REQ 3-46: The MMC **shall** support other Module Hot Swap sensor states and events as defined in the AMC.0 specification.

3.5.4 FRU Activation and Deactivation

¶ 67 The MicroTCA Carrier Activation and Current Descriptor record includes a MicroTCA Carrier Activation and Current Descriptor for each FRU connected to a Power Channel. The MicroTCA Carrier Activation and Current Descriptor specifies the current limitations of the Power Channel and whether the System Manager, Shelf Manager or Carrier Manager is responsible for activating and deactivation the corresponding FRU.

REQ 3-47: μRTMs **shall** be listed in the MicroTCA Carrier Activation and Current Descriptor record.

REQ 3-48: MicroTCA Carrier Activation and Current Descriptors corresponding to μRTMs **shall** have their *Site Type* field set to a value of 09h (Rear Transition Module as defined in the PICMG 3.0 R3.0 specification).

REQ 3-49: Because μRTMs do not directly connect to Power Channels, MicroTCA Carrier Activation and Current Descriptors corresponding to μRTMs **shall** have their *Power Channel* and *Maximum Channel Current* fields set to 0.

REQ 3-50: Each MicroTCA Carrier Activation and Current Descriptor corresponding to a μRTM **shall** be listed after the associated Front AMC's MicroTCA Carrier Activation and Current Descriptor in the MicroTCA Carrier Activation and Current Descriptor record.

¶ 68 It should be noted that μRTMs receive their power via the Front AMC. If a Front AMC is deactivated, its Payload Power will be disabled; in this case, the μRTM connected to that AMC will also have its Payload Power disabled.

REQ 3-51: A System Manager, Shelf Manager, or Carrier Manager **may** implement an activation/deactivation policy that activates Front AMCs prior to µRTMs and deactivates µRTMs prior to Front AMCs.

3.5.5 Compatibility Check

¶ 69 The Zone 3 Interface connecting the Front AMC and the µRTM has a few standardized pins for basic management, but most of the pins are user defined. In order to help prevent damage if an AMC is connected to an incompatible µRTM, a compatibility check is performed to determine if the AMC and µRTM are compatible with each other.

¶ 70 The result of the compatibility check is reported via the µRTM Compatible and µRTM Incompatible state bits in the Module Hot Swap sensor. Additionally, incompatible µRTMs are left in the M1 Hot Swap state so Payload Power and the Zone 3 Interface are never enabled unless the AMC and µRTM are determined to be compatible.

¶ 71 The MMC performs the compatibility check by reading Zone 3 Interface Compatibility records from the AMC's FRU information and from the µRTM's FRU information. If matching records are found, the AMC and µRTM are considered as compatible. If matching records are not found, then the AMC and µRTM are considered incompatible.

Table 3-3: Zone 3 Interface Compatibility record

Offset	Length	Field description
0	1	*Record Type ID*. Value C0h (OEM).
1	1	[7:7] End of list. Set to one for the last record. [6:4] Reserved, write as 0h. [3:0] Record format version (=2h for this definition).
2	1	*Record Length*.
3	1	*Record Checksum*. Holds the zero checksum of the record.
4	1	*Header Checksum*. Holds the zero checksum of the header.
5	3	*Manufacturer ID*. For this specification the value is 12634 (0x00315A, LSB first)
8	1	*PICMG Record ID*. Value 30h.
9	1	*Record Format Version*. Value 1h.
10	1	*Type of Interface Identifier*: 0h = PICMG IRTM.0 REP Number (see Table 3-4) 1h = Other PICMG Specification-defined Interface Identifier (see Table 3-5) 2h = Interface Identifier GUID (see Table 3-6) 3h = OEM interface identifier (see Table 3-7) 4h = PICMG MTCA.4 REP Number (see Table 3-8) 5h-FFh = Reserved
11	N	*Interface Identifier Body* (format depends on the type), terminated by the end of record.

¶ 72 An Interface identifier body of type 0 (PICMG IRTM.0 REP Number) is not applicable for an AMC/µRTM because µRTMs are explicitly not IRTM.0 R1.0 compliant. The PICMG IRTM.0 REP Number format in Table 3-4 is listed here only for completeness.

Table 3-4: PICMG IRTM.0 REP Number

Offset	Length	Field description
11	4	The IRTM.0 REP number, 32 bits, LS byte first

¶ 73 An Interface identifier body of type 1 (Other PICMG specification-defined interface identifier) has the format in Table 3-5:

Table 3-5: Other PICMG Specification-defined Interface Identifier

Offset	Length	Field description
11	4	The PICMG specification unique identifier, LS byte first (format TBD by other interface specs)
15	1	The PICMG specification major revision number
16	1	The PICMG specification minor revision number
17	M	The opaque interface identifier body

¶ 74 The interface Identifier Body of type 2 (Interface identifier GUID) has the format in Table 3-6.

Table 3-6: Interface identifier GUID

Offset	Length	Field description
11	16	Interface identifier GUID, LS byte first. Globally Unique Identifier generated in accordance with AMC.0.

¶ 75 An Interface Identifier Body of type 3 (OEM interface identifier) has the format in Table 3-7.

Table 3-7: Interface identifier OEM

Offset	Length	Field description
11	3	Manufacturer ID (IANA) of the OEM that owns the definition of this interface. LS Byte first.
14	4	OEM-defined interface designator, 32 bits, LS byte first.

¶ 76 An Interface identifier body of type 4 (PICMG MTCA.4 REP Number, see Table 3-3) is used for an AMC/µRTM that has a connector set defined in the PICMG µRTM repository.

Table 3-8: PICMG MTCA.4 REP Number

Offset	Length	Field Description
11	4	The MTCA.4 REP Number, 32 bits, LS byte first

REQ 3-52: AMCs and µRTMs **shall** provide at least one Zone 3 Interface Compatibility record in their FRU information.

REQ 3-53: When the MMC detects a µRTM is present, the MMC **shall** perform a compatibility check.

REQ 3-54: If any Zone 3 Interface Compatibility record in the µRTM's FRU information matches any Zone 3 Interface Compatibility record in the AMC's FRU information, the AMC and µRTM **shall** be considered compatible, otherwise the AMC and µRTM **shall** be considered incompatible.

REQ 3-55: Zone 3 Interface compatibility records **shall** be considered as matching if the records are the same length and are identical from Offset 9 through the end of the records, otherwise, the records **shall** be considered as not matching.

REQ 3-56: After performing the compatibility check, the MMC **shall** generate a Module Hot Swap sensor event indicating the result of the compatibility check.

3.5.6 Sensor Management

¶ 77 µRTM sensors are dynamically populated or depopulated on the MMC when the µRTM is detected as present or absent. Similarly, the Carrier Manager dynamically populates and depopulates local sensor mapped to the µRTM sensors when µRTM presence or absence is reported via the Module Hot Swap sensor events.

REQ 3-57: When the Front AMC's MMC detects that a µRTM is present, the MMC **shall** enable the Module Hot Swap sensor for the µRTM.

REQ 3-58: When the MMC determines that the µRTM is compatible with the Front AMC, the MMC **shall** enable any additional µRTM sensors.

REQ 3-59: When the MMC detects that the µRTM is no longer present it **shall** disable all µRTM sensors except for the Module Hot Swap sensor associated with the µRTM.

REQ 3-60: The MMC **shall** disable the Module Hot Swap sensor associated with the µRTM after generating the Module Hot Swap (µRTM Absent) event.

REQ 3-61: The MMC **shall** provide an SDR for the Module Hot Swap sensor associated with the µRTM.

¶ 78 This allows the MMC to provide a Module Hot Swap sensor for the µRTM regardless of the result of the compatibility check. Although it is likely that the MMC also provides the SDRs for other µRTM sensors, the exact implementation of µRTM sensor SDRs is design-specific and is beyond the scope of this specification.

REQ 3-62: The SDRs for sensors associated with the µRTM **shall** use the PICMG Rear Transition Module entity ID COh and the AMC's site number + 60h as a device-relative entity instance number.

3.5.7 Quiesce Actions

REQ 3-63: When the Front AMC's MMC receives a FRU Control (Quiesce) command with FRU Device ID set to 1, the MMC **shall** take appropriate action (implementation specific) to bring the Zone 3 interface to a quiesced state and generate a Module Hot Swap (Quiesced) event from the Module Hot Swap sensor associated with the µRTM.

REQ 3-64: If the µRTM is determined to be compatible and the µRTM supports a Zone 3 Interface enable mechanism, the MMC **shall** disable the Zone 3 Interface after it is quiesced, but before generating the Module Hot Swap sensor (Quiesced) event.

¶ 79 Because the Zone 3 Interface is mostly user defined pins, the actions needed to quiesce the Zone 3 Interface can vary greatly from one design to another. In the simplest cases, there might not be any action required. In other cases some or all of the user defined pins may need to be isolated, and in some cases, all or part of the Front AMC might even need to be powered off under MMC control. The specific actions needed are design specific and are beyond the scope of this specification.

3.6 Power Management

REQ 3-65: The Front AMC's Module Current Requirements record **shall** include the power required for any compatible µRTM.

REQ 3-66: If a µRTM is determined to be incompatible, the MMC **shall not** enable Payload Power to the µRTM.

REQ 3-67: If a µRTM is determined to be compatible, upon receipt of a Set Power Level (Level = 1, FRU Device ID = 1) command, the MMC **shall** enable Payload Power to the µRTM.

REQ 3-68: If the µRTM supports a Zone 3 Interface enable mechanism, the MMC **shall** enable the Zone 3 Interface after enabling Payload Power to the µRTM.

REQ 3-69: Upon receipt of a Set Power Level (Level = 0, FRU Device ID = 1) command, the MMC **shall** disable Payload Power to the µRTM.

¶ 80 Disabling the Zone 3 Interface happens as part of the quiesce actions as defined in Section 3.5.7.

3.7 Cooling Management

¶ 81 To reduce power consumption and noise, and maintain the temperature of critical devices on MTCA.4 µRTMs, it may be desirable to independently control the speed of the fans that cool the AMCs and µRTMs.

¶ 82 The Shelf Manager needs a method to determine if the Cooling Units implement independent control of the µRTM fans. The ATCA Get Fan Speed Properties command has been enhanced to include a response bit that indicates that µRTM Fan Control Supported.

¶ 83 The Shelf Manager also needs a method to independently control the µRTM fan level. The ATCA Get Fan Level and Set Fan Level commands have been modified so that a Cooling Unit that supports independent control of the µRTM fans can determine if the command is for the AMC or the µRTM fans.

¶ 84 The physical implementation of the MTCA.4 Cooling Unit is not defined in this specification.

REQ 3-70: An MTCA.4 chassis that supports µRTMs **may** support independent speed control of the AMC and µRTM fans.

REQ 3-71: MTCA.4 Cooling Units that support independent speed control of the AMC and µRTM fans **shall** implement the Get Fan Speed Properties Response Byte 6 as described in Table 3-9.

REQ 3-72: MTCA.4 Cooling Units that support independent speed control of the AMC and µRTM fans **shall** implement the Get Fan Level and Set Fan Level commands as described in Tables 3-10 and 3-11.

¶ 85: Table 3-9 has the additions to PICMG 3.0 R3.0 Table 3-86 in the Request Data byte 2 to implement RTM Fan speed control. The additions have a light yellow background.

Table 3-9: MTCA.4 Get Fan Speed Properties

Data Type	Byte	Data Field
Request Data	1	*PICMG Identifier*. Indicates that this is a PICMG-defined group extension command. A value of 00h is used.
	2	If the Fan Tray does **not support** RTM Fan control: *FRU Device ID.* Indicates the FRU device for which the command is intended. If the Fan Tray **supports** RTM Fan control: [7] – *RTM Fan Speed Properties.* This bit is set to 1b to indicate that the Get Fan Speed Properties query is for the RTM fans. This bit is set to 0b to indicate that the Get Fan Speed Properties query is for the front fans. [6..0] – *FRU Device ID.* Indicates the FRU device for which the command is intended.
Response Data	1	*Completion Code*
	2	*PICMG Identifier*. Indicates that this is a PICMG-defined group extension command. A value of 00h is used.
	3	*Minimum Speed Level.* This field describes the minimum setting that is accepted by the *Set Fan Level* command.
	4	*Maximum Speed Level*. This field describes the maximum setting that is accepted by the *Set Fan Level* command.
	5	*Normal Operating Level.* This field represents the default normal fan speed recommended by the fan manufacturer.
	6	*Fan Tray Properties.* This field holds properties of the Fan Tray. [7] – *Local Control Mode Supported.* This bit is set to 1b if the Fan Tray supports automatic adjustment of the fan speed. [6:0] – *Reserved*

¶ 86: Table 3-10 has the additions to PICMG 3.0 R3.0 Table 3-87 in the Request Data byte 2 to implement RTM Fan speed control. The additions have a light yellow background.

Table 3-10: Get Fan Level command

Data Type	Byte	Data Field
Request Data	1	*PICMG Identifier*. Indicates that this is a PICMG-defined group extension command. A value of 00h is used.
	2	If the Fan Tray does **not support** RTM Fan control: *FRU Device ID.* Indicates the FRU device for which the command is intended. If the Fan Tray **supports** RTM Fan control: [7] – *RTM Fan Level.* This bit is set to 1b to indicate that the Get Fan Level query is for the RTM fans. This bit is set to 0b to indicate that the Fan Level query is for the front fans. [6..0] – *FRU Device ID*. Indicates the FRU device for which the command is intended.
Response Data	1	*Completion Code*
	2	*PICMG Identifier*. Indicates that this is a PICMG-defined group extension command. A value of 00h is used.
	3	*Override Fan Level*. Indicates the fan level that the Shelf Manager has selected, which must be in the range *Minimum Speed Level* to *Maximum Speed Level*, or equal to FEh or FFh. FEh = Fan has been placed in “Shut Down” by the Shelf Manager FFh = Fan operating in Local Control mode
	(4)	*Local Control Fan Level*. This byte is optional if the Fan Tray does not support Local Control. When present, this byte always indicates the Local Control fan level as determined by the Fan Tray controller. When Local Control is supported, the actual fan level is: 1) the value of this byte if Override Fan Level is FFh, or 2) the larger of this byte and Override Fan Level if Local Control Enable State is 01h, 3) the value of Override Fan Level if Local Control Enable State is 00h, or 4) Shut Down if either Override Fan Level or this byte has a value FEh.
	(5)	*Local Control Enable State*. This byte is omitted if the Fan Tray does not support Local Control. When present, this byte indicates the Local Control State. A value of 0 indicates that Local Control mode is disabled and a value of 1 indicates Local Control mode is enabled.

¶ 87: Table 3-11 has the additions to PICMG 3.0 R3.0 Table 3-88 in the Request Data byte 2 to implement RTM Fan speed control. The additions have a light yellow background.

Table 3-11: Set Fan Level command

Data Type	Byte	Data Field
Request Data	1	*PICMG Identifier*. Indicates that this is a PICMG-defined group extension command. A value of 00h is used.
	2	If the Fan Tray does **not support** RTM Fan control: *FRU Device ID.* Indicates the FRU device for which the command is intended. If the Fan Tray **supports** RTM Fan control: [7] – *RTM Fan Level.* This bit is set to 1b to indicate that the Set Fan Level command is for the RTM fans. This bit is set to 0b to indicate that the Fan Level query is for the front fans. [6..0] – *FRU Device ID.* Indicates the FRU device for which the command is intended.
	3	[7..0] – *Fan Level.* To be accepted, this value is: 1) greater than or equal to Minimum Speed Level and less than or equal to Maximum Speed Level, or 2) FEh (Shut Down), or 3) FFh (Local Control)
	(4)	*Local Control Enable State*. This field is optional. Set this to 0 to disable, or 1 to enable, Local Control mode.
Response Data	1	*Completion Code*
	2	*PICMG Identifier*. Indicates that this is a PICMG-defined group extension command. A value of 00h is used.

3.8 E-Keying

¶ 88 Certain applications require special clock, trigger, and interlock connections between modules. For this reason, they use special backplanes with specific connections on AMC ports 12 through 15 and 17 through 20.

REQ 3-73: Ports 12 through 15 are routed using point-to-point links and **shall** be E-Keyed using the standard E-Keying mechanisms defined in the AMC.0 R2.0 specification.

¶ 89 These applications are likely to use custom protocols on ports 12 through 15.

REQ 3-74: When using custom protocols, the corresponding Link Descriptors **shall** specify *Link Type* values of F0h – FEh (E-Keying OEM GUID definition as defined in the PICMG AMC.0 specification).

¶ 90 Ports 17 through 20 are routed in a multi-drop bus topology. This is incompatible with point-to-point E-Keying. A Carrier Bused Connectivity record in the Carrier FRU information describes the bused connections.

Table 3-12: Carrier Bused Connectivity Record

Offset	Length	Field description
0	1	*Record Type ID*. Value C0h (OEM).
1	1	[7:7] End of list. Set to one for the last record. [6:4] Reserved, write as 0h. [3:0] Record format version (=2h for this definition).
2	1	*Record Length*.
3	1	*Record Checksum*. Holds the zero checksum of the record.
4	1	*Header Checksum*. Holds the zero checksum of the header.
5	3	*Manufacturer ID*. For this specification 12634 (0x00315A, LSB first) **shall** be used for the *Manufacturer ID*.
8	1	*PICMG Record ID*. The value 31h **shall** be used for the *PICMG Record ID*.
9	1	*Record Format Version*. For this specification, the value 0h **shall** be used for the *Record Format Version*.
10	1	*Bused Connection Count*. Number of Bused Connection Descriptors (N) that follow.
11	Variable	*Bused Connection Descriptors*. This is a list of Bused Connection Descriptors. Each entry is formatted as defined in Table 3-13.

¶ 91 The Carrier Bused Connectivity record includes a list of *Bused Connection Descriptors*. Each *Bused Connection Descriptor* describes a bused connection.

Table 3-13: Bused Connection Descriptor

Offset	Length	Field description
0	1	*Bused Device Count*. The number of devices (D) connected to the corresponding bus.
1	2 * D	*Bused Device Descriptors.* This is an array of D *Bused Device Descriptors*. Each *Bused Device Descriptor* is formatted as defined in Table 3-14.

¶ 92 Each *Bused Connection Descriptors* includes an array of *Bused Device Descriptors*. Each *Bused Device Descriptor* specifies a single port on a specific AMC or on-Carrier device that is connected to the bus.

Table 3-14: Bused Device Descriptor

Offset	Length	Field description
0	1	*Resource ID.* Indicates the AMC Slot ID or on-Carrier device. [7] Resource Type. 1 AMC, 0 indicates on-Carrier device ID [5:4] Reserved; write 0h [3:0] On-Carrier device ID or AMC Site Number
1	1	*Port.* Indicates the Port number within the AMC Slot or on-Carrier device.

REQ 3-75: MicroTCA Carriers implementing bused connections **shall** include a Carrier Bused Connectivity record in the Carrier FRU Information.

REQ 3-76: A Bused Connection Descriptor **shall** be provided for each bus.

REQ 3-77: A Bused Device Descriptor **shall** be provided for each port of each AMC Slot or on-Carrier Device that is connected to a bus.

REQ 3-78: During the E-Keying process, the Carrier Manager **shall** explicitly disable all Ports listed in both an AMC's AdvancedMC Point-to-Point Connectivity record and a Carrier Bused Connectivity record.

¶ 93 Use of an AMC that implements Point-to-Point Connectivity on Ports bused by the Carrier could result in damage to devices connected to the bus. Disabling the Port via E-Keying does not guarantee electrical compatibility in this case. It is the system integrator's responsibility to ensure that all AMCs used in a bused Carrier are electrically compatible with the bused implementation.

REQ 3-79: If an AMC provides an AdvancedMC Point-to-Point Connectivity record for a Channel that uses a Port listed in the Carrier Bused Connectivity record, the Carrier Manager **should** issue a warning to an appropriate user interface.

¶ 94 This warning is intended to alert a system integrator during development and testing that an electrical incompatibility might exist. Specifics of the warning and the user interface are design specific and are outside the scope of this specification.

¶ 95 Compatibility checking, enabling and disabling of bused ports, and arbitration of transmitters and receivers is application specific and is outside the scope of this specification.

3.9 Zone 3 Interface Documentation

¶ 96 FRU information can contain a variety of information about a FRU. It might be desirable to include information describing where to get documentation for the Zone 3 interface. Table 3-15 defines the Zone 3 Interface Documentation record. This record provides a Uniform Resource Locator (URL) that can be used to locate documentation for the Zone 3 Interface of the corresponding FRU.

Table 3-15: Zone 3 Interface Documentation record

Offset	Length	Field description
0	1	*Record Type ID*. Value C0h (OEM).
1	1	[7:7] End of list. Set to one for the last record. [6:4] Reserved, write as 0h. [3:0] Record format version (=2h for this definition).
2	1	*Record Length*. = N+4
3	1	*Record Checksum*. Holds the zero checksum of the record.
4	1	*Header Checksum*. Holds the zero checksum of the header.
5	3	*Manufacturer ID*. For this specification 12634 (0x00315A, LSB first) **shall** be used for the *Manufacturer ID*.
8	1	*PICMG Record ID*. The value 32h **shall** be used for the *PICMG Record ID*.
9	1	*Record Format Version*. For this specification, the value 0h **shall** be used for the *Record Format Version*.
10	N	*URL*. The Internet Uniform Resource Locator string that can be used through a World Wide Web browser to obtain documentation information about this Zone 3 interface. (*e.g.* “http://www.my_vendor.com:280?docu=my_board”)

REQ 3-80: AMCs and µRTMs **may** provide a Zone 3 Interface Documentation record in their FRU information.

This page intentionally left blank

4 Electrical

4.1 General

¶ 97 This document uses the electrical specifications for AMCs and MicroTCA shelves. This specification adds a connector in Zone 3 of a Double AMC and an associated µRTM. Other than defining the Zone 3 connector, the µRTM and the MicroTCA subrack this specification relies on previous documents for most details.

4.2 Power

4.2.1 AMC and µRTM Power

REQ 4-1: Total power delivered to and used by AMC front board and its associated µRTM **shall** conform to PICMG AMC.0 R2.0 except that the maximum Management Power current **shall** be increased from 150 mA to 180 mA.

REQ 4-2: Of the 180 mA of MP the µRTM **shall** be limited to 30 mA.

¶ 98 The current limit for the AMC remains at 150 mA.

REQ 4-3: The Payload Power **shall** not be enabled to the µRTM until system management has performed a compatibility check.

4.2.2 µRTM Power

¶ 99 Two voltages are fed from the front board to the µRTM. One is Payload Power (µRTM-PWR) and the other is Management Power (µRTM-MP).

REQ 4-4: The MP current **shall** conform to AMC.0 R2.0, Section 4.2.2.

REQ 4-5: The front board MMC **shall** control the switching of the PWR to the µRTM.

REQ 4-6: The designer **shall** consider the voltage drop that will be introduced if these voltages are switched by the AMC.

REQ 4-7: The voltage drops introduced by the switching and contact resistance **shall not** exceed 50 mV for µRTM-MP and 200 mV for µRTM-PWR.

REQ 4-8: For AMCs and associated µRTMs following the specifications in Sections 2.1.3.2 and 2.2.3.1, the four power pins (PWRA1, PWRB1, PWRA2, PWRB2) on the J30/RP30 ADF connectors **shall** be connected together on both modules with impedances that do not differ by more than 20% to insure current flow is the same to 20%.

REQ 4-9: For other connectors the power pins assigned **shall** conform to the specifications in this and other sections.

REQ 4-10: The combined AMC and µRTM MP surge current **shall** be limited to 270 mA for a maximum of 200 ms.

REQ 4-11: The µRTM-PWR current drawn by the µRTM **shall not** exceed 3 amperes.

¶ 100 The voltages for the µRTM's PWR and MP pins are the same as those defined in AMC.0 R2.0, Section 4.2 with the drop of the PWR switch taken into account by the module designer.

REQ 4-12: The µRTM **shall** be designed so that sudden power loss **shall not** cause permanent damage to the module.

REQ 4-13: The average power calculation in AMC.0, REQ 4.4b **shall** include the µRTM in the calculation.

REQ 4-14: The µRTM **should** provide an input capacitance of at least 0.5 µF on Payload Power per W of its maximum Payload Power requirement.

REQ 4-15: The voltage tolerances in AMC.0, Section 4.2.1.2 **shall** be applied to the µRTM.

REQ 4-16: The power and grounding in AMC.0, Section 4.2.2 and 4.2.3 **shall** be applied to the µRTM.

4.2.3 Power Module

REQ 4-17: The Power Modules **shall** be capable of providing 180 mA of continuous MP to each AMC slot.

REQ 4-18: The Power Modules **shall** support MP inrush current up to 270 mA for 200 ms to each AMC slot.

4.3 Data

REQ 4-19: ADF Zone 3 data connectors **shall** conform to PICMG 3.0 R3.0, Appendix A.4.

REQ 4-20: The Zone 1 backplane connectors **shall** conform to PICMG MTCA.0 R1.0, Section 7.

4.4 Clocks

¶ 101 Clocks on the Zone 3 plug are not defined by this specification. User defined pins can be used for this purpose. Other clocks in the AMC connector follow MTCA.0 and Section 6 below.

4.5 Isolation

¶ 102 Input isolation is defined in PICMG MTCA.0 R1.0, Section 4.8.1.11. AC isolation is defined in PICMG MTCA.0 R1.0, Section 4.8.2.2.

4.6 ESD

¶ 103 See PICMG AMC.0 R2.0, Section 2.2.6.

4.7 Signal Levels

REQ 4-21: User specified signal levels in Zone 3 at the AMC/µRTM interface in Zone 3 **shall not** exceed the levels specified by the mechanical keying in Table 2-1.

This page intentionally left blank

5 Thermal

5.1 Thermal Requirements

REQ 5-1: The cooling requirements for this specification **shall** be those in PICMG 3.0 R3.0.

REQ 5-2: The following documents **should** be used as a guide for thermal requirements for both the Front Board and the µRTM.

- PICMG AMC.0 R2.0: Advanced Mezzanine Module specification, Section 5
- PICMG MTCA.0 R1.0: MicroTCA base specification, Section 5
- PICMG MTCA.1 R1.0: Air Cooled Rugged MicroTCA specification, Section 5

5.2 Subrack Cooling

REQ 5-3: Empty slots in the front and rear of the subrack **shall** have airflow Impedance Matching Devices on the AMC and µRTM Filler Modules to balance the cooling air in the shelf.

REQ 5-4: All Filler Modules **shall** follow the construction method outlined in this document so units from different vendors will work together to properly control the cooling air flow.

5.2.1 AMC Filler Modules

REQ 5-5: AMC Filler Modules **shall** have an Air Impedance Matching Device.

¶ 104 PICMG Rugged MicroTCA.1 R1.0, Section 5.4 can serve as a reference when designing this module.

REQ 5-6 The AMC Filler Module Impedance Matching Device **should** be adjustable.

¶ 105 Figure 5-1 shows the Air Impedance Matching Device placed directly above the backplane AMC connector. This may be fixed or (preferably) adjustable. The exact details are left to the designer.

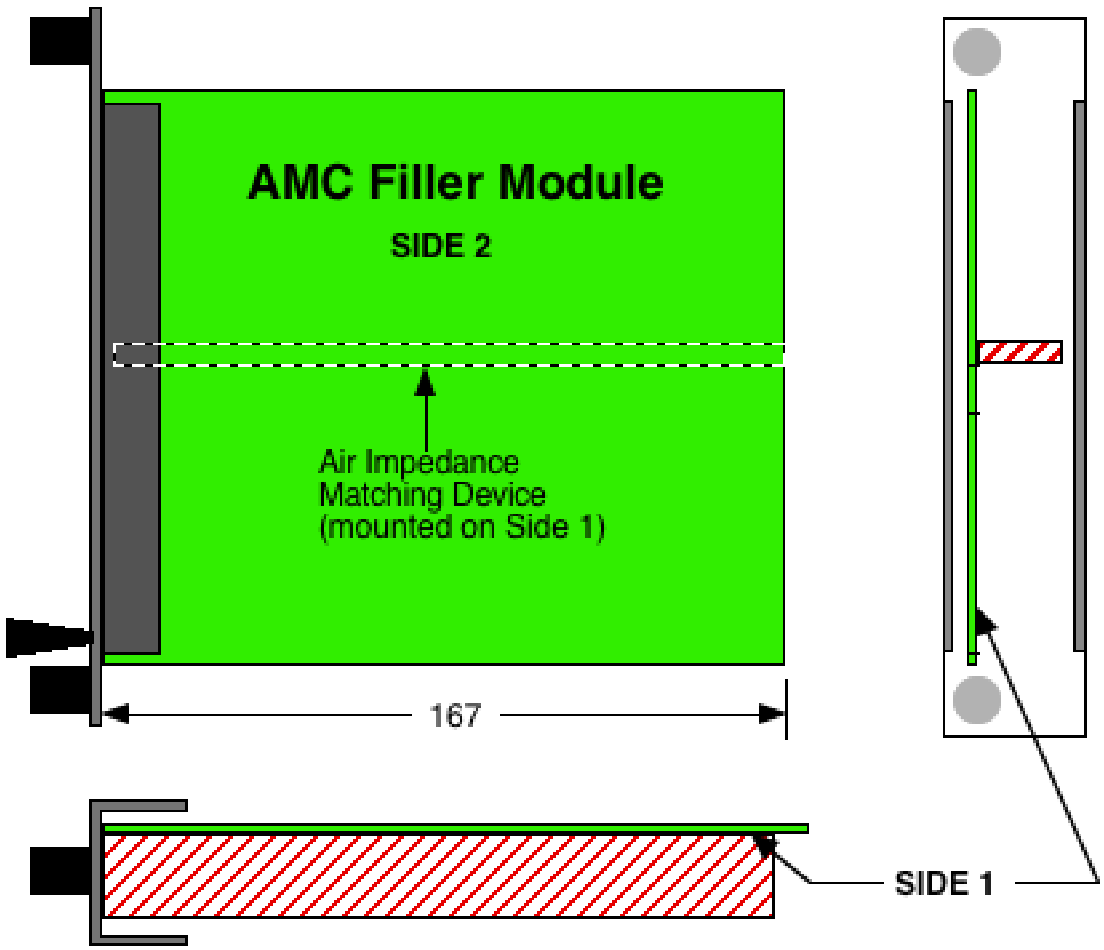


Figure 5-1: AMC Filler Module Assembly

5.2.2 µRTM Modules

REQ 5-7: µRTM Modules **shall** block at least 85% of the Zone 3 area. The 85% includes the connector(s), key and, if necessary, a Connector Air Block (see Figure 5-2).

REQ 5-8: The Backplane Air Block Plate shown in Figure 5-2 **should not** be used if electronics on the rear of the backplane requires cooling.

¶ 106 Figure 5-2 shows a µRTM that connects to the front AMC. In this case the horizontal block may not be necessary since components on the PCB may provide the required air impedance. An air block plate may be necessary in Zone 3 if the connectors and key/alignment hardware to not block at least 85% of the air that can spill either direction between front and back.

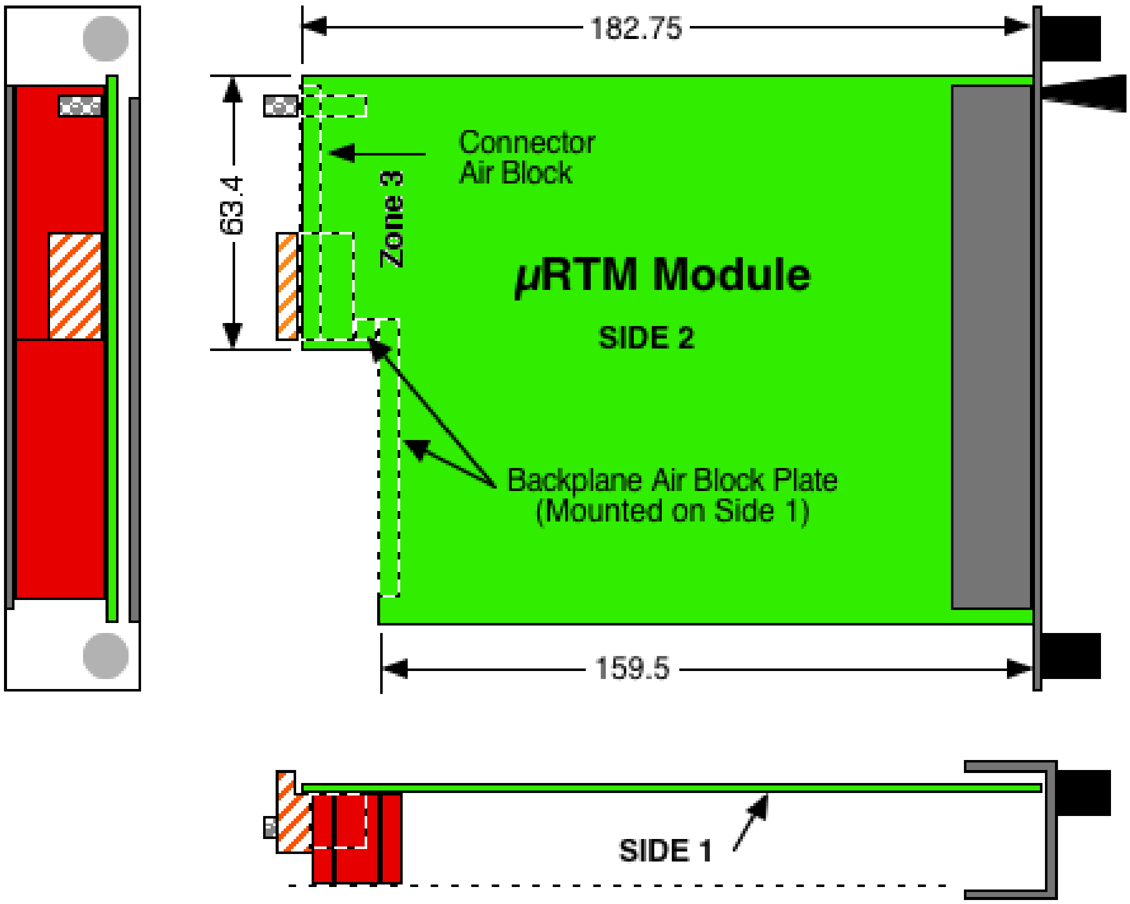


Figure 5-2: RTM Assembly with Air Block

5.2.3 µRTM Filler Modules

REQ 5-9: µRTM Filler Modules **shall** have an Air Impedance Matching Device.

¶ 107 PICMG Rugged MicroTCA.1 R1.0, Section 5.4 can serve as a reference when designing this module.

REQ 5-10: The µRTM Filler Module Air Impedance Matching Device **should** be adjustable.

REQ 5-11: µRTM Filler Modules **shall** have an airflow blocking mechanism that fills a minimum of 85% of the Zone 3 area between the front and rear if AMC connections are present.

¶ 108 The µRTM Filler Module shown in Figure 5-3 has more blocking plates than the AMC Filler Module to control the airflow behind the backplane. This area has a large open area for mounting a mezzanine on the rear of the backplane. The plates confine the airflow behind the backplane and also block Zone 3 to prevent air flowing to/from the front of the subrack. This µRTM Filler Module has a horizontal Air Impedance Matching Device that is preferably adjustable. The adjustment gives the system designer better control when balancing the cooling in the shelf.

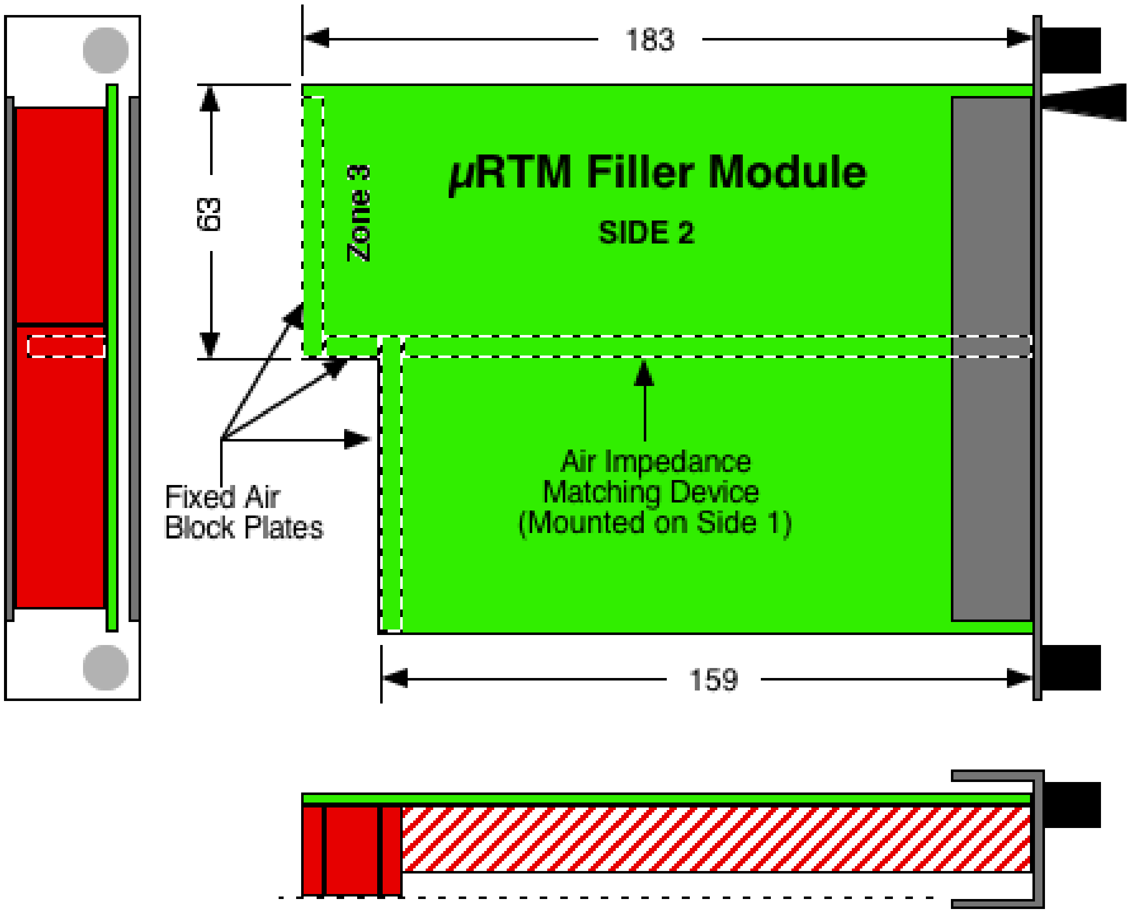


Figure 5-3: µRTM Filler Module Assembly

5.2.4 Subrack Air Cooling

¶ 109 Cooling requirements are similar to AMC.0 R2.0 and MicroTCA.0 R1.0. In the MicroTCA subrack specified in this document there is also the rear µRTM area to cool. See Section 4.2 for power ratings on front AMCs and rear µRTMs that will set the cooling requirements.

REQ 5-12: The cooling air supplied to the front of the subrack **shall** meet the specifications in the AMC.0 and MicroTCA.0.

REQ 5-13: The cooling air supplied to the rear of the subrack **shall** meet the specifications in the AMC.0 and MicroTCA.0 that has been scaled to the reduced maximum power allowed for the µRTM.

REQ 5-14: Monitoring of cooling for the front and rear of the subrack **shall** be integrated into the system management system.

5.2.5 Filler Module Configurations in Subracks

¶ 110 Figure 5-4 shows the subrack with both front and rear Filler Modules. The horizontal impedance plates (air block) balance the airflow both front and rear when functional modules are not in place. The fixed air block plates on the µRTM keep the air from shunting around the module at the rear of the backplane. The fixed air block plates in the Zone 3 area takes the place of a backplane and confines the front and rear airflow in their respective channels.

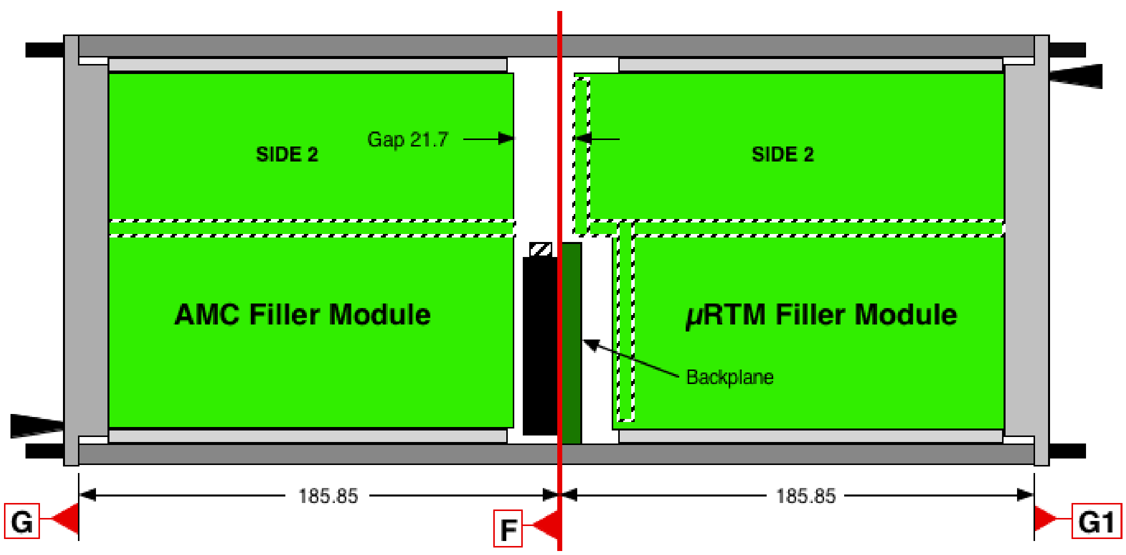


Figure 5-4: Subrack with Filler Panels

¶ 111 Figure 5-5 shows a subrack with a functional AMC Module but no Zone 3 connection to a µRTM. The µRTM Filler Module is necessary to constrain the airflow in the correct areas.

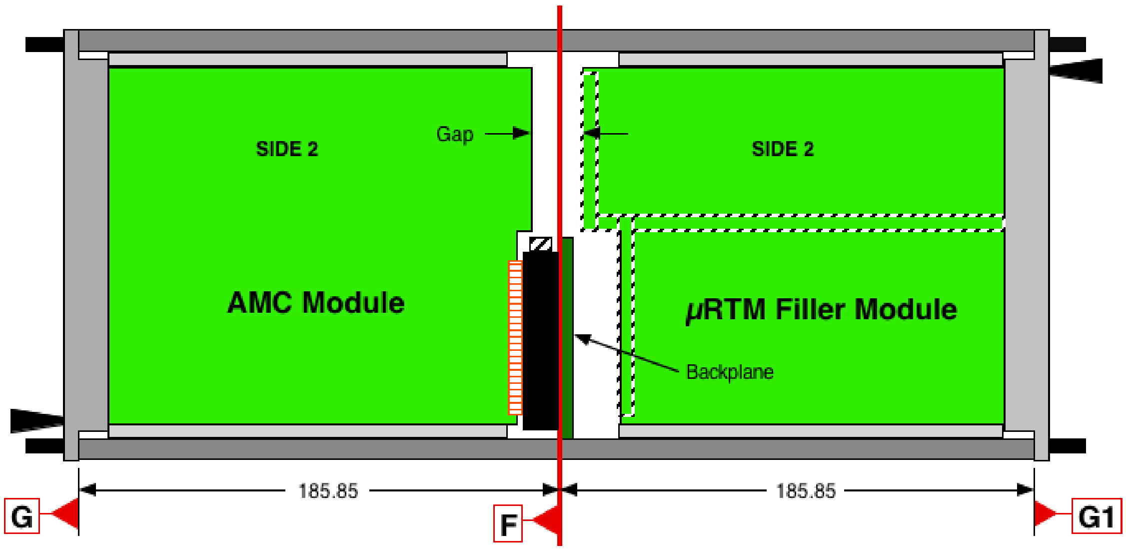


Figure 5-5: Subrack with AMC Module and µRTM Filler Module

¶ 112 Figure 5-6 shows a subrack with an AMC Filler Module with a functional µRTM with a Zone 3 connection. The AMC Filler Module is necessary to constrain the airflow in the correct areas. This is an unlikely configuration but can occur if the AMC is removed and the subrack cooling is required to function properly.

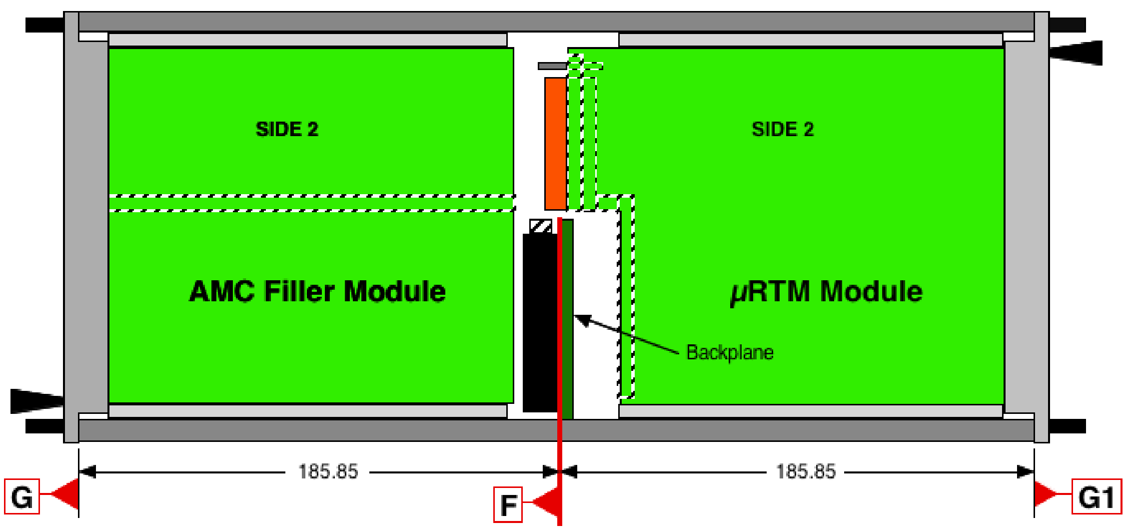


Figure 5-6: Subrack with AMC Filler Module and µRTM Module

5.3 µRTM power

REQ 5-15: The average power on the µRTM **shall not** exceed 30 watts.

¶ 113 The power limit is calculated from the 3 A limit on the pins and the minimum of 10 V as given in AMC.0 R2.0, Section 4.2.

REQ 5-16: Since all power is supplied by the front AMC Module, the power used by the µRTM **shall** be subtracted from that available to the AMC front board.

¶ 114 The maximum power available to the AMC/µRTM combination is 80 W.

This page intentionally left blank

6 Interconnect

6.1 Introduction

¶ 115 This section describes a backplane for use in MTCA.4 that has features to facilitate the data acquisition and control of accelerators, experiments. Uses of this backplane may be of use outside the area of research.

6.2 Fabric interface

¶ 116 Specific fabric technologies are outside the scope of this specification. Refer to the appropriate AMC.x specification for information related to specific fabric technologies.

6.3 MCH Specifications

¶ 117 The MicroTCA Carrier Hub (MCH) interconnects are defined in the MicroTCA.0 specification.

6.4 Clocking

6.4.1 General clocking topology

¶ 118 Figure 6-1 shows the general concept of the clock, trigger and interlock signal connections. Two radial clocks as defined in AMC.0 are used to distribute low jitter, high quality clocks by radial links from all AMC slots to the MCH. FCLKA is reserved and provided for PCIe usage. Ports 17 to 20 (Rx17/Tx17 to Rx20/Tx20) are used as a bus for triggers, clocks and interlock signal distribution.

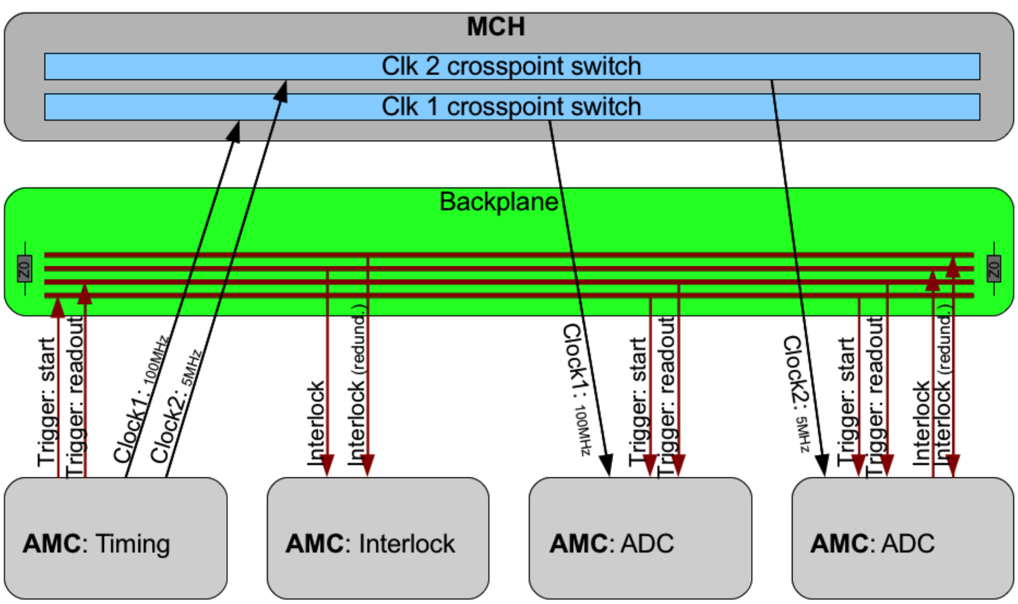


Figure 6-1: Example using radial clocks and bused triggers

6.4.2 Radial clock circuitry

¶ 119 Two point-to-point lines from all AMC Modules to the MCH implement the clocks as differential pairs as defined in AMC.0, Section 6.3.1. The lines are bidirectional. Any AMC can be the source or the receiver of clock TCLKA or TCLKB.

¶ 120 Where low jitter is required on point-to-point links, LVDS transmitters have higher bandwidth than M-LVDS transmitters specified in AMC.0 R2.0 and therefore provide more precise timing. LVDS transmitters on AMC and MCH modules need to meet the line drive requirements in REQ 6-2. The lower bandwidth (rise time) of M-LVDS devices makes them appropriate for driving busses (see Section 6.5).

REQ 6-1: An AMC Module **may** implement a receiver or transmitter or both.

REQ 6-2: A 100 Ω line-termination **shall** be on both ends of the backplane. These terminations are in both the MCH and the AMC Module as shown in Figure 6-2. Long stubs in the PCB layout **shall** to be avoided (see AMC.0 R2.0, Section 6.3.1).

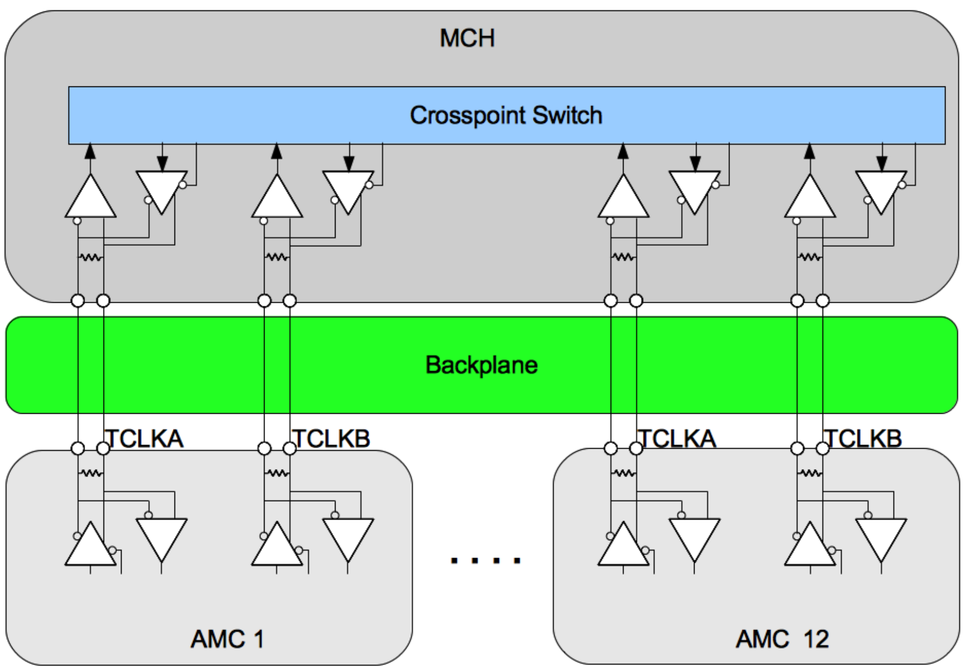


Figure 6-2: TCLKA and TCLKB are bidirectional example.

¶ 121 TCLKC and TCLKD are implemented in a similar manner to TCLKA and TCLKB except they are connected to the redundant MCH module.

6.5 Bus lines general topology

¶ 122 In Figure 6-3 an example usage of the bus lines is given. The differential Receiver and Transmitter lines of the ports 17 to 20 of all AMCs are connected together on the backplane.

REQ 6-3: At both ends of the backplane these lines **shall** be terminated by 100 Ω.

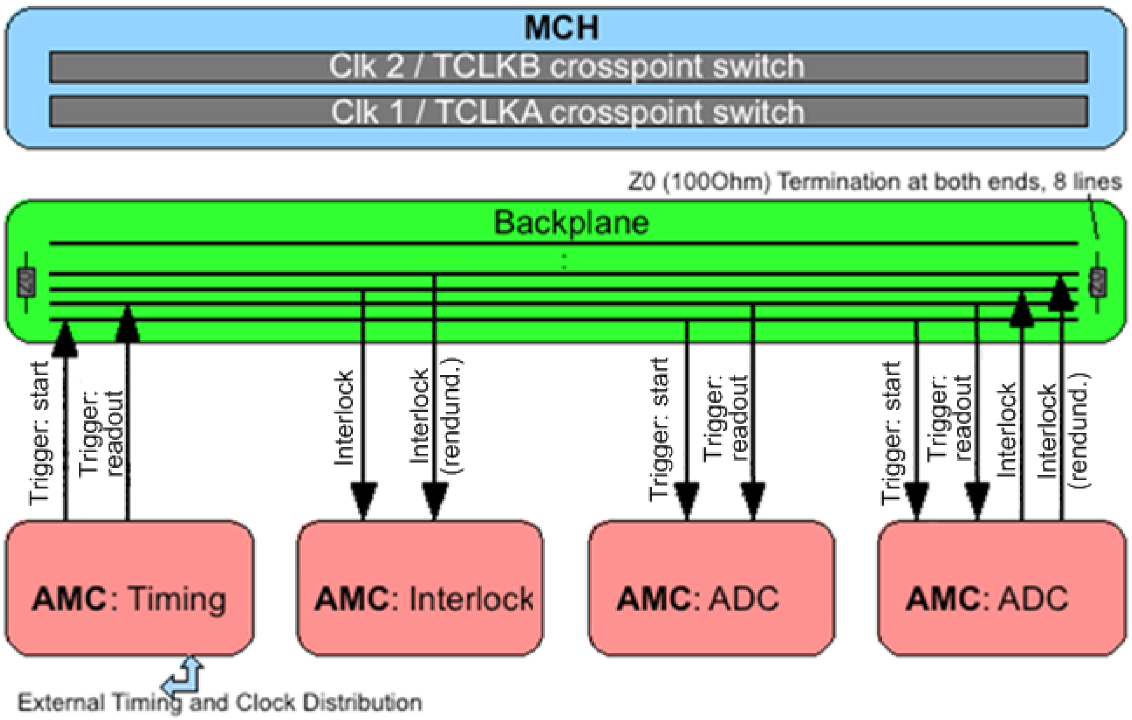


Figure 6-3: Example using the 8 bus lines

6.5.1 Ports 17 to 20 usage

REQ 6-4: The differential lines **shall** be driven by M-LVDS, according to EIA/TIA-899.

¶ 123 The AMC Modules may implement a receiver or a transmitter or both on every Rx and Tx pair of the ports 17 to 20.

REQ 6-5: The differential lines on AMC Modules (stubs) **should** be as short as possible and **shall** not exceed 30 mm.

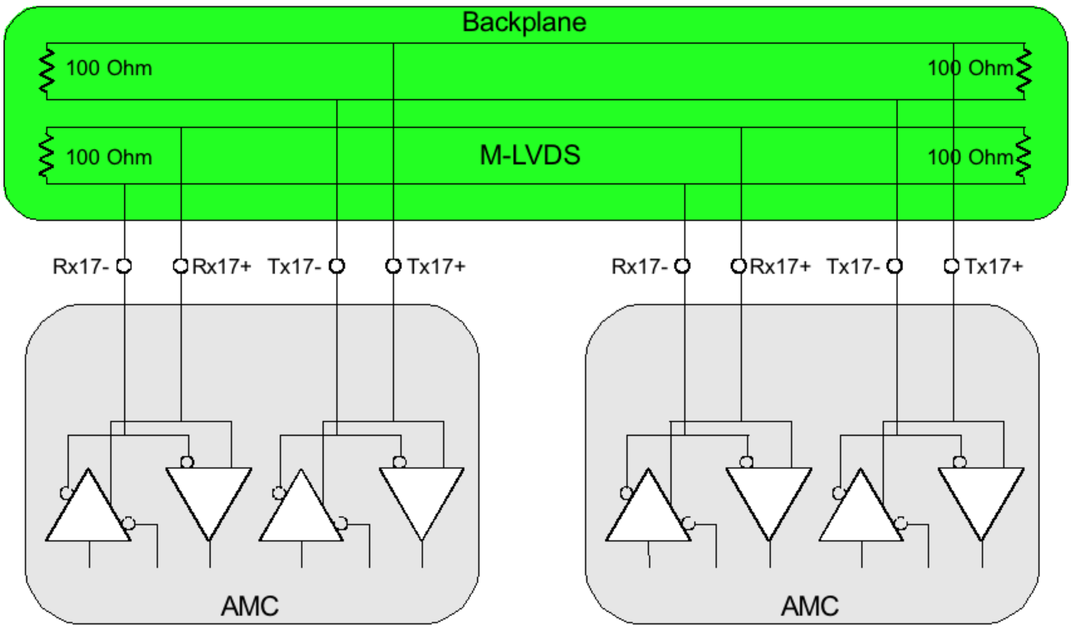


Figure 6-4: M-LVDS transceiver shown for port 17

¶ 124 The usages of the bus lines are application dependent. Table 6-1 indicates a possible usage.

Table 6-1: Example usage of the 8 bus lines for triggers, interlocks and clocks

AMC Port	Name	Description	Usage
Rx17	TrigStart	Start sampling data	Triggers
Tx17	TrigEnd	Stop sampling data	
Rx18	TrigReadOut	Start data transfer to CPU	
Tx18	ClkAux	Low performance clock	
Rx19	Reset	Reset of counter, dividers	
Tx19	Interlock 0	Interlock line 0	3 interlocks to provide 2 out of 3 redundancy
Rx20	Interlock 1	Interlock line 1	
Tx20	Interlock 2	Interlock line 2	

6.6 JTAG interface

¶ 125 See PICMG MTCA.0 R1.

6.7 MicroTCA interface topologies

6.7.1 Backplane

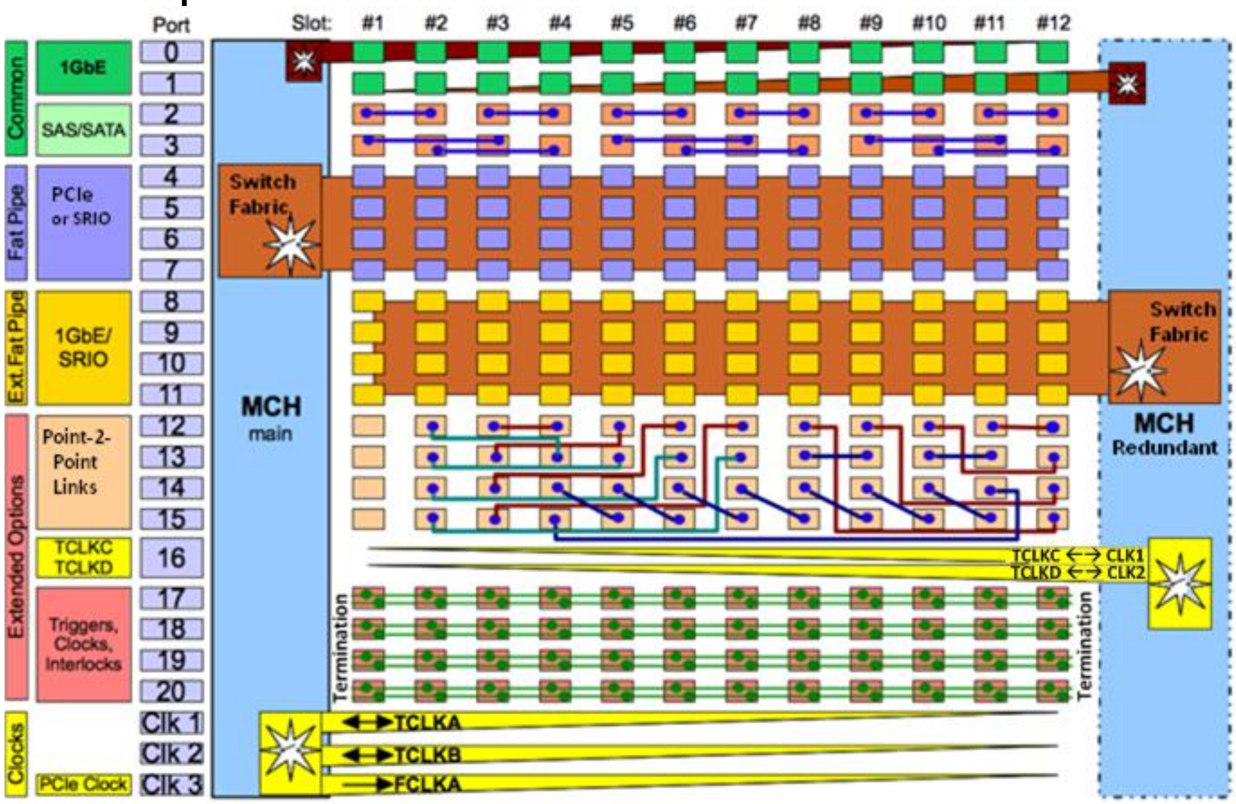


Figure 6-5: Example of a MicroTCA backplane

¶ 126 The following are the uses of the various Ports and Clocks for this backplane.

REQ 6-6: Port 0 **should** be used for base Ethernet interface. Port 1 is connected to the optional (redundant) MCH.

REQ 6-7: Port 4 to 7 **should** be used for PCIe.

REQ 6-8: Port 12 to 15 **may** be used for application specific wire-ring.

REQ 6-9: Ports 17 – 20 **should** be wired as a bus according Section 6.4.

REQ 6-10: FCLKA (Clk3) **should** be used for PCIe clock distribution as defined in MTCA.0 R1.0

REQ 6-11: TCLKA and TCLKB **should** be wired from the main MCH to all AMC slots.

REQ 6-12: TCLKC and TCLKD **should** be wired from the redundant MCH to all AMC slots.

6.8 MCH Connector pin allocations

¶ 127 The MCH is connected according to MTCA.0.

6.9 System examples

¶ 128 This section describes examples of applications in science. The same principles can be used in industrial or medical systems as well. Applications in these fields usually collect a lot of different analog signals, slow and high-speed digital data, and often control actuators in the field. Single or multiple CPU's, FPGA's or DSP's are within the shelf to execute slow and fast feedbacks and to provide the data to other processes and the users.

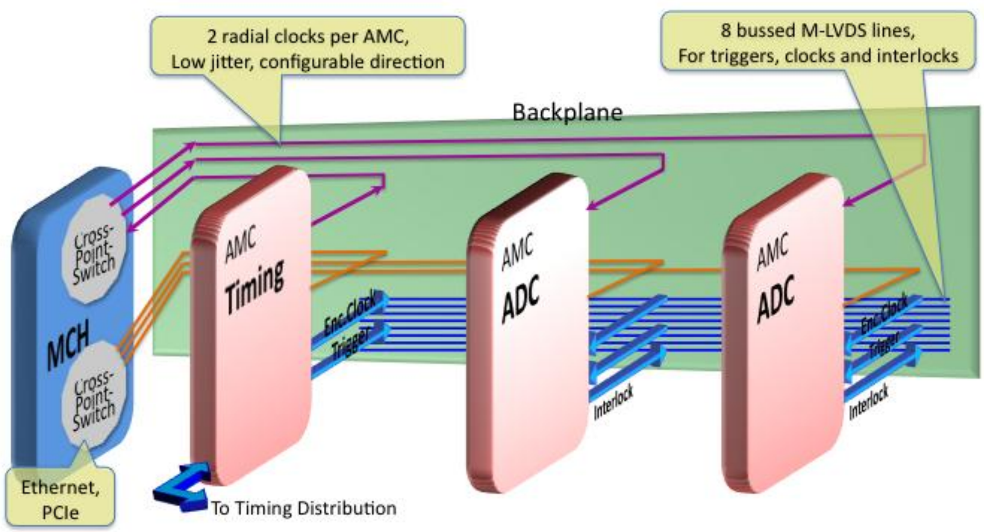


Figure 6-6: A 'typical' analog front-end.
CPU and further AMC's are not shown

¶ 129 Figure 6-5 shows the distribution of clocks and triggers within a shelf. Some high-speed ADC's require precise clocks: radial clock lines switch in the MCH are provided for these applications. Less demanding clocks and triggers are distributed via the eight bussed M-LVDS lines. Clock frequencies around 100 MHz are foreseen on the 100 Ω impedance matched bus. Triggers can be used to arm data recording of the ADC's or to trigger readout processes in CPU's. Figure 6-6 is an example of a fast digitizer with a FPGA controlling the processing of data. A radial distributed clock is used for the ADC's. Data acquisition is triggered from the M-LVDS bus. And the board is able to compare ADC readings with a threshold to generate interlock signals. Those are distributed within the shelf on the bussed lines.

¶ 130 PCIe accomplishes data transfer between the ADC, FPGA and the CPU. The MicroTCA system provides more then 400 MB/sec transfer speed over 4 lanes available in each AMC. Further lines of ports 12 to 15 of the backplane (see Figure 6-4) can be used to combine ADC data of several boards via Giga-bit links of the controlling FPGA's. An example from accelerators is the calculation of a vector sum of 32 cavities. Four ADC AMCs are collecting the data; a fifth AMC implements a feedback controller. Such a complex system does not need external clock trigger or fast link lines since the backplane can distribute the required signals.

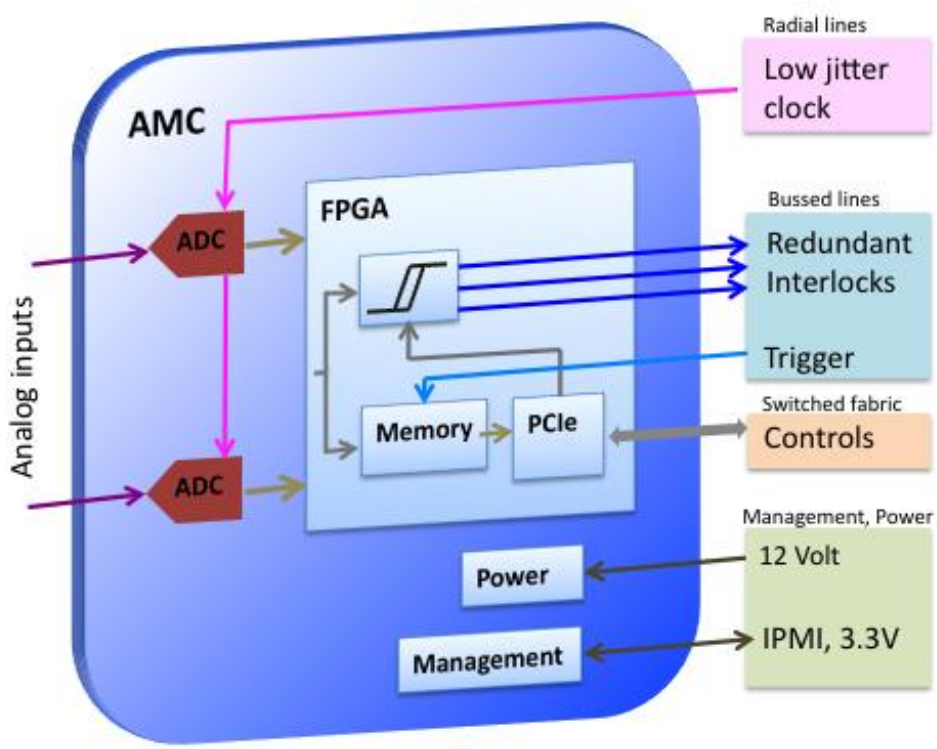
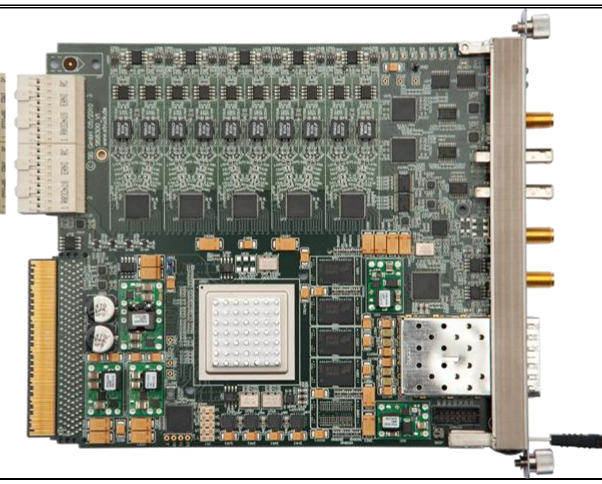


Figure 6-7: An example of a fast front-end (ADC AMC0)

¶ 131 Sufficient space for connectors is a further requirement for front-end electronics. And ADC's often need complex signal conditioning. Double size AMCs and the same PCB size on the µRTM provide enough space for digital and analog electronics. Sensitive analog parts of the signal chain needs to be well separated and shielded from power converters and noisy digital lines. The layout of the AMC-µRTM connections is designed to support critical analog designs.

¶ 132 The equal space on the AMC and µRTM allows flexible combinations to design modular systems. An AMC with a FPGA requires many PCB layers and high-speed strip-line designs. This is time consuming development. It is an advantage to use these complex boards in multiple applications by providing µRTMs as the adapter. µRTMs can be implemented with 4 to 6 layers and more designers are able to do this. In other applications an expert RF designer is required to create high frequency RF front-end. The front and rear division of the task is convenient since one can partition the tasks to different skilled designers.

Table 6-2: Examples of AMCs with different µRTM to adapt to different applications

µRTM	AMC
	
1. Down-converter as RF front-end 2. Fiber-optic receiver 3. Pulse shaper to stretch photo diode signals	Multi channel ADC
1. 20 MHz ADCs and signal conditioning 2. Stepper controller and position read-back 3. Interlock systems (analog and digital inputs)	FPGA with memory, fast links, FMC
Disks and peripheral connections	CPU

A. Twenty and Thirty Pair Advanced Differential Fabric connector definitions

¶ 133 The information in this Appendix is similar to that in PICMG 3.0 R3.0 except that is delineates 20 and 30 pair versions of the Advanced Differential Fabric (ADF) connector.

¶ 134 The user of this section should note that the row and column designations used in this document are consistent with those used in other PICMG xTCA documents. These designations are the opposite of the way connector manufacturers label their products.

A.1 General data

A.1.1 Objective of this document

¶ 135 See PICMG 3.0 R3.0

A.1.2 Scope

¶ 136 See PICMG 3.0 R3.0

A.1.3 Intended method of mounting

¶ 137 See PICMG 3.0 R3.0

A.1.4 Ratings and characteristics.

¶ 138 See PICMG 3.0 R3.0

A.1.5 Normative references

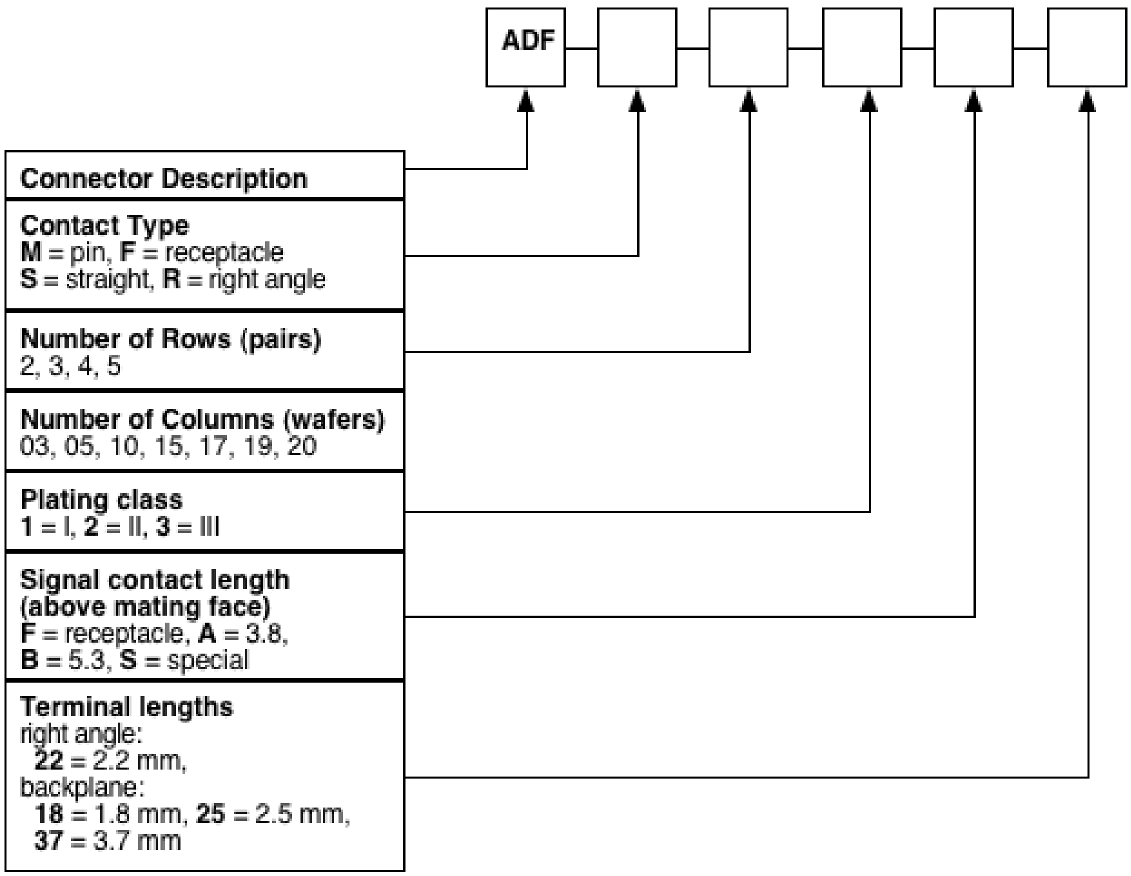
¶ 139 See PICMG 3.0 R3.0

A.1.6 Markings

¶ 140 See PICMG 3.0 R3.0

A.1.7 Type designation

Table A-1: ADF part number designator



¶ 141 Using this nomenclature a receptacle 30 pair ADF receptacle connector in Zone 3 of the AMC would be designated:

ADF-FR-3-10-2-F-22

The mating connector on the µRTM would be designated:

ADF-MR-3-10-2-B-22

Note that for the male right angle a Short Pin is available and designated as “S”. The user is responsible for indicating which pin lengths are in which positions. This connector would be designated as:

ADF-MR-3-10-2-S-22

Typically the “S” designator would be used in the RP30 position.

A.2 Technical information

A.2.1 Definitions

A.2.1.1 Contacts and terminations

¶ 142 See PICMG 3.0 R3.0 except on line 37 and change “Front Board” to “Front Board and μRTM”.

A.3 30 Pair ADF Connectors

A.3.1 General isometric view and common features

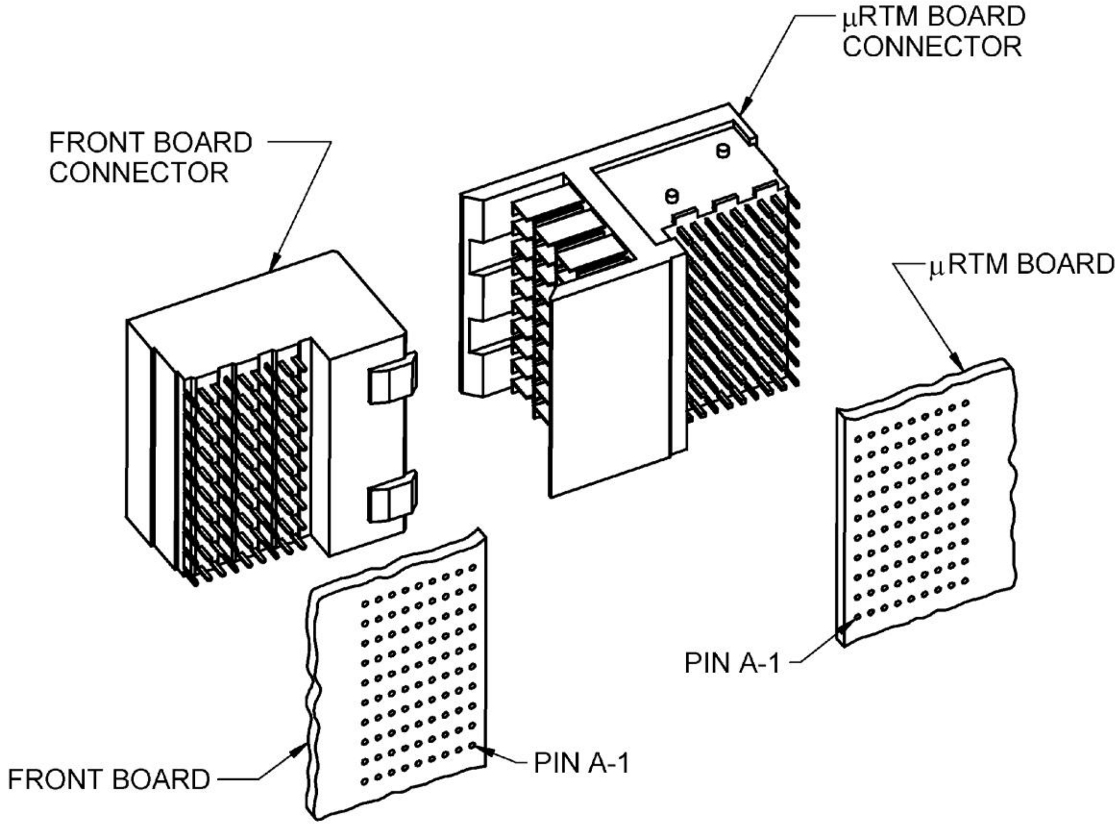


Figure A-1: Zone 3 front board and μRTM mating illustration

A.3.2 Dimensional Information

A.3.2.1 Right Angle Receptacle Connector

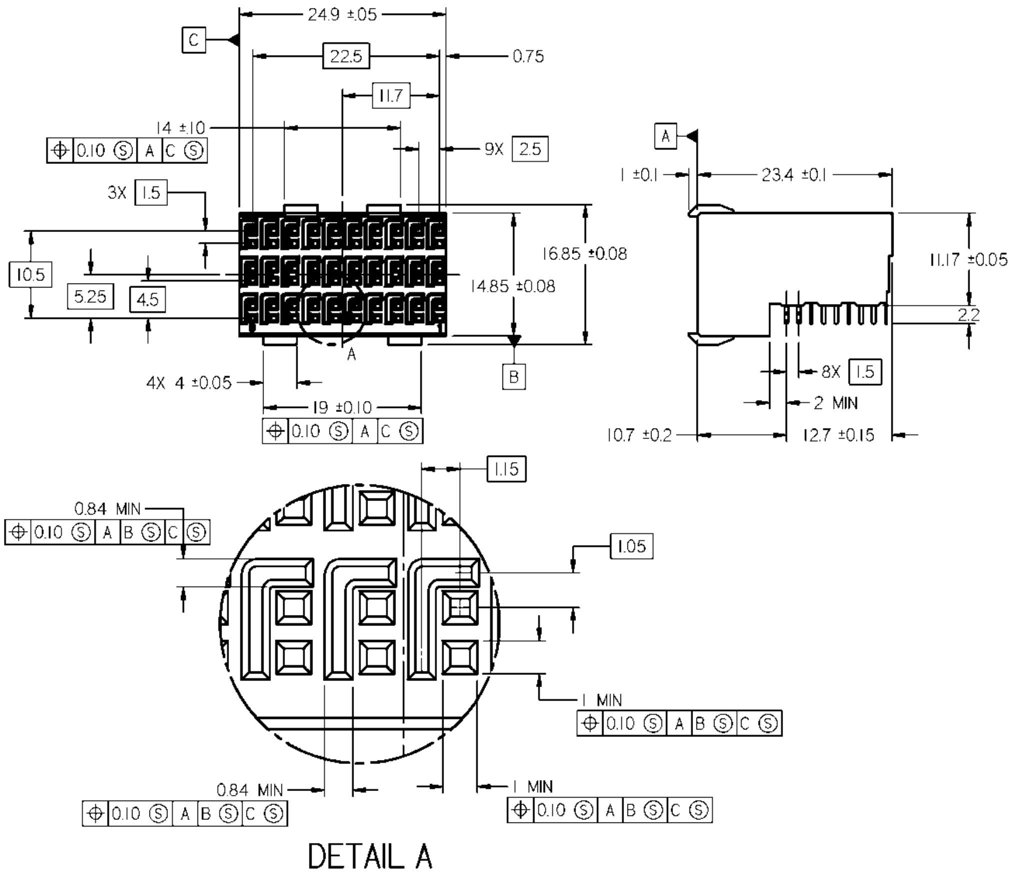


Figure A-2: Three row ADF female connector dimensions

A.3.2.1.1 Terminations

¶ 143 See PICMG 3.0, Section A.3.4.2

A.3.2.2 Right Angle Pin Connector

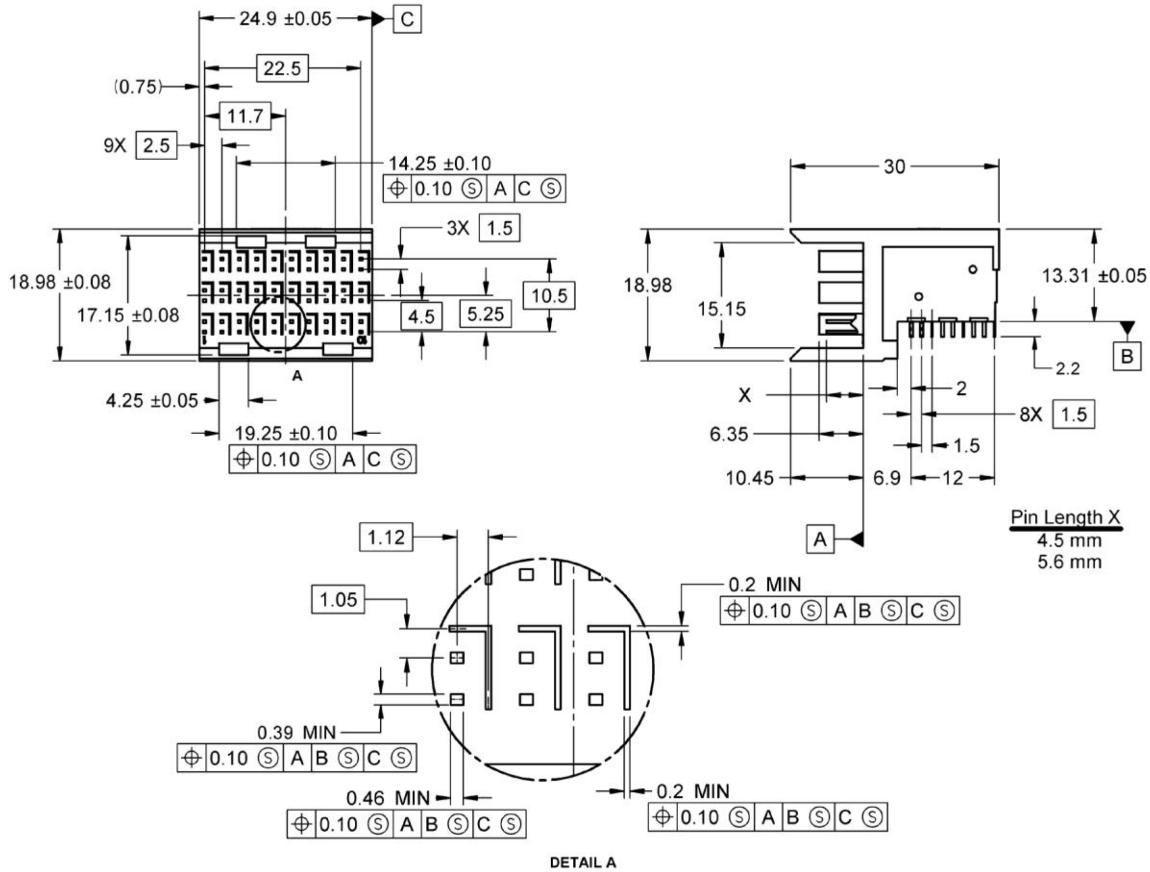


Figure A-3: Three row ADF male connector dimensions

A.3.2.2.1 Contacts

¶ 144 See PICMG 3.0, Section A.3.3.2

A.3.2.2.2 Contacts tip geometry

¶ 145 See PICMG 3.0, Section A.3.3.3

A.3.2.2.3 Terminations

¶ 146 See PICMG 3.0, Section A.3.3.4

A.4 Dimensional information for 20 Pair Connectors

A.4.1 General isometric view and common features

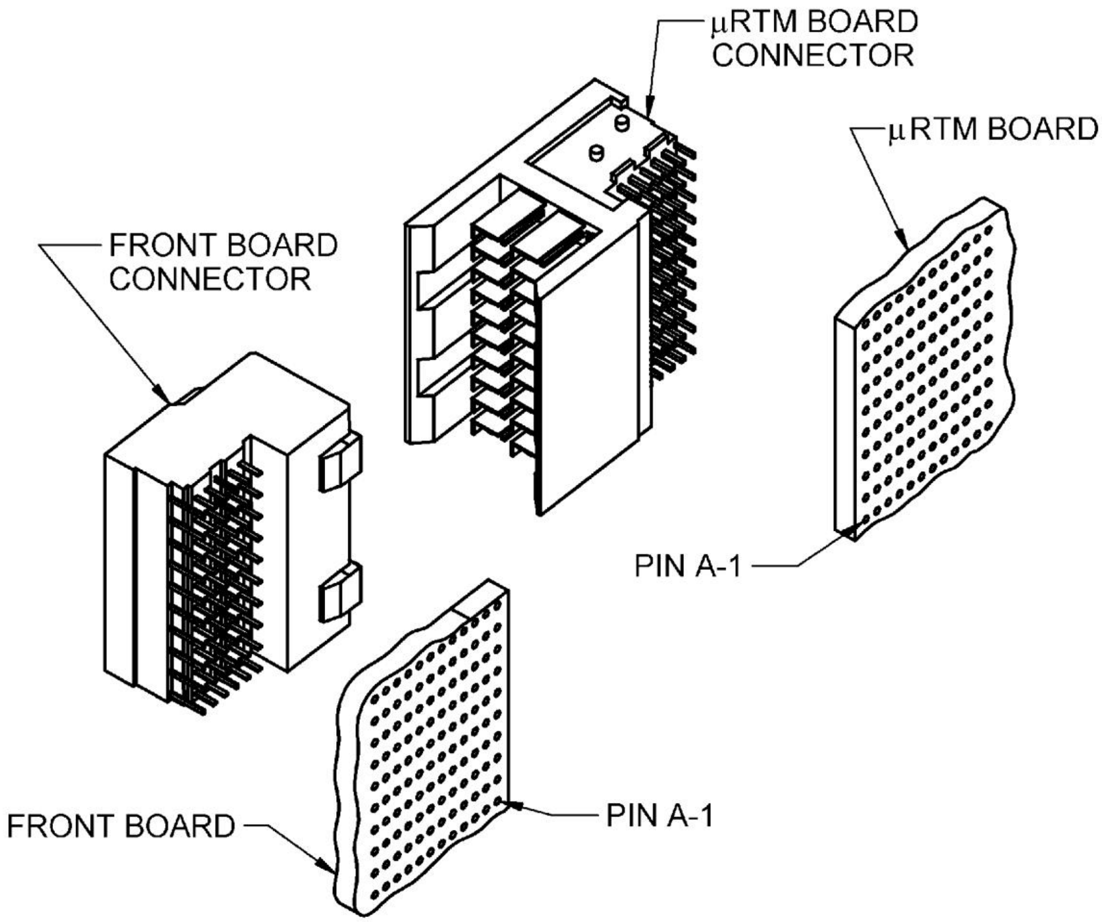


Figure A-4: Zone 3 front board and µRTM mating illustration

A.4.2 Dimensional Information

A.4.2.1 Right Angle Receptacle Connector

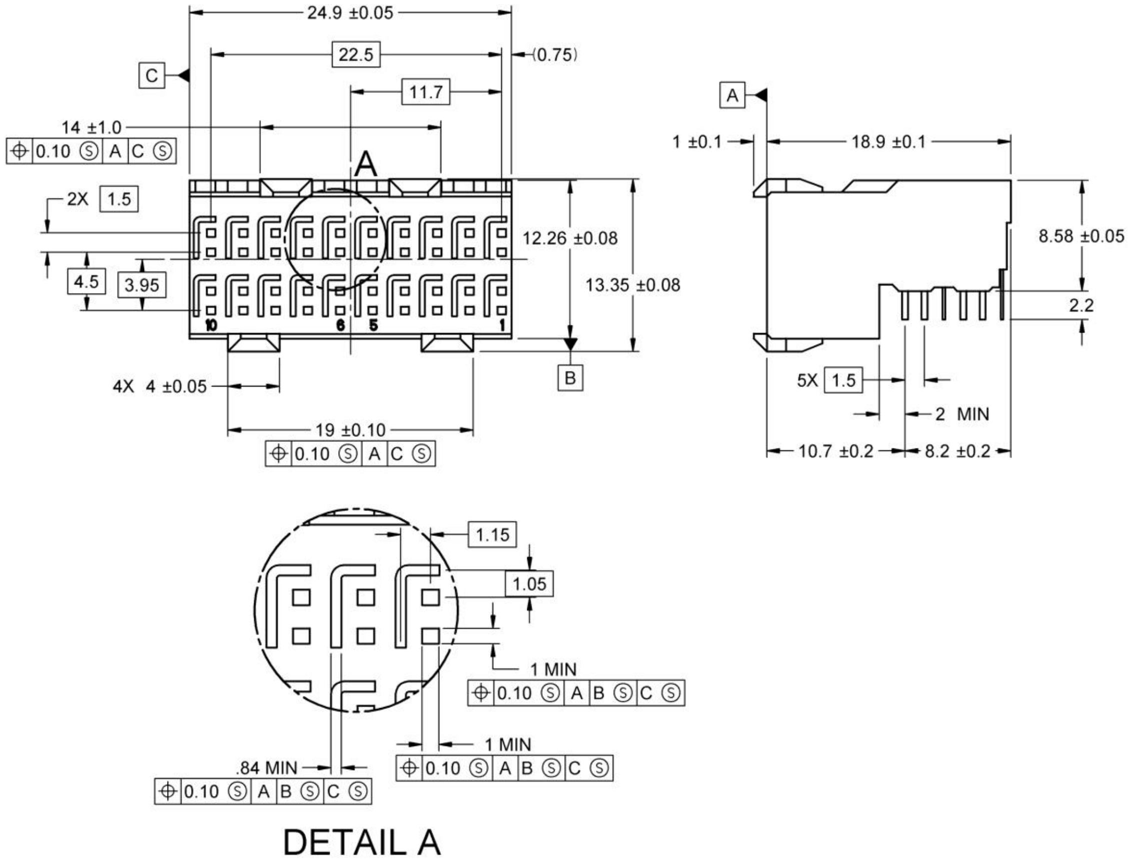


Figure A-5: Two row ADF female connector dimensions

A.4.2.1.1 Terminations

¶ 147 See PICMG 3.0, Section A.3.4.2

A.4.2.1 Right Angle Pin Connector

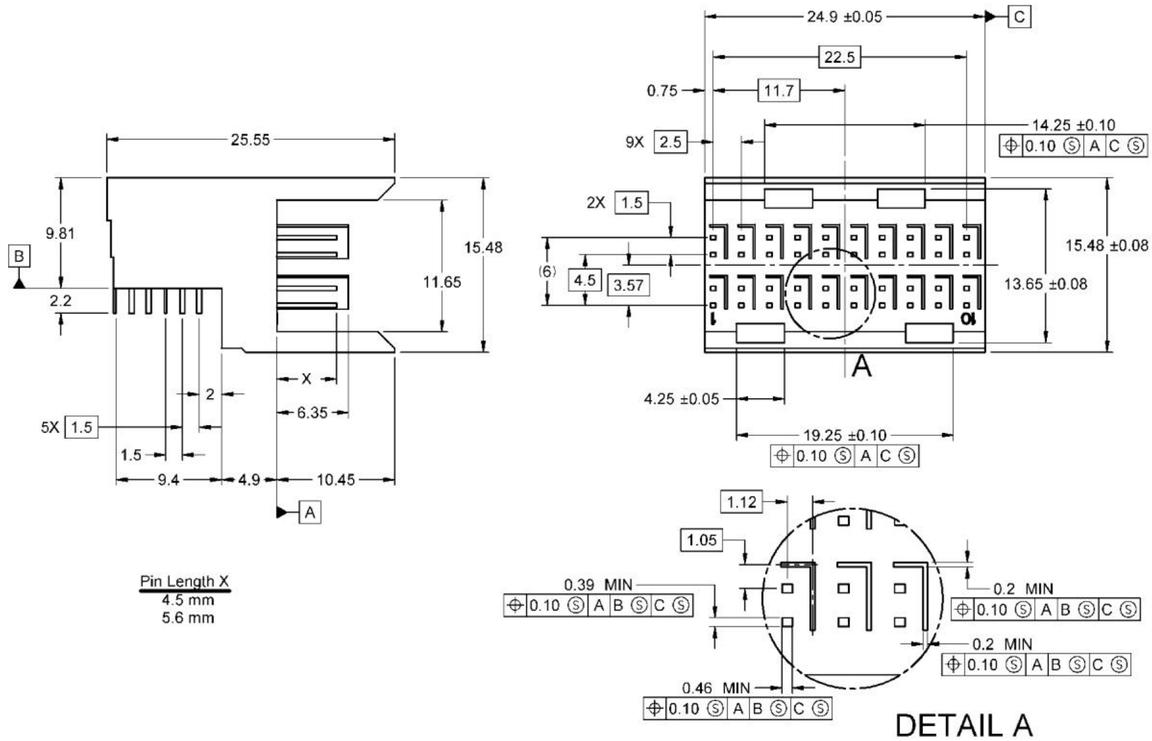


Figure A-6: Two row ADF male connector dimensions

A.4.2.2.1 Contacts

¶ 148 See PICMG 3.0, Section A.3.3.2

A.4.2.2.2 Contacts tip geometry

¶ 149 See PICMG 3.0, Section A.3.3.3

A.4.2.4 Terminations

¶ 150 See PICMG 3.0, Section A.3.3.4

A.5 Engagement information

A.5.1 Electrical engagement length

¶ 151 Three levels of mating are supported in mating pin and receptacle right angle connectors. The first contact to mate is the ground blade. The second to mate is Signal Level 2. The third is the 4.5 mm "Short Pin". In the right angle pin connector there is no Level 1 (3.8 mm) pin as in the backplane male connector.

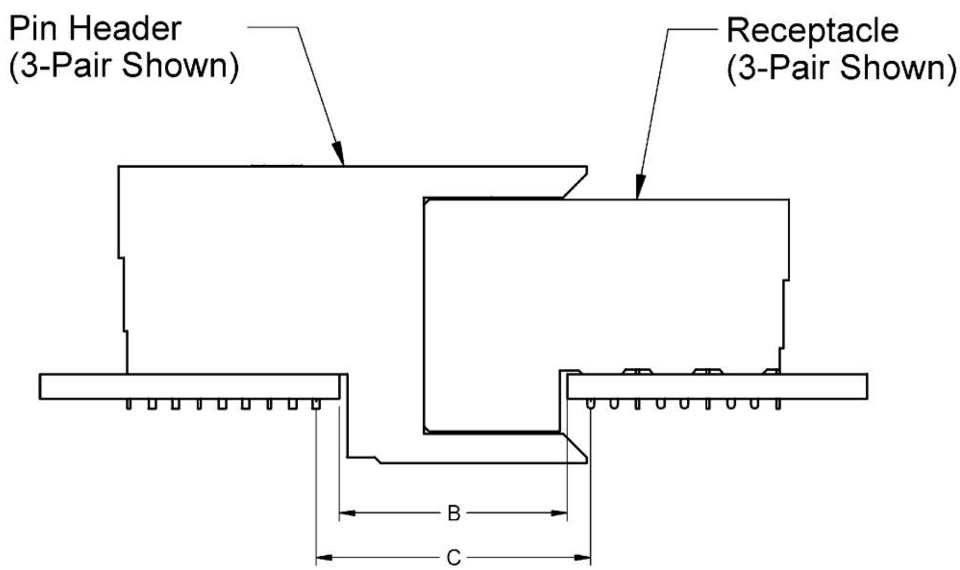


Figure A-7: Right Angle – Right Angle Connector Mating

Note: The dimensions for mating are the same for the 20 and 40 pair connectors.

Table A-2: Connector Mating Sequence

Product Family	Dim B (mm) fully mated	Contact	Dim C (mm) min	
			Reliable mate	**Fully mated**
ADF	14.8	Ground Shield	22.08	17.8
		Signal Level 2 5.3 mm	20.71	17.8
		Short Pin 4.5 mm	19.91	17.8

A.5.2 Perpendicular to engagement direction

¶ 152 See PICMG 3.0 R3.0, Section A.3.2.3

A.5.4 Inclination

¶ 153 See PICMG 3.0 R3.0, Section A.3.2.4

A.6 PCB Layout for Connectors

A.6.1 PCB Layout for AMC Zone 3 ADF connectors

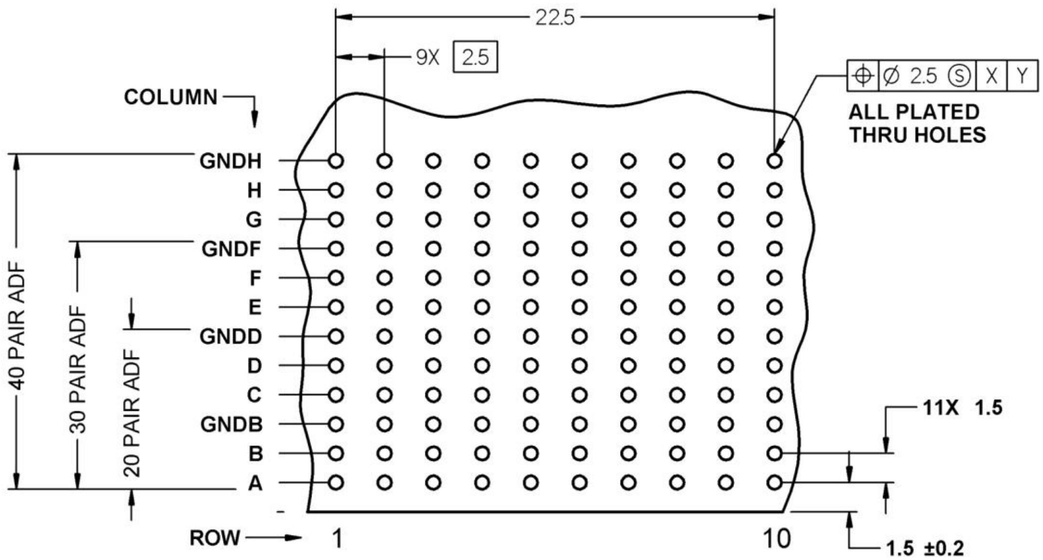


Figure A-8: ADF connector PCB hole layout

Note: View from component side 2.

REQ A-1: The ADF right angle receptacle connector **shall** use the hole pattern in Figure A-8 sized appropriately.

¶ 154 The position of hole A1 on the AMC PCB is shown in Figure 2-1.

A.6.2 PCB Layout for µRTM Zone 3 ADF connectors

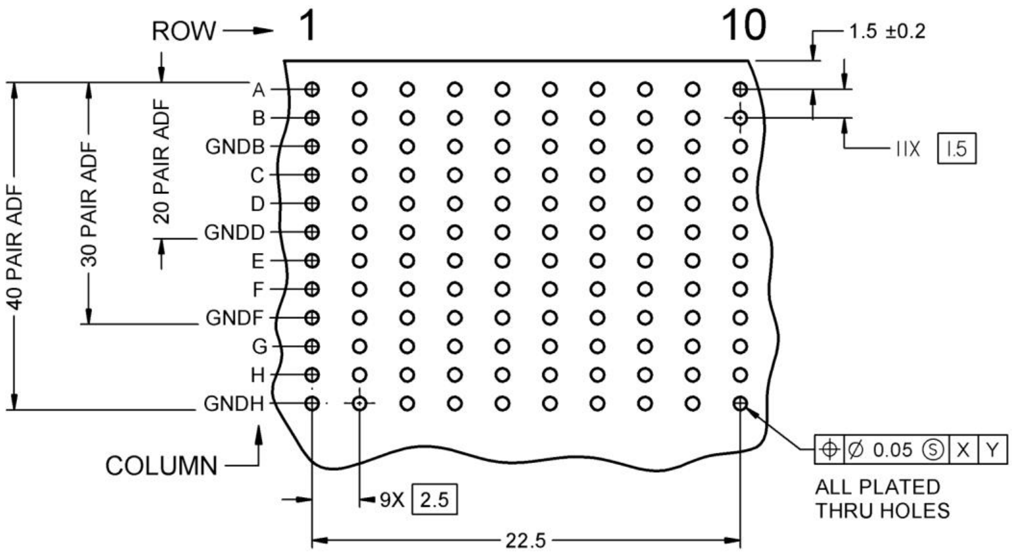


Figure A-9: ADF connector µRTM PCB hole layout

Note: View from component side 2.

REQ A-2: The ADF right angle pin connector **shall** use the hole pattern in Figure A-9 sized appropriately.

¶ 155 The position of hole A1 on the µRTM PCB is shown in Figure 2-4.

A.7 Characteristics

¶ 156 Section A-7 is the same as PICMG 3.0 R3.0, Appendix A.4 except as noted in the following sections.

A.7.1 Propagation Delay

¶ 157 Remove G an H Pins from PICMG 3.0 R3.0 Table A-9 for three connectors and E, F, G, and H for the two-row connector. After the appropriate modification the table in PICMG 3.0 R3.0 can be used.

This page intentionally left blank

B. Keys

B.1 Male Key Dimensions

REQ B-1: The male key/alignment pin in Figure B-1 **shall** be used on the µRTM module. Orientation codes are in Table B-1.

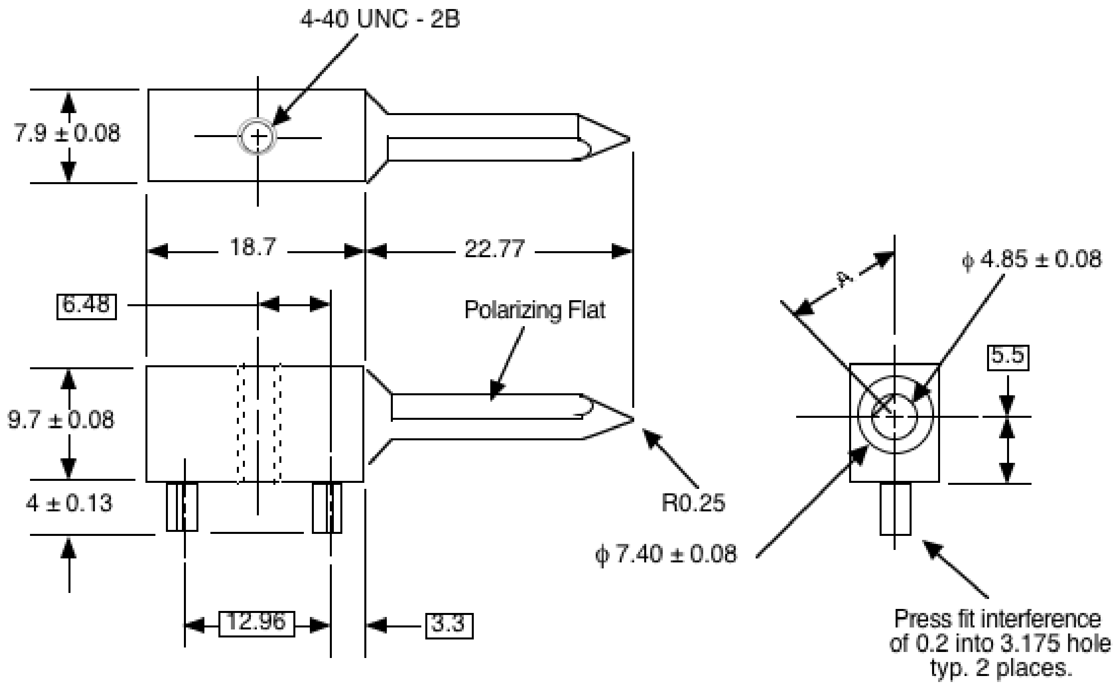


Figure B-1: Male key

B.2 Female Key Dimensions

REQ B-2: The female key/alignment pin in Figure B-1 **shall** be used on the AMC module. Orientation codes are in Table B-1.

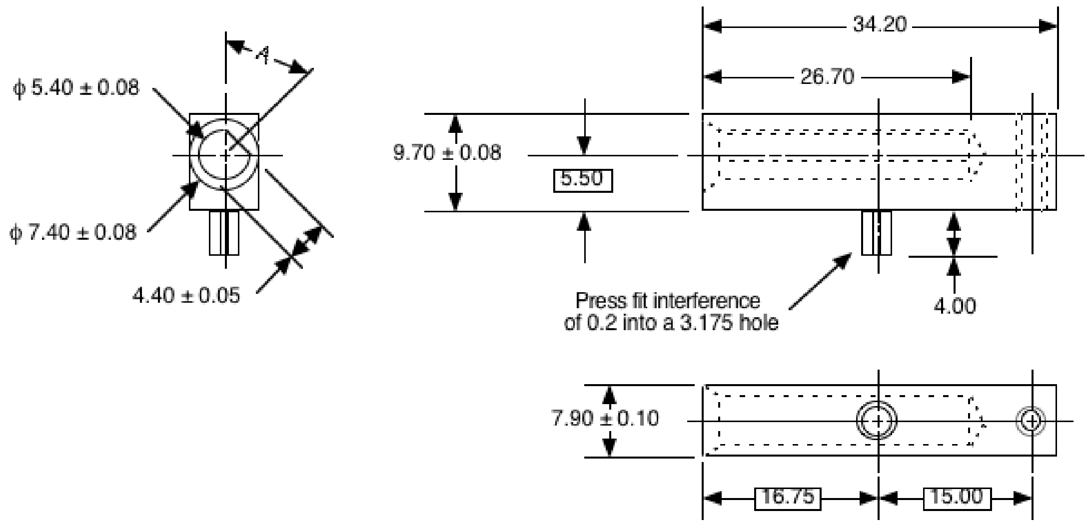


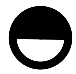
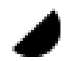
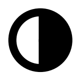
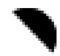
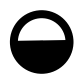
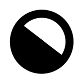
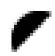
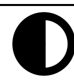
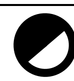
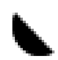
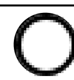
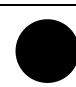
Figure B-2: Female key

¶ 158 For cases where keying is not used (e.g. some test equipment) an un-keyed version of the female block is available. The un-keyed version is value 0 in Table B-1.

B.3 Key Orientation

¶ 159 Table B-1 indicates the orientation of the male and female keys. The meaning of the values is contained in Table 2-2 of this document.

Table B-1: Key positions (standard orientation)

N	A Rotation in degrees	View into rear of AMC Receptacle	View into rear of µRTM Post
1	0		
2	45		
3	90		
4	135		
5	180		
6	225		
7	270		
8	315		
0	NA		

Note 1: N = 2 is shown in Figures B-1 and B-2.
Note 2: White area in receptacle drawing is the hole that the post inserts into

¶ 160 N = 0 has a unique position in the table. If the receptacle does not have a flat any post will fit into it. The receptacle might serves as an alignment mechanism. This feature might be of use in test fixtures. The user should be aware of the following:

a) N = 0 posts cannot be inserted into N ≠ 0 receptacles.

b) N ≠ 0 posts can be inserted into N = 0 receptacles.

This page intentionally left blank

Table of Requirements