10/100/1000 BASE-T Gigabit Ethernet Transceiver

GENERAL DESCRIPTION

The BCM5482S is a dual triple-speed 1000BASE-T/100BASE-TX/10BASE-T Gigabit Ethernet transceiver integrated in a single monolithic CMOS chip. The device performs all physical-layer functions for 1000BASE-T, 100BASE-TX, and 10BASE-T Ethernet on standard category 5 UTP cable. 10BASE-T can also run on standard category 3, 4, and 5 UTP. The BCM5482S also has a serial interface for connection to serial MAC interfaces and fiber modules.

The BCM5482S is a highly integrated solution combining digital adaptive equalizers, ADCs, phase-locked loops, line drivers, encoders, decoders, echo cancellers, crosstalk cancellers, and all required support circuitry. Based on Broadcom's proven digital signal processor technology, the BCM5482S is designed to be fully compliant with RGMII, allowing compatibility with industry-standard Ethernet MACs and switch controllers.

The BCM5482S includes two SerDes cores. The primary SerDes can be configured for SGMII protocol to connect to an SGMII MAC, and the Secondary SerDes can be configured to interface with an SFP/fiber transceiver. The BCM5482S supports 100BASE-FX optical modules through the SerDes interface pins. Media Converter mode provides SerDes-to-copper translation capability.

Note Designed for reliable operation over worst-case Category 5 cable, the BCM5482S automatically negotiates with its link partner to determine the highest possible operating speed. The device detects and corrects most common wiring problems. The digital nature of the BCM5482S allows data to be brought out for displaying cable diagnostics such as attenuation and return loss, using available software.

FEATURES

- Single-chip integrated triple-speed Ethernet transceiver — MAC to magnetics:
  - 1000BASE-T IEEE 802.3ab
  - 100BASE-TX IEEE 802.3u
  - 10BASE-T IEEE 802.3
- IEEE 802.3z
- RGMII, SGMII, and SerDes MAC interface options
- Line-side copper and fiber (1000SX/LX and 100BASE-FX) interfaces
- SGMII-to-SGMII and RGMII-to-SGMII support for 10/100/1000BASE-T SFP modules
- SerDes-to-copper translation for media-converter applications
- Automatic auto-sense mode automatically configures for dual medium applications
- Integrated voltage regulators
- Low EMI emissions
- Super Isolate mode
- Ethernet@WireSpeed™
- Cable plant diagnostic
- Robust CESD tolerance
- Support for jumbo packets up to 10 KB
- Detection and correction of pair swaps (MDI crossover), pair skew, and pair polarity
- Trace matched output impedance
- MAC-side and line-side loopback
- Auto-negotiation with next page support
- 125-MHz clock generator and timing recovery
- JTAG support
- Low-power, 1.2V CMOS core
- 2.5V or 3.3V CMOS I/O
- Industrial temperature available
- Devices packages: 121-pin BGA

APPLICATIONS

- Gigabit Ethernet uplinks
- SGMII-to-SGMII slave converter

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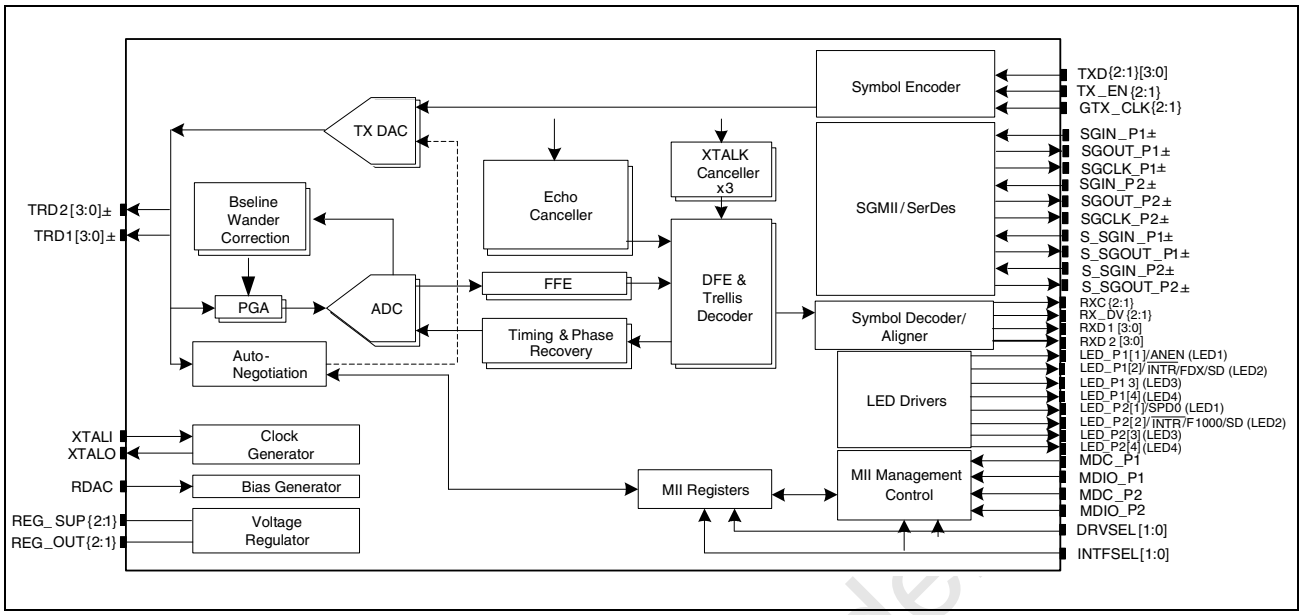

Figure 1: Functional Block Diagram

Revision History

Revision	*Date*	*Change Description*
5482S-DS11-R	01/02/12	**Updated:** • Added notes regarding the Secondary SerDes Interrupt to Table 3: “Hardware Signal Descriptions,” on page lvi
5482S-DS10-R	8/30/11	**Updated:** • Table 3: “Hardware Signal Descriptions,” on page 16 • “CLK125 Clock Output” on page 30 • “RGMII to Copper Configuration” on page 32 • Table 66: “Primary SerDes Control Register (Address 1C, Shadow Value = 10110),” on page 126 • Table 67: “Misc 1000BASE-X Control 2 Register (Address 1C, Shadow Value = 10111),” on page 127 • Table 91: “SGMII Recover Control Register (Address 44h),” on page 167 • Table 101: “Misc 1 Register (Address 10h),” on page 178 • Table 129: “Main Differences Between Standard and RoHS-Compliant Packages,” on page 208 • “Thermal Information” on page 210

Revision	*Date*	*Change Description*
5482S-DS09-R	02/13/09	**Updated:** • Table 3: “Hardware Signal Descriptions,” on page 16: Changed pin description for pin A6 description, and pin label for J1, J2, K1, K2 • Figure 8: “121-Pin FBGA Pinout Diagram, Top View,” on page 27: Changed pin names for E4, K1, and K2. • “RGMII-to-Copper or SGMII-to-Copper Configuration” on page 33: Updated signal names and register name. • “RGMII Interface” on page 40: Text changes. • “Interrupt Function” on page 46: Text changes. • “Media Converter Mode LED” on page 48: Changed LED definitions. • Table 41: “1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Register (Address 18h, Shadow Value 000),” on page 84: Bit 14 description. • “Extended Packet Length” on page 85. Changed maximum packet length. • Table 50: “1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 Register (Address 1Ch, Shadow Value 00010),” on page 103: Changed bits 2 definition. • Table 58: “1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 Register (Address 1Ch, Shadow Value 01101),” on page 113 and Table 58: “1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 Register (Address 1Ch, Shadow Value 01101),” on page 113: Changed definition of bits [7:4] and [3:0]. • Table 90: “Expansion Reg 42h: Operating Mode Status Register,” on page 164: Updated bit 15 description. • Table 101: “Misc 1 Register (Address 10h),” on page 178: Modified definition of bits 4 and [2:1]. • “Secondary SerDes Registers” on page 168: Changed reference to “Secondary SerDes”. • “Ordering Information” on page 212: Deleted obsolete part numbers.
5482S-DS08-R	10/18/07	**Updated:** • Table 119, ”Clock Input Timing,” on page 171 • RGMII parameter in Table 128, ”DC Characteristics,” on page 176 • “Ordering Information” on page 184

Revision	*Date*	*Change Description*
5482S-DS07-R	09/07/07	**Added:** • Figure 8, ”Management Interface,” on page 6 • Note to “Fiber Mode” on page 12 • “Synchronous Ethernet” on page 13 • “BCM5482SE SGMII-to-Fiber Mode” on page 13 • “BCM5482SE SGMII-to-Copper Mode” on page 13 • Table 91, ”SGMII Recover Control Register (Address 44h),” on page 144 • “Shadow Register Selector” on page 111 • “Expansion Register 44h: SGMII Recover Control” on page 144 **Updated:** • D1, D11, C7, and E4 description rows in Table 3, ”Hardware Signal Descriptions,” on page 18 • Figure 9, ”121-Pin FBGA Pinout Diagram, Top View,” on page 25 • Descriptive text in “RGMII Interface” on page 37 • Expansion value register information (44h) Table 19, ”Register Map,” on page 48 • Default values for Bits 7 and 8 in Table 45, ”1000BASE-T/100BASE-TX/ 10BASE-T Misc Control Register (Address 18h, Shadow Value 111),” on page 81 • Descriptive text in “RGMII Timing Mode” on page 82 • Descriptive text in “Shadow Register Selector” on page 97 • Bit values in Table 66, ”Primary SerDes Control Register (Address 1C, Shadow Value = 10110),” on page 111 • XTALI input clock jitter tolerance Max value in Table 119, ”Clock Input Timing,” on page 172 • “Ordering Information” on page 185

Revision	*Date*	*Change Description*
5482S-DS06-R	2/15/07	**Added:** • "SGMII-to-Secondary SerDes 100 FX Application" on page 13 • "ppd = peak to peak differential" on page 14 • "External Control 2" on page 96 • Table 57 on page 96 • "Extended Packet Length (100-FX mode)" on page 150 • "Far End Fault Enable" on page 152 **Updated:** • Table 3 on page 15 • "Ultra-Low Power-Down Mode" on page 26 • "SGMII to 1000BASE-X or SGMII-to-100BASE-FX Configuration" on page 27 • "RGMII-to-100BASE-FX or RGMII-to-1000Base-X Configuration" on page 28 • Table 13 on page 35 • "Interrupt Function" on page 40 • Table 19 on page 45 • "Test Mode" on page 61 • Table 57 on page 96 • Table 58 on page 97 • "LED3 (LINKSPD[2]) Selector" on page 98 • Table 59 on page 99 • "LED4 (Activity) Selector" on page 100 • "SerDes 100BASE-FX Status" on page 101 • Table 61 on page 101 • "SerDes 100BASE-FX Extend Register" on page 102 • Table 62 on page 103 • "SerDes 100BASE-FX Extend Register" on page 102 • Table 66 on page 108 • "SerDes Auto-Negotiation Parallel Detect Enable" on page 108 • Table 67 on page 109 • "Disable Media Converter Updates From GPHY SerDes" on page 109 • "Misc 1 Register (Address 10h)" on page 150 • Table 102 on page 152 • "SerDes Auto-Negotiation Parallel Detect Enable" on page 155 • Table 118 on page 167 • Table 127 on page 171

Revision	*Date*	*Change Description*
5482S-DS05-R	08/10/06	**Updated:** • Table 2, ”Hardware Mode Selection INTFSEL[1:0],” on page 3 • Figure 1, ”Functional Block Diagram,” on page ii • Pins E11, F10, F11, G11, H7, H8, H9, H10, J1, J2, K1, K2 in Table 3, ”Hardware Signal Descriptions,” on page 16 • Figure 8, ”121-Pin FBGA Pinout Diagram, Top View,” on page 23 • “Lineside (Remote) Loopback Mode” on page 29 • “General-Purpose LED Programmability” on page 42 • “Interrupt Function” on page 43 • Table 15, ”Dual Input Configuration/LED Output LEDs,” on page 41 • Table 16, ”Programmable LEDs,” on page 42 • Default values in Table 45, ”1000BASE-T/100BASE-TX/10BASE-T Misc Control Register (Address 18h, Shadow Value 111),” on page 82 and Table 51, ”1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control Register (Address 1Ch, Shadow Value 00011),” on page 94 • Table 19, ”Register Map,” on page 47 • “1000BASE-T/100BASE-TX/10BASE-T LED Selector 1” on page 102 • “1000BASE-T/100BASE-TX/10BASE-T LED Selector 2” on page 104 • “Secondary SerDes Control” on page 109 • Power-Down in “1000BASE-T/100BASE-TX/10BASE-T Registers Descriptions” on page 51, “Primary SerDes Register Descriptions” on page 130, “Secondary SerDes Registers” on page 150 • Table 103, ”Secondary SerDes Control Register,” on page 164 • “Misc 1” on page 160 • “Ordering Information” on page 192

Revision	*Date*	*Change Description*
		Added: • Table 64, ”Primary SerDes Control Register (Address 1C, Shadow Value = 10110),” on page 113 • Table 93, ”1000BASE-X Auto-Negotiation Secondary SerDes Register,” on page 156 • Table 94, ”1000BASE-X Auto-Negotiation Next Page Transmit Register,” on page 157 • Table 95, ”1000BASE-X Auto-Negotiation Link Partner Next Page Register,” on page 158 • Table 103, ”Secondary SerDes Control Register,” on page 164 • Table 113, ”Secondary SerDes Lineside Loopback Control Register,” on page 176 • “Expansion Register 42h: Operating Mode Status” on page 146 • “Expansion Register 50H:SerDes/SGMII RX Control” on page 149 • “1000BASE-X Extended Status” on page 159 • “Packet Counter” on page 162 • “Error Counter” on page 163 • “Misc 1000BASE-X Control 2” on page 165 • “Misc 1000-X Control 3” on page 166 • “Auto-Negotiation 1000BASE-X Debug” on page 167 • “Auxiliary 1000BASE-X Status” on page 170 • “Misc 1000BASE-X Status” on page 171 • “Spare Register” on page 173
5482S-DS04-R	03/14/06	**Updated:** • ”Interrupt Function” on page 42 • Table 104, ”Clock Input Timing,” on page 157 • Table 112, ”DC Characteristics,” on page 162 • ”Mechanical Drawings” on page 167 **Added:** • Table 60, ”SerDes 100BASE-FX Status Register (Address 1Ch, Shadow Value = 10001),” on page 102 • Table 89, ”Auto-Negotiation Advertisement Register (Address 04h),” on page 142 • Table 94, ”Misc 1 Register (Address 10h),” on page 147 • Table 95, ”100BASE-FX Status Register (Address 11h),” on page 148 • Table 96, ”100BASE-FX Test Register (Address 12h),” on page 149 • Table 99, ”Secondary SerDes Auxiliary 1000BASE-X Control Register (Address 1Bh),” on page 151

Revision	*Date*	*Change Description*
5482S-DS03-R	01/16/06	**Updated:** • "Secondary SerDes Interface Data Input" description, pins A3/B3 and A9/B9 in Table 3, "Hardware Signal Descriptions," on page 16 • "DAC Bias Resistor" description, pin L1 in Table 3, "Hardware Signal Descriptions," on page 16 • "Shadow value XXX" to "shadow value 111" in "RGMII-to-Copper Mode" on page 34 • Table note, "Expansion register 03h, bit 1 = 1," to "Expansion register 52h, bit 2 = 1" in Table 13, "SGMII Interface Pins," on page 36 • Step 3 below "SGMII-to-SGMII Slave Mode" on page 36 • Included reference to Table 86, "Expansion Register 52h: SerDes/SGMII Control," on page 137 in Table 19, "Register Map," on page 45 • Bit 11 description in Table 44, "1000BASE-T/100BASE-TX/10BASE-T Misc Test Register (Address 18h, Shadow Value 100)," on page 78 • Table 53 on page 92, to include descriptions for bits 5 and 6 • Typographical errors throughout relating to the phrase, "10/100/1000BASE-T" • Figure 20, "121-Pin FBGA Package," on page 158 **Added:** • Description for "Bias VDD," pin L2, to Table 3, "Hardware Signal Descriptions," on page 16 • Third paragraph below "PHY Address" on page 24 • Step 4 below "SGMII-to-SGMII Slave Mode" on page 36 • Below Table 53 on page 92, added "Signal Detect/Energy Detect Enable" on page 93 • "Expansion Register 52h: SerDes/SGMII Control" on page 137, and Table 86, "Expansion Register 52h: SerDes/SGMII Control," on page 137 • Table 88, "1000BASE-X Auto-Negotiation Link Partner Ability Register," on page 140 • Table 94, "Secondary SerDes Interrupt MASK Register," on page 146
5482S-DS03-R (continued)	01/16/06	**Removed:** • The note "In RGMII-to-fiber mode the following features are not supported: RXC clock delay with respect to RXD data, In-band status (optional) mode" from "RGMII-to-Copper Mode" on page 34 • The phrase "Use the following methods to enter and exit the ultra-low-power mode" from "Ultra-Low Power-Down Mode" on page 27 • The sentence "CRS is still asserted when a valid frame is received" from "Bypass 4B/5B Encoder/Decoder (100BASE-T)" on page 66 • The sentence "The TXEN signal also echoes on the CRS pin and CRS deassertion directly follows the TXEN deassertion" from "10BASE-T Echo Mode" on page 76
5482S-DS02-R	11/07/05	**Updated:** • "Ultra-Low Power-Down Mode" on page 27

Revision	*Date*	*Change Description*
5482S-DS01-R	07/29/05	**Added:** • Industrial temperature version • Table 99, "Theta-Ja vs. Airflow for the FBGA Package with Heat Sink," on page 161 **Updated:** • "Ordering Information" on page 162
5482S-DS00-R	05/19/05	Initial release.

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About This Document

Purpose and Audience

This document describes the BCM5482S dual triple-speed 1000BASE-T/100BASE-TX/10BASE-T Gigabit Ethernet transceiver and is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Document Conventions

The following conventions may be used in this document:

Convention	*Description*
Bold	User input and actions: for example, type **exit**, click **OK,** press **Alt+C**
`Monospace`	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

References

The references in this section may be used in conjunction with this document.

Note: Broadcom provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads & Support site (see Technical Support).

For Broadcom documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	*Number*	*Source*
Broadcom Items		
[1] Configuration Guide for SFP Module with Optical/Copper Applications application note	5482S-AN10x-R	CSP
[2] Reflow Process Guidelines for Surface Mount Assemblies application note	PACKAGING-AN10x-R	CSP

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Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (https://support.broadcom.com). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads & Support site (http://www.broadcom.com/support/).

Section 1: Functional Description

Overview

The BCM5482S is a dual-core Gigabit Ethernet (GbE) transceiver that performs all of the physical layer (PHY) interface functions for 1000BASE-T, 100BASE-TX/FX, and 10BASE-T Ethernet using Category 5 unshielded twisted-pair (UTP) cabling. The 10BASE-T operation is supported on Category 3, 4, and 5 UTP cabling. The BCM5482S connects to a Media Access Controller (MAC) or switch controller through various interfaces, including RGMII, SGMII, and SerDes. Additionally, the BCM5482S offers an SGMII-to-SGMII and an RGMII-to-SGMII converter mode for 10/100/1000BASE-T SFP modules, and a media converter mode that features SerDes-to-copper translation.

SerDes refers to a serial differential digital interface operating at 1.25 Gbaud with an effective 1-Gbps data rate. The interface consists of one differential transmit data and one differential receive data pair. Coding, framing, and protocol comply with IEEE 802.3™, Clauses 36 and 37. The SerDes interface is typically used to interoperate with 1-Gbps fiber-optic modules or other SerDes interfaces.

The BCM5482S supports 1000BASE-SX/LX mode to interface with optical modules through the SerDes interface. The BCM5482S can also be configured to interface with 100BASE-FX optical modules through the BCM5482S twisted-pair signaling.

The device connects directly to network twisted-pair wiring (through isolation transformers) on the other side. The BCM5482S is fully compliant with the IEEE 802.3 standard. The BCM5482S can be programmed to auto-negotiate its operating speed and duplex mode based on the capabilities of the link partner and the quality of the cabling plant.

The BCM5482S adheres to Broadcom's quality procedures and meets, or exceeds, the performance and functionality tests as part of our comprehensive product characterization, qualification, and functional verification process.

Modes of Operation

The BCM5482S supports several operating modes.

Copper Mode

- RGMII-copper (10/100/1000BASE-T)

Fiber Mode

- RGMII-SerDes (1000BASE-X)
- RGMII-SGMII Slave (10/100/1000BASE-T)

SGMII Mode

- SGMII-copper (10/100/1000BASE-T)
- SGMII-SGMII Slave (10/100/1000BASE-T)

Media Converter Mode

SerDes-Copper (Media Converter; 1000BASE-X/1000BASE-T).

These modes are hardware pin configured using the INTFSEL[1:0] and DRVSEL[1:0] pins. Table 1 lists the selectable modes.

Table 1: Hardware Driver Selection DRVSEL[1:0]

Hardware Strapping	***MAC Interface***
DRVSEL[1:0]	***Pad Type***
00	RGMII 2.5V
01	RGMII 2.5V
10	RGMII HSTL without termination
11	RGMII HSTL with termination

Table 2: Hardware Mode Selection INTFSEL[1:0]

Hardware Strapping	***MAC Interface***	***Media Interface***	
INTSEL[1:0]	***Mode***	***Copper***	***SerDes***
00	Copper (RGMII-Copper)	X	–
01	Fiber (RGMII-1000X/100FX or RGMII-SGMII Slave)	–	X
10	SGMII (SGMII-Copper) SGMII (SGMII-SGMII Slave or SGMII-1000X/100FX) ***Note:*** Enabling Secondary SerDes for SGMII-SGMII Slave applications requires register writes (see "SGMII-to-SGMII Slave Mode" on page lxxxii).	X	X
11	Media Converter	X	X

Note: Enabling Secondary SerDes for SGMII-SGMII Slave or SGMII-100FX application requires register writes (see "100BASE-FX" on page lxxix or "SGMII-to-SGMII Slave Mode" on page lxxxii for more information).

Note: The strap pin configuration can be set by software through register 1C shadow 1F bit {2:1]:
00 = Copper (RGMII-Copper)
01 = Fiber (RGMII-1000X/100FX or RGMII-SGMII Slave)
10 = SGMII (SGMII-Copper) SGMII (SGMII-SGMII Slave or SGMII-1000X/100FX)
11 = Media Converter

Reduced Gigabit Media Independent Interface

The Reduced Gigabit Media Independent Interface (RGMII) is a subset of GMII, which allows the MAC with a reduced pin count to connect to the PHY. If this interface is active, the number of data signal pins required to and from the MAC is reduced to half by clocking data on both the rising and falling edge of the transmit clock. This effectively makes the RGMII digital data bit transmission rate twice that of the GMII, while the clock speed remains the same. For more information about this mode, see "RGMII Interface" on page lxxx.

Serial GMII Interface

The BCM5482S can communicate with Ethernet MACs that support the SGMII interface. The Serial GMII (SGMII) interface transmits serial data differentially at 1.25 Gbaud via the SGOUT_Px± pin and receives serial data differentially via the SGIN_Px± pin, which includes an on-chip 100Ω differential termination resistor. In SGMII mode, serial output data is clocked on both edges of a differential 625-MHz clock via the SCLK± pin. Because the BCM5482S provides clock recovery on the SGMII input data, the input clock is not required. The SGMII interface pins are shared with the SerDes interface pins described in "SerDes Interface (Complies with IEEE 802.3™, Clauses 36 and 37)" on page xlii.

This serial interface can also connect to any SerDes-compatible media device (such as a fiber module) to allow transmission to and from a link partner. For additional information regarding the SGMII/SerDes interface, refer to the BCM5482S Design Guide.

SerDes Interface (Complies with IEEE 802.3™, Clauses 36 and 37)

The BCM5482S SerDes interface can be used in numerous applications. Figure 2 through Figure 7 on page xliv illustrate the various applications in which the BCM5482S can be used (also see "SerDes Interface" on page lxxxii).

- SerDes interface can be connected to SerDes fiber modules in a fiber-to-copper media-convertor application.
- SerDes interface can be connected to a SerDes MAC or switch for a SerDes MAC-to-copper application.
- SerDes interface can be used in the RGMII SerDes mode for gigabit fiber application.

The SerDes interface transmits serial data differentially at 1.25 Gbaud via the SGOUT_Px± pin and receives serial data differentially via the SGIN_Px± pin. The SerDes interface pins are shared with the SGMII interface pins.

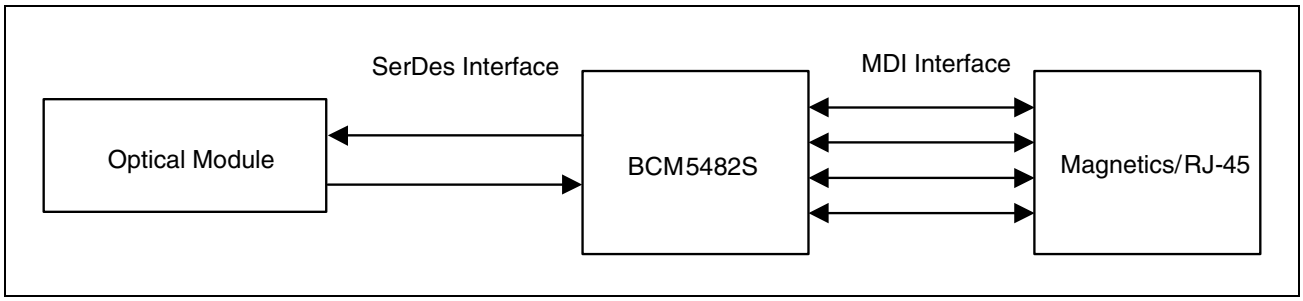


Figure 2: SerDes Fiber-to-Copper Media-Converter Application

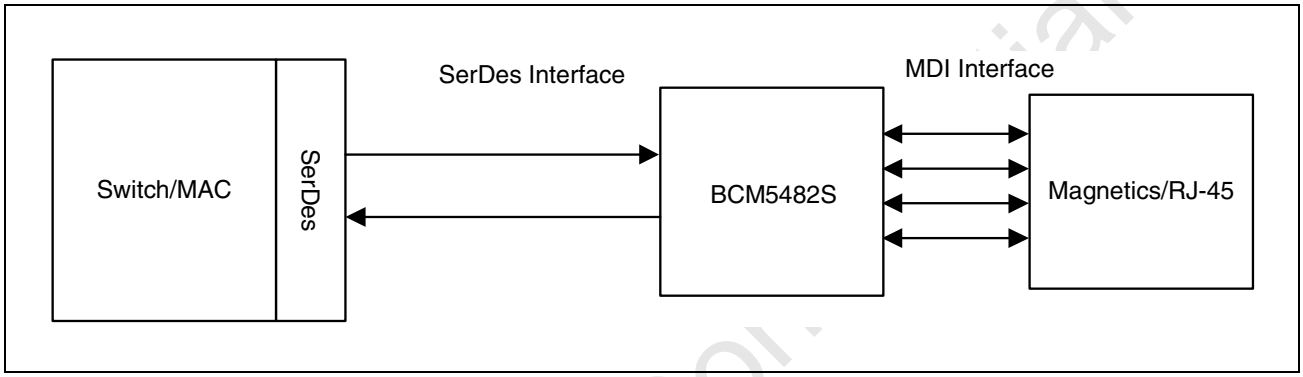


Figure 3: SGMII/SerDes MAC-to-Copper Application

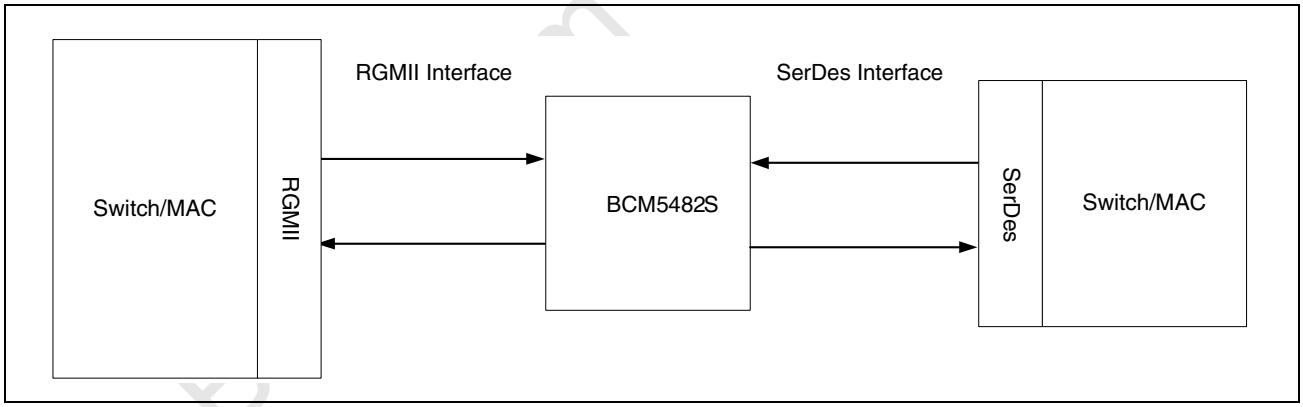


Figure 4: RGMII-to-SGMII/SerDes Application

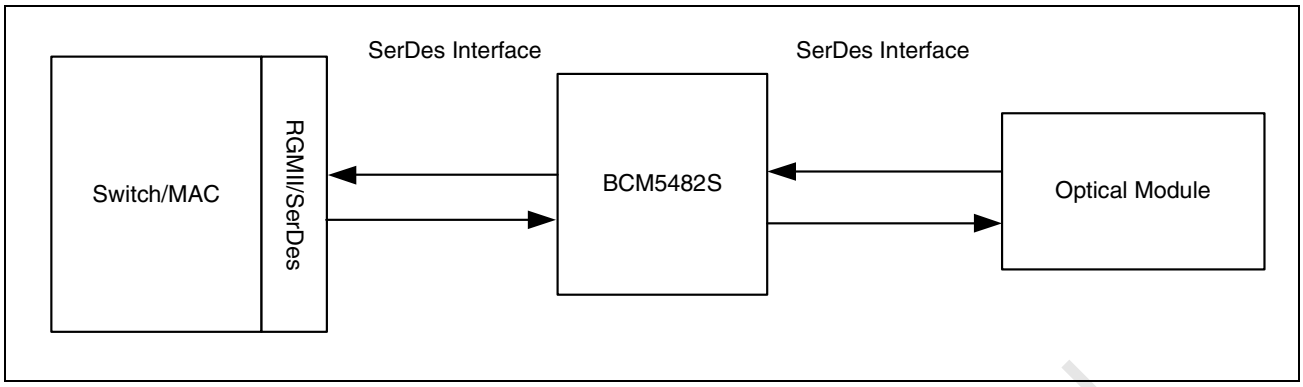


Figure 5: RGMII/SerDes-to-SerDes Application

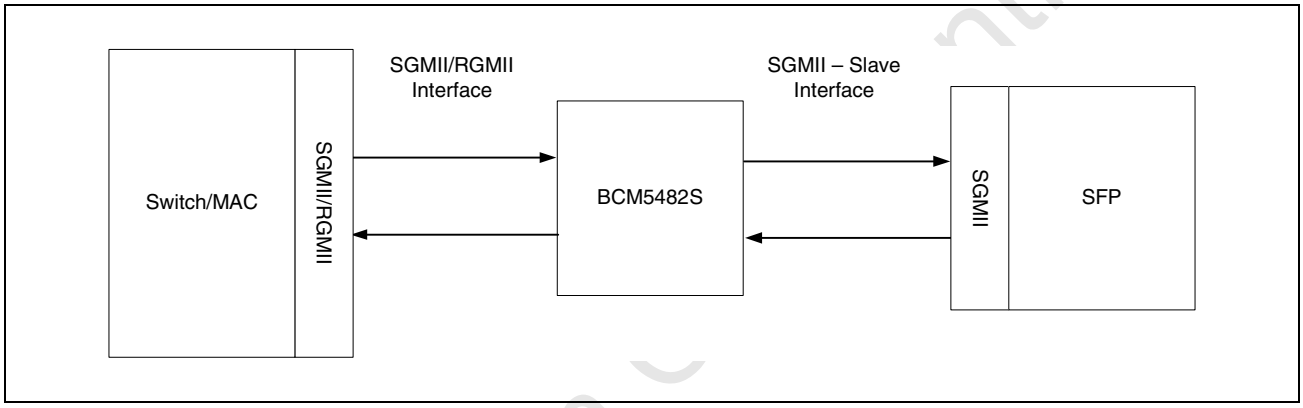


Figure 6: SGMII/RGMII-to-SGMII Slave

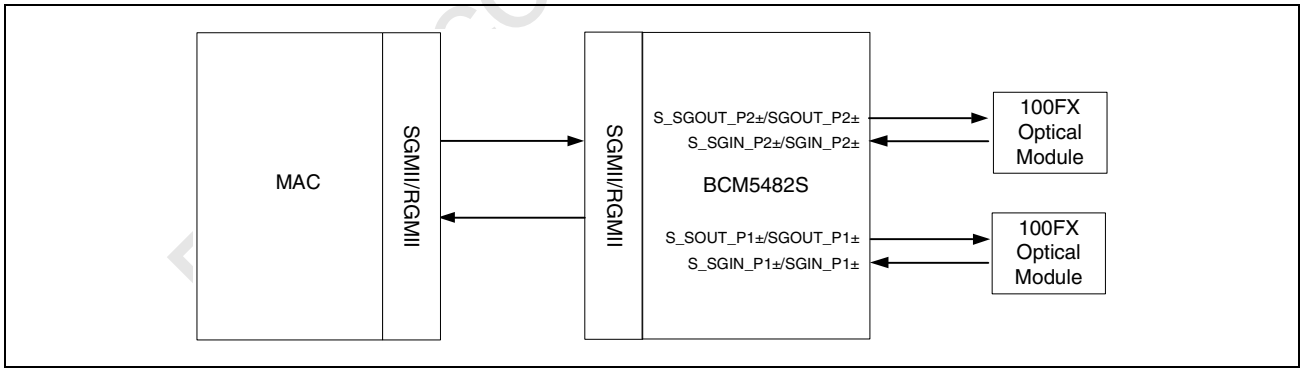


Figure 7: SGMII/RGMII-to-100BASE-FX Application

Management Interface

The BCM5482S contains a large set of management registers. The Status and Control registers of the BCM5482S are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22, and support MDC clock rates up to 12.5 MHz. The management interface supports the defined Status and Control registers of IEEE 802.3, Clauses 22, 28, 37, and 40. In addition, the BCM5482S contains multipurpose registers for extended software control.

There are two MDIO interface pins for each PHY in the dual PHY transceiver. Each PHY transceiver can be accessed independently through its associated MDIO interface pins.

Note: The MDIO and MDC of each port can be connected to use a single serial interface to access both ports. The address of the second port in the BCM5482S is PHY address pin plus one.

Figure 8 shows the management interface connection when a single MDIO bus is used to access both ports.

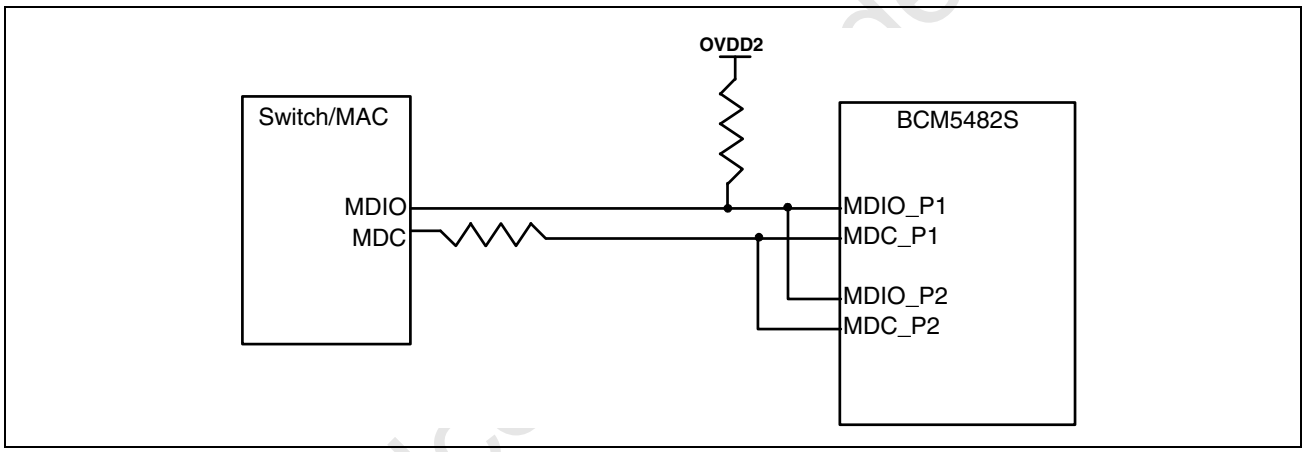


Figure 8: Management Interface

Encoder

In 10BASE-T mode, Manchester encoding is performed on the data stream that is transmitted on the twisted-pair cable. The multimode transmit digital-to-analog converter (DAC) performs pre-equalization for 100m of Category 3 cabling.

In 100BASE-TX mode, the BCM5482S transmits a continuous data stream over the twisted-pair cable. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start-of-stream delimiter (/J/K codes) and appending an end-of-stream delimiter (/T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code groups between packets. The encoded data stream is serialized and then scrambled by the stream cipher block, as described in "Stream Cipher" on page xlix. The scrambled data is then encoded into MLT3 signal levels.

In 1000BASE-T mode, the BCM5482S simultaneously transmits and receives a continuous data stream on all four pairs of the Category 5 cable. Byte-wide data from the transmit data pins is scrambled when the transmit enable is asserted, and the trellis (a PAM5 symbol on each of the four twisted pairs) is encoded into a four-dimensional code group and then inserted into the transmit data stream. The transmit packet is encapsulated by replacing the first two bytes of the preamble with a start-of-stream delimiter and appending an end-of-stream delimiter to the end of the packet. When the transmit error input is asserted during a packet transmission, a transmit error code group is sent in place of the corresponding data code group. The transmitter sends idle code groups or carrier extend code groups between packets. Carrier extension is used by the MAC to separate packets within a multiple-packet burst, and is indicated by asserting the transmit error signal and placing 0Fh on the transmit data pins while the transmit enable is low. A carrier extend error is indicated by replacing the transmit data input with 1Fh during carrier extension.

The encoding complies with IEEE standard 802.3ab and is fully compatible with previous versions of the Broadcom 1000BASE-T PHY.

Decoder

In 10BASE-T mode, Manchester decoding is performed on the data stream.

In 100BASE-TX mode, following equalization and clock recovery, the receive data stream is converted from MLT3 to serial nonreturn to zero (NRZ) data. The NRZ data is descrambled by the stream cipher block, as described later in this document. The descrambled data is then deserialized and aligned into 5-bit code groups. The 5-bit code groups are decoded into 4-bit data nibbles. The start-of-stream delimiter is replaced with preamble nibbles, and the end-of-stream delimiter and idle codes are replaced with 0h. The decoded data is driven onto the RGMII receive data pins. When an invalid code group is detected in the data stream, the BCM5482S will flag the error with an in-band RGMII status code that indicates error. See the RGMII standard for the in-band status reporting code support.

In 1000BASE-T mode, the receive data stream is:

- Passed through the Viterbi decoder
- Descrambled
- Translated back into byte-wide data

The start-of-stream delimiter is replaced with preamble bytes, and the end-of-stream delimiter and idle codes are replaced with 00h. Carrier extend codes are replaced with 0Fh or 1Fh. The decoded data is driven onto the SGMII receive data pins. Decoding complies with IEEE standard 802.3ab and is fully compatible with previous versions of Broadcom 1000BASE-T PHY.

Carrier Sense

Carrier sense is reported with the in-band status mechanized according to the RGMII standard.

In 1000BASE-T SGMII mode and RGMII mode, the carrier sense information is encoded into the control signals.

Link Monitor

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the TRD± pins for the presence of valid link pulses.

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal is detected on the receive pair, the link monitor enters the Link Fail state and the transmission and reception of data packets are disabled. When a valid signal is detected on the receive pair for a minimum of 1 millisecond (ms), the link monitor enters link-pass state and the transmit and receive functions are enabled.

Following auto-negotiation in 1000BASE-T mode, the master transceiver begins sending data on the media. The slave transceiver also begins transmitting when it has recovered the master transceiver's timing. Each end of the link continuously monitors its local receiver status. When the local receiver status has been good for at least 1 microsecond (µs), the link monitor enters the link-pass state and the transmission and reception of data packets are enabled. When the local receiver status is bad for more than 750 ms, the link monitor enters the link-fail state, and the transmission and reception of data packets are then disabled.

Digital Adaptive Equalizer

The digital adaptive equalizer removes intersymbol interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the analog-to-digital converter (ADC) on each channel and produces equalized data. The BCM5482S achieves optimum signal-to-noise ratio by using a combination of feed forward equalization (FFE) and decision feedback equalization (DFE) techniques. Under harsh noise environments, these powerful techniques achieve a bit error rate (BER) of less than 1×10^{-12} for transmissions up to 100m on Category 5 twisted-pair cabling (100m on Category 3 UTP cable for 10BASE-T mode). The all-digital nature of the design makes the performance very tolerant to noise. The filter coefficients are self-adapting to accommodate varying conditions of cable quality and cable length.

Echo Canceler

Because of the bidirectional nature of the channel in 1000BASE-T mode, an echo impairment is caused by each transmitter. The output of the echo filter is added to the FFE output to remove the transmitted signal impairment from the incoming receive signal. The echo canceler coefficients are self-adapting to manage the varying echo impulse responses caused by different channels, transmitters, and environmental conditions.

Crosstalk Canceler

The BCM5482S transmits and receives a continuous data stream on four channels. For a given channel, the signals sent by the other three local transmitters cause impairments on the received signal because of near-end crosstalk (NEXT) between the pairs. The effect can be cancelled because each receiver has access to the data for the other three pairs that cause this interference. The output of the adaptive NEXT canceling filters is added to the FFE output to cancel the NEXT impairment.

Analog-to-Digital Converter

Each receive channel has its own 125-MHz analog-to-digital converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital adaptive equalizer. Advanced analog circuit techniques achieve the following results:

- Low offset
- High-power supply noise rejection
- Fast settling time
- Low bit error rate

Clock Recovery/Generator

The clock recovery and generator block creates the transmit and receive clocks for 1000BASE-T, 100BASE-TX, and 10BASE-T operation. In 10BASE-T or 100BASE-TX mode, the transmit clock is locked to the 25-MHz crystal input, and the receive clock is locked to the incoming data stream.

In 1000BASE-T mode, the two ends of the link perform loop timing. One end of the link is configured as the master, and the other is configured as the slave. The master transmit and receive clocks are locked to the 25-MHz crystal input. The slave transmit and receive clocks are locked to the incoming receive data stream. Loop timing allows for the cancellation of echo and NEXT impairments by ensuring that the transmitter and receiver at each end of the link are operating at the same frequency.

Baseline Wander Correction

1000BASE-T and 100BASE-TX data streams are not always DC-balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can vary with data content. This effect, which is known as baseline wander, can greatly reduce the noise immunity of the receiver. The BCM5482S automatically compensates for baseline wander by removing the DC offset from the input signal, thereby significantly reducing the probability of a receive symbol error.

In 10BASE-T mode, baseline wander correction is not performed because the Manchester coding provides perfect DC balance.

Multimode TX Digital-to-Analog Converter

The multimode transmit digital-to-analog converter (DAC) transmits PAM5, MLT3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that decreases the unwanted high-frequency signal components and reduces electromagnetic interference (EMI). The transmit DAC uses a current drive output that is well-balanced, and, therefore, produces low-noise transmit signals.

Stream Cipher

In 1000BASE-T and 100BASE-TX modes, the transmit data stream is scrambled to reduce radiated emissions and to ensure that there are adequate transitions within the data stream. The 1000BASE-T scrambler also ensures that there is no correlation among symbols on the four different wire pairs and in the transmit and receive data streams. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies. The randomization of the data stream also assists the digital adaptive equalizers and echo/crosstalk cancelers. The algorithms in these circuits require there to be no sequential or cross-channel correlation among symbols in the various data streams.

In 100BASE-TX mode, the transmit data stream is scrambled by exclusive-ORing the encoded serial data stream. This is done with the output of an 11-bit-wide Linear Feedback Shift Register (LFSR), producing a 2047-bit nonrepeating sequence.

In 1000BASE-T mode, the transmit data stream is scrambled by exclusive-ORing the input data byte with an 8-bit-wide cipher text word. The cipher text word generates each symbol period from eight uncorrelated maximal length data sequences that are produced by linear remappings of the 33-bit-wide LFSR output. After the scrambled data bytes are encoded, the sign of each transmitted symbol is again randomized by a 4-bit-wide cipher text word that is generated in the same manner as the 8-bit word. The master and slave transmitters use different scrambler sequences to generate the cipher text words. For repeater or switch applications, where all ports can transmit the same data simultaneously, signal energy is randomized further by using a unique seed to initialize the scrambler sequence for each PHY.

The receiver descrambles the incoming data stream by exclusive-ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle code groups. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle codes. The BCM5482S enables transmission and reception of packet data only when the descrambler is locked. The receiver continually monitors the input data stream to ensure that it has not lost synchronization by checking that inter-packet gaps containing idles or frame extensions are received at expected intervals. When the BCM5482S detects loss of synchronization, it notifies the remote PHY of the inability to receive packets (1000BASE-T mode only) and attempts to resynchronize to the received data stream. If the descrambler is unable to resynchronize for a period of 750 ms, the BCM5482S is forced into the link-fail state.

In 10BASE-T mode, scrambling is not required to reduce radiated emissions.

Wire Map and Pair Skew Correction

During 1000BASE-T operation, the BCM5482S has the ability to automatically detect and correct some UTP cable wiring errors. The symbol decoder detects and compensates for (internal to the BCM5482S) the following errors:

- Wiring errors caused by the swapping of pairs within the UTP cable
- Polarity errors caused by the swapping of wires within a pair

The BCM5482S also automatically compensates for differences in the arrival times of symbols on the four pairs of the UTP cable. The varying arrival times are caused by differing propagation delays (commonly referred to as delay skew) between the wire pairs. The BCM5482S can tolerate delay skews of up to 64 ns. Auto-negotiation must be enabled to take advantage of the wire map correction. During 10/100-Mbps operation, pair swaps are corrected. Delay skew is not an issue though, because only one pair of wires is used in each direction.

Automatic MDI Crossover

Note: This function only operates when the copper auto-negotiation is enabled.

During copper auto-negotiation, one end of the link needs to perform an MDI crossover so that each transceiver's transmitter is connected to the other receiver. The BCM5482S can perform an automatic media dependent interface (MDI) crossover, eliminating the need for crossover cables or cross-wired (MDIX) ports. During auto-negotiation, the BCM5482S normally transmits on the TRD±{0} pin and receives on the TRD±{1} pin.

When connecting to another device that does not perform MDI crossover, the BCM5482S automatically switches its TRD± pin pairs, when necessary, to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

During 1000BASE-T operation, the BCM5482S swaps the transmit symbols on pairs 0 and 1 and pairs 2 and 3 if auto-negotiation completes in the MDI crossover state. The 1000BASE-T receiver automatically detects pair swaps on the receive inputs and aligns the symbols properly within the decoder. During 100BASE-TX and 1000BASE-T operation, pair swaps automatically occur within the device and do not require user intervention.

10/100BASE-T Forced Mode Auto-MDIX

Note: This function only operates when the copper auto-negotiation is disabled.

This feature allows the user to disable the copper auto-negotiation in either 10BASE-T or 100BASE-T and still take advantage of the automatic MDI crossover function. Whenever the forced link is down for a least 4 seconds, then auto-negotiation is internally enabled with its automatic MDI crossover function until link pulses or 100Tx idles are detected. Once detected, the PHY returns to forced mode operation.

The user should set the same speed in register 0 and the auto-negotiation advertisement register 4. For example, the user wanting to force 100Tx full-duplex should write register 0 with 2100h and register 4 with 0181h. The feature is enabled by writing register 18h, shadow 7, bit 9 = 1. Copper link can be determined by reading register 19h, bit 2.

Auto-negotiation

Copper Mode

The BCM5482S, when configured to copper mode (INTF_SEL[1:0] pin set to 00), negotiates its mode of operation over the copper media using the auto-negotiation mechanism, defined in the IEEE 802.3u and 802.3ab specifications. When the auto-negotiation function is enabled, the BCM5482S automatically chooses the mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM5482S can be configured to advertise the following modes:

- 1000BASE-T full-duplex and/or half-duplex
- 100BASE-TX full-duplex and/or half-duplex
- 10BASE-T full-duplex and/or half-duplex

The transceiver negotiates with its link partner and chooses the highest common operating speed and duplex mode commonly referred to as highest common denominator (HCD). Auto-negotiation can be enabled or disabled by hardware and software control, but is always required for 1000BASE-T operation. For details on auto-negotiation using Next Page Exchange, see “Next Page Exchange” on page lxxviii.

Fiber Mode

When configured to fiber mode (INTF_SEL[1:0] pins set to 01), the BCM5482S sends base-page code words according to 1000BASE-X auto-negotiation as described in IEEE 802.3, Clause 37. The duplex ability is advertised, but the speed ability is not. The base page is encoded based on the bits contained in 1000BASE-X Auto-negotiation Advertisement Register (Address 04h). The values of the received base page are stored in 1000BASE-X Auto-Negotiation Link Partner Ability Register–Base Page (Address 05h). The flow control and remote fault status bits are sourced from 1000BASE-X Auto-negotiation Advertisement Register (Address 04h). By default, the SerDes auto-negotiation specifies no flow control, but this can be changed by writing to this register.

Note: When Auto-negotiation is off for the fiber interface, the parallel detect should be off (register 1C, shadow 16, bit 1 = 0, or Secondary SerDes register 16, bit 1=0).

SGMII Mode

When configured to SGMII mode (INTF_SEL[1:0] pins set to 10), the BCM5482S copper interface auto-negotiates based on Clauses 28 and 40 of IEEE 802.3. The SGMII interface auto-negotiates according to 1000BASE-X auto-negotiation as described in IEEE 802.3, Clause 37, except for a few changes to operate in SGMII mode. The link timer is reduced to 1.6 ms and the auto-negotiation code-word is changed to reflect the copper link, copper duplex, and copper speed. Whenever the copper link changes, the SGMII auto-negotiation is restarted with the current copper duplex, speed, and link control information transmitted to the MAC/ switch.

Media Converter Mode

When configured to media converter mode (INTF_SEL[1:0] pins set to 11), the BCM5482S SerDes interface auto-negotiates according to 1000BASE-X auto-negotiation as described in IEEE 802.3, Clause 37. The copper interface auto-negotiates based on Clauses 28 and 40 of IEEE 802.3. The copper and SerDes auto-negotiation abilities are passed through the media. The negotiated highest common denominator (HCD) ability must match between the copper and SerDes interface before a link is established. The SerDes does not link up when there is an HCD mismatch between the SerDes link partners, similar to the copper interface. The SerDes does not link up until the copper links up. The SerDes continues to cycle through auto-negotiation, transmitting an offline remote fault until the copper is linked up. The transmission of the remote fault can be disabled by software control.

The ANEN, SPD0, and F1000 pins change functionality when the device is in media converter mode. The SPD0 becomes the default advertised PAUSE ability, F1000 becomes the default advertised Asymmetric PAUSE ability, and ANEN becomes the default advertised half-duplex ability. The copper and SerDes interfaces are set to auto-negotiation enabled mode, advertising 1-Gbps speed only.

Synchronous Ethernet

The BCM5482S provides a recovery clock from the line to synchronize between two Ethernet point-to-point link partners to a telecom standard in the SGMII or RGMII MAC interface mode. A Clean Up PLL should be used to clean up the recovery clock to filter excessive jitter accumulated by signal propagation through the channel or added randomly. The synchronous Ethernet function is only supported in the BCM5482S version.

The BCM5482S provides two recovered clock outputs for the fiber mode (RF_CLK1, RF_CLK2), and two recovered clock outputs for the copper mode (RC_CLK1, RC_CLK2).

BCM5482SSGMII-to-Fiber Mode

The recovery clock from the line side of the SGMII-to-Fiber mode has been multiplexed on RGMII data bit 0 for the synchronous ethernet application.

RXD1[0]/RF_CLK1 is the recovered clock from fiber interface port 1. This is a dual-function pin. When expansion register 44 bit 4 of port 1 is clear, this pin is configured for RXD1[0]. When expansion register 44 bit 4 of port 1 is set, this pin is configured for the recovered (RF_CLK1) clock from fiber interface port 1.

RXD2[0]/RF_CLK2 is the recovered clock from fiber interface port 2. This is a dual-function pin. When expansion register 44 bit 4 of port 2 is clear, this pin is configured for RXD2[0]. When expansion register 44 bit 4 of port 2 is set, this pin is configured for the recovered clock (RF_CLK2) from fiber interface port 2.

BCM5482SSGMII-to-Copper Mode

The recovery clock from the line side for the SGMII-to-copper mode has been multiplexed on the RXC signal for the synchronous ethernet application.

RXC1/RC_CLK1 is the recovered clock from copper Interface port 1. This is a dual-function pin. When expansion register 44 bit 4 of port 1 is clear, this pin is configured for RXC1. When expansion register 44 bit 4 of port 1 is set, this pin is configured for the recovered clock (RC_CLK1) from copper interface port 1.

RXC2/RC_CLK2 is the recovered clock from copper interface port 2. This is a dual-function pin. When expansion register 44 bit 4 of port 2 is clear, this pin is configured for RXC2. When expansion register 44 bit 4 of port 2 is set, this pin is configured for the recovered clock (RC_CLK2) from copper interface port 2.

Note: Expansion Register 44 bit 4 should not be set when the device is configured for the RGMII-to-copper/fiber mode.

Energy Detect

The energy-detect feature provides an output signal (ENERGYDET) indicating the presence or absence of energy being received on the copper analog input pins of the chip. Additionally, the copper energy-detection status can be monitored from register 1Ch, shadow 11111, bit 5. See “Operational Description” on page lxviii for details.

Internal Voltage Regulators

Two independent integrated voltage regulators have been provided for designs where a supply of 1.2V is not available. These regulators accept input voltage from 1.8V to 2.5V and regulate down to 1.2V, and do not require any external components. See “Operational Description” on page lxviii for details.

Power-Down Modes

Three low-power modes are supported in the BCM5482S:

- Ultra-low power-down mode (IDDQ)
- Standby power-down mode
- Auto power-down mode

For details, see "Auto Power-Down Mode" on page lxx.

Additional power savings can be made by:

- Using 2.5V instead of 3.3V for OVDD.
- Using external 1.2V supplies for power groups that run at 1.2V.
- Using 1.8V instead of 2.5V at the TRD± pull-up resistors and magnetics center tap.

Jumbo Packets

Copper Modes

Packets up to 10 KB in length can be supported with the following register writes:

- Register 18h, shadow 000, bit 14 = 1 (default = 0)
- Register 10h, bit 0 = 1 (default = 0)

Fiber Mode

Packets up to 10 KB in length can be supported with the following register write:

- Register 1Ch, shadow 11011, bit 1 = 1 (default = 1)

SGMII/Media Converter Mode

Packets up to 10 KB in length can be supported with the following register writes:

- Register 1Ch, shadow 11011, bit 1 = 1 (default = 1)
- Register 1Ch, shadow 11000, bit 2 = 1 (default = 1)
- Register 18h, shadow 000, bit 14 = 1 (default = 1 in media converter mode; otherwise, default = 0)

SGMII-to-Secondary SerDes 100 FX Application

Set secondary SerDes 10h bit 0 to 1

Section 2: Hardware Signal Descriptions

The following conventions are used in Table 3 on page lvi:

- I = Input
- O = Output
- I/O = Bidirectional
- OD = Open drain output
- OT= Tristate signal
- B = Bias
- PU = Internal pull-up
- PD = Internal pull-down
- SOR = Sample on reset
- CS = Continuously sampled
- ppd = peak to peak differential

The following conventions are used to express the I/O types in Table 3 on page lvi. The I/O pin type is useful in referencing the DC pin characteristics contained in Section 7: “Electrical Characteristics,” on page ccxliv:

- XT = Crystal inputs/outputs pin type
- D = Digital pin type
- G = GMII pin type
- S = SerDes pin type
- A = Analog pin type
- PECL = Positive Emitter Coupled Logic
- ST = Schmitt trigger

Note: Pin groups that are not found on a certain package are represented by an en dash (–).

Refer to the *BCM5482S Configuration Guide for SFP Module with Optical/Copper Applications* application note for additional information regarding the configurations and bypassing of the power supply pins.

Table 3: Hardware Signal Descriptions

121-Pin BGA	Label	I/O	Description
Media Connections			
K3/L3	TRD1[0]±	A	Transmit/Receive Pairs For Port1. In 1000BASE-T mode, differential data from copper media is transmitted and received on all four TRD± signal pairs. In auto-negotiation, 10BASE-T, and 100BASE-TX modes, the BCM5482S normally transmits on TRD±[0] and receives on TRD±[1]. Auto-MDIX operation can reverse the pairs.
K4/L4	TRD1[1]±		
K5/L5	TRD1[2]±		
K6/L6	TRD1[3]±		
K10/L10	TRD2[0]±	A	**Transmit/Receive Pairs For Port2.** In 1000BASE-T mode, differential data from copper media is transmitted and received on all four TRD± signal pairs. In auto-negotiation, 10BASE-T, and 100BASE-TX modes, the BCM5482S normally transmits on TRD±[0] and receives on TRD±[1]. Auto-MDIX operation can reverse the pairs
K9/L9	TRD2[1]±		
K8/L8	TRD2[2]±		
K7/L7	TRD2[3]±		
Clock			
A6	XTALI	I/XT	**25-MHz Crystal Oscillator Input/Output.** A continuous 25-MHz reference clock must be supplied to the BCM5482S by connecting a 25-MHz crystal to the BCM5482S by connecting a 25-MHz crystal between these two pins or by driving XTALI with an external 25-MHz clock. When using a crystal, connect a loading capacitor from each pin to GND. When using an oscillator, leave XTALO unconnected. The maximum XTALI input voltage level is XTALVDD + 0.5V.
B6	XTALO	O/XT	
E3	CLK125	O,G	**MAC Reference Clock.** Continuous 125-MHz output generated off the PLL (phase locked to the XTALI input). This clock output remains active and stable during both hardware and software reset. ***Note:*** CLK125 is running in RGMII mode. ***Note:*** CLK125 is not running in SGMII mode.
RGMII/SGMII			
C1	GTXCLK1	I PD,G	**RGMII Transmit Clock for Port1.** This input clock needs a: • 125-MHz clock in 1000BASE-X mode • 25-MHz clock in 100BASE-TX and 100BASE-FX mode • 2.5-MHz clock in 10BASE-T mode In RGMII mode, both edges of the clock are used to align with TXD1[3:0].
C11	GTXCLK2	I PD,G	**RGMII Transmit Clock for Port2.** This input clock needs a: • 125-MHz clock in 1000BASE-X mode • 25-MHz clock in 100BASE-TX and 100BASE-FX mode • 2.5-MHz clock in 10BASE-T mode In RGMII mode, both edges of the clock are used to align with TXD2[3:0].

Table 3: Hardware Signal Descriptions (Cont.)

121-Pin BGA	Label	I/O	Description
C5 C4 C3 C2	TXD1[0] TXD1[1] TXD1[2] TXD1[3]	I PD, G	**Transmit Data Input For Port1.** Nibble-wide transmit data is input synchronously to the RGMII transmit clock. TXD[3] is the most significant bit. In 10BASE-T, 100BASE-TX, and RGMII mode, only In 10BASE-T, 100BASE-TX, and RGMII mode, only TXD[3:0] are used. TXD[3] is the most significant bit.
D10 D9 C9 C10	TXD2[0] TXD2[1] TXD2[2] TXD2[3]	I PD, G	**Transmit Data Input For Port2.** Nibble-wide transmit data is input synchronously to the RGMII transmit clock. TXD[3] is the most significant bit. In 10BASE-T, 100BASE-TX, and RGMII mode, only In 10BASE-T, 100BASE-TX, and RGMII mode, only TXD[3:0] are used. TXD[3] is the most significant bit.
D5 D8	TX_EN1 TX_EN2	I PD, G	**Transmit Enable.** Active high. When TX_EN is asserted, the data on the TXD pins is encoded and transmitted. TX_EN1 is for port1 and TX_EN2 is for port2.
D2	RX_DV1	OT, G	**Receive Data Valid For Port1.** Active high. RX_DV indicates that a receive frame is in progress and that the data present on the RXD output pins is valid. RXDV1 output is a 50 ohm driver.
E8	RX_DV2	OT, G	**Receive Data Valid For Port2.** Active high. RX_DV indicates that a receive frame is in progress and that the data present on the RXD output pins is valid. RX_DV2 output is a 50Ω driver.
D1	RXC1/RC_CLK1	OT, G	**Receive Clock/Copper Recovered Clock.** This is a dual function signal. • **Receive clock**. In the RGMII mode, this signal is Receive Clock for the RGMII interface. The frequency of the receive clock is set according to the link speed as follows: – 1000BASE-TX/1000BASE-X mode; the clock is 125 MHz, byte-aligned on RXD[3:0]. – 100BASE-TX/100BASE-FX mode; the clock is 25 MHz, nibble-aligned on RXD[3:0]. – 10BASE-T mode; the clock is 2.5 MHz, nibble-aligned on RXD[3:0]. • **Copper recovered clock**: – This signal can be configured to become the recovered clock from the copper interface when the BCM5482S is in SGMII-to-copper mode. When register 44 bit 4 of port 1 is set (1), this signal becomes RC_CLK1. When the register 44 bit 4 of port 1 is clear (0), the signal operates in the normal mode as RXC1 clock for the RGMII interface. ***Note:*** RXC1/RC_CLK1 output is a 50Ω driver.

Table 3: Hardware Signal Descriptions (Cont.)

121-Pin BGA	Label	I/O	Description
D11	RXC2/RC_CLK2	OT, G	**Receive Clock/Copper Recovered Clock.** This is a dual function signal with a 2.5/25/125-MHz output. This clock is recovered from the incoming analog waveforms and is used to synchronize the receive data outputs for port2: • **Receive clock**. In the RGMII mode, this signal is Receive Clock for the RGMII interface. The frequency of the receive clock is set according to the link speed as follows: – 1000BASE-TX/1000BASE-X mode; the clock is 125MHz, byte-aligned on RXD[3:0]. – 100BASE-TX/100BASE-FX mode; the clock is 25MHz, nibble-aligned on RXD[3:0]. – 10BASE-T mode; the clock is 2.5MHz, nibble-aligned on RXD[3:0]. • **Copper recovered clock**: – This signal can be configured to become the recovered clock from the copper interface when the BCM5482S is in SGMII-to-copper mode. When register 44 bit 4 of port 2 is set (1), this signal becomes RC_CLK2. When the register 44 bit 4 of port 2 is clear (0), the signal operates in the normal mode as RXC2 clock for the RGMII interface. ***Note:*** RXC2/RC_CLK2 output is a 50Ω driver.
E4 E5 D4 D3	RXD1[0]/RF_CLK1 RXD1[1] RXD1[2] RXD1[3]	OT,G	**Receive Data Outputs for Port1.** Byte-wide receive data output synchronous with the receive clock. • Receive data outputs: – RXD[3] is the most significant bit. – RXD output is a 50Ω output driver. – RXD1[0]/RF_CLK1 is a dual-function signal. – The recover clock from the fiber interface is enabled when expansion register 44 bit 4 of port 1 is set (1) in the SGMII-to-fiber mode. When expansion register 44 bit 4 is clear (0), this signal functions as RXD1[0]
C7 C8 D7 E7	RXD2[0]/RF_CLK2 RXD2[1] RXD2[2] RXD2[3]	OT,G	**Receive Data Outputs for Port2.** Byte-wide receive data output synchronous with the receive clock. • Receive data outputs: – RXD[3] is the most significant bit. – RXD output is a 50Ω output driver. – RXD2[0]/RF_CLK2 is a dual function signals. – The recover clock from the fiber interface is enabled when expansion register 44 bit 4 of port 2 is set (1) in the SGMII-to-fiber mode. When expansion register 44 bit 4 is clear (0), this signal functions as RXD2[0]
SGMII/SerDes Interface			

Table 3: Hardware Signal Descriptions (Cont.)

121-Pin BGA	Label	I/O	Description
A1 B1	SGIN_P1+ SGIN_P1–	I S	**SGMII/SerDes Interface Data Input.** Differential serial data input when the BCM5482S is in SGMII or SerDes interface mode. Each of the pins has an internal 50Ω termination resistor to ground.
A7 B7	SGIN_P2+ SGIN_P2–	I S	**SGMII/SerDes Interface Data Input.** Differential serial data input when the BCM5482S is in SGMII or SerDes interface mode. Each of the pins has an internal 50Ω termination resistor to ground.
A5 B5	SGOUT_P1+ SGOUT_P1–	O S	**SGMII/SerDes Interface Data Output.** Differential serial data output when the BCM5482S is in SGMII or SerDes interface mode.
A11 B11	SGOUT_P2+ SGOUT_P2–	O S	**SGMII/SerDes Interface Data Output.** Differential serial data output when the BCM5482S is in SGMII or SerDes interface mode.
A4 B4	SGCLK_P1+ SGCLK_P1–	O S	**SGMII Output Clock.** Differential serial clock output running at 625 MHz when the BCM5482S is in SGMII mode. The SGMII clock can be disabled by setting Expansion Register 52h, bit 2.
A10 B10	SGCLK_P2+ SGCLK_P2–	O S	**SGMII Output Clock.** Differential serial clock output running at 625 MHz when the BCM5482S is in SGMII mode. The SGMII clock can be disabled by setting Expansion register 52h, bit 2.
A3 B3	S_SGIN_P1+ S_SGIN_P1–	I S	**Secondary SerDes Interface Data Input.** Differential serial data input of secondary SerDes. Each of the differential pairs have an internal 100Ω termination resistor.
A9 B9	S_SGIN_P2+ S_SGIN_P2–	I S	**Secondary SerDes Interface Data Input.** Differential serial data input of secondary SerDes. Each of the differential pairs have an internal 100Ω termination resistor.
A2 B2	S_SGOUT_P1+ S_SGOUT_P1–	O S	**Secondary SerDes Interface Data Output.** Differential serial data output when the BCM5482S secondary SerDes is enabled.
A8 B8	S_SGOUT_P2+ S_SGOUT_P2–	O S	**Secondary SerDes Interface Data Output.** Differential serial data output when the BCM5482S secondary SerDes is enabled.
Mode			
J9	PHYA[0]	I PD, SOR	**PHY Address Selects.** Active high. **Reset.** The PHY address selects the MII management. **PHY Address. The device goes into isolate mode.** When the PHY address is strapped to 00000. To get out of isolate mode, write to register 00h, bit 10 = 0.
H11	PHYA[1]	I PD, SOR	
J11	PHYA[2]	I PD, SOR	
K11	PHYA[3]	I PD, SOR	
L11	PHYA[4]	I PD, SOR	
F11	MDC_P1	I PD, ST	**Management Data Clock for Port1.** The MDC clock input must be provided to allow MII management functions. MDC_P1 is for port1.
G11	MDC_P2	I PD, ST	**Management Data Clock for Port2.** The MDC clock input must be provided to allow MII management functions. MDC_P2 is for port2.

Table 3: Hardware Signal Descriptions (Cont.)

121-Pin BGA	Label	I/O	Description
E10	MDIO_P1	I/O PU, D,ST	**Management Data I/O for Port1.** This serial input/output bit is used to read from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC_P1.
F10	MDIO_P2	I/O PU, D,ST	**Management Data I/O for Port2.** This serial input/output bit is used to read from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC_P2.
G10	RESET	I PU, CS, ST	**Reset.** Active low, Schmitt Trigger Input. The BCM5482S requires a hardware RESET prior to normal operation. Configuration settings obtained via Hardware Strap Option pins are latched on the rising edge of RESET. During RESET, if PHYAD[4:0] = 00000, then all RGMII signals are tristated.
H5	DRVSEL[0]	I PD, CS	**Pad Drive Select.**
H4	DRVSEL[1]	I PD, CS	**Pad Drive Select.** ***Note:*** If the driver select of the pad for RGMII is not used, leave them unconnected. 00 = RGMII 2.5V 01 = RGMII 2.5V 10 = RGMII HSTL without termination 11 = RGMII HSTL with termination
G5	INTFSEL[0]	I PD, CS	**MAC Interface Mode Select [1:0].**
G6	INTFSEL[1]	I PD, CS	00 = RGMII-copper (copper mode) 01 = RGMII-fiber (fiber mode) 10 = SGMII-copper (SGMII mode) 11 = SerDes-copper (media converter mode) ***Note:*** The INTFSEL[1:0] pins should strap to 01 when the user wants to configure one port to RGMII-copper and the other port to SGMII/Fiber through register 1C shadow 1F.[2:1].
H7	LED_P1[1]/ANEN	I PU, O	**Programmable LED/ANEN Mode Select During Power Reset.** For more details, see LED Note below. **Active low.** Default is programed to LINKSPD[1] status signal for port1. This pin can be programmed to alternates mode. See "General-Purpose LED Programmability" on page lxxxv (LED1) for more details. **Auto-negotiation Select (ANEN).** Active high. Sampled on reset. When this pin is high, auto-negotiation is enabled. When low, auto-negotiation is disabled. After reset, the auto-negotiation function is under software control. This pin works in conjunction with the SPD0 and F1000 to setup the default speed of the device. When the device is configured to media converter mode by the INTF_SEL[1:0] pins, the ANEN pin becomes the half-duplex advertise pin. ***Note:*** Secondary SerDes Interrupt is only supported on LED1 (H7).

Table 3: Hardware Signal Descriptions (Cont.)

121-Pin BGA	Label	I/O	Description
H8	LED_P1[2]/$\overline{\text{INTR}}$/FDX/ SD	I PU, O, Od	**Programmable LED/FDX Mode Select During Power Reset.** For more details, see LED Note below. **PHY Interrupt.** Active low. Driven low when an unmasked PHY interrupt occurs. The functionality of the PHY Interrupt pin can be monitored and altered by writing to registers 1Ah and 1Bh. This pin can be programmed to alternate modes. See "General-Purpose LED Programmability" on page lxxxv (LED2) for more details. ***Note:*** When the pin is programmed to be used as the INTR pin, it will become an open drain driver. **Full-Duplex Select (FDX).** Active high. Sampled on reset. This pin sets the default value of the copper interface manual duplex mode bit in the MII Control register. This pin also sets the default value of the auto-negotiation advertised abilities for 10BASE-T, 100BASE-TX, and 1000BASE-T full-duplex capability. After reset, all duplex mode bits are under software control. **Signal Detect.** Active high. When the BCM5482S operates in 1000BASE-SX/LX/100BASE-FX, this signal is sourced from the external fiber module to indicate a valid optical-fiber signal. In 1000BASE-SX/LX, the input can be inverted by software, qualified with the PCS synchronization, and filtered and debounced. ***Note:*** Secondary SerDes Interrupt is not supported on this LED2 (H8).
J1	LED_P1[3] ***Note:*** Only for BCM5482SHXXXXXX package; other packages this pin is NC	I PU, O	**Programmable LED.** For more details see LED Note below. **Active low.** Default is programed to LINKSPD[1] status signal for port1. This pin can be programmed to alternates mode. See "General-Purpose LED Programmability" on page lxxxv (LED3) for more details. ***Note:*** Secondary SerDes Interrupt is not supported on this LED3 (J1).
J2	LED_P1[4] ***Note:*** Only for BCM5482SHXXXXXX package; other packages this pin is NC	I PU, O	**Programmable LED.** For more details see LED Note below. **Active low.** Default is programed to activity status signal for port1. This pin can be programmed to alternates mode. See "General-Purpose LED Programmability" on page lxxxv (LED4) for more details. ***Note:*** Secondary SerDes Interrupt is not supported on this LED4 (J2).

Table 3: Hardware Signal Descriptions (Cont.)

121-Pin BGA	Label	I/O	Description
H9	LED_P2[1]/SPD0	I PD, O	**Programmable LED/SPD0 Mode Select During Power Reset.** For more details, see LED Note below. **Active low.** Default is programed to LINKSPD[1] status signal for port2. This pin can be programmed to alternates mode. See "General-Purpose LED Programmability" on page lxxxv (LED1) for more details. **Speed Select (SPD0).** Active high. These pins set the default advertisement of the BCM5482S according to the following table. ***Note:*** Secondary SerDes Interrupt is only supported on LED1 (H9) for A2 version.
K1	LED_P2[3] ***Note:*** Only for BCM5482SHXXXXXX package; other packages this pin is NC	I PU, O	**Programmable LED.** For more details see LED Note below. **Active low.** Default is programed to LINKSPD[2] status signal. This pin can be programmed to alternates mode. See "General-Purpose LED Programmability" on page lxxxv (LED3) for more details. ***Note:*** Secondary SerDes Interrupt is not supported on this LED3 (JK1).
K2	LED_P2[4] ***Note:*** Only for BCM5482SHXXXXXX package; other packages this pin is NC	I PU, O	**Programmable LED.** For more details see LED Note below. **Active low.** Default is programed to alternates mode. See "General-Purpose LED Programmability" on page lxxxv (LED4) for more details. ***Note:*** Secondary SerDes Interrupt is not supported on this LED4 (K2).
H10	LED_P2[2]/$\overline{\text{INTR}}$/F1000/SD	I PU, O, Od	**Programmable LED/F1000 Mode Select During Power Reset.** For more details, see Note LED below. **PHY Interrupt.** Active low. Driven low when an unmasked PHY interrupt occurs. The functionality of the PHY Interrupt pin can be monitored and altered by writing to registers 1Ah and 1Bh. This pin can be programmed to alternate modes. See "General-Purpose LED Programmability" on page lxxxv (LED2) for more details. ***Note:*** When the pin is programmed to be used as the INTR pin, it will become an open drain driver. **ANENF1000SPD0Description** 0 0 0 Force 10BASE-T 0 0 1 Force 100BASE-TX 0 1 X Force 1000BASE-T (See Note below) 1 0 0 Auto-negotiate advertise: 10BASE-T 1 0 1 Auto-negotiate advertise: 10/100BASE-TX 1 1 0 Auto-negotiate advertise: 10/100/1000BASE-T 1 1 1 Auto-negotiate advertise: 1000BASE-T

Table 3: Hardware Signal Descriptions (Cont.)

121-Pin BGA	Label	I/O	Description
			When the device is configured to media converter mode by the INTF_SEL[1:0] pins, the F1000 and SPD0 functionality become the following: • F1000: Asymmetric PAUSE advertised • SPD0: PAUSE advertised ***Note:*** FORCE 1000BASE-T mode is for test purposes only, and disabling auto-negotiation can lead to link configuration mismatches and no-link situations. ***Note:*** The Annex 28D.5 Extensions Required for Clause 40 (1000BASE-T) IEEE 802.3 specification requires that auto-negotiation be used in 1000BASE-T operation. There are no standards that govern a protocol for 1000BASE-T operation without auto-negotiation. Broadcom recommends enabling and using auto-negotiation. For systems that only need 1000BASE-T functionality, Broadcom recommends enabling auto-negotiation with only 1000BASE-T being advertised and that the advertising bits for all other modes be disabled. **Signal Detect.** Active high. When the BCM5482S operates in 1000BASE-SX/LX/100BASE-FX, this signal is sourced from the external fiber module to indicate a valid optical-fiber signal. In 1000BASE-SX/LX, the input can be inverted by software, qualified with the PCS synchronization, and filtered and debounced. ***Note:*** Secondary SerDes Interrupt is not supported on this LED2 (H10).

Table 3: Hardware Signal Descriptions (Cont.)

121-Pin BGA	Label	I/O	Description
			LED Note: All four of the LED outputs behave as either push-pull outputs or open drain outputs, depending on the function selected for that LED pin. Any LED pin programmed to output the interrupt function (INTR) behaves like an open drain output. Any LED programmed for the following behave as push-pull outputs: • LINKSPD1 • LINKSPD2 • XMITLED • ACTIVITY • FDXLED • SLAVE • QUALITY • RCVLED • WSPDNGD • MULTICOLOR • OPENSHORT • ENERGYLNK When in media converter mode, the LEDs are open drain. All other LED output functions behave as push-pull drivers. The programmable LED default values for the four per-port LEDs are as follows for SGMII/GMII/RGMII to copper modes.
Test			
F8 F9 H2	TEST0 TEST1 TVCO	I PD, CS, A	**Test Mode Enables.** Active high. These pins must always be pulled low during normal operation. Pulling both pins high tristates all outputs. These pins are used by Broadcom for test purposes only. **GHPY PLL Output Clock.** Analog clock output. This pin should be left unconnected.
JTAG			
F7	TCK	I PU, CS	**Test Clock.** JTAG serial clock.
G8	TDI	I PU, CS	**Test Data Input.** JTAG serial data input.
G9	TDO	OT	**Test Data Output.** JTAG serial data output.
G7	TMS	I PU	**Test Mode Select.** JTAG mode select input.
H6	TRST	I PU, CS	**JTAG Reset.** Active low. Resets the JTAG controller. This signal must be pulled low during normal operation.
Bias			
L1	RDAC	A	**DAC Bias Resistor.** Adjusts the reference current of the transmitter digital to analog converter. A 1.24-kΩ ±1% resistor must be connected between the RDAC pin and AGND.
Power			

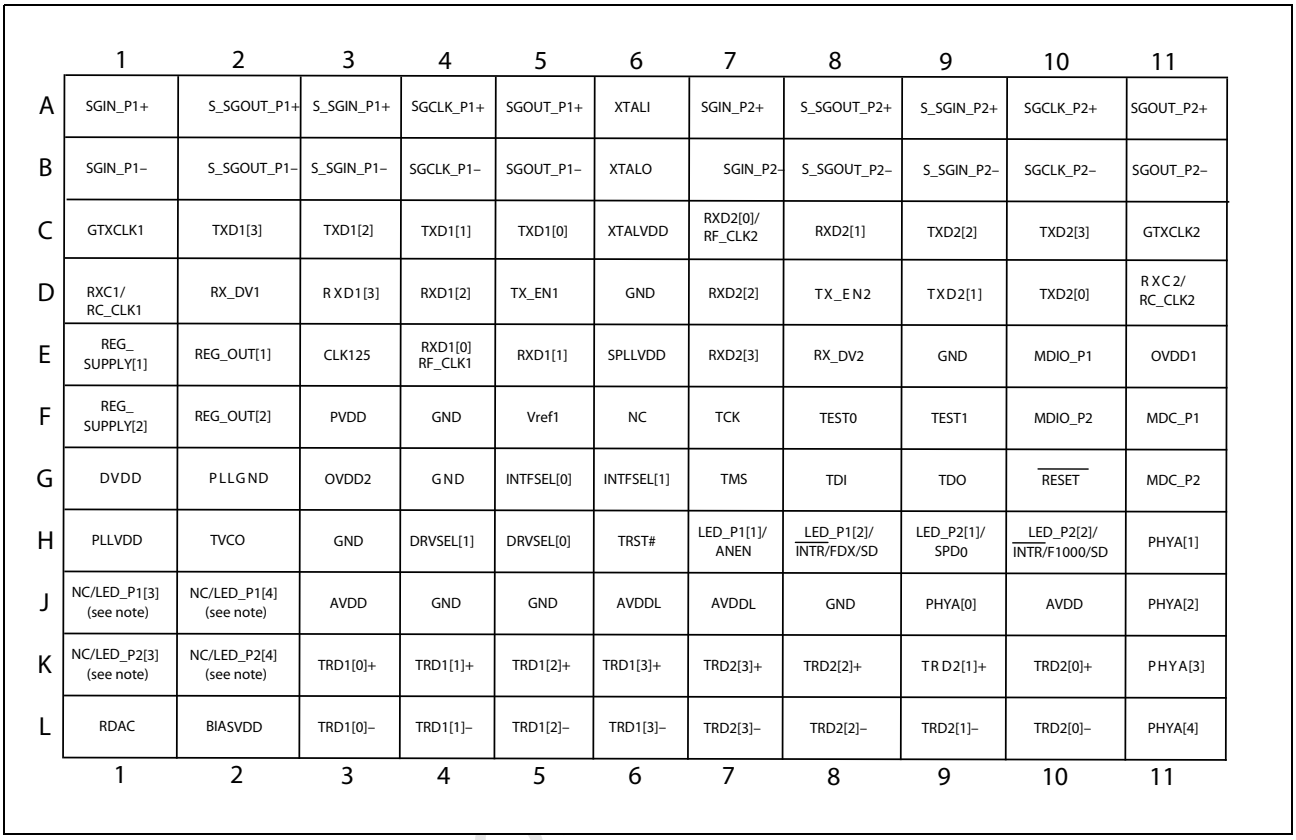
Table 3: Hardware Signal Descriptions (Cont.)

121-Pin BGA	Label	I/O	Description
E2	REG_OUT[1]	A	**Regulator 1 Output.** Internal PMOS. 1.2V output
F2	REG_OUT[2]	A	**Regulator 2 Output.** Internal PMOS. 1.2V output
E1	REG_SUPPLY[1]	A	**Regulator 1 Supply.** 1.8V-2.5V input
F1	REG_SUPPLY[2]	A	**Regulator 2 Supply.** 1.8V-2.5V input
J3 J10	AVDD	PWR	**Analog High-Voltage VDD.** +2.5V
J6 J7	AVDDL	PWR	**Analog Low-Voltage VDD.** +1.2V
L2	BIASVDD	PWR	**Bias VDD.** +2.5V. Normally filtered with a low resistance ferrite bead such as a Murata® BLM11A601S or equivalent, as well as a 0.1-µF capacitor.
G1	DVDD	PWR	**Digital Core VDD.** +1.2V
E6	SPLLVDD	PWR	SerDes Phase Lock Loop VDD. 1.2V. Each pin filtered with a low resistance series ferrite bead and a 0.1-µF + 2.2-µF (ESR value < 0.5Ω) shunt capacitor to ground.
F4 G4 H3 D6 E9 J4 J5 J8	GND	GND	**GND.** 0.0V
F5	Vref1	PWR	**HSTL Reference Voltage.** HSTL input logic level reference. When in HSTL mode, connect this pin to 1/2 OVDD1. When in non-HSTL mode, connect to DVDD (1.2V).
E11	OVDD1	PWR	**MAC Interface VDD.** 2.5V CMOS, 1.8V HSTL, or 1.5V HSTL for RGMII interface pins.
G3	OVDD2	PWR	**Digital Interface VDD.** 3.3V or 2.5V for all other I/O pins (MDIO, MDC, ...).
F3	PVDD	PWR	**Digital I/O.** Pad low-voltage VDD, 2.5V.
H1	PLLVDD	PWR	**Phase Lock Loop VDD.** 1.2V. Each pin filtered with a low resistance series ferrite bead and 0.1 µF + 2.2 µF (ESR value < 0.5Ω) shunt capacitors to ground.
G2	PLLGND	GND	**GND.**
C6	XTALVDD	PWR	**Crystal VDD.** +2.5V

Table 3: Hardware Signal Descriptions (Cont.)

121-Pin BGA	*Label*	*I/O*	*Description*
F6, J1, J2, K1, K2	NC ***Note:*** J1, J2, K1, K2 are NC for all other packages except BCM5482SHXXXXXX	NC	**Do Not Connect.**

Section 3: Pinout Diagram



	1	2	3	4	5	6	7	8	9	10	11
A	SGIN_P1+	S_SGOUT_P1+	S_SGIN_P1+	SGCLK_P1+	SGOUT_P1+	XTALI	SGIN_P2+	S_SGOUT_P2+	S_SGIN_P2+	SGCLK_P2+	SGOUT_P2+
B	SGIN_P1–	S_SGOUT_P1–	S_SGIN_P1–	SGCLK_P1–	SGOUT_P1–	XTALO	SGIN_P2–	S_SGOUT_P2–	S_SGIN_P2–	SGCLK_P2–	SGOUT_P2–
C	GTXCLK1	TXD1[3]	TXD1[2]	TXD1[1]	TXD1[0]	XTALVDD	RXD2[0]/ RF_CLK2	RXD2[1]	TXD2[2]	TXD2[3]	GTXCLK2
D	RXC1/ RC_CLK1	RX_DV1	RXD1[3]	RXD1[2]	TX_EN1	GND	RXD2[2]	TX_EN2	TXD2[1]	TXD2[0]	RXC2/ RC_CLK2
E	REG_ SUPPLY[1]	REG_OUT[1]	CLK125	RXD1[0] RF_CLK1	RXD1[1]	SPLLVDD	RXD2[3]	RX_DV2	GND	MDIO_P1	OVDD1
F	REG_ SUPPLY[2]	REG_OUT[2]	PVDD	GND	Vref1	NC	TCK	TEST0	TEST1	MDIO_P2	MDC_P1
G	DVDD	PLLGND	OVDD2	GND	INTFSEL[0]	INTFSEL[1]	TMS	TDI	TDO	$\overline{\text{RESET}}$	MDC_P2
H	PLLVDD	TVCO	GND	DRVSEL[1]	DRVSEL[0]	TRST#	LED_P1[1]/ ANEN	LED_P1[2]/ $\overline{\text{INTR}}$/FDX/SD	LED_P2[1]/ SPD0	LED_P2[2]/ $\overline{\text{INTR}}$/F1000/SD	PHYA[1]
J	NC/LED_P1[3] (see note)	NC/LED_P1[4] (see note)	AVDD	GND	GND	AVDDL	AVDDL	GND	PHYA[0]	AVDD	PHYA[2]
K	NC/LED_P2[3] (see note)	NC/LED_P2[4] (see note)	TRD1[0]+	TRD1[1]+	TRD1[2]+	TRD1[3]+	TRD2[3]+	TRD2[2]+	TRD2[1]+	TRD2[0]+	PHYA[3]
L	RDAC	BIASVDD	TRD1[0]–	TRD1[1]–	TRD1[2]–	TRD1[3]–	TRD2[3]–	TRD2[2]–	TRD2[1]–	TRD2[0]–	PHYA[4]
	1	2	3	4	5	6	7	8	9	10	11

Figure 9: 121-Pin FBGA Pinout Diagram, Top View

Note: J1, J2, K1, and K2 pins are LED pins for the BCM5482SHXXXXXX package. For other packages, J1, J2, K1, and K2 are NC.

Section 4: Operational Description

Reset

The BCM5482S provides a hardware reset pin, $\overline{\text{RESET}}$, which resets all internal nodes to a known state. The reset pin must be asserted for at least 2.0 µs. Hardware reset should always be applied to the BCM5482S after power-up.

The BCM5482S also has a software reset capability. To enable the software reset, 1 must be written to bit 15 of the MII Control register (address 00h). This bit is self-clearing, meaning that a second write operation is not necessary to end the reset. There is no effect if 0 is written to this bit.

Mode pins that are labelled *sample on reset* (SOR) are latched during hardware reset. Similarly, software resets also latch new values for some SOR mode pins, except for those pins that contain LED functions. SOR mode pins that contain LED functions during normal operation retain the values latched during the previous hardware reset.

During reset, the MAC output pins are driven low. However, when the PHY address is set to 00h, the device is placed into isolate mode, and the MAC interface output pins are tristated during and after reset.

PHY Address

The BCM5482S allows a unique PHY address for MII management. The address is set through the logic value of the PHYA [4:0] pins latched during reset. The PHY checks each MII management read or write command on its MDIO pin and performs the operation only if the address in the command matches the latched PHY address stored in the device.

Setting the PHY address to 00h puts the device into isolate mode during and after reset. To return to normal operation, write 0 to bit 10 of the MII Control register (address 00h).

There are two MDIO interface pins for each PHY in the dual PHY transceiver. Each PHY transceiver can be accessed independently through its associated MDIO interface pins.

Note: The MDIO and MDC of each port can be connected to use a single serial interface to access both ports. The address of the second port in the BCM5482S is PHY address pin plus one.

Isolate Mode

Copper Mode

The BCM5482S can be isolated from the RGMII MAC interface by writing 1 to bit 10 of 1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h). When the transceiver is put into isolate mode, all RGMII MAC inputs are ignored, and all RGMII MAC outputs are tristated. While in isolate mode, the PHY still sends out link pulses or FLPs, depending on whether the PHY was configured for forced or auto-negotiation mode. A link is established if the link partner is forced or is advertising the same technologies. The MII management pins (MDC and MDIO), along with the MII registers, operate normally. When the PHY address is set to 00000 and the device is reset (hardware or software), the device is put into isolate mode. Alternatively, setting bit 10 of 1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h) puts the transceiver in isolate mode. In either case, clearing the same bit removes the device from isolate mode.

The BCM5482S can also be put into super isolate mode by writing to register 18h, shadow value 010, bit 5 = 1. Super isolate mode tristates the RGMII outputs, ignores the RGMII input signals, and disables the transmission of copper link pulses. This mode is useful when the BCM5482S needs to coexist with another PHY on the same adapter card, where only one PHY is active. Unlike the isolate mode, the super isolate mode is available only when the BCM5482S device is in the copper mode.

Fiber Mode

The RGMII SerDes interface can be isolated when the device is in fiber mode. Register 00h bit 10 of the 1000BASE-X register isolates the SerDes interface.

Standby Power-Down Mode

The BCM5482S can be placed into standby power-down mode using software commands. In this mode, all PHY functions, except the serial management interface and CLK125 output, are disabled. To enter standby power-down mode, set 1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h), bit 11 = 1.

There are 3 ways to exit this mode:

- Clear MII Control register (address 00h), bit 11 = 0.
- Set the software RESET bit 15, MII Control register (address 00h).
- Assert the hardware $\overline{\text{RESET}}$ pin.

A read or write to any MII register other than MII Control register (address 00h) while the device is in the standby power-down mode may cause unpredictable results. Upon exiting this mode, the BCM5482S remains in an internal reset state for 40 µs and then resumes normal operation. When clearing 1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h), bit 11 = 0, the internal reset state does not reset the writable MII management registers.

To save additional power, CLK125 output can be disabled by setting register 1Ch, shadow value 00101, bit 0 = 0. Also the DLL can be powered down by setting register 1Ch, shadow value 00101, bit 1 = 0. These writes should be performed before enabling the standby power-down mode. When the device is configured in fiber mode, the copper interface is automatically powered down, and vice versa. However, when the BCM5482S is placed in media converter mode or SGMII mode, both fiber and copper interfaces remain powered up.

Note: When auto-medium mode detection is enabled, power bit of register 00h bit 11 is controlled by the internal state machine to power down the interface when it is selected. A 1 should not be written to this bit.

Auto Power-Down Mode

The BCM5482S can be placed into auto power-down mode to reduce chip power when the signal from the copper link partner is not present. Auto power-down mode can be enabled in copper, fiber, SGMII, or media converter modes. Auto power-down mode works whether the device has copper auto-negotiation enabled or disabled. This mode is enabled by setting Auto Power-Down Register (Address 1Ch, Shadow Value 01010), bit 5 = 1. However, when the BCM5482S is in forced 10 or 100 mode, the 1000BASE-T/100BASE-TX/10BASE-T Misc Control Register (Address 18h, Shadow Value 111), bit 9 should be set to 1. When auto power-down mode is enabled, the BCM5482S automatically enters the low-power mode when energy on the line is lost, and it resumes normal operation when energy is detected. When the BCM5482S is in auto power-down mode, it "wakes up" after 2.7 sec. or 5.4 sec. (determined by bit 4 of Auto Power-Down Register (Address 1Ch, Shadow Value 01010)) and sends link pulses while monitoring for energy from the link partner. The BCM5482S enters normal operation and establishes a link if energy is detected, otherwise wake-up mode continues for a duration of 84 to 1260 ms. This is determined by the timer bits [3:0] of Auto Power-Down Register (Address 1Ch, Shadow Value 01010) before going back to low-power mode.

Additional power savings can be realized by disabling the DLL by writing to 1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 Register (Address 1Ch, Shadow Value 00101), bit 1 = 0. This automatically disables the DLL when energy is lost. The DLL is automatically enabled during wake-up or when energy is detected. Do not enable this mode if the CLK125 signal is used by a MAC that needs a continuously running clock source.

TXC and RXC outputs can be disabled during auto power down by setting the 1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 Register (Address 1Ch, Shadow Value 00101), bit 8 = 1.

CLK125 Clock Output

A 125-MHz output clock is generated by the BCM5482S device from a 5× PLL, using the 25-MHz clock at XTALI as a reference. The 125-MHz clock can drive ASIC and MAC clock inputs, saving the cost of a high-precision clock oscillator. The clock output remains active during and after hardware or software reset. It also remains active when the Power-down bit (bit 11) in 1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h) is set. In the KFB (100-FBGA) package, the CLK125 output is disabled by default.

There are two ways to disable the CLK125 output:

- Powering down the DLL as described in "Auto Power-Down Mode" on page lxx

- Setting 1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 Register (Address 1Ch, Shadow Value 00101), bit 0 = 0

- CLK125 is not enabled in SGMII mode.
- When INTFSEL[1;0] =10 after hard reset, the CLK125 is disabled. To have CLK125 enabled for SGMII mode, set the INTFSEL[1:0] =00 during hard reset and change the configuration mode by writing to register 1C, shadow 1F bit [2:1]=10

Ultra-Low Power-Down Mode

The BCM5482S can be placed into the ultra-low power-down mode (IDDQ), consuming the lowest power possible while voltage is being supplied to the device. This mode is especially useful for saving battery life in laptop designs when the user does not require a network connection.

- To enter ultra-low power-down mode:
  - Write to register 1Ch, shadow value 01100, bit 6 = 1
- To exit ultra low-power mode:
  - Force the $\overline{\text{RESET}}$ pin low. See Table 118 on page ccxxxviii for reset timing information.
  - Write to register 1Ch, shadow value 01100, bit 6 = 0.

To achieve the lowest power consumption when using the internal regulators, the regulator source voltage needs to be set to 1.8V, not 2.5V.

Reset Requirements

At least one hardware reset is required before entering IDDQ mode to ensure that the BCM5482S is properly configured before going into IDDQ mode.

Note: After exiting IDDQ mode, normal operation can be resumed following either a hardware or software reset. The software reset can be used only if a hardware reset has been done at least once since power was applied to the BCM5482S.

Energy Detect Function

The BCM5482S can be programmed to output the result of the energy-detect logic through an LED pin. See Table 58 on page cliii and Table 59 on page clv. When copper auto-negotiation is enabled, on-chip detection circuitry constantly monitors two cable pairs—pair A (RJ-45 pins 1 and 2) and pair B (RJ-45 pins 3 and 6)—for energy on the copper interface, including 10BASE-T data, 100BASE-TX data, 1000BASE-T data, 10BASE-T link pulses, and auto-negotiation link pulses. If auto-negotiation is disabled in 10BASE-T or 100BASE-TX, then on-chip detection circuitry constantly monitors the receive pair for energy based on the current MDI state.

Internal Loopback Mode

RGMII to Copper Configuration

The internal loopback mode allows in-circuit testing of the BCM5482S device. All packets sent through the RGMII TXD pins are looped back internally to the RGMII RXD pins. The transmitter outputs TRD± are set to high impedance, and incoming packets on the cable are ignored. Loopback mode can be entered by writing 1 to bit 14 of Table 20: “1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h),” on page xcvi. To resume normal operation, bit 14 of the MII Control register must be 0.

SGMII to Copper Configuration

The internal loopback mode allows in-circuit testing of the BCM5482S device. All packets sent through the SGMII SGIN_Px± pins are looped-back internally to the SGOUT_Px± pins. The transmitter outputs, TRD±, are set to high impedance, and incoming packets on the cable are ignored. Loopback mode can be entered by writing 1 to bit 14 of 1000BASE-X MII Control Register (Address 00h). To resume normal operation, bit 14 of the MII Control register must be 0.

RGMII to 1000BASE-X Configuration

During fiber mode, internal loopback behaves very similarly to that in copper mode, allowing in-circuit testing of the BCM5482S device. All packets sent through the RGMII TXD pins are looped back internally to the RGMII RXD pins. Incoming packets on the cable are ignored. Loopback mode can be entered by writing 1 to bit 14 of 1000BASE-X MII Control Register (Address 00h). To resume normal operation, bit 14 of the MII Control register must be 0.

SGMII to 1000BASE-X or SGMII-to-100BASE-FX Configuration

The internal loopback mode allows in-circuit testing of the BCM5482S device. All packets sent through the SGMII SGIN_Px± pins are looped back internally to the SGOUT_Px± pins. The incoming packets on the cable are ignored. Loopback mode can be entered by writing 1 to bit 14 of 1000BASE-X Control Register (Address 00h) of the secondary SerDes. To resume normal operation, bit 14 of the 1000BASE-X Control Register (Address 00h) must be 0.

Note: When the device is configured to SGMII (master)-to-SGMII (slave), the SGMII (slave) bit 1 in the SGMII Slave Register (Address 15h) should be set to 0; otherwise, the speed at which the BCM5482S should operate is not determined.

Lineside (Remote) Loopback Mode

RGMII-to-Copper or SGMII-to-Copper Configuration

Lineside loopback mode allows the testing of the copper MDI interface from the link partner. This mode is enabled by setting bit 15 of 1000BASE-T/100BASE-TX/10BASE-T Misc Test Register (Address 18h, Shadow Value 100). The MDI receive packet is passed through the PCS and sent back out as the MDI transmit packet. The PCS receive data appears on the MAC interface. The MAC interface can be tristated by setting bit 11 of 1000BASE-T/100BASE-TX/10BASE-T Misc Test Register (Address 18h, Shadow Value 100).

SGMII-to-1000BASE-X Configuration

SerDes lineside loopback mode allows the testing of the SerDes interface from the link partner. The S_SGIN_Px± receive packet is passed through the PCS and sent back out as the S_SGOUT_Px± transmit packet.

Write Primary SerDes register (1000-X) 00h bit 14 to 1.

RGMII-to-100BASE-FX or RGMII-to-1000Base-X Configuration

Set Register 18 Shadow 4 bit 15 to 1.

SGMII-to-100BASE-FX Configuration

Set Secondary SerDes register 44 bit 2 to 1.

SGMII/Media Converter Mode

Copper lineside loopback mode allows the testing of the copper MDI interface from the link partner. The MDI receive packet is passed through the PCS and sent back out as the MDI transmit packet. This mode can be enabled by the following register write sequence:

1. Register 1Ch, Shadow 11111, bit 0 = 1
2. Register 00h, bit 14 = 1

The SerDes lineside loopback mode allows the testing of the SerDes interface from the MAC/switch. The SGIN_Px± receive packet is passed through the PCS and sent back out as the SGOUT_Px± transmit packet. This mode can be enabled by the following register write sequence:

1. Register 1Ch, Shadow 11111, bit 0 = 0
2. For SGMII 10BASE-T: Register 00h 4100h
   For SGMII 100BASE-T: Register 00h 6100h
   For SGMII 1000BASE-T: Register 00h 4140h
   For Media Converter: Register 00h 4140h

External Loopback Mode

The external loopback mode allows in-circuit testing of the BCM5482S as well as the transmit path through the magnetics and the RJ-45 connector. External Loopback can be performed with a jumper block and without a jumper block. External loopback using a jumper block tests the path through the magnetics and RJ45 connector. External loopback without the jumper block, only tests the BCM5482S's transmit and receive circuitry. In 1000BASE-T, 100BASE-TX, and 10BASE-T modes, a jumper block must be inserted into the RJ-45 connector to support external loopback. The jumper block should have the following RJ-45 pins connected together:

1----------3
2----------6
4----------7
5----------8

The following six tables (Table 4 through Table 9 on page lxxv) describe how the external loopback is enabled for
1000BASE-T, 100BASE-TX, and 10BASE-T modes with and without a jumper block.

Table 4: 1000BASE-T External Loopback With External Loopback Plug

Register Writes	*Comments*
Write 1800h to register 09h	Enable 1000BASE-T master mode
Write 0040h to register 00h	Enable force 1000BASE-T
Write 8400h to register 18h	Enable external loopback mode with external loopback plug

Table 5: 1000BASE-T External Loopback Without External Loopback Plug

Register Writes	*Comments*
Write 1800h to register 09h	Enable 1000BASE-T master mode
Write 0040h to register 00h	Enable force 1000BASE-T
Write 8400h to register 18h	Enable external loopback mode
Write 0014h to register 18h	Enable external loopback mode without external loopback plug

Table 6: 100BASE-TX External Loopback With External Loopback Plug

Register Writes	*Comments*
Write 2100h to register 00h	Enable force 100BASE-TX full-duplex mode
Write 8400h to register 18h	Enable external loopback mode with external loopback plug

Table 7: 100BASE-TX External Loopback Without External Loopback Plug

Register Writes	*Comment*
Write 2100h to register 00h	Enable force 100BASE-TX full-duplex mode
Write 8400h to register 18h	Enable external loopback mode
Write 0014h to register 18h	Enable external loopback mode without external loopback plug

Table 8: 10BASE-TX External Loopback With External Loopback Plug

Register Writes	*Comments*
Write 0100h to register 00h	Enable force 10BASE-T full-duplex mode
Write 8400h to register 18h	Enable external loopback mode with external loopback plug

Table 9: 10BASE-T External Loopback Without External Loopback Plug

Register Writes	*Comments*
Write 0100h to register 00h	Enable force 10BASE-T full-duplex mode
Write 8400h to register 18h	Enable external loopback mode
Write 0014h to register 18h	Enable external loopback mode without external loopback plug

Note: To exit the external loopback mode, Broadcom recommends a software or hardware reset.

Full-Duplex Operation

The BCM5482S supports full-duplex operation. While in full-duplex mode, a transceiver can simultaneously transmit and receive packets on the cable.

Copper Mode

When auto-negotiation is disabled, full-duplex operation can be enabled by setting bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h). The default value is controlled by the FDX pin at reset.

When auto-negotiation is enabled, the full-duplex capability is advertised for:

- 10BASE-TX when bit 6 in 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement Register (Address 04h) is set.
- 100BASE-TX when bit 8 in 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement Register (Address 04h) is set.
- 1000BASE-T when bit 9 in 1000BASE-T Control Register (Address 09h) is set.

The default value of all three advertisement bits is controlled by the SLAVE/ANEN, FDX, F1000, and SPD0 pins, but the bits can be overwritten at any time after reset.

Fiber Mode

When auto-negotiation is disabled, full-duplex operation can be enabled by setting bit 8 of 1000BASE-X MII Control Register (Address 00h). The default value is controlled by the FDX pin at reset.

When auto-negotiation is enabled, full-duplex capability is advertised for 1000BASE-X when bit 5 in the 1000-X Auto-negotiation Advertisement register (Address 04h) is set. The default value is controlled by the FDX pin, but the bit can be overwritten at any time after reset.

Ethernet@Wirespeed™

Ethernet@Wirespeed mode controls auto-negotiation advertising. If 1000BASE-T, 100BASE-TX, and 10BASE-T are advertised per registers 04h and 09h, and the link partner advertises the same capabilities at start up, an attempt is made to establish a 1000BASE-T link is made. If a 1000-BASE-T link is not established within five attempts, 1000BASE-T capability is masked and the next highest advertised capability (100BASE-TX) is advertised. If a link is not established within five attempts with 100BASE-TX being advertised, 100BASE-TX is masked and the next highest advertised capability (10BASE-T) is advertised. If a link is not established in 10BASE-T, all advertising capabilities are enabled (1000BASE-T, 100BASE-TX, and 10BASE-T) and the entire process begins again. Ethernet@Wirespeed mode is disabled after power-up or reset on both ports.

Note: The number of failed link attempts before downgrading to a lower speed is programmable. The number can be programmed anywhere from one to nine failed link attempts before downgrading to a lower speed. The default value is five link attempts. See "Changing the Number of Failed Link Attempts Before Ethernet@Wirespeed Downgrade" on page lxxvii for more details.

Software Enable

Ethernet@Wirespeed mode is disabled after power-up or reset on both ports. To enable Ethernet@Wirespeed mode, write to register 18h, shadow value 111, bit 4 = 1 for each port.

Changing the Number of Failed Link Attempts Before Ethernet@Wirespeed Downgrade

The number of failed link attempts before downgrading to a lower speed can be programmed by writing to register 1Ch, shadow value 00100, bits[4:2]. The number of attempts can be programmed from one to nine attempts as shown in Table 10.

Table 10: Changing the Number of Failed Link Attempts Before Downgrade

Register 1Ch, Shadow Value 00100		
Bit 8	***Bits[4:2]***	***Description***
1	XXX	Number of failed link attempts before Ethernet@Wirespeed downgrade = 1
0	000	Number of failed link attempts before Ethernet@Wirespeed downgrade = 2
0	001	Number of failed link attempts before Ethernet@Wirespeed downgrade = 3
0	010	Number of failed link attempts before Ethernet@Wirespeed downgrade = 4
0	011	Number of failed link attempts before Ethernet@Wirespeed downgrade = 5 (default value)
0	100	Number of failed link attempts before Ethernet@Wirespeed downgrade = 6
0	101	Number of failed link attempts before Ethernet@Wirespeed downgrade = 7
0	110	Number of failed link attempts before Ethernet@Wirespeed downgrade = 8
0	111	Number of failed link attempts before Ethernet@Wirespeed downgrade = 9

Monitoring Ethernet@Wirespeed

The status of the Ethernet@Wirespeed downgrade can be monitored through the following registers and LEDs:

- Ethernet@Wirespeed Downgrade Status (register 11h, bit 14)
- Ethernet@Wirespeed Downgrade ([register 1Dh, bit 15 = 1], bit 12)
- Ethernet@Wirespeed Disable Gigabit Advertising ([register 1Dh, bit 15 = 1], bit 14)
- Ethernet@Wirespeed Disable 100BASE-TX Advertising ([register 1Dh, bit 15 = 1], bit 13)
- HCD Status ([register 1Dh, bit 15 = 1], bits[11:0])
- Auto-negotiation HCD and Current Status (register 19h, bits[10:8])
- Ethernet@Wirespeed Downgrade LED and LED1 (register 1Ch, shadow value 01101, bits[3:0] = 1001
- Ethernet@Wirespeed Downgrade LED and LED2 (register 1Ch, shadow value 01110, bits[7:4] = 1001

Master/Slave Configuration

In 1000BASE-T mode, the BCM5482S and its link partner perform loop timing. One end of the link must be configured as the timing master and the other end as the slave, as defined by IEEE 802.3ab. Master/slave configuration is performed by the auto-negotiation function. The auto-negotiation function first looks at the manual master/slave configuration bits advertised by the local PHY and the link partner. If neither PHY requests manual configuration, then the auto-negotiation function looks at the advertised repeater/DTE settings. If one PHY is advertised as a repeater port and the other is advertised as a DTE port, then the repeater port is configured as the master and the DTE port as the slave. However, if both partners are configured with identical repeater/DTE settings, each generates an 11-bit random seed. The partner with the higher seed is configured as the master. If the local PHY and the link partner happen to generate the same random seed, auto-negotiation is restarted.

If both ends of the link attempt to force the same manual configuration (both master or both slave), or the random seeds match seven consecutive times, the BCM5482S sets the Master/Slave Configuration Fault bit in the 1000BASE-T Status register and auto-negotiation is restarted. To set the manual master/slave and advertised repeater/DTE configurations, see Table 28: “1000BASE-T Control Register (Address 09h),” on page cx.

Next Page Exchange

The 1000BASE-T configuration requires the exchange of three auto-negotiation Next Pages between the BCM5482S and its link partner. Exchange of 1000BASE-T Next Page information takes place automatically when the BCM5482S is configured to advertise 1000BASE-T capability.

The BCM5482S also supports software controlled Next Page exchanges. When 1 is written to bit 15 of 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement Register (Address 04h), all Next Page transactions are controlled through the MII management interface. This includes the three 1000BASE-T Next Pages, which are always sent first. The BCM5482S automatically generates the appropriate message code field for the 1000BASE-T pages. When the BCM5482S is not configured to advertise 1000BASE-T capability, the 1000BASE-T Next Pages are not sent.

When the BCM5482S is not configured to advertise 1000BASE-T capability and bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement Register (Address 04h) is 0, the BCM5482S does not advertise Next Page ability.

100BASE-FX

The BCM5482S transceiver supports the external 100BASE-FX optical module through its SGOUT_Px± or S_SGOUT_Px± interface pins. Follow these steps to enable 100BASE-FX mode:

RGMII-100BASE-FX:

1. Place the device into the RGMII-fiber mode by strapping INTFSEL [1:0] = 01.
2. Write MII reg00h, bit 14 = 1 (set loopback).
3. Write register 1C shadow 13h, bit 0 = 1 (select 100FX mode).
4. Write Expansion reg50h = 0C3Bh (power-down SerDes RX path).
5. Write Expansion reg50h = 0C3Ah (power-up/reset SerDes RX path).
6. Write MII reg00h, bit 14 = 0 (reset loopback to switch clock back to SerDes RX clock).

The following step switches the BCM5482S back from 100BASE-FX mode to 1000BASE-X mode.

1. Set register 1C, shadow 10011, bit 0 = 0 to enable 1000BASE-X.
2. Write MII reg00h bit 15 = 1 (reset).

The external fiber-optic receiver detects the signal status and passes it into the BCM5482S for each port. The BCM5482S uses this signal to auto-detect between the copper and fiber interfaces.

SGMII-100BASE-FX:

1. Place the device into the SGMII-fiber mode by strapping INTFSEL [1:0] = 10.
2. Set register 1C, shadow 10100, bit 0 = 1 to enable Secondary SerDes 1000BASE-X.
3. Set register 1C, shadow 10100, bit 4 = 1 to change Secondary SerDes speed to 100BASE-FX.
4. Write Secondary SerDes register 00h, bit 15 = 1 (reset secondary SerDes)
5. Write Secondary SerDes register 00h, bit 11 = 0 (power-up the secondary SerDes)
6. Set register 1C, shadow 10100, bit [2:1] = 11 to select the signal detect and sync state to secondary SerDes for the auto-detect option.
7. Set register 1C, shadow 01101, bit 0 to 1 to enable link indicator on the LED1 (LED_Px[1]).

The following steps switch the BCM5482S back from 100BASE-FX mode to 1000BASE-X mode.

1. 1. Set register 1C, shadow 10011, bit 4 = 0 (to change Secondary SerDes spec to 1000BASE-X).
2. Write Secondary SerDes register 00h, bit 15 = 1 (reset secondary SerDes)
3. Write Secondary SerDes register 00h, bit 11 = 0 (power-up the secondary SerDes)

The external fiber-optic receiver detects the signal status and passes it into the BCM5482S for each port. The BCM5482S uses this signal to auto-detect between the copper and fiber interfaces.

RGMII Interface

The BCM5482S can communicate with Ethernet MACs through a reduced-pin-count Gigabit MII known as RGMII. This interface reduces the number of MAC signal pins by half with respect to GMII. Transmit and receive data are transferred on both edges of the GTXCLK and RXC clocks, respectively.

The GTXCLK and RXC clock rates are:

- 125 MHz for 1000-Mbps data
- 25 MHz for 100-Mbps data
- 2.5 MHz for 10-Mbps data

Data is sent with the least significant nibble first. The RGMII mode can be enabled by hardware or software. See Table 2: “Hardware Mode Selection INTFSEL[1:0],” on page xli and Table 1: “Hardware Driver Selection DRVSEL[1:0],” on page xli for an explanation of hardware-enabled settings. To enable by software, write register 18h, shadow 111, bit 7 = 1.

While in RGMII mode, the RGMII receive timing (RXD to RXC skew) is delayed by approximately 1.9 ns. When register 18h shadow value is 111 bit 8 = 0, the RXD is not delayed with respect to RXC.

The RGMII transmit timing can be adjusted, if needed, by software control. The TXD-to-GTXCLK delay time can be increased by approximately 1.9 ns by setting bit 9 of register 1Ch, shadow value 00011.

The default timing delay can eliminate the need for board delay traces required by the RGMII specification.

Table 11: RGMII Transmit Data

RGMII Signal	*Signal Latched at GTXCLK Rising Edge*	*Signal Latched at GTXCLK Falling Edge*
TX_EN	TX_EN	TX_EN (XOR) TX_ER
TXD[3]	TXD[3]	TXD[7]
TXD[2]	TXD[2]	TXD[6]
TXD[1]	TXD[1]	TXD[5]
TXD[0]	TXD[0]	TXD[4]

Table 12: RGMII Receive Data

RGMII Signal	*Signal Latched at RXC Rising Edge*	*Signal Latched at RXC Falling Edge*
RX_DV	RX_DV	RX_DV (XOR) RX_ER
RXD[3]	RXD[3]	RXD[7]
RXD[2]	RXD[2]	RXD[6]
RXD[1]	RXD[1]	RXD[5]
RXD[0]	RXD[0]	RXD[4]

RGMII-to-SGMII Slave Mode

The BCM5482S offers an interface converter mode that supports RGMII-to-SGMII slave data conversion. To enable this function, set register 1Ch, shadow 10101, bit 1, to 1. This RGMII-to-SMGII slave mode can auto-detect between 1000X and SGMII slave modes based on the SerDes received auto-negotiation code word.

To enable the auto-detect between 1000X and SGMII slave modes, set register 1Ch, shadow 10101, bit 0, to 1.

SGMII Interface

The SGMII interface uses 2 data signals and 1 clock signal to convey frame data and link rate information between the BCM5482S transceiver and an Ethernet MAC. The data signals operate at 1.25 Gbaud, and the clock signals operate as a 625-MHz double data rate (DDR) interface. Each of these signals is realized as a differential pair because of the speed of operation, providing signal integrity while minimizing system noise. The SGMII signals use LVDS voltage levels. Both the data and clock signals are DC-balanced; therefore, implementations that meet the AC parameters, but fail to meet the DC voltage requirements, can be AC-coupled.

The 1.25-Gbaud transfer rate of the SGMII is greater than required for the BCM5482S transceiver operating at 100 Mbps or 10 Mbps. When these situations occur, the BCM5482S elongates the frame by replicating each frame byte: 10 times for 100 Mbps and 100 times for 10 Mbps. This frame elongation takes place above the 802.3z PCS layer, making the start frame delimiter appear only once per frame.

At the receive side, the BCM5482S transceiver passes the signals from the copper interface through the BCM5482S PCS layer. The BCM5482S serializes the PCS data to create a SGOUT_Px± signal pair and sends it to the MAC at 1.25 Gbps along with the 625-MHz DDR SCLK± signal pair.

At the transmit side, the BCM5482S deserializes the SGIN_Px± pin to recover encoded parallel data. The BCM5482S passes parallel data through a SerDes PCS state machine to determine the appropriate transmit signals. The decoded transmit signals are passed through the transmit block and are output to the BCM5482S copper port at the predetermined speed.

Control Information Exchange Between Links

The BCM5482S passes control information to the MAC to notify of the change of the copper link status. The SGMII interface uses the auto-negotiation block to pass control information. If the BCM5482S detects a copper link change, it restarts its SGMII auto-negotiation process, sending out the updated control information. The receive block in the MAC receives and decodes control information and transmits an acknowledgement of the link status change back to the BCM5482S also using the auto-negotiation mechanism. Upon receiving the acknowledgement from the MAC, the BCM5482S finishes the auto-negotiation process and returns to the normal data mode. Table 13 summarizes the SGMII interface pins.

Table 13: SGMII Interface Pins

SGMII Signal Pin	*Description*
SGIN_Px±	SGMII differential data input pin with internal 100Ω termination
SGOUT_Px±	SGMII differential data output pin
SCLK±	SGMII differential clock output pin[a]

a. An additional 25 mW of power per port can be saved by turning off the SCLK± output; It is performed by the following register write: Write to Expansion register 52h, bit 2 = 1. This register write is on a per-port basis and must be performed after any hardware or software reset.

SGMII-to-SGMII Slave Mode

The BCM5482S offers an interface converter mode that supports SGMII-to-SGMII slave data conversion. Each one of the PHY ports has a secondary SerDes that is used to perform conversion.

To enable this function:

1. Configure the BCM5482S to SGMII mode by strapping INT_SEL[1:0] pins to 10, or write to register 1Ch, shadow 1F, bit [2:1] = 10.
2. Set bit 0 of the Secondary SerDes Control Register (Address 1Ch, Shadow Value 10100) to 1 to enable the secondary SerDes.
3. Set bit 1 of the SGMII Slave Register (Address 15h) to configure the second SerDes-to-SGMII (slave) mode.
4. Write a 0 to bit 11 of the 1000BASE-X Control Register (Address 00h) to disable the power-down of the Secondary SerDes.

This SGMII-to-SGMII slave mode can auto-detect between 100BASE-FX, 1000BASE-X, and SMGII slave modes based on the SerDes-received auto-negotiation code word.

Note: The SGMII slave requires the device to configure for 1000BASE-X first before enabling the SGMII salve through register 1Ch, shadow 15h, bit 0.

SerDes Interface

The SerDes interface shares the same differential data pins as the SGMII interface, except that SCLK± is disabled. The SerDes auto-negotiation is similar to the SGMII except for the link timer and the base page code word. Table 14 summarizes the auto-negotiation differences between the two interfaces.

Table 14: SGMII and SerDes Auto-negotiation

	Link Timer	*Remote Fault*	*PAUSE Frame*	*Speed Bit*	*Link Status*	*Duplex Bit*
SGMII	1.6 ms	Not supported	Not supported	Supported	Supported	Supported
SerDes	10 ms	Supported	Supported	Not supported (always 1000BASE-X)	Not supported	Supported

Media Converter Mode

The BCM5482S offers a media converter mode that supports SerDes-to-copper data conversion. In this mode, the RGMII interfaces are not used. The SerDes interface can connect to a SerDes compatible device or to a fiber module. The copper interface must be limited to 1000BASE-T mode. The MAC/switch controller that is connected to the SerDes should be capable of both half-duplex and full-duplex operation. For more information on media converter auto-negotiation, see "Auto-negotiation" on page li. Also, refer to the BCM5482S Design Guide for additional information.

Copper/Fiber Mode Auto-Detection

This feature allows a RGMII MAC to automatically detect and process data from either the copper interface or the fiber interface. In fiber mode, the PHY uses the external fiber signal detect from the fiber module along with the synchronization state machine to determine a valid connection. In copper mode, the PHY uses the copper energy detect for determining a valid connection. Based on the priority and default settings (register 1Ch, shadow 11110, bits[2:1]), the PHY will select the mode of operation. The priority setting is used to select the mode of operation when both the copper and fiber media have active link partners. Certain on-chip functional blocks for the mode of operation that is not selected will be powered down. The polarity of the external fiber signal detect input can be inverted (active low) by writing register 1Ch, shadow 11110, bit 8 = 1.

The copper/fiber mode auto-detection feature can be enabled by writing register 1Ch, shadow 11110, bit 0 = 1.

The current mode of operation can be determined by reading register 1Ch, shadow 11111, bits[2:1]. The link status can be determined by reading register 1Ch, shadow 11111, bit 6 for fiber, bit 7 for copper. The copper energy detect can be determined by reading register 1Ch, shadow 11111, bit 5, and fiber signal detect on bit 4.

SGMII/Media Converter Mode Auto-Detection

This feature enables the PHY to change its mode of operation (SGMII/media converter) to match the SerDes link partner. The auto-negotiation base-page code word, bit 0, is used to determine the SerDes link partner mode of operation. If a mismatch is detected, the PHY mode of operation is changed based on a LFSR, and SerDes auto-negotiation is restarted.

The SGMII/media converter mode auto-detection feature can be enabled by hardware-strapping pin INTF_SEL[1:0] = 11 or by writing register 1Ch, shadow 11000, bit 0 = 1. Once the link is up, the mode of operation can be determined by reading register 1Ch, shadow 11111, bits[2:1].

Voltage Regulators

Two voltage regulators are provided to ease power supply requirements for designs lacking a 1.2V source. The regulator source pins, REGSUP[2:1], can be supplied with 1.8V to 2.5V. The output pins, REGSEN[2:1], are brought out to allow filtering and power distribution. These two regulator outputs must not be tied to the same power plane.

Dual-Input Configuration/LED Output Function

Several output LED pins have a secondary input function. Each of these pins serve as an input pin during the power-on/reset sequence. The logic level of the pin is sampled at reset and configures the secondary function. After the reset process is completed, the pin acts as an output LED during normal operation. The polarity of the output LED is determined based on the latched input value at reset. For example, if the value at the pin is high during reset, the LED output during normal operation is active low. The user must first decide, based on the individual application, the values of each of the input configuration pins shown in Table 15 on page lxxxiv to provide the correct device configuration. The LED circuit must then be configured to accommodate either an active-low or active-high LED output (see Figure 10 on page lxxxv).

The $\overline{\text{QUALITY}}$ pin has a secondary function by setting the RGMII timing mode as described in "RGMII Interface" on page lxxx, and it can also change polarity. If this pin is pulled low during reset when the RGMIIEN pin is pulled high, the output is active high. Under conditions when the $\overline{\text{QUALITY}}$ pin is connected to the power supply through an LED, the pin is pulled high at reset, and the pin is configured to active low. For more details, see "RGMII Interface" on page lxxx. Refer to the BCM5482S Design Guide for further information. The LED output is active high if the pin was strapped low during reset. Conversely, the output is active low if the pin was strapped high during reset.

Table 15: Dual Input Configuration/LED Output LEDs

LED Output (Normal Operation)	*Input Configuration Pin (Latched During Reset)*
$\overline{\text{LED\_P1[1]}}$	ANEN
$\overline{\text{LED\_P1[2]}}$	FDX
$\overline{\text{LED\_P2[1]}}$	SPD0
$\overline{\text{LED\_P2[2]}}$	F1000

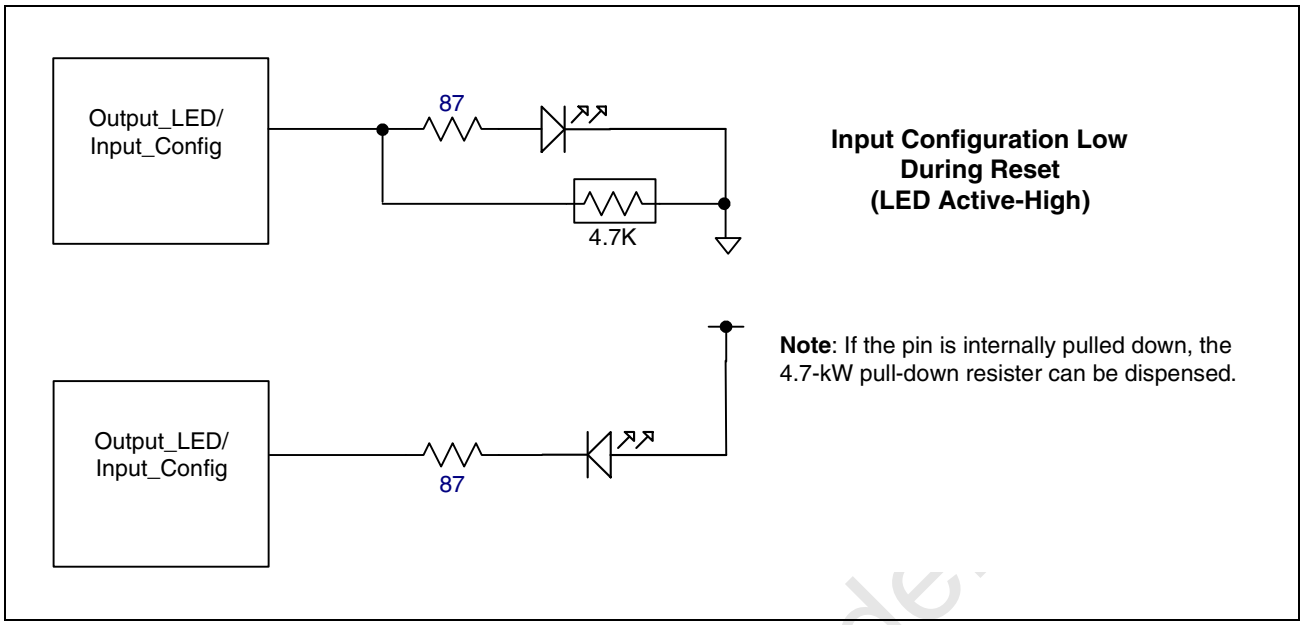


Figure 10: LED Circuit for Dual Input Configuration/LED Output Pins

General-Purpose LED Programmability

The BCM5482S has four LED pins for each port. LED_P1[1], LED_P1[2], LED_P1[3], and LED_P1[4] are for port 1 while LED_P2[1], LED_P2[2], LED_P2[3], and LEDP2[4] are for port 2. These LED pins can be program to many useful LED functions. Because any of these LEDs can be programmed by any of the LED functions, they are referred to in this document as LED1 through LED4. For each port, four 4-bit control register words are provided to allow the user to select the LED function for each of the pins. These control words are located in register 1Ch, shadow value 01101 and shadow value 01110. Table 16 on page lxxxv details each of the four programmable LEDs, their corresponding register bits, and default settings.

Table 16: Programmable LEDs

121-Pin FBGA	*Pin Name*	*Register Bits*	*Register Address*	*Default Value*	*Default Function*
			Port (PHY) 1		
H7	LED_P1[1]	LED_P1[1]/ANEN/$\overline{\text{INTR}}$	1Ch Shadow 01101 (0Dh) [3:0]	0000	LINKSPD[1]
H8	LED_P1[2]	LED_P1[2]/$\overline{\text{INTR}}$/FDX/SD	1Ch Shadow 01110 (0Eh) [7:4]	0110	INTR
J1	LED_P1[3]	LED_P1[3]	1Ch Shadow 01101 (0Dh) [7:4]	0001	LINKSPD[2]
J2	LED_P1[4]	LED_P1[4]	1Ch Shadow 01110 (0Eh) [3:0]	0011	ACTIVITY
			Port (PHY) 2		
H9	LED_P2[1]	LED_P2[1]/SPD0/$\overline{\text{INTR}}$	1Ch Shadow 01101 (0Dh) [3:0]	0000	LINKSPD[1]
H10	LED_P2[2]	LED_P2[2]/$\overline{\text{INTR}}$/F1000/SD	1Ch Shadow 01110 (0Eh) [7:4]	0110	INTR

Table 16: Programmable LEDs

121-Pin FBGA	Pin Name	Register Bits	Register Address	Default Value	Default Function
K1	LED_P2[3]	LED_P2[3]	1Ch Shadow 01101 (0Dh) [7:4]	0001	LINKSPD[2]
K2	LED_P2[4]	LED_P2[4]	1Ch Shadow 01110 (0Eh) [3:0]	0011	ACTIVITY

Each output function exists as an internal device signal that is multiplexed to a given general-purpose LED pin when the corresponding register bits are written with the appropriate register value. Figure 11 is a graphical representation of the multiplexer functionality of the programmable LED and uses LED1 as an example.

Note: Secondary SerDes Interrupt is only supported on this LED1 (H7 and H9) and on no other LED pins. Version A2 supports Secondary SerDes Interrupt.

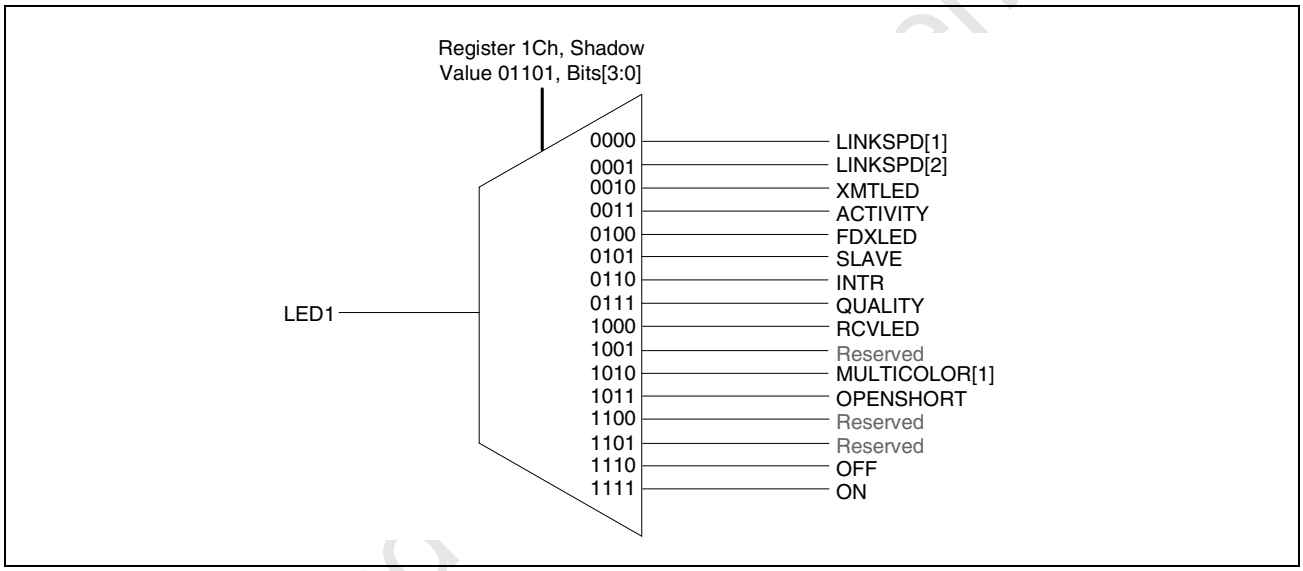


Figure 11: Programmable LED Multiplexer

Interrupt Function

The BCM5482S can be programmed to provide an interrupt output based on changes in the PHY status. Each individual interrupt condition is represented by a read-only bit in the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status Register (Address 1Ah), the Expansion Interrupt Status Register (Address 01h), and the Secondary SerDes Interrupt Status Register (Address 30h). Interrupts can be individually masked by setting or clearing bits in the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask Register (Address 1Bh), the Expansion Interrupt Mask Register (Address 02h), and the Secondary SerDes Interrupt MASK Register (Address 31h). When an unmasked interrupt condition occurs, the interrupt pin is driven active until the interrupt is cleared. Most interrupts are cleared automatically by reading the Interrupt Status register.

The interrupt function can be globally disabled by setting the interrupt disable bit, register 10h, bit 12.

The interrupt event from the copper or primary SerDes interface is programmable on any of the LEDx pins. The LED pin, which is programmed to the interrupt pin, is an open-drain pad driver for the copper and primary SerDes.

The following steps enable the Interrupt for the secondary SerDes:

1. Secondary SerDes register 10 bit 7 = 1 (enable Secondary SerDes interrupt function).
2. Write register 1C shadow 0Dh [3:0] = 1111 (disable primary SerDes and copper interrupt source).
3. Clear the desired interrupt mask bit in the Secondary SerDes mask register 31h.

LED Modes

Many additional LED functions and modes are supported by the BCM5482S. Table 17 on page lxxxviii describes many of these modes in detail.

The LEDs can be forced on by setting bit 4 of register 10h. This forces all LEDs on. Similarly, the LEDs can be forced off continuously by setting bit 3 of register 10h. This overrides all other LED modes except the force LEDs ON mode. The LED outputs are open drain when programmed to INTR, XMTLED, and ACTIVITYLED mode.

Table 17 on page lxxxviii describes the different modes in which each individual pin can be programmed. For each pin, the modes are listed in order of priority. For example, when the receive LED is programmed to one of the link-utilization modes, the register bit enabling activity/link LED mode is not relevant. The last mode listed for each pin is the default mode.

Multicolor LED

The MULTICOLOR mode uses two programmable LED output pins to control a single LED unit that is capable of producing 3 different colors: green, amber, and red. The multicolor LED mode is enabled by writing value B4AAh to 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 Register (Address 1Ch, Shadow Value 01101) and B8AAh to 11000BASE-T/100BASE-TX/10BASE-T LED Selector 2 Register (Address 1Ch, Shadow Value 01110). After this register write, the multicolor LED signals appear on LED1 and LED2. The subfunction and other parameters can be selected by setting control bits in the Multicolor LED Selector Register (Address 04h), the Multicolor LED Flash Rate Controls Register (Address 05h), and Multicolor LED Programmable Blink Controls Register (Address 06h).

Open/Short LED

The OPENSHORT LED is a function of the cable diagnostic mode. The OPENSHORT LED can be programmed to appear on any of the programmable LEDs by writing to the appropriate LED Selector register.

> ***Example:*** Write value B40Bh to 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 Register (Address 1Ch, Shadow Value 01101).

This LED turns on after the cable diagnostic function is completed and when an open or short is found on any of the four cable pairs attached to the PHY.

Energy Link LED

When one of the programmable LED outputs is programmed in the ENERGYLNK mode, the LED uses blinking and solid-on appearances to indicate energy detection and valid links. The ENERGYLNK LED is off when there is no link or energy detected. The LED blinks as soon as energy is detected on the wire. When the link is established, the LED remains continuously on for the duration. Shortly after a loss of energy is detected, the ENERGYLNK LED begins to blink and remains in this state for the length of the Disconnect Timer value, defined in register 1Ch, Shadow value 10000, bits [3:0]. After the timer expires, the LED is turned off. For additional information and control bits, see "Energy Detect Function" on page lxxi.

Media Converter Mode LED

When the BCM5482S is configured to SerDes-copper media converter mode (INTF_SEL[1:0] = 11), the LED functionality changes.

- LED1: Copper link, active-low signal when copper media is linked (RX_LOS, Active high)
- LED2: LINK, active-low, SerDes and Copper both linked
- LED3: RX activity, active-low, copper receive
- LED4: TX activity, active-low, copper transmit

Additional LED Modes

Some of the LEDs can also be programmed to additional modes. The different modes that each LED output can assume are described in Table 17. Because the modes are listed in the order of priority for each pin, the register bit enabling activity/link LED mode is not relevant when the receive LED is programmed to one of the link utilization modes. The last mode listed for each pin is the default mode. The table is valid for devices configured to copper, RGMII/copper, SerDes, RGMII/SerDes, and SGMII/copper modes only.

Table 17: LED Modes (Except in SerDes-Copper Media Converter Mode)

LEDs	*Description*
All LEDs (Except for INTR and OPENSHORT Modes)	Force LEDs: • On (register 10h, bit 4 = 1): LED is on solid. • Off (register 10h, bit 3 = 1): LED is off solid.
All LEDs	• General-purpose I/O input mode • General-purpose I/O output mode (default) Register address 1Ch, shadow value 01111, bits 3:0 = 0000. Each port can be individually programmed to input or output mode.
QUALITY LED	• Remote fault (register 1Ch, shadow value 01001, bit 2 = 1): LED is on when the Remote Fault bit (register 05h, bit 13) is set. The LED turns off if auto-negotiation is turned off, restarted, or if the Remote Fault bit is cleared. • Quality (default)

Table 17: LED Modes (Except in SerDes-Copper Media Converter Mode) (Cont.)

LEDs	*Description*
$\overline{\text{ACTIVITY}}$ LED	Link utilization. This mode provides the estimated activity in terms of blink rate. The blink rate of the LED increases as the activity duty cycle increases by 10% increments. For duty cycles of 0.001–10%, the LED blinks at 3 Hz, for duty cycles of 10–20%, the LED blinks at 6 Hz, and for duty cycles of 90–96%, the LED blinks at 30 Hz. Though the frequency of the LED blink increases, the duty cycle of the LED stays at about 50%. This LED mode is enabled to include all activity, transmit activity only, or receive activity only. • Transmit (register 1Ch, shadow value 01001, bits[1:0] = 01) • Receive (register 1Ch, shadow value 01001, bits[1:0] = 10) • Activity (register 1Ch, shadow value 01001, bits[1:0] = 11) Activity/link LED (register 1Ch, shadow value 01001, bits 4 = 1; register 10h, bit 5 = 0). LED is off when there is no link. The LED is on when there is a link. The LED blinks when the link is up and there is either transmit or receive activity. The LED blinks with a 167-ms cycle and a 50% duty cycle. Receive (register 1Ch, shadow value 01001, bit 3 = 0): This mode expresses receive activity in either of the two modes described below: • Traffic (register 10h, bit 5 = 1). LED is clocked at 5.2 ms cycles. The LED is on for the entire cycle if activity occurs. • Normal (register 10h, bit 5 = 0). LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if activity occurs. Activity (default). This mode expresses both transmit and receive activity in either of the two modes described below. • Traffic (register 10h, bit 5 = 1). LED is clocked at 5.2 ms cycles. The LED is on for the entire cycle if activity occurs. • Normal (register 10h, bit 5 = 0). LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if activity occurs.
$\overline{\text{XMTLED}}$ LED	• Traffic (register 10h, bit 5 = 1): LED is clocked at 5.2 ms cycles. The LED is on for entire cycle if TX activity occurs. • Normal (register 10h, bit 5 = 0): LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if TX activity occurs.
$\overline{\text{RCVLED}}$ LED	• Traffic (register 10h, bit 5 = 1): LED is clocked at 5.2 ms cycles. The LED is on for the entire cycle if TX activity occurs. • Normal (register 10h, bit 5 = 0): LED is clocked at 167 ms cycles. The LED blinks with a 50% duty cycle if TX activity occurs.
$\overline{\text{INTR}}$ LED (Open Drain)	• Force interrupt (register 10h, bit 11 = 1): LED is forced continuously on. • Disable interrupt (register 10h, bit 12 = 1): LED is forced continuously off. • Normal interrupt (default): LED is forced continuously on until interrupt is cleared.

Section 5: Register Summary

MII Management Interface Register Programming

The BCM5482S transceiver is designed to be fully compliant with Clause 22 of the IEEE 802.3u Ethernet specification. The MII management interface registers are written and read serially using the MDIO and MDC pins. A clock of up to 12.5 MHz must drive the MDC pin of the BCM5482S.

The BCM5482S has two unique PHY addresses for MII management:

- Port 1 is set through the PHYA[4:0] pins
- Port 2 is the PHY address pins + 1

Data transferred to and from the MDIO pin is synchronized with the MDC clock. Each MII read or write instruction contains the following:

- **Preamble (PRE).** To signal the beginning of an MII instruction after reset, at least 32 consecutive 1 bits must be written to the MDIO pin of the BCM5482S. A preamble of 32 1 bits is required only for the first read or write following reset. If bit 6 of MII register 01h is cleared, a preamble is always required. A preamble of fewer than 32 1 bits causes the remainder of the instruction to be ignored.
- **Start of Frame (ST).** A 01 pattern indicates the start of an instruction.
- **Operation Code (OP).** A read instruction is indicated by 10, while a write instruction is indicated by 01.
- **PHY Address (PHYAD)**. A 5-bit PHY address follows with the most significant bit (MSB) transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips.
- **Register Address (REGAD).** A 5-bit register address follows with the MSB transmitted first. The addresses for the registers used by the BCM5482S are shown in Table 19 on page xci.
- **Turnaround (TA).** The next bit times are used to avoid contention on the MDIO pin when a read operation is performed. When a write operation is being performed, 10 must be sent to the BCM5482S chip during these 2-bit times. When a read operation is being performed, the MDIO pin of the MAC must be put in high-impedance state during these bit times. The BCM5482S transceiver drives the MDIO pin to 0 during the second bit time.
- **Data.** The last 16 bits of the instruction are the actual data bits. During a write operation, these bits are written to the MDIO pin with the MSB transmitted first. During a read operation, the data bits are driven by the BCM5482S with the MSB transmitted first.

The complete management frame format is summarized in Table 18.

When writing to the MDIO pin, the bit value must be stable for 10 ns before the rising edge of the MDC and must be held valid for 10 ns after the rising edge of the MDC. When reading from the MDIO pin, the data bit is valid at the rising edge of the MDC until the next falling edge of the MDC.

Example: To put a PHY with address 00001 into loopback mode, issue the following write MII instruction:

```
1111 1111 1111 1111 1111 1111 1111 1111    0101 00001 00000 10 0100 0000 0000 0000
```

To determine if a PHY is in the link pass state, issue the following read MII instruction:

```
1111 1111 1111 1111 1111 1111 1111 1111    0110 00001 00001 ZZ ZZZZ ZZZZ ZZZZ ZZZZ
```

The BCM5482S drives the MDIO line during the last 17 bit times. If the link status is valid, the third bit from the end (bit 2) is 1.

Table 18: MII Management Frame Format

Operation	*PRE*	*ST*	*OP*	*PHYAD*	*REGAD*	*TA*	*Data*	*Direction*
Read	1 ... 1	01	10	AAAAA	RRRRR	ZZ Z0	Z ... Z D ... D	Driven to BCM5482S Driven by BCM5482S
Write	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Driven to BCM5482S

Register Map

The following table contains the set of registers for the BCM5482S transceiver.

Note: The primary SerDes registers are described in "Primary SerDes Registers (Enabled by Register 1Ch, Shadow Value 11111, Bit 0 = 1)" on page xciv.

Table 19: Register Map

Address	*Register Table*
1000BASE-T/100BASE-TX/10BASE-T Registers	
00h	Table 20: "1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h)," on page xcvi
01h	Table 21: "1000BASE-T/100BASE-TX/10BASE-T MII Status Register (Address 01h)," on page xcix
02h–03h	Table 22: "1000BASE-T/100BASE-TX/10BASE-T PHY Identifier Register (Addresses 02h and 03h)," on page ci
04h	Table 23: "1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement Register (Address 04h)," on page cii
05h	Table 24: "1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Link Partner Ability Register (Address 05h)," on page cv
06h	Table 25: "1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Expansion Register (Address 06h)," on page cvii
07h	Table 26: "1000BASE-T/100BASE-TX/10BASE-T Next Page Transmit Register (Address 07h)," on page cviii
08h	Table 27: "1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page Register (Address 08h)," on page cix
09h	Table 28: "1000BASE-T Control Register (Address 09h)," on page cx
0Ah	Table 29: "1000BASE-T Status Register (Address 0Ah)," on page cxii
0Ch–0Eh	Reserved (do not read from or write to a reserved register)
0Fh	Table 30: "1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status Register (Address 0Fh)," on page cxiv
10h	Table 31: "1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control Register (Address 10h)," on page cxv

Table 19: Register Map (Cont.)

Address	*Register Table*
11h	Table 32: “1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status Register (Address 11h),” on page cxvii
12h	Table 33: “1000BASE-T/100BASE-TX/10BASE-T Receive Error Counter Register (Address 12h),” on page cxx
13h	Table 34: “1000BASE-T/100BASE-TX/10BASE-T False Carrier Sense Counter Register (Address 13h),” on page cxx
14h	Table 35: “1000BASE-T/100BASE-TX/10BASE-T Receiver NOT_OK Counter Register (Address 14h),” on page cxxi
15h–16h	Reserved (Do not read from or write to a reserved register except when accessing the Expansion or Secondary SerDes registers through register 15h.)
17h	Table 36: “1000BASE-T/100BASE-TX/10BASE-T Expansion and Secondary SerDes Register Access Register (Address 17h),” on page cxxi
18h	• Table 41: “1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Register (Address 18h, Shadow Value 000),” on page cxxiv • Table 42: “10BASE-T Register (Address 18h, Shadow Value 001),” on page cxxvi • Table 43: “1000BASE-T/100BASE-TX/10BASE-T Power/MII Control Register (Address 18h, Shadow Value 010),” on page cxxix • Table 44: “1000BASE-T/100BASE-TX/10BASE-T Misc Test Register (Address 18h, Shadow Value 100),” on page cxxx • Table 45: “1000BASE-T/100BASE-TX/10BASE-T Misc Control Register (Address 18h, Shadow Value 111),” on page cxxxi
19h	Table 46: “1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary Register (Address 19h),” on page cxxxiv
1Ah	Table 47: “1000BASE-T/100BASE-TX/10BASE-T Interrupt Status Register (Address 1Ah),” on page cxxxvii
1Bh	Table 48: “1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask Register (Address 1Bh),” on page cxl

Table 19: Register Map (Cont.)

Address	*Register Table*
1Ch	• Table 50: "1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 Register (Address 1Ch, Shadow Value 00010)," on page cxliii • Table 51: "1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control Register (Address 1Ch, Shadow Value 00011)," on page cxliv • Table 52: "1000BASE-T/100BASE-TX/10BASE-T Spare Control 2 Register (Address 1Ch, Shadow Value 00100)," on page cxlv • Table 53: "1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 Register (Address 1Ch, Shadow Value 00101)," on page cxlvi • Table 54: "1000BASE-T/100BASE-TX/10BASE-T LED Status Register (Address 1Ch, Shadow Value 01000)," on page cxlviii • Table 55: "1000BASE-T/100BASE-TX/10BASE-T LED Control Register (Address 1Ch, Shadow Value 01001)," on page cl • Table 56: "Auto Power-Down Register (Address 1Ch, Shadow Value 01010)," on page cli • Table 58: "1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 Register (Address 1Ch, Shadow Value 01101)," on page cliii • Table 59: "1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 Register (Address 1Ch, Shadow Value 01110)," on page clv • Table 57: "External Control 2 (Address 1Ch, Shadow Value 01100)," on page cliii • Table 60: "1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status Register (Address 1Ch, Shadow Value 01111)," on page clvi • Table 61: "SerDes 100BASE-FX Status Register (Address 1Ch, Shadow Value = 10001)," on page clviii • Table 62: "SerDes 100BASE-FX Extend Register," on page clx • Table 63: "SerDes 100BASE-FX Control Register (Address 1Ch, Shadow Value 10011)," on page clx • Table 64: "Secondary SerDes Control Register (Address 1Ch, Shadow Value 10100)," on page clxi • Table 65: "SGMII Slave Register (Address 1Ch, Shadow Value 10101)," on page clxiv • Table 66: "Primary SerDes Control Register (Address 1C, Shadow Value = 10110)," on page clxvi • Table 67: "Misc 1000BASE-X Control 2 Register (Address 1C, Shadow Value = 10111)," on page clxvii • Table 68: "1000BASE-X Auto-Detect SGMII/Media Converter Register (Address 1Ch, Shadow Value 11000)," on page clxviii • Table 69: "1000BASE-X Auto-negotiation Debug Register (Address 1Ch, Shadow Value 11010)," on page clxix • Table 70: "Auxiliary 1000BASE-X Control Register (Address 1Ch, Shadow Value 11011)," on page clxxii • Table 71: "Auxiliary 1000BASE-X Status Register (Address 1Ch, Shadow Value 11100)," on page clxxiii • Table 72: "Misc 1000BASE-X Status Register (Address 1Ch, Shadow Value 11101)," on page clxxvi • Table 73: "Copper/Fiber Auto-Detect Medium Register (Address 1Ch, Shadow Value 11110)," on page clxxvii • Table 74: "Mode Control Register (Address 1Ch, Shadow Value 11111)," on page clxxix • Table 57: "External Control 2 (Address 1Ch, Shadow Value 01100)," on page cliii • Table 60: "1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status Register (Address 1Ch, Shadow Value 01111)," on page clvi

Table 19: Register Map (Cont.)

Address	Register Table
	• Table 61: "SerDes 100BASE-FX Status Register (Address 1Ch, Shadow Value = 10001)," on page clviii • Table 63: "SerDes 100BASE-FX Control Register (Address 1Ch, Shadow Value 10011)," on page clx • Table 64: "Secondary SerDes Control Register (Address 1Ch, Shadow Value 10100)," on page clxi • Table 65: "SGMII Slave Register (Address 1Ch, Shadow Value 10101)," on page clxiv • Table 66: "Primary SerDes Control Register (Address 1C, Shadow Value = 10110)," on page clxvi • Table 67: "Misc 1000BASE-X Control 2 Register (Address 1C, Shadow Value = 10111)," on page clxvii • Table 68: "1000BASE-X Auto-Detect SGMII/Media Converter Register (Address 1Ch, Shadow Value 11000)," on page clxviii • Table 69: "1000BASE-X Auto-negotiation Debug Register (Address 1Ch, Shadow Value 11010)," on page clxix • Table 70: "Auxiliary 1000BASE-X Control Register (Address 1Ch, Shadow Value 11011)," on page clxxii • Table 71: "Auxiliary 1000BASE-X Status Register (Address 1Ch, Shadow Value 11100)," on page clxxiii • Table 72: "Misc 1000BASE-X Status Register (Address 1Ch, Shadow Value 11101)," on page clxxvi • Table 73: "Copper/Fiber Auto-Detect Medium Register (Address 1Ch, Shadow Value 11110)," on page clxxvii • Table 74: "Mode Control Register (Address 1Ch, Shadow Value 11111)," on page clxxix
1Dh	• Table 75: "1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed Register (Address 1Dh) Bit 15=0," on page clxxxi • Table 76: "1000BASE-T/100BASE-TX/10BASE-T HCD Status Register (Address 1Dh) Bit 15 = 1," on page clxxxiii
1Eh	Table 77: "1000BASE-T/100BASE-TX/10BASE-T Test Register 1 (Address 1Eh)," on page clxxxvi
1Fh	Reserved (do not read from or write to a reserved register)
Primary SerDes Registers (Enabled by Register 1Ch, Shadow Value 11111, Bit 0 = 1)	
00h	Table 78: "1000BASE-X MII Control Register (Address 00h)," on page clxxxvii
01h	Table 79: "1000BASE-X MII Status Register (Address 01h)," on page clxxxix
04h	Table 80: "1000BASE-X Auto-negotiation Advertisement Register (Address 04h)," on page cxcii
05h	Table 81: "1000BASE-X Auto-Negotiation Link Partner Ability Register–Base Page (Address 05h)," on page cxciv
06h	Table 82: "1000BASE-X Auto-Negotiation Extended Status Register (Address 06h)," on page cxcvi
07h–0Eh	Reserved (do not read from or write to reserved register)
0Fh	Table 83: "1000BASE-X IEEE Extended Status Register (Address 0Fh)," on page cxcvii
Expansion Registers: Read/Write Through Register 15h (Accessed by Writing to Register 17h, Bits [11:0] = 1111 + Expansion Register Number)	
00h	Table 84: "Receive/Transmit Packet Counter Register (Address 00h)," on page cxcviii
01h	Table 85: "Expansion Interrupt Status Register (Address 01h)," on page cxcviii

Table 19: Register Map (Cont.)

Address	*Register Table*
02h	Table 86: “Expansion Interrupt Mask Register (Address 02h),” on page cxcix
04h	Table 87: “Multicolor LED Selector Register (Address 04h),” on page cc
05h	Table 88: “Multicolor LED Flash Rate Controls Register (Address 05h),” on page ccii
06h	Table 89: “Multicolor LED Programmable Blink Controls Register (Address 06h),” on page cciii
42h	Table 90: “Expansion Reg 42h: Operating Mode Status Register,” on page cciv
44h	Table 91: “SGMII Recover Control Register (Address 44h),” on page ccvii
50h	Table 92: “SerDes/SGMII Control RX Register (Address 50h),” on page ccvii
52h	Table 93: “SerDes/SGMII Control Register (Address 52h),” on page ccviii
Secondary SerDes Registers: Read/Write Through Register 15h (Accessed by Writing to Register 17h, Bits [11:0] = 1110 + Secondary SerDes Register Number)	
00h	Table 94: “1000BASE-X Control Register (Address 00h),” on page ccviii
04h	Table 95: “Auto-Negotiation Advertisement Register (Address 04h),” on page ccxi
05h	Table 96: “1000BASE-X Auto-Negotiation Link Partner Ability Register (Address 05h),” on page ccxii
06h	Table 97: “1000BASE-X Auto-Negotiation Secondary SerDes Register,” on page ccxv
07h	Table 98: “1000BASE-X Auto-Negotiation Next Page Transmit Register,” on page ccxvi
08h	Table 99: “1000BASE-X Auto-Negotiation Link Partner Next Page Register,” on page ccxvii
0Fh	Table 100: “1000BASE-X Extended Status Register,” on page ccxvii
10h	Table 101: “Misc 1 Register (Address 10h),” on page ccxviii
11h	Table 102: “100BASE-FX Status Register (Address 11h),” on page ccxix
12h	Table 103: “100BASE-FX Test Register (Address 12h),” on page ccxxi
13h	Table 104: “Packet Counter Register,” on page ccxxi
14h	Table 105: “Error Counter Register,” on page ccxxii
15h	Table 106: “SGMII Slave Register (Address 15h),” on page ccxxii
16h	Table 107: “Secondary SerDes Control Register,” on page ccxxiv
17h	Table 108: “Misc 1000BASE-X Control 2 Register,” on page ccxxiv
18h	Table 109: “Misc 1000-X Control 3 Register,” on page ccxxv
1Ah	Table 110: “Auto-Negotiation 1000BASE-X Debug Register,” on page ccxxvii
1Bh	Table 111: “Secondary SerDes Auxiliary 1000BASE-X Control Register (Address 1Bh),” on page ccxxix
1Ch	Table 112: “Auxiliary 1000BASE-X Status Register,” on page ccxxx
1Dh	Table 113: “Misc 1000BASE-X Status Register,” on page ccxxxii
21h	Table 114: “Spare Register,” on page ccxxxiii
30h	Table 115: “Secondary SerDes Interrupt Status Register (Address 30h),” on page ccxxxiv
31h	Table 116: “Secondary SerDes Interrupt MASK Register (Address 31h),” on page ccxxxvi
44h	Table 117: “Secondary SerDes Lineside Loopback Control Register,” on page ccxxxvii

Register Notations

In the register description tables, the following notation in the R/W column is used to describe the read or write ability:

- R/W = Read or write
- RO = Read only
- LH = Latched high
- LL = Latched low
- H = Fixed high
- L = Fixed low
- SC = Self clearing
- CR = Clear on reset

Reserved bits must be written as the default value and ignored when read.

1000BASE-T/100BASE-TX/10BASE-T Registers Descriptions

1000BASE-T/100BASE-TX/10BASE-T MII Control

Table 20: 1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Reset	R/W SC	1 = PHY reset 0 = Normal operation	0
14	Internal Loopback	R/W	1 = Loopback mode 0 = Normal operation	0
13	Speed Selection (LSB)	R/W	Bits [6,13]: 1 1 = Reserved 1 0 = 1000 Mbps 0 1 = 100 Mbps 0 0 = 10 Mbps	SPD0 and F1000 pins
12	Auto-negotiation Enable	R/W	1 = Auto-negotiation enabled 0 = Auto-negotiation disabled	ANEN or (INTFSEL[1:0] = 11)
11	Power Down	R/W	1 = Power down 0 = Normal operation	(INTFSEL[1:0] = 01)
10	Isolate	R/W	1 = Electrically isolate PHY from RGMII 0 = Normal operation	0
9	Restart Auto-negotiation	R/W SC	1 = Restarting auto-negotiation 0 = Auto-negotiation restart complete	0

Table 20: 1000BASE-T/100BASE-TX/10BASE-T MII Control Register (Address 00h) (Cont.)

Bit	Name	R/W	Description	Default
8	Duplex Mode	R/W	1 = Full duplex 0 = Half duplex	FDX pin
7	Collision Test Enable	R/W	1 = Enable the collision test mode 0 = Disable the collision test mode	0
6	Speed Selection (MSB)	R/W	Work in conjunction with bit 13	SPD0 and F1000 pins
5:0	Reserved	R/W	Write as 00h, ignore on read	00h

Reset

To reset the BCM5482S by software control, 1 must be written to bit 15 of the MII Control register. This bit self-clears after the reset process is complete and does not need to be cleared using a second MII write. Writes to other MII Control register bits have no effect until the reset process is completed, which requires approximately 2.0 µs. Writing 0 to this bit has no effect. When this bit is read during the reset process, a 1 is returned; otherwise, a 0 is returned.

Internal Loopback

The BCM5482S can be placed into internal loopback mode by setting bit 14 of the MII Control register. Loopback mode can be cleared by writing 0 to bit 14 of the MII Control register or by resetting the chip. When this bit is read and the chip is in loopback mode, a 1 is returned; otherwise, a 0 is returned.

Speed Selection (LSB)

When auto-negotiation is disabled, bits 6 and 13 of the MII Control register can be used to manually select the speed of operation. When bit 6 is set and bit 13 is cleared, 1000BASE-T operation is selected. When bit 6 is cleared and bit 13 is set, 100BASE-TX operation is selected. When both bits are cleared, 10BASE-T operation is selected. Setting both bits is not permitted. When read, these bits return the last value written. The default values of these bits are determined by the state of the SPD0 and F1000 pins at reset.

Auto-negotiation Enable

When bit 12 of the MII Control register is set, the BCM5482S mode of operation is controlled by auto-negotiation. When this bit is cleared, the BCM5482S mode of operation is determined by the manual speed, duplex mode, and master/slave configuration bits. When this bit is read with auto-negotiation enabled, a 1 is returned; otherwise, a 0 is returned. The default value of this bit is determined by the state of the ANEN pin at reset.

Power-Down

When bit 11 of the MII Control register is set, the BCM5482S is placed into low-power standby mode. At the default, the SerDes interface is powered down when the device is in copper mode, and vice versa, except in media converter or SGMII modes, where both media are powered on. For more details, see "Standby Power-Down Mode" on page lxix.

Note: When auto-medium mode detection is enabled, power bit of register 00h bit 11 is controlled by the internal state machine to power down the interface when it is selected. A 1 should not be written to this bit.

Isolate

The BCM5482S can be isolated from the RGMII bus by setting bit 10 of the MII Control register. All RGMII outputs are tristated, and all RGMII inputs are ignored. Because the management interface is still active, isolate mode can be cleared by writing 0 to bit 10 of the MII Control register or by resetting the chip. When this bit is read and the chip is in isolate mode, a 1 is returned; otherwise, a 0 is returned. This default of this bit is 0.

Restart Auto-negotiation

Setting bit 9 of the MII Control register forces the auto-negotiation process to be restarted, regardless of the current state of the auto-negotiation state machine. When auto-negotiation is enabled, setting this bit restarts the auto-negotiation process. Clearing this bit has no effect. This bit is self-clearing. After the auto-negotiation process has restarted, it returns 0.

Duplex Mode

When auto-negotiation is disabled, duplex mode of the BCM5482S can be controlled by writing to bit 8 of the MII Control register. Setting this bit forces the BCM5482S into full-duplex operation while clearing this bit forces the BCM5482S into half-duplex operation. When this bit is read, it returns the last value written. The default value of this bit is determined by the FDX pin at reset.

Speed Selection (MSB)

When auto-negotiation is disabled, bits 6 and 13 of the MII Control register can be used to manually select the speed of operation. When bit 6 is set and bit 13 is cleared, 1000BASE-T operation is selected. When bit 6 is cleared and bit 13 is set, 100BASE-TX operation is selected. When both bits are cleared, 10BASE-T operation is selected. Setting both bits is not permitted. When read, these bits return the last value written. The default values of these bits are determined by the state of the SPD0 and F1000 pins at reset.

Collision Test

The BCM5482S can be placed into collision test mode by setting to bit 7 of the MII Control register. In this mode, the COL pin is asserted whenever the TX_EN pin is driven high. Collision test mode can be cleared by writing 0 to bit 7 of the MII Control register or by resetting the chip. When this bit is read and the chip is in collision test mode, 1 is returned; otherwise, 0 is returned.

1000BASE-T/100BASE-TX/10BASE-T MII Status

Table 21: 1000BASE-T/100BASE-TX/10BASE-T MII Status Register (Address 01h)

Bit	Name	R/W	Description	Default
15	100BASE-T4 Capable	RO L	1 = 100BASE-T4 capable 0 = Not 100BASE-T4 capable	0
14	100BASE-X Full-duplex Capable	RO H	1 = 100BASE-X full-duplex capable 0 = Not 100BASE-X full-duplex capable	1
13	100BASE-X Half-duplex Capable	RO H	1 = 100BASE-X half-duplex capable 0 = Not 100BASE-X half-duplex capable	1
12	10BASE-T Full-duplex Capable	RO H	1 = 10BASE-T full-duplex capable 0 = Not 10BASE-T full-duplex capable	1
11	10BASE-T Half-duplex Capable	RO H	1 = 10BASE-T half-duplex capable 0 = Not 10BASE-T half-duplex capable	1
10	100BASE-T2 Full-duplex Capable	RO L	1 = 100BASE-T2 full-duplex capable 0 = Not 100BASE-T2 full-duplex capable	0
9	100BASE-T2 Half-duplex Capable	RO L	1 = 100BASE-T2 half-duplex capable 0 = Not 100BASE-T2 half-duplex capable	0
8	Extended Status	RO H	1 = Extended status information in reg 0Fh 0 = No extended status information in reg 0Fh	1
7	Reserved	RO	Ignore on read	0
6	Management Frames Preamble Suppression	RO H	1 = Preamble can be suppressed 0 = Preamble always required	1
5	Auto-negotiation Complete	RO	1 = Auto-negotiation complete 0 = Auto-negotiation in progress	0
4	Remote Fault	RO LH	1 = Remote fault detected 0 = No remote fault detected	0
3	Auto-negotiation Ability	RO H	1 = Auto-negotiation capable 0 = Not auto-negotiation capable	1
2	Link Status	RO LL	1 = Link is up (Link Pass state) 0 = Link is down (Link Fail state)	0
1	Jabber Detect	RO LH	1 = Jabber condition detected 0 = No jabber condition detected	0
0	Extended Capability	RO H	1 = Extended register capabilities 0 = No extended register capabilities	1

100BASE-T4 Capable

The BCM5482S is not capable of 100BASE-T4 operation and returns 0 when bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

100BASE-X Full-Duplex Capable

The BCM5482S is capable of 100BASE-TX full-duplex operation and returns 1 when bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

100BASE-X Half-Duplex Capable

The BCM5482S is capable of 100BASE-X half-duplex operation and returns 1 when bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

10BASE-T Full-Duplex Capable

The BCM5482S is capable of 10BASE-T full-duplex operation and returns 1 when bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

10BASE-T Half-Duplex Capable

The BCM5482S is capable of 10BASE-T half-duplex operation and returns 1 when bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

100BASE-T2 Full-Duplex Capable

The BCM5482S is not capable of 100BASE-T2 full-duplex operation and returns 0 when bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

100BASE-T2 Half-Duplex Capable

The BCM5482S is not capable of 100BASE-T2 half-duplex operation and returns 0 when bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

Extended Status

The BCM5482S contains IEEE Extended Status register at address 0Fh and returns 1 when bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

Management Frames Preamble Suppression

The BCM5482S accepts MII management frames whether or not they are preceded by the preamble pattern, and returns 1 when bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

Note: Preamble is still required on the first read or write.

Auto-negotiation Complete

The BCM5482S returns 1 in bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register when auto-negotiation has completed and the contents of registers 4, 5, and 6 are valid. This bit returns 0 while auto-negotiation is in progress.

Remote Fault

The BCM5482S returns 1 in bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register when its link partner has signaled a remote fault condition. When a remote fault occurs, the bit is set and remains so until the remote fault condition has been cleared and the register is read.

Auto-negotiation Ability

Even if the auto-negotiation function has been disabled, the BCM5482S is capable of performing IEEE auto-negotiation and returns 1 when bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

Link Status

The BCM5482S returns 1 in bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register when the link monitor is in the link pass state (indicating that a valid link has been established), otherwise it returns 0. When a link failure occurs, the Link Status bit is latched to 0 and remains so until the bit is read and the BCM5482S is in the link pass state.

Jabber Detect

Jabber detection is performed within the PHY and the result is latched into this bit. When a jabber condition has been detected, the BCM5482S returns 1 in bit 1 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register. The bit is cleared with a read.

Extended Capability

The BCM5482S supports Extended Capability registers and returns 1 when bit 0 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register is read.

1000BASE-T/100BASE-TX/10BASE-T PHY Identifier

Table 22: 1000BASE-T/100BASE-TX/10BASE-T PHY Identifier Register (Addresses 02h and 03h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:0	Address 02: ID MSBs	RO	16 MSBs of PHY Identifier	0143 (hex)
15:0	Address 03: ID LSBs	RO	16 LSBs of PHY Identifier	BCB*n*[a] (hex)

a. The revision number (*n*) changes with each silicon revision.

The IEEE has issued an Organizationally Unique Identifier (OUI) to Broadcom Corporation. This 24-bit number allows devices made by Broadcom to be distinguished from all other manufacturers. The OUI combined with model numbers and revision numbers assigned by Broadcom precisely identifies a device manufactured by Broadcom.

The [15:0] bits of MII register 02h (PHYID HIGH) contain OUI bits [3:18]. The [15:0] bits of MII register 03h (PHYID LOW) contain the most significant OUI bits [19:24], six Manufacturer Model Number bits, and four Revision Number bits. The two least significant OUI binary bits are not used.

Broadcom Corporation's OUI is 00-10-18, expressed as hexadecimal values. The binary OUI is 0000-0000-0000-1000-0001-1000. The model number for the BCM5482S is 0Bh. Revision numbers start with 0h and are incremented by 1 for each chip modification.

- PHYID HIGH[15:0] = OUI[3:18]
- PHYID LOW[15:0] = OUI[19:24] + Model[5:0] + Revision [3:0]

Table 22 (above) shows the result of concatenating these values to form the PHY identifiers for the BCM5482S.

1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement

Table 23: 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement Register (Address 04h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	R/W	1 = Next page ability supported 0 = Next page ability not supported	0
14	Reserved	R/W	Write as 0, ignore on read	0
13	Remote Fault	R/W	1 = Advertise remote fault detected 0 = Advertise no remote fault detected	0
12	Reserved Technology	R/W	Write as 0, ignore on read	0
11	Asymmetric Pause	R/W	1 = Advertise asymmetric pause 0 = Advertise no asymmetric pause	F1000 and INTFSEL[1:0] = 11
10	Pause Capable	R/W	1 = Capable of full-duplex pause operation 0 = Not capable of pause operation	F1000 and INTFSEL[1:0] = 11
9	100BASE-T4 Capable	R/W	1 = 100BASE-T4 capable 0 = Not 100BASE-T4 capable	0
8*	100BASE-TX Full-duplex Capable	R/W	1 = 100BASE-TX full-duplex capable 0 = Not 100BASE-TX full-duplex capable	Changed by hardware pin settings
7*	100BASE-TX Half-duplex Capable	R/W	1 = 100BASE-TX half-duplex capable 0 = Not 100BASE-TX half-duplex capable	Changed by hardware pin settings
6*	10BASE-T Full-duplex Capable	R/W	1 = 10BASE-T full-duplex capable 0 = Not 10BASE-T full-duplex capable	Changed by hardware pin settings

Note: *Bits 8:5 are internally forced to 0 at all times when media converter mode is active. (Register 1Ch, shadow 11111, bits 2:1 = 11)

Table 23: 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement Register (Address 04h)

Bit	Name	R/W	Description	Default
5*	10BASE-T Half-duplex Capable	R/W	1 = 10BASE-T half-duplex capable 0 = Not 10BASE-T half-duplex capable	Changed by hardware pin settings
4:0	Selector Field	R/W	00001 indicates IEEE 802.3 CSMA/CD	00001

Note: *Bits 8:5 are internally forced to 0 at all times when media converter mode is active. (Register 1Ch, shadow 11111, bits 2:1 = 11)

Next Page

Bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement register must be set when the management software wants to control Next Page exchange. When this bit is cleared, Next Page exchange is controlled automatically by the BCM5482S. When this bit is cleared and the BCM5482S is not advertising 1000BASE-T capability, no Next Page exchange occurs.

Remote Fault

Setting bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement register sends a remote fault indication to the link partner during auto-negotiation. Writing 0 to this bit clears the Remote Fault transmission bit. This bit returns 1 when advertising remote fault; otherwise, it returns 0.

Reserved Technology

Bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement register is reserved for future versions of the auto-negotiation standard, and must always be written as 0.

Asymmetric Pause

When bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement register is set, the BCM5482S advertises that an asymmetric pause is preferred. When the bit is cleared, the BCM5482S advertises that asymmetric pause is not needed. This bit returns 1 when advertising an asymmetric pause, otherwise it returns 0. When advertising asymmetric pause, bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement register indicates the preferred direction of the pause operation. Setting bit 10 indicates that the pause frames flow toward the BCM5482S. Clearing bit 10 indicates that pause frames flow toward the link partner.

Pause Capable

When bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement register is set, the BCM5482S advertises full-duplex pause capability. When the bit is cleared, the BCM5482S advertises no pause capability. This bit returns 1, when advertising pause capability; otherwise, it returns 0.

100BASE-T4 Capable

The BCM5482S does not support 100BASE-T4 capability. Do not write 1 to bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement register.

100BASE-TX Full-Duplex Capable

When bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement register is set, the BCM5482S advertises 100BASE-TX full-duplex capability. When the bit is cleared, the BCM5482S advertises no 100BASE-TX full-duplex capability. This bit returns 1 when advertising 100BASE-TX full-duplex capability; otherwise, it returns 0. This bit updates during reset based on configuring the hardware pins in the following way:

```
FDX AND (F1000 OR SPD0) AND NOT ((INTF_SEL[1] AND INTF_SEL[0]) OR (F1000 AND SPD0) OR (SD AND NOT
INTF_SEL[0])).
```

100BASE-TX Half-Duplex Capable

When bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement register is set, the BCM5482S advertises 100BASE-TX half-duplex capability. When the bit is cleared, the BCM5482S advertises no 100BASE-TX half-duplex capability. This bit returns 1 when advertising 100BASE-TX half-duplex capability; otherwise, it returns 0. This bit updates during reset based on configuring the hardware pins in the following way:

```
NOT FDX AND (F1000 OR SPD0) AND NOT ((INTF_SEL[1:0] = 11) OR F1000 AND SPD0) OR (SD AND NOT
INTF_SEL[1])).
```

10BASE-T Full-Duplex Capable

When bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement register is set, the BCM5482S advertises 10BASE-T full-duplex capability. When the bit is cleared, the BCM5482S advertises no 10BASE-T full-duplex capability. This bit returns 1 when advertising 10BASE-T full-duplex capability; otherwise, it returns 0. This bit updates during reset based on configuring the hardware pins in the following way:

```
FDX AND NOT ((INTF_SEL[1] AND INTF_SEL[0]) OR (F1000 AND SPD0) OR (SD AND NOT INTF_SEL[1])).
```

10BASE-T Half-Duplex Capable

When bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement register is set, the BCM5482S advertises 10BASE-T half-duplex capability. When the bit is cleared, the BCM5482S advertises no 10BASE-T half-duplex capability. This bit returns 1 when advertising 10BASE-T half-duplex capability; otherwise, it returns 0. This bit updates during reset based on configuring the hardware pins in the following way:

```
NOT FDX AND NOT ((INTF_SEL[1] AND INTF_SEL[0]) OR (F1000 and SPD0) OR (SD AND NOT INTF_SEL[1])).
```

Selector Field

Bits [4:0] of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Advertisement register indicate the protocol type. The value 00001 indicates that the BCM5482S belongs to the 802.3 class of PHY transceivers.

1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Link Partner Ability

Table 24: 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Link Partner Ability Register (Address 05h)

Bit	Name	R/W	Description	Default
15	Next Page	RO	1 = Link partner has Next Page ability. 0 = Link partner does not have Next Page ability.	0
14	Acknowledge	RO	1 = Link partner has received link code word. 0 = Link partner has not received link code word.	0
13	Remote Fault	RO	1 = Link partner has detected remote fault. 0 = Link partner has not detected remote fault.	0
12	Reserved Technology	RO	Write as 0. Ignore during a read.	0
11	Asymmetric Pause	RO	1 = Link partner wants asymmetric pause. 0 = Link partner does not want asymmetric pause.	0
10	Pause Capable	RO	1 = Link partner is capable of pause operation. 0 = Link partner is not capable of pause operation.	0
9	100BASE-T4 Capable	RO	1 = Link partner is 100BASE-T4 capable. 0 = Link partner is not 100BASE-T4 capable.	0
8	100BASE-TX Full-duplex Capable	RO	1 = Link partner is 100BASE-TX full-duplex capable. 0 = Link partner is not 100BASE-TX full-duplex capable.	0
7	100BASE-TX Half-duplex Capable	RO	1 = Link partner is 100BASE-TX half-duplex capable. 0 = Link partner not 100BASE-TX half-duplex capable.	0
6	10BASE-T Full-duplex Capable	RO	1 = Link partner is 10BASE-T full-duplex capable. 0 = Link partner is not 10BASE-T full-duplex capable.	0
5	10BASE-T Half-duplex Capable	RO	1 = Link partner is 10BASE-T half-duplex capable. 0 = Link partner is not 10BASE-T half-duplex capable.	0
4:0	Protocol Selector Field	RO	Link partner protocol selector field	00000

Note: As indicated by bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T MII Status register, the values contained in the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Link Partner Ability register are only guaranteed to be valid after auto-negotiation has successfully completed.

Next Page

The BCM5482S returns 1 in bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner wants to transmit Next Page information.

Acknowledge

The BCM5482S returns 1 in bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has acknowledged reception of the link code word; otherwise, it returns 0.

Remote Fault

The BCM5482S returns 1 in bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised detection of a remote fault; otherwise, it returns 0.

Reserved Technology

Bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register is reserved for future versions of the auto-negotiation standard and must be ignored when read.

Asymmetric Pause

The BCM5482S returns 1 in bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised an asymmetric pause; otherwise, it returns 0.

Pause Capable

The BCM5482S returns 1 in bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised Pause Capability; otherwise, it returns 0.

100BASE-T4 Capable

The BCM5482S returns 1 in bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised 100BASE-T4 capability; otherwise, it returns 0.

100BASE-TX Full-Duplex Capable

The BCM5482S returns 1 in bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised 100BASE-TX full-duplex capability; otherwise, it returns 0.

100BASE-TX Half-Duplex Capable

The BCM5482S returns 1 in bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised 100BASE-TX half-duplex capability; otherwise, it returns 0.

10BASE-T Full-Duplex Capable

The BCM5482S returns 1 in bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised 10BASE-T full-duplex capability; otherwise, it returns 0.

10BASE-T Half-Duplex Capable

The BCM5482S returns 1 in bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register when the link partner has advertised 10BASE-T half-duplex capability; otherwise, it returns 0.

Protocol Selector Field

Bits [4:0] of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register return the value of the link partner's advertised Protocol Selector field.

1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Expansion

Table 25: 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Expansion Register (Address 06h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:5	Reserved	RO	Write as 000h. Ignore on read	000h
4	Parallel Detection Fault	RO LH	1 = Parallel link fault detected 0 = Parallel link fault not detected	0
3	Link Partner Next Page Ability	RO	1 = Link partner has Next Page capability 0 = Link partner does not have Next Page capability	0
2	Next Page Capable	RO LH	1 = BCM5482S is Next Page capable 0 = BCM5482S is not Next Page capable	1
1	Page Received	RO LH	1 = New page has been received from link partner 0 = New page has not been received	0
0	Link Partner Auto-negotiation Ability	RO	1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation	0

Parallel Detection Fault

When a parallel detection fault has occurred in the auto-negotiation state machine, bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Expansion register returns 1. When a parallel detection fault occurs, this bit is latched at 1 and remains so until the register is read. If a parallel detection fault has not occurred since the last time it was read, this bit returns 0.

Link Partner Next Page Ability

The BCM5482S returns 1 in bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Expansion register when the link partner needs to transmit Next Page information; otherwise, it returns 0. This bit is a copy of bit 15 in the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Ability register.

Next Page Capable

When bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Expansion register is read, the BCM5482S supports Next Page capability and returns 1.

Page Received

The BCM5482S returns 1 in bit 1 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Expansion register when a new link code word has been received from the link partner since the last time this register was read; otherwise, it returns 0.

Link Partner Auto-negotiation Ability

When the link partner shows auto-negotiation capability, the BCM5482S returns 1 in bit 0 of the 1000BASE-T/100BASE-TX/10BASE-T Auto-negotiation Expansion register. Before any auto-negotiation information is exchanged or if the link partner does not comply with IEEE auto-negotiation, the bit returns 0.

1000BASE-T/100BASE-TX/10BASE-T Next Page Transmit

Table 26: 1000BASE-T/100BASE-TX/10BASE-T Next Page Transmit Register (Address 07h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	R/W	1 = Additional next pages follow 0 = Sending last next page	0
14	Reserved	RO	Write as 0, ignore on read	0
13	Message Page	R/W	1 = Formatted page 0 = Unformatted page	1
12	Acknowledge2	R/W	1 = Complies with message 0 = Cannot comply with message	0
11	Toggle	RO	Toggles between exchanges of different next pages	0
10:0	Message/Unformatted Code Field	R/W	Next page message code or unformatted data	001h

Next Page

Bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Next Page Transmit register must be set to indicate that more Next Pages are to be sent. This bit must be cleared to indicate that this is the last Next Page to be transmitted. When this bit is read, it returns the last value written.

Message Page

Bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Next Page Transmit register must be set to indicate that a formatted message page is being sent. This bit must be cleared to indicate that an unformatted page is being sent. When this bit is read, it returns the last value written.

Acknowledge2

When this bit is set, the BCM5482S indicates compliance with the Next Page request. When this bit is cleared, the BCM5482S indicates that it cannot comply with the Next Page request. When this bit is read, it returns the last value written.

Note: This bit is not used with 1000BASE-T next pages.

Toggle

This bit toggles between different Next Page exchanges to ensure a functional synchronization to the link partner.

Message/Unformatted Code Field

These 11 bits make up the message code defined by IEEE 802.3, Clause 28, Annex C, when sending formatted pages. When sending unformatted Next Pages, these 11 bits contain an arbitrary data value.

1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page

Table 27: 1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page Register (Address 08h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	RO	1 = Additional next pages follow 0 = Sending last Next Page	0
14	Acknowledge	RO	1 = Acknowledge 0 = No acknowledge	0
13	Message Page	RO	1 = Formatted page 0 = Unformatted page	0
12	Acknowledge2	RO	1 = Complies with message 0 = Cannot comply with message	0
11	Toggle	RO	Toggles between exchanges of different next pages	0
10:0	Message Code field	RO	Next Page message code or unformatted data	000h

Next Page

When the link partner has indicated that more Next Pages are to be sent, bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page register returns 1. This bit returns 0 when the link partner indicates that this is the last Next Page to be transmitted.

Acknowledge

Bit 14 returns 1 to indicate that the link partner has received and acknowledged a Next Page. The bit returns 0 until the link partner has acknowledged the page.

Message Page

Bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page register returns 1 to indicate that the link partner has sent a formatted message page. This bit returns 0 when the link partner has sent an unformatted page.

Acknowledge2

When the link partner has indicated compliance with the Next Page request, bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Link Partner Received Next Page register returns 1. When the link partner has indicated that it cannot comply with the Next Page request, this bit returns 0.

Note: This bit is not used with 1000BASE-T Next Pages.

Toggle

To ensure a functional synchronization to the BCM5482S transceiver, the link partner toggles this bit between different Next Page exchanges.

Message Code Field

These 11 bits make up the message code defined by IEEE 802.3, Clause 28, Annex C, when the link partner has sent a formatted page. When the link partner has sent unformatted next pages, these 11 bits contain an arbitrary data value.

1000BASE-T Control

Table 28: 1000BASE-T Control Register (Address 09h)

Bit	Name	R/W	Description	Default
15:13	Test Mode	R/W	1 X X = Test mode 4—Transmitter distortion test 0 1 1 = Test mode 3—Slave transmit jitter test 0 1 0 = Test mode 2—Master transmit jitter test 0 0 1 = Test mode 1—Transmit waveform test 0 0 0 = Normal operation	000
12	Master/Slave Configuration Enable	R/W	1 = Enable master/slave manual configuration value 0 = Automatic master/slave configuration	0

Table 28: 1000BASE-T Control Register (Address 09h) (Cont.)

Bit	Name	R/W	Description	Default
11	Master/Slave Configuration Value	R/W	1 = Configure PHY as master 0 = Configure PHY as slave	0
10	Repeater/DTE	R/W	1 = Repeater/switch device port 0 = DTE device	0
9	Advertise 1000BASE-T Full-duplex Capability	R/W	1 = Advertise 1000BASE-T full-duplex capability 0 = Advertise no 1000BASE-T full-duplex capability	Default = FDX and (F1000 or INTFSEL[1:0] = 11)
8	Advertise 1000BASE-T Half-duplex Capability	R/W	1 = Advertise 1000BASE-T half-duplex capability 0 = Advertise no 1000BASE-T half-duplex capability	(INTFSEL[1:0] = 11 and ANEN) or (not [INTFSEL[1:0] = 11 and F1000])
7:0	Reserved	RO	Write as 0. Ignore on read	00h

Test Mode

The BCM5482S can be placed in one of four transmit test modes by writing bits [15:13] of the 1000BASE-T Control register. The transmit test modes are defined in IEEE 802.3ab. When read, these bits return the last value written. For test modes 1, 2 and 4, the PHY must have auto-negotiation disabled, forced to 1000BASE-T mode and Auto-MDIX disabled.

- Disable auto-neg and Force to 1000BASE-T mode (write to register 00h = 0x0040)
- Disable Auto-MDIX (write to register 18h, shadow value 111, bit 9 = 0)
- Enter test modes (write to register 09h, bits[15:13] = the test mode you want)

Master/Slave Configuration Enable

When bit 12 of the 1000BASE-T Control register is set, the master/slave mode is configured using the manual master/slave configuration value. When the bit is cleared, the master/slave mode is configured using the automatic resolution function. This bit returns 1 when manual master/slave configuration is enabled; otherwise, it returns 0.

Master/Slave Configuration Value

When bit 12 of the 1000BASE-T Control register is set, bit 11 of the 1000BASE-T Control register determines the master/slave mode of operation. When bit 11 is set, the BCM5482S is configured as the master. When bit 11 is cleared, the BCM5482S is configured as the slave. When read, this bit returns the last value written.

Repeater/DTE

When bit 10 of the 1000BASE-T Control register is set, the BCM5482S advertises that it is a repeater or switch device port. When the bit is cleared, the BCM5482S advertises that it is a DTE port. The advertised value is used in the automatic master/slave configuration resolution. The link partner, which advertises repeater mode, is configured to master if the opposing link partner advertises data terminal equipment (DTE); otherwise, this bit has no effect. This bit returns 1 when advertising repeater/switch mode; otherwise, it returns 0.

Advertise 1000BASE-T Full-Duplex Capability

When bit 9 of the 1000BASE-T Control register is set, the BCM5482S advertises 1000BASE-T full-duplex capability. When the bit is cleared, the BCM5482S advertises no 1000BASE-T full-duplex capability. This bit returns 1 when advertising 1000BASE-T full-duplex capability; otherwise, it returns 0. The default value of this bit is determined by the state of the FDX pin at reset.

Advertise 1000BASE-T Half-Duplex Capability

When bit 8 of the 1000BASE-T Control register is set, the BCM5482S advertises 1000BASE-T half-duplex capability. When the bit is cleared, the BCM5482S advertises no 1000BASE-T half-duplex capability. This bit returns 1 when advertising 1000BASE-T half-duplex capability; otherwise, it returns 0.

1000BASE-T Status

Table 29: 1000BASE-T Status Register (Address 0Ah)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Master/Slave Configuration Fault	RO LH	1 = Master/slave configuration fault detected 0 = No master/slave configuration fault detected	0
14	Master/Slave Configuration Resolution	RO	1 = Local transmitter is master 0 = Local transmitter is slave	0
13	Local Receiver Status	RO	1 = Local receiver OK 0 = Local receiver not OK	0
12	Remote Receiver Status	RO	1 = Remote receiver OK 0 = Remote receiver not OK	0
11	Link Partner 1000BASE-T Full-duplex Capability	RO	1 = Link partner is 1000BASE-T full-duplex capable 0 = Link partner not 1000BASE-T full-duplex capable	0
10	Link Partner 1000BASE-T Half-duplex Capability	RO	1 = Link partner is 1000BASE-T half-duplex capable 0 = Link partner not 1000BASE-T half-duplex capable	0
9:8	Reserved	RO	Write as 00, ignore on read	00
7:0	Idle Error Count	RO CR	Number of idle errors since last read	00h

Note: As indicated by bit 5 of the MII Status register, the values contained in bits 14, 11, and 10 of the 1000BASE-T Status register are guaranteed to be valid only after auto-negotiation has successfully completed.

Master/Slave Configuration Fault

When a master/slave configuration fault has occurred during auto-negotiation, the BCM5482S returns 1 in bit 15 of the 1000BASE-T Status register. When a configuration fault occurs, the bit is latched at 1 and remains so until either the register is read, auto-negotiation is restarted by writing bit 9 in the MII Control register, or auto-negotiation completes successfully with no master/slave configuration fault.

Master/Slave Configuration Resolution

When the BCM5482S transceiver has been configured as the master, it returns 1 in bit 14 of the 1000BASE-T Status register. When the BCM5482S transceiver has been configured as the slave, it returns 0.

Local Receiver Status

The BCM5482S transceiver returns 1 in bit 13 of the 1000BASE-T Status register when the local receiver status is OK; otherwise, it returns 0.

Remote Receiver Status

The BCM5482S returns 1 in bit 12 of the 1000BASE-T Status register when the remote receiver status is OK; otherwise, it returns 0.

1000BASE-T Full-Duplex Capability

The BCM5482S returns 1 in bit 11 of the 1000BASE-T Status register when the link partner has advertised 1000BASE-T full-duplex capability; otherwise, it returns 0.

1000BASE-T Half-Duplex Capability

The BCM5482S returns 1 in bit 10 of the 1000BASE-T Status register when the link partner has advertised 1000BASE-T half-duplex capability; otherwise, it returns 0.

Idle Error Count

The BCM5482S counts the number of idle errors received while the local receiver status is OK. Bits 7 through 0 of the 1000BASE-T Status register return the number of idle errors counted since the last register read. The counter freezes at the maximum value (FFh) to prevent overflow.

1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status

Table 30: 1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status Register (Address 0Fh)

Bit	Name	R/W	Description	Default
15	1000BASE-X Full-duplex Capable	RO L	1 = 1000BASE-X full-duplex capable 0 = Not 1000BASE-X full-duplex capable	0
14	1000BASE-X Half-duplex Capable	RO L	1 = 1000BASE-X half-duplex capable 0 = Not 1000BASE-X half-duplex capable	0
13	1000BASE-T Full-duplex Capable	RO H	1 = 1000BASE-T full-duplex capable 0 = Not 1000BASE-T full-duplex capable	1
12	1000BASE-T Half-duplex Capable	RO H	1 = 1000BASE-T half-duplex capable 0 = Not 1000BASE-T half-duplex capable	1
11:0	Reserved	RO	Write as 000h, ignore on read	000h

1000BASE-X Full-Duplex Capable

The BCM5482S is not capable of 1000BASE-X full-duplex operation and returns 0 when bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status register is read.

1000BASE-X Half-Duplex Capable

The BCM5482S is not capable of 1000BASE-X half-duplex operation and returns 0 when bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status register is read.

1000BASE-T Full-Duplex Capable

The BCM5482S is capable of 1000BASE-T full-duplex operation and returns 1 when bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status register is read.

1000BASE-T Half-Duplex Capable

The BCM5482S is capable of 1000BASE-T half-duplex operation and returns 1 when bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T IEEE Extended Status register is read.

1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control

Table 31: 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control Register (Address 10h)

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Reserved	0
14	Disable Automatic MDI Crossover	R/W	1 = Automatic MDI crossover disabled 0 = Automatic MDI crossover enabled	0
13	Transmit Disable	R/W	1 = Transmitter outputs disabled 0 = Normal operation	0
12	Interrupt Disable	R/W	1 = Interrupt status output disabled 0 = Interrupt status output enabled	0
11	Force Interrupt	R/W	1 = Force interrupt status to active 0 = Normal operation	0
10	Bypass 4B/5B Encoder/Decoder (100BASE-T)	R/W	1 = Transmit and receive 5B codes over MII pins 0 = Normal MII	0
9	Bypass Scrambler/Descrambler (100BASE-T)	R/W	1 = Scrambler and descrambler disabled 0 = scrambler and descrambler enabled	0
8	Bypass MLT3 Encoder/Decoder (100BASE-T)	R/W	1 = Bypass NRZI/MLT3 encoder and decoder 0 = Normal operation	0
7	Bypass Receive Symbol Alignment (100BASE-T)	R/W	1 = 5B receive symbols not aligned 0 = Receive symbols aligned to 5B boundaries	0
6	Reset Scrambler (100BASE-T)	R/W SC	1 = Reset scrambler to initial state 0 = Normal scrambler operation	0
5	Enable LED Traffic Mode	R/W	1 = LED Traffic mode enabled 0 = LED Traffic mode disabled	0
4	Force LEDs On	R/W	1 = Force all LEDs into on state 0 = Normal LED operation	0
3	Force LEDs Off	R/W	1 = Force all LEDs into off state 0 = Normal LED operation	0
2:1	Reserved	R/W	Write as 00, ignore on read	00
0	1000BASE-T PCS Transmit FIFO Elasticity (Copper Mode)	R/W‘	1 = High latency 0 = Low latency	0

Disable Automatic MDI Crossover

The automatic MDI crossover function can be disabled by setting bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. When the bit is cleared, the BCM5482S performs the automatic MDI crossover function (see “Automatic MDI Crossover” on page l for details).

Transmit Disable

The transmitter can be disabled by setting bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. The transmitter outputs (TRD± [3:0]) are forced into a high-impedance state.

Interrupt Disable

When this bit is set, the interrupt pin is forced to its inactive state except when the Force Interrupt bit is set.

Force Interrupt

When this bit is set, the INTR pin is forced to its active state.

Bypass 4B/5B Encoder/Decoder (100BASE-T)

The 100BASE-TX4B/5B encoder/decoder can be bypassed by setting bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. The transmitter sends 5B codes from the TX_ER and TXD[3:0] pins directly to the scrambler. TX_EN is ignored and frame encapsulation (insertion of J/K and T/R codes) is not performed. The receiver places descrambled and aligned 5B codes onto the RX_ER and RXD[3:0] pins.

Bypass Scrambler/Descrambler (100BASE-T)

The 100BASE-TX stream cipher function can be disabled by setting bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. The stream cipher function can be re-enabled by writing 0 to this bit.

Bypass MLT3 Encoder/Decoder (100BASE-T)

The 100BASE-TX MLT3 encoder and decoder can be bypassed by setting bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. NRZ data is transmitted and received on the cable. The MLT3 encoder can be re-enabled by clearing this bit.

Bypass Receive Symbol Alignment (100BASE-T)

The 100BASE-TX receive symbol alignment can be bypassed by setting bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register. When used in conjunction with the bypass 4B/5B encoder/decoder bit, unaligned 5B codes are placed directly on the RX_ER and RXD[3:0] pins.

Reset Scrambler (100BASE-T)

When bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register is set, the BCM5482S resets the scrambler to an all 1’s. This bit is self-clearing and always returns 0 when read.

Enable LED Traffic Mode

When bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register is set, the BCM5482S enables the LED traffic mode for activity, ACTIVITYLED and XMITLED. When the bit is cleared, the BCM5482S disables the LED traffic mode.

Force LEDs On

When bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register is set, the BCM5482S forces all LEDs into the on state. When the bit is cleared, the BCM5482S resets all LEDs to normal operation.

Force LEDs Off

When bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Control register is set, the BCM5482S forces all LEDs into the off state. When the bit is cleared, the BCM5482S resets all LEDs to normal operation.

1000-Mbps PCS Transmit FIFO Elasticity (Jumbo Packets)

When bit 0 of the PHY Extended Control register is set, the BCM5482S sets the FIFO elasticity to high latency. In this mode, the BCM5482S can transmit packets up to 9 kilobytes in length. When this bit is cleared, the FIFO elasticity is set to low latency. In this mode, the BCM5482S can transmit packets up to 4.5 kilobytes in length. Setting this bit to 1 adds 16 ns to the 1000BASE-T/1000BASE-X transmit latency.

1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status

Table 32: 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status Register (Address 11h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Auto-negotiation Base Page Selector Field Mismatch	RO LH	1 = Link partner base page selector field mismatched advertised selector field since last read 0 = No mismatch detected since last read	0
14	Ethernet@WireSpeed Downgrade	RO	1 = Auto-negotiation advertised speed downgraded 0 = No advertised speed downgrade	0
13	MDI Crossover State	RO	1 = Crossover MDI mode 0 = Normal MDI mode	0
12	Interrupt Status	RO	1 = Unmasked interrupt currently active 0 = Interrupt cleared	0
11	Remote Receiver Status	RO LL	1 = Remote receiver OK 0 = Remote receiver not OK since last read	0
10	Local Receiver Status	RO LL	1 = Local receiver OK 0 = Local receiver not OK since last read	0
9	Locked	RO	1 = Descrambler locked 0 = Descrambler unlocked	0

Table 32: 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status Register (Address 11h) (Cont.)

Bit	Name	R/W	Description	Default
8	Link Status	RO	1 = Link pass 0 = Link fail	0
7	CRC Error Detected	RO LL	1 = CRC error detected 0 = No CRC error since last read	0
6	Carrier Extension Error Detected	RO LH	1 = Carrier extension error detected since last read 0 = No carrier extension error since last read	0
5	Bad SSD Detected (False Carrier)	RO LH	1 = Bad SSD error detected since last read 0 = No bad SSD error since last read	0
4	Bad ESD Detected (Premature End)	RO LH	1 = Bad ESD error detected since last read 0 = No bad ESD error since last read	0
3	Receive Error Detected	RO LH	1 = Receive error detected since last read 0 = No receive error since last read	0
2	Transmit Error Detected	RO LH	1 = Transmit error code received since last read 0 = No transmit error code received since last read	0
1	Lock Error Detected	RO LH	1 = Lock error detected since last read 0 = No lock error since last read	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 code error detected since last read 0 = No MLT3 code error since last read	0

Auto-negotiation Base Page Selector Field Mismatch

When this bit is set, the auto-negotiation base page selector does not match the Advertised Selector field since the previous read. When this bit reads back 0, there is no mismatched Page Selector field and Advertised Selector field.

Ethernet@WireSpeed Downgrade

The BCM5482S returns 1 in bit 14 when an Ethernet@WireSpeed downgrade has occurred.

MDI Crossover State

When the BCM5482S is automatically switching the transmit and receive pairs to communicate with a remote device, the BCM5482S returns 1 in bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register. This bit returns 0 when the BCM5482S is in normal MDI mode.

Interrupt Status

The BCM5482S returns 1 in bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register when any unmasked interrupt is currently active; otherwise, it returns 0.

Remote Receiver Status

When the remote receiver status is OK, the BCM5482S returns 1 in bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register. When the BCM5482S detects that the remote receiver is not OK, this bit is latched at 0 and remains so until the bit is read and the remote receiver status is OK.

Local Receiver Status

When the local receiver status is OK, the BCM5482S returns 1 in bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register. When the BCM5482S detects that the local receiver is not OK, this bit is latched at 0 and remains so until the bit is read and the remote receiver status is OK.

Locked

The BCM5482S returns 1 in bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register when the descrambler is locked to the incoming data stream; otherwise, it returns 0.

Link Status

The BCM5482S returns 1 in bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register when the device has established a link; otherwise, it returns 0.

CRC Error Detected

The BCM5482S **retur**ns 1 in bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a CRC error has been detected since the last time this register was read; otherwise, it returns 0.

Carrier Extension Error Detected

The BCM5482S returns 1 in bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a carrier extension error has been detected since the last time this register was read; otherwise, it returns 0.

Bad SSD Detected (False Carrier)

The BCM5482S returns 1 in bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a bad start-of-stream error has been detected since the last time this register was read; otherwise, it returns 0.

Bad ESD Detected (Premature End)

The BCM5482S returns 1 in bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a bad end-of-stream error has been detected since the last time this register was read; otherwise, it returns 0.

Receive Error Detected

The BCM5482S returns 1 in bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a packet was received with an invalid code since the last time this register was read; otherwise, it returns 0.

Transmit Error Detected

The BCM5482S returns 1 in bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if a packet was received with a transmit error code since the last time this register was read; otherwise, it returns 0.

Lock Error Detected

The BCM5482S returns 1 in bit 1 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if the descrambler has lost lock since the last time this register was read; otherwise, it returns 0.

MLT3 Code Error Detected

The BCM5482S returns 1 in bit 0 of the 1000BASE-T/100BASE-TX/10BASE-T PHY Extended Status register if an MLT3 coding error has been detected in the receive data stream since the last time this register was read; otherwise, it returns 0.

1000BASE-T/100BASE-TX/10BASE-T Receive Error Counter

Table 33: 1000BASE-T/100BASE-TX/10BASE-T Receive Error Counter Register (Address 12h)[a]

Bit	Name	R/W	Description	Default
15:0	Receive Error Counter	R/W CR	Number of non-collision packets with receive errors since last read	0000h

a. Bits 15:0 of this register become the SerDes data bit when register 1Ch, shadow 11011, bit 9 is set.

Receive Error Counter

This counter increments each time the BCM5482S receives a noncollision packet containing at least 1 receive error. This counter freezes at the maximum value of FFFFh. The counter automatically clears when read.

1000BASE-T/100BASE-TX/10BASE-T False Carrier Sense Counter

Table 34: 1000BASE-T/100BASE-TX/10BASE-T False Carrier Sense Counter Register (Address 13h)[a]

Bit	Name	R/W	Description	Default
15:8	Reserved	R/W	Write as 00h, ignore on read	00h
7:0	False Carrier Sense Counter	R/W CR	Number of false carrier sense events since last read	00h

a. Bits 15:0 of this register become the SerDes data bit when register 1Ch, shadow 11011, bit 9 is set.

False Carrier Sense Counter

The False Carrier Sense Counter increments each time the BCM5482S detects a false carrier sense on the receive input. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

1000BASE-T/100BASE-TX/10BASE-T Receiver NOT_OK Counter

Table 35: 1000BASE-T/100BASE-TX/10BASE-T Receiver NOT_OK Counter Register (Address 14h)[a]

Bit	Name	R/W	Description	Default
15:8	Local Receiver NOT_OK Counter	R/W CR	Number of times local receiver was NOT_OK since last read	00h
7:0	Remote Receiver NOT_OK Counter	R/W CR	Number of times BCM5482S detected that the remote receiver was NOT_OK since last read	00h

a. Bits 15:0 of this register become the CRC error bits when register 1Eh bit 15 is set. Bits 15:0 of this register become the SerDes data bit when register 1Ch, shadow 11011, bit 9 is set.

Local Receiver NOT_OK Counter

This counter increments each time the local receiver enters the NOT_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

Remote Receiver NOT_OK Counter

This counter increments each time the remote receiver enters the NOT_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

1000BASE-T/100BASE-TX/10BASE-T Expansion Register Access

Table 36: 1000BASE-T/100BASE-TX/10BASE-T Expansion and Secondary SerDes Register Access Register (Address 17h)

Bit	Name	R/W	Description	Default
15:12	Reserved	R/W	Write as 0h, ignore on read	0h
11:8	Expansion and Secondary SerDes Register Select	R/W	1111 = Expansion register selected 1110 = Secondary SerDes Selected 0000 = Expansion register not selected All Others = Reserved (Do not use)	0h
7:0	Expansion and Secondary SerDes Register Accessed	R/W	Sets the Expansion register number accessed when read/write to register 15h.	00h

Expansion Register Select

Setting bits [11:8] to 1111 enable the reading from and writing to the Expansion registers through register 15h. These bits should be cleared after the Expansion registers are accessed or when the Expansion registers are not being accessed. See "Expansion Registers" on page cxcviii for details.

Expansion Register Accessed

Bits [7:0] of the Expansion Register Access register set the Expansion register number accessed. The Expansion register is read/write through register 15h when bits [11:8] of this register are set to 1111. The available expansion registers are listed in Table 37.

Table 37: Expansion Register Select Values

Expansion Register	*Register Name*
00h	”Receive/Transmit Packet Counter Register (Address 00h)” on page cxcviii
01h	”Expansion Interrupt Status Register (Address 01h)” on page cxcviii
04h	”Multicolor LED Selector Register (Address 04h)” on page cc
05h	”Multicolor LED Flash Rate Controls Register (Address 05h)” on page ccii
06h	”Multicolor LED Programmable Blink Controls Register (Address 06h)” on page cciii

1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register

The following table lists the available 18h registers.

Table 38: 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Values Access

Shadow Value	*Register Name*
000	”1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Register (Address 18h, Shadow Value 000)” on page cxxiv
001	”10BASE-T Register (Address 18h, Shadow Value 001)” on page cxxvi
010	”1000BASE-T/100BASE-TX/10BASE-T Power/MII Control Register (Address 18h, Shadow Value 010)” on page cxxix
100	”1000BASE-T/100BASE-TX/10BASE-T Misc Test Register (Address 18h, Shadow Value 100)” on page cxxx
111	”1000BASE-T/100BASE-TX/10BASE-T Misc Control Register (Address 18h, Shadow Value 111)” on page cxxxi

The following table shows the read from register 18h, shadow value zzz.

Table 39: Reading Register 18h

Register Reads/Writes	*Description*
Write register 18h, bits [2:0] = 111	This selects the Misc Control register, shadow value 111. All reads must be done through the Misc Control register.
Bit [15] = 0	This allows only bits [14:12] and [2:1] to be written.
Bits [14:12] = zzz	This selects shadow value register zzz to be read.
Bits [11: 3] = <don't care>	When bit [15] = 0, these bits are ignored.
Bits [2:0] = 111	This sets the Shadow Register Select to 111 (Misc Control register).
Read register 18h	Data read back is the value from shadow register zzz.

The following table shows the write to register 18h, shadow value yyy.

Table 40: Writing Register 18h

Register Writes	*Description*
Set Bits [15:3] = Preferred write values	Bits [15:3] contain the preferred bits to be written to.
Set Bits [2:0] = yyy	This enables shadow value register yyy to be written. For shadow value 111, bit 15 must also be written.

Table 41: 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Register (Address 18h, Shadow Value 000)

Bit	*Name*	*R/W*	*Description*	*Default*
15	External Loopback	R/W	1 = External Loopback enabled 0 = Normal operation	0
14	Extended Packet Length	R/W	1 = Allow reception of extended length packets for 100BASE-FX mode 0 = Allow normal length Ethernet packets only	(INTFSEL[1:0] = 11) for 100BASE-TX or FX
13:12	Edge Rate Control (1000BASE-T)	R/W	00 = 4.0 ns 01 = 5.0 ns 10 = 3.0 ns 11 = 0.0 ns	00
11	Reserved	R/W	Write as 0, ignore on read	0
10	Transmit Mode	R/W	1 = Normal operation 0 = Test mode	1
9:8	Reserved	R/W	Write as 0, ignore on read	0
7	Disable Partial Response Filter	R/W	1 = Transmitter partial response filter disabled 0 = Transmitter partial response filter enabled	0
6	Reserved	R/W	Write as 0, ignore on read	0
5:4	Edge-Rate Control (100BASE-TX)	R/W	00 = 4.0 ns 01 = 5.0 ns 10 = 3.0 ns 11 = 0.0 ns	00
3	Reserved	R/W	Write as 0, ignore on read	0

Table 41: 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Register (Address 18h, Shadow Value 000) (Cont.)

Bit	Name	R/W	Description	Default
2:0	Shadow Register Select	R/W	000 = Auxiliary Control register 001 = 10BASE-T register 010 = Power/MII Control register 011 = Reserved 100 = Misc Test register 101 = Reserved 110 = Reserved 111 = Misc Control register	000

External Loopback

When bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register shadow value 000 is set, external loopback operation is enabled. When the bit is cleared, normal operation resumes.

Extended Packet Length

When bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register shadow value 000 is set, the BCM5482S receives packets up to 10 KB in length. When the bit is cleared, the BCM5482S only receives packets up to 4.5 KB in length.

Edge-Rate Control (1000BASE-T)

Bits 13 and 12 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register 18h shadow value 000 control the edge rate of the 1000BASE-T transmit DAC output waveform.

Note: The ER pin status is not reflected in the register 18 shadow 000.

Transmit Mode

Bit 10 of the Auxiliary Control register shadow value 000 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register must be set for normal PHY operation.

Disable Partial Response Filter

When bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register shadow value 000 is set, the transmitter partial response filter is disabled. When the bit is cleared, the transmitter partial response filter is enabled.

Edge-Rate Control (100BASE-TX)

Bits 5 and 4 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register 18h, shadow value 000 control the edge rate of the 100BASE-TX transmit DAC output waveform.

Note: The ER pin status is not reflected in Register 18, shadow 000.

Shadow Register Select

The Auxiliary Control register provides access to eight registers using a shadow technique. The lower 3 bits written define which set of 13 upper bits are used in accordance with Table 41 on page cxxiv, defined under bits [2:0]. See the note in "1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page cxxiii describing reading/writing register 18h.

The register set previously shown is for Auxiliary Control operation, obtained when the lower 3 bits are 000.

10BASE-T

Table 42: 10BASE-T Register (Address 18h, Shadow Value 001)

Bit	Name	R/W	Description	Default
15	Manchester Code Error	RO LH	1 = Manchester code error (10BASE-T) 0 = No Manchester code error	0
14	EOF Error	RO LH	1 = EOF error detected (10BASE-T) 0 = No EOF error detected	0
13	Polarity Error	RO	1 = Channel polarity inverted 0 = Channel polarity correct	0
12	Block RX_DV Extension (IPG)	R/W	1 = Block RX_DV for 4 additional RXC cycles for IPG 0 = Normal operation	0
11	10BASE-T TXC Invert Mode	R/W	1 = Invert TXC output 0 = Normal operation	0
10	Reserved	RO	Write as 0, ignore on read	0
9	Jabber Disable	R/W	1 = Jabber function disabled 0 = Jabber function enabled	0
8	Reserved	RO	Write as 0, ignore on read	0
7	10BASE-T Signal Detect Threshold	R/W	1 = Low SD threshold 0 = Normal threshold	0
6	10BASE-T Echo Mode	R/W	1 = Echo transmit data to receive data 0 = Normal operation	0
5	SQE Enable Mode	R/W	1 = Enable SQE 0 = Disable SQE	0

Table 42: 10BASE-T Register (Address 18h, Shadow Value 001) (Cont.)

Bit	Name	R/W	Description	Default
4	10BASE-T No Dribble	R/W	1 = Correct 10BASE-T dribble nibble 0 = Normal operation	0
3	Reserved	RO	Write as 0, ignore on read	0
2:0	Shadow Register Select	R/W	000 = Auxiliary Control register 001 = 10BASE-T register 010 = Power/MII Control register 011 = Reserved 100 = Misc Test register 101 = Reserved 110 = Reserved 111 = Misc Control register	001

Manchester Code Error

When a Manchester code violation is received, bit 15 of the 10BASE-T register returns 1. This bit is valid only during 10BASE-T operation.

EOF Error

When the end-of-frame (EOF) sequence was improperly received (or not received at all), bit 14 of the 10BASE-T register returns 1. This bit is valid only during 10BASE-T operation.

Polarity Error

When an analog input polarity error has been detected and corrected, bit 13 of the 10BASE-T register returns 1. This bit is valid only during 10BASE-T operation.

Block RX_DV Extension (IPG)

When bit 12 of the 10BASE-T register is set, blocking of the RX_DV signal is extended for an additional four RXC cycles to extend the IPG.

10BASE-T TXC Invert Mode

When bit 11 of the 10BASE-T register is set, the polarity of the 10BASE-T transmit clock is inverted. Clearing this bit restores normal transmit clock polarity. This bit is valid only during 10BASE-T operation.

Jabber Disable

Setting bit 9 of the 10BASE-T register allows the user to disable the jabber detect function defined in the IEEE standard. When a transmission request has exceeded a maximum time limit, this function shuts off the transmitter. Clearing this bit or resetting the chip restores normal operation. Reading this bit returns the value of jabber detect disable. This bit is valid only during 10BASE-T operation.

1000BASE-T Signal Detect Threshold

Setting bit 8 of the 10BASE-T register enables the low 1000BASE-T signal detect threshold. The bit is cleared when in the normal or default mode.

10BASE-T Signal Detect Threshold

Setting bit 7 of the 10BASE-T register enable the low 10BASE-T signal detect threshold. The bit is cleared when in the normal or default mode.

10BASE-T Echo Mode

When bit 6 of the 10BASE-T register is enabled during 10BASE-T half-duplex transmit operation, the transmitted data is replicated on the receive data pins and the TXEN signal echoes on the RX_DV pin.

SQE Enable Mode

Setting bit 5 of the 10BASE-T register enables SQE mode. Clearing disables it. This bit is valid only during 10BASE-T operation.

10BASE-T No Dribble

When bit 4 of the 10BASE-T register is set, the PHY rounds down to the nearest nibble when dribble bits are present on the 10BASE-T input stream.

Shadow Register Select

The 10BASE-T register provides access to 8 registers using shadow technique. The lower 3 bits written define the set of 13 upper bits used in accordance with Table 42 on page cxxvi, defined under bits [2:0]. See the note on “1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register” on page cxxiii describing reading from and writing to register 18h.

The register set previously shown is for 10BASE-T operation, obtained when the lower 3 bits are 001.

1000BASE-T/100BASE-TX/10BASE-T Power/MII Control

Table 43: 1000BASE-T/100BASE-TX/10BASE-T Power/MII Control Register (Address 18h, Shadow Value 010)

Bit	Name	R/W	Description	Default
15:7	Reserved	R/W	Write as 00Eh, ignore on read	00Eh
6	Low-Power Driver	R/W	1= Low power output driver 0 = High performance output driver	Media Converter = 1 Other modes = 0
5	Super Isolate (Copper only)	R/W	1 = Isolate mode with no link pulses transmitted 0 = Normal operation	0
4:3	Reserved	R/W	Write as 00, ignore on read	00
2:0	Shadow Register Select	R/W	000 = Auxiliary Control register 001 = 10BASE-T register 010 = Power/MII Control register 011 = Reserved 100 = Misc Test register 101 = Reserved 110 = Reserved 111 = Misc Control register	010

Low-Power Driver

When the device is strapped for media converter mode, the default value is set to 1. For other modes, it is set to 0. In Media Converter, the device is set for low-power mode. High-performance mode has a 40% greater cable reach than low-power mode. Setting bit 6 to 0 places the device in high-performance mode.

Super Isolate (Copper Only)

Setting bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T Power/MII Control register places the BCM5482S into the super isolate mode. Similar to the isolate mode, all RGMII inputs are ignored and all RGMII outputs are tristated. All link pulses are suppressed.

Shadow Register Select

The 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control register provides access to 8 registers using a shadow technique. The lower 3 bits written define the set of 13 upper bits used in accordance with the table defined under bits [2:0] above. See the note in "1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page cxxiii describing reading from and writing to register 18h.

The register set previously shown is for power/MII control, obtained when the lower 3 bits are 010.

1000BASE-T/100BASE-TX/10BASE-T Misc Test Register

Table 44: 1000BASE-T/100BASE-TX/10BASE-T Misc Test Register (Address 18h, Shadow Value 100)

Bit	Name	R/W	Description	Default
15	Lineside [Remote] Loopback Enable	R/W	1 = Enable lineside [remote] loopback from MDI (cable end) receive packet, through PCS and back to MDI transmit packet. 0 = Disable loopback	0
14:12	Reserved	R/W	Write as 000, ignore on read	000
11	Lineside [Remote] Loopback Tristate	R/W	1 = Tristate the receive RGMII pins (RX_DV, RXD, and so forth) when lineside [remote] loopback is enabled 0 = Lineside [remote] loopback packets appear on RGMII	0
10:5	Reserved	R/W	Write as 00h, ignore on read	00h
4	Swap RX MDIX	R/W	1 = RX and TX operate on same pair 0 = Normal operation	0
3	10BASE-T Halfout	R/W	1 = Transmit 10BASE-T at half amplitude 0 = Normal operation	0
2:0	Shadow Register Select	R/W	000 = Auxiliary Control register 001 = 10BASE-T register 010 = Power/MII Control register 011 = Reserved 100 = Misc Test register 101 = Reserved 110 = Reserved 111 = Misc Control register	100

Lineside [Remote] Loopback Enable

Setting bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Misc Test register enables lineside (remote) loopback of the copper receive packet back out through the MDI transmit path.

Lineside [Remote] Loopback Tristate

Setting this bit tristates the receive RGMII pins when the device is in lineside (remote) loopback mode.

Swap RX MDIX

When bit 4 of the Misc Test register is set to 1, the transmitter and receiver operate on the same twisted pair. This function is for use in a test mode where the transmitter output is detected by the receiver attached to the same pair.

10BASE-T Halfout

When operating in 10BASE-T mode, setting bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T Misc Test register to 1 reduces the output of the transmitter to half of its normal amplitude. Clearing this bit restores full amplitude operation. This function is used in a test mode where an unterminated output generates a signal with twice the amplitude of a terminated output.

Shadow Register Select

The Misc Test register provides access to 8 registers using a shadow technique. The lower 3 bits written define the set of 13 upper bits used in accordance with Table 44 on page cxxx under bits [2:0]. See the note on "1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page cxxiii describing reading from and writing to register 18h.

The register set previously shown is for miscellaneous testing, obtained when the lower 3 bits are 100.

1000BASE-T/100BASE-TX/10BASE-T Misc Control

Table 45: 1000BASE-T/100BASE-TX/10BASE-T Misc Control Register (Address 18h, Shadow Value 111)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable (Bits 11:3)	R/W SC	1 = Write bits [14:0] 0 = Only write bits [14:12] and [2:0]	0
14:12	Shadow Register Read Selector	R/W	000 = Normal operation 001 = 10BASE-T register 010 = Power Control register 011 = Reserved 100 = Misc Test register 101 = Reserved 110 = Reserved 111 = Misc Control register These bits are written when bit 15 is not set. This sets the shadow value for address 18h register read.	000
11	Packet Counter Mode	R/W	1 = Receive packet counter 0 = Transmit Packet counter	0
10	Reserved	R/W	Write as 0, ignore on read	0
9	Force Auto-MDIX Mode	R/W	1 = Auto-MDIX is enabled when auto-negotiation is disabled 0 = Auto-MDIX is disabled when auto-negotiation is disabled	0
8	RGMII Timing Mode	R/W	1 = RGMII RXC delayed timing mode 0 = RGMII RXC/RXD aligned timing mode	(Invert (INTFSEL[1]))
7	Reserved	R/W	Reserved	(Invert (INTFSEL[1]))

Table 45: 1000BASE-T/100BASE-TX/10BASE-T Misc Control Register (Address 18h, Shadow Value 111) (Cont.)

Bit	Name	R/W	Description	Default
6	RGMII RX_DV Mode	R/W	1 = Mux RX_ER with RX_DV in RGMII mode 0 = Mux CRS with RX_DV in RGMII mode	1
5	RGMII Out-of-Band Status Disable	R/W	1 = Send regular data during IPG 0 = Send out-of-band status information in RGMII mode	1
4	Ethernet@WireSpeed Enable	R/W	1 = Enable Ethernet@WireSpeed 0 = Disable Ethernet@WireSpeed	1
3	MDIO All PHY Select	R/W	1 = All PHY selected during MDIO writes when PHY Address = 00000 0 = Normal operation	0
2:0	Shadow Register Select	R/W	000 = Auxiliary register 001 = 10BASE-T register 010 = Power Control register 011 = Reserved 100 = Misc Test register 101 = Reserved 110 = Reserved 111 = Misc Control register	111

Write Enable (Bits 11:3)

If bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Misc Control register is set when writing to this register, then bits [11:3] of this register can be modified. Bits [2:0] and [14:12] can always be written regardless of the state of bit 15. When this bit is set, bits [11:3] are written. When this bit is cleared, only bits [14:12] and [2:0] are written.

Shadow Register Read Selector

Bits [14:12] of the 1000BASE-T/100BASE-TX/10BASE-T Misc Control register are written, regardless of the value of bit 15. These bits determine the shadow value for an MII register 18h read operation. See the note in "1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register" on page cxxiii describing reading from and writing to register 18h.

Packet Counter Mode

Bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Misc Control register sets the packet counter mode in Expansion register 00h. The counter counts the receive packet when this bit is set; otherwise, it counts the transmit packet.

Force Auto-MDIX Mode

Bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T Misc Control register enable the auto-MDIX mode while auto-negotiation is disabled. The default setting disables the auto-MDIX function when auto-negotiation is disabled.

RGMII Timing Mode

Bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T Misc Control register adjusts the RGMII (RX_DV/RXD[3:0]-to-RXC) timing in the RGMII-to-copper and RGMII-to-fiber mode. When this bit is cleared, the RXC to RXD[3:0] timing is aligned. When this bit is set, the RXC is delayed 1.9 ns with respect to the RXD[3:0].

RGMII RX_DV Mode

If bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T Misc Control register is set in RGMII mode, RX_ER is multiplexed with RX_DV. If this bit is cleared, CRS is multiplexed with RX_DV.

RGMII Out-of-Band Status (OOBS) Disable

If bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T Misc Control register is 0 in RGMII mode, OOBS is sent during IPG. If this bit is set, the BCM5482S operates normally during IPG.

Ethernet@WireSpeed Enable

When bit 4 = 1, Ethernet@WireSpeed mode is enabled. If the link cannot be established within two to nine attempts (the number of attempts is set by bits[4:2] in register 1Ch, shadow value 00100), the BCM5482S downgrades its advertised abilities and again tries to establish a link. When bit 4 is cleared, it advertises its abilities according to registers 04h and 09h.

MDIO All PHY Select

When bit 3 of the Misc Control register is set, an MDIO write operation with PHY Address = 00000 affects all four ports in the device.

Shadow Register Select

Using a shadow technique, the 1000BASE-T/100BASE-TX/10BASE-T Misc Control register provides access to 8 registers. The lower 3 bits written define which set of 13 upper bits are used in accordance with Table 45 on page cxxxi, defined under bits 2:0.

See the note about the “1000BASE-T/100BASE-TX/10BASE-T Auxiliary Control Shadow Value Access Register” on page cxxiii describing reading from and writing to register 18h. The register set previously shown is for miscellaneous control, obtained when the lower 3 bits are 111.

1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary

Table 46: 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary Register (Address 19h)

Bit	Name	R/W	Description	Default
15	Auto-negotiation Complete	RO	1 = Auto-negotiation complete 0 = Auto-negotiation in progress	0
14	Auto-negotiation Complete Acknowledge	RO LH	1 = Entered auto-negotiation link good check state 0 = State not entered since last read	0
13	Auto-negotiation Acknowledge Detect	RO LH	1 = Entered auto-negotiation acknowledge detect state 0 = State not entered since last read	0
12	Auto-negotiation Ability Detect	RO LH	1 = Entered auto-negotiation ability detect state 0 = State not entered since last read	0
11	Auto-negotiation Next Page Wait	RO LH	1 = Entered auto-negotiation Next Page wait state 0 = State not entered since last read	0
10:8	Auto-negotiation HCD (Current Operating Speed and Duplex Mode)	RO	111 = 1000BASE-T full-duplex[a] 110 = 1000BASE-T half-duplex[a] 101 = 100BASE-TX full-duplex[a] 100 = 100BASE-T4 011 = 100BASE-TX half-duplex[a] 010 = 10BASE-T full-duplex[a] 001 = 10BASE-T half-duplex[a] 000 = No highest common denominator or auto-negotiation not complete When the auto-negotiation function has been disabled, bits[10:8] report the manually selected mode of operation when Register 18h, shadow value 111, bit 9 = 0. If auto-negotiation is disabled and Register 18h, shadow value 111, bit 9 = 1, then bits [10:8] = 000.	000
7	Parallel Detection Fault	RO LH	1 = Parallel link fault detected 0 = Parallel link fault not detected	0
6	Remote Fault	RO	1 = Link partner has detected remote fault 0 = Link partner has not detected remote fault	0
5	Auto-negotiation Page Received	RO LH	1 = New page has been received from link partner 0 = New page has not been received	0
4	Link Partner Auto-negotiation Ability	RO	1 = Link partner has auto-negotiation capability 0 = Link partner does not perform auto-negotiation	0

Table 46: 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary Register (Address 19h) (Cont.)

Bit	Name	R/W	Description	Default
3	Link Partner Next Page Ability	RO	1 = Link partner has Next Page capability 0 = Link partner does not have Next Page capability	0
2	Link Status	RO	1 = Link is up (link pass state) 0 = Link is down (link fail state)	0
1	Pause Resolution—Receive Direction	RO	1 = Enable pause receive 0 = Disable pause receive	0
0	Pause Resolution—Transmit Direction	RO	1 = Enable pause transmit 0 = Disable pause transmit	0

a. Indicates the negotiated HCD when auto-negotiation enable = 1, or indicates the manually selected speed and duplex mode when auto-negotiation enable = 0.

Auto-negotiation Complete

When auto-negotiation is complete, the BCM5482S returns 1 in bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register. This bit returns 0 while auto-negotiation is in progress.

Auto-negotiation Complete Acknowledge

The BCM5482S returns 1 in bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the auto-negotiation state machine has entered the link good check state since the last time this register was read; otherwise, it returns 0.

Auto-negotiation Acknowledge Detect

The BCM5482S returns 1 in bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the auto-negotiation state machine has entered the acknowledge detect state since the last time this register was read; otherwise, it returns 0.

Auto-negotiation Ability Detect

The BCM5482S returns 1 in bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the auto-negotiation state machine has entered the ability detect state since the last time this register was read; otherwise, it returns 0.

Auto-negotiation Next Page Wait

The BCM5482S returns 1 in bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the auto-negotiation state machine has entered the Next Page wait state since the last time this register was read; otherwise, it returns 0.

Auto-negotiation HCD (Current Operating Speed and Duplex Mode)

Bits [10:8] of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register report the mode of operation negotiated between the BCM5482S and its link partner. As reported by bit 15 of the Auxiliary Status Summary register, the bits return **000** until auto-negotiation has completed. When the auto-negotiation function has been disabled, bits [10:8] report the manually selected mode of operation.

Parallel Detection Fault

When a parallel detection fault has occurred in the auto-negotiation state machine, bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register returns 1. When a parallel detection fault occurs, this bit is latched to 1 and remains so until the next register read. This bit returns 0 when a parallel detection fault has not occurred since the last time it was read.

Remote Fault

The BCM5482S returns 1 in bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the link partner has detected a remote fault; otherwise, it returns 0.

Auto-negotiation Page Received

The BCM5482S returns 1 in bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when a new link code word has been received from the link partner since the last time this register was read; otherwise, it returns 0.

Link Partner Auto-negotiation Ability

The BCM5482S returns 1 in bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the link partner is known to have auto-negotiation capability. Before any auto-negotiation information is exchanged or if the link partner does not comply with IEEE auto-negotiation, the bit returns 0.

Link Partner Next Page Ability

The BCM5482S returns 1 in bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the link partner needs to transmit Next Page information; otherwise, it returns 0.

Link Status

The BCM5482S returns 1 in bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register when the link status is good; otherwise, it returns 0.

Pause Resolution—Receive Direction and Transmit Direction

When auto-negotiation has completed, the BCM5482S returns the result of the pause resolution function for full-duplex flow control on bits [1:0] of the 1000BASE-T/100BASE-TX/10BASE-T Auxiliary Status Summary register. When bit 1 returns 1, the link partner can send pause frames toward the local device. When bit 0 returns 1, pause frames can be transmitted by the local device to the link partner. These bits are only guaranteed to be valid when bit 15 of the Auxiliary Status Summary register is 1.

1000BASE-T/100BASE-TX/10BASE-T Interrupt Status

Table 47: 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status Register (Address 1Ah)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Signal Detect/Energy Detect Change	RO LH	1 = Filtered fiber signal detect change or energy detect change since last read (enabled by register 1Ch, shadow 00101, bit 5 = 1) 0 = Interrupt cleared	0
14	Illegal Pair Swap	RO LH	1 = Illegal pair swap detected 0 = Interrupt cleared	0
13	MDIX Status Change	RO LH	1 = MDIX status changed since last read 0 = Interrupt cleared	0
12	Exceeded High Counter Threshold	RO	1 = Value in one or more counters is above 32K 0 = All counters below 32K	0
11	Exceeded Low Counter Threshold	RO	1 = Value in one or more counters is above 128K 0 = All counters below 128K	0
10	Auto-negotiation Page Received	RO LH	1 = Page received since last read 0 = Interrupt cleared	0
9	No HCD Link	RO LH	1 = Negotiated HCD, did not establish link 0 = Interrupt cleared	0
8	No HCD	RO LH	1 = Auto-negotiation returned HCD = none 0 = Interrupt cleared	0
7	Negotiated Unsupported HCD	RO LH	1 = Auto-negotiation HCD not supported by BCM5482S 0 = Interrupt cleared	0
6	Scrambler Synchronization Error	RO LH	1 = Scrambler synchronization error occurred since last read 0 = Interrupt cleared	0
5	Remote Receiver Status Change	RO LH	1 = Remote receiver status changed since last read 0 = Interrupt cleared	0
4	Local Receiver Status Change	RO LH	1 = Local receiver status changed since last read 0 = Interrupt cleared	0
3	Duplex Mode Change	RO LH	1 = Duplex mode changed since last read 0 = Interrupt cleared	0

Table 47: 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status Register (Address 1Ah) (Cont.)

Bit	Name	R/W	Description	Default
2	Link Speed Change	RO LH	1 = Link speed changed since last read 0 = Interrupt cleared	0
1	Link Status Change	RO LH	1 = Link status changed since last read 0 = Interrupt cleared	0
0	CRC Error	RO LH	1 = CRC error occurred since last read 0 = Interrupt cleared	0

The INTR output is asserted when any bit in 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register is set and the corresponding bit in the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask register is cleared.

Signal Detect/Energy Detect Change

This bit indicates that the fiber SD or the copper ED has changed since the last read.

Illegal Pair Swap

The BCM5482S returns 1 in bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when an uncorrectable pair swap error on the twisted-pair cable has been detected since the last time this register was read; otherwise, it returns 0.

MDIX Status Change

The BCM5482S returns 1 in bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when a link pulse or 100BASE-TX carrier was detected on a different pair than previously detected since the last time this register was read; otherwise, it returns 0.

Exceeded High Counter Threshold

The BCM5482S returns 1 in bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when one or more of the counters in registers 12–14h is above 32 000; otherwise, it returns 0.

Exceeded Low Counter Threshold

The BCM5482S returns 1 in bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when one or more of the counters in registers 12–14h is above 128 000; otherwise, it returns 0.

Auto-negotiation Page Received

The BCM5482S returns 1 in bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when a new link code word has been received from the link partner since the last time this register was read; otherwise, it returns 0.

No HCD Link

When the negotiated HCD is not able to establish a link, bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register returns 1 by the BCM5482S. The bit is cleared when the register is read.

No HCD

When auto-negotiation returns no HCD, bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register returns 1 by the BCM5482S. The bit is cleared when the register is read.

Negotiated Unsupported HCD

When the auto-negotiation HCD is not supported by the BCM5482S, bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register returns 1. The BCM5482S does not support 100BASE-T4. The bit is cleared when the register is read.

Scrambler Synchronization Error

The BCM5482S returns 1 in bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when a scrambler synchronization error has been detected since the last time this register was read; otherwise, it returns 0.

Remote Receiver Status Change

The BCM5482S returns 1 in bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when the remote receiver status has changed since the last time this register was read; otherwise, it returns 0.

Local Receiver Status Change

The BCM5482S returns 1 in bit 4 of the Interrupt Status register when the local receiver status has changed since the last time this register was read; otherwise, it returns 0.

Duplex Mode Change

The BCM5482S returns 1 in bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when the duplex mode has changed since the last time this register was read; otherwise, it returns 0.

Link Speed Change

The BCM5482S returns 1 in bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when the link speed has changed since the last time this register was read; otherwise, it returns 0.

Link Status Change

The BCM5482S returns 1 in bit 1 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when the link status has changed since the last time this register was read; otherwise, it returns 0.

CRC Error

The BCM5482S returns 1 in bit 0 of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Status register when a receive CRC error has been detected since the last time this register was read; otherwise, it returns 0.

1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask

Table 48: 1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask Register (Address 1Bh)

Bit	Name	R/W	Description	Default
15	Signal Detect/Energy Detect Change	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1
14	Illegal Pair Swap	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1
13	MDIX Status Change	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1
12	Exceeded High Counter Threshold	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1
11	Exceeded Low Counter Threshold	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1
10	Auto-negotiation Page Received	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1
9	HCD No Link	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1
8	No HCD	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1
7	Negotiated Unsupported HCD	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1

Table 48: 1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask Register (Address 1Bh)

Bit	Name	R/W	Description	Default
6	Scrambler Synchronization Error	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1
5	Remote Receiver Status Change	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1
4	Local Receiver Status Change	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1
3	Duplex Mode Change	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1
2	Link Speed Change	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1
1	Link Status Change	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1
0	CRC Error	R/W	1 = Interrupt masked, status bits operate normally 0 = Interrupt enabled, status bits operate normally	1

Interrupt Mask Vector

When bit *n* of the 1000BASE-T/100BASE-TX/10BASE-T Interrupt Mask register is written to 1, the interrupt corresponding to the same bit in the Interrupt Status register is masked. The status bits still operate normally when the interrupt is masked, but do not generate an interrupt output. When the bit is written to 0, the interrupt is unmasked.

1000BASE-T/100BASE-TX/10BASE-T Register 1Ch Access

Reading and writing to the 1000BASE-T/100BASE-TX/10BASE-T register 1Ch is through register 1Ch bits [15:10]. Bits [14:10] set the shadow value of register 1Ch, and bit 15 enables the writing of the bits [9:0]. Setting bit 15 allows writing to bits [9:0] of register 1Ch. To read register 1C shadow zzzzz, set writes to register 1Ch with bit 15 = 0, and bits 14:10 to zzzzz first. The subsequent register read from register 1Ch contains the shadow zzzzz register value. The register 1Ch shadow values are listed in Table 49.

Table 49: 1000BASE-T/100BASE-TX/10BASE-T Register 1Ch Shadow Values

Shadow Value	*Register Name*
00010	”1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 Register (Address 1Ch, Shadow Value 00010)” on page cxliii
00011	”1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control Register (Address 1Ch, Shadow Value 00011)” on page cxliv
00100	”1000BASE-T/100BASE-TX/10BASE-T Spare Control 2 Register (Address 1Ch, Shadow Value 00100)” on page cxlv
00101	”1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 Register (Address 1Ch, Shadow Value 00101)” on page cxlvi
01000	”1000BASE-T/100BASE-TX/10BASE-T LED Status Register (Address 1Ch, Shadow Value 01000)” on page cxlviii
01001	”1000BASE-T/100BASE-TX/10BASE-T LED Control Register (Address 1Ch, Shadow Value 01001)” on page cl
01010	”Auto Power-Down Register (Address 1Ch, Shadow Value 01010)” on page cli
01101	”1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 Register (Address 1Ch, Shadow Value 01101)” on page cliii
01110	”1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 Register (Address 1Ch, Shadow Value 01110)” on page clv
01111	”1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status Register (Address 1Ch, Shadow Value 01111)” on page clvi
10011	”SerDes 100BASE-FX Control Register (Address 1Ch, Shadow Value 10011)” on page clx
10101	”SGMII Slave Register (Address 1Ch, Shadow Value 10101)” on page clxiv
11000	”1000BASE-X Auto-Detect SGMII/Media Converter Register (Address 1Ch, Shadow Value 11000)” on page clxviii
11010	”1000BASE-X Auto-negotiation Debug Register (Address 1Ch, Shadow Value 11010)” on page clxix
11011	”Auxiliary 1000BASE-X Control Register (Address 1Ch, Shadow Value 11011)” on page clxxii
11100	”Auxiliary 1000BASE-X Status Register (Address 1Ch, Shadow Value 11100)” on page clxxiii
11101	”Misc 1000BASE-X Status Register (Address 1Ch, Shadow Value 11101)” on page clxxvi
11110	”Copper/Fiber Auto-Detect Medium Register (Address 1Ch, Shadow Value 11110)” on page clxxvii
11111	”Mode Control Register (Address 1Ch, Shadow Value 11111)” on page clxxix

1000BASE-T/100BASE-TX/10BASE-T Spare Control 1

1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 is enabled by register 1Ch with the shadow value in bits [14:10] = 00010.

Table 50: 1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 Register (Address 1Ch, Shadow Value 00010)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	00010 = Spare Control 1 register	00010
9:5	Reserved	R/W	Write as 00h, ignore when read.	00h
4	Reserved	R/W	Write as 00h, ignore when read.	0
3	Reserved	R/W	Write as 00h, ignore when read.	00h
2	Bicolor Link Speed Led Mode	R/W	1 = enable Bicolor Link Speed led mode. LINKSPD[1:0] = speed 10 = 1000BASE-T 01 = 100BASE-T 11 = auto-negotiation, 10BASE-T	0
1	Reserved	R/W	Write as 00h, ignore when read.	00h
0	Link LED Mode	R/W	1 = Enable link LED mode LINKSPD[2:1] = speed 00: 1000BASE-T link 01: 100BASE-TX link 10: 10BASE-T link or no link SLAVE = Active low 10/100/1000BASE-T link 0 = Normal link LED mode	0

Write Enable

During a write to this register, setting Spare Control 1 register bit 15 to 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 00010 to enable a read/write to the 1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 register address 1Ch.

Link LED Mode

Bit 0 of 1000BASE-T/100BASE-TX/10BASE-T Spare Control 1 register 1Ch with shadow value 00010 selects the link LED mode. When this bit is set, it enables the link LED mode. The LINKSPD2/LINKSPD1 are Link/Speed LED and SLAVE LED is LINK LED to indicate a link for 10BASE-T, 100BASE-TX, or 1000BASE-T. When this bit is cleared, LINKSPD2, LINKSPD1, and SLAVE are in normal mode.

1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control

1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control is enabled by register 1Ch with shadow value in bits [14:10] = 00011.

Table 51: 1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control Register (Address 1Ch, Shadow Value 00011)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	00011 = Clock Alignment Control register	00011
9	GTXCLK Clock Delay Enable	R/W	1 = Enable GTXCLK delay 0 = Normal mode (bypass GTXCLK delay)	1
8:0	Reserved	R/W	Write as 000h, ignore when read.	000h

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T Clock Alignment register bit 15 to 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 00011 to enable a read/write to the Clock Alignment Control register address 1Ch.

GTXCLK Clock Delay Enable

Setting Bit 9 of 1000BASE-T/100BASE-TX/10BASE-T Clock Alignment Control register 1Ch with shadow value 00011 enables the GTXCLK internal delay. When this bit is cleared, the GTXCLK delay is bypassed.

1000BASE-T/100BASE-TX/10BASE-T Spare Control 2

1000BASE-T/100BASE-TX/10BASE-T Spare Control 2 is enabled by register 1Ch with shadow value in bits [14:10] = 00100.

Table 52: 1000BASE-T/100BASE-TX/10BASE-T Spare Control 2 Register (Address 1Ch, Shadow Value 00100)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	00100 = Spare Control 2 register	00100
9:6	Reserved	R/W	Write as 00h, ignore when read.	00h
5	Enable rbc0/1 and txc/rxc Tristate	R/W	1 = Enable tristating of the rbc0/1 & txc/rxc 0 = Disable tristating of the rbc0/1 & txc/rxc	
4 3 2	Ethernet@WireSpeed Retry Limit	RO	000 = Downgrade after two failed auto-negotiation attempts 001 = Downgrade after three failed auto-negotiation attempts 010 = Downgrade after four failed auto-negotiation attempts 011 = Downgrade after five failed auto-negotiation attempts 100 = Downgrade after six failed auto-negotiation attempts 101 = Downgrade after seven failed auto-negotiation attempts 110 = Downgrade after eight failed auto-negotiation attempts 111 = Downgrade after nine failed auto-negotiation attempts	0 1 1
1	Energy Detect on INTR Pin	R/W	1 = Routes Energy Detect to interrupt signal. Use LED selectors (register 1Ch shadow 01101 and 01110) and program to INTR mode. 0 = INTR pin is Interrupt function.	0
0	Reserved	R/W	Write as 0, ignore when read.	0

Write Enable

During a write to this register, setting bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Spare Control 2 register allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] must be set to 00100 to enable a read/write to the 1000BASE-T/100BASE-TX/10BASE-T Spare Control 2 register.

Ethernet@WireSpeed Retry Limit

Bits [4:2] set the number of auto-negotiation attempts to link up prior to speed downgrade. The Ethernet@WireSpeed mode must be enabled for these bits to work.

Energy Detect on INTR Pin

Bit 1 enables the signal detect or energy detect input on the INTR pin. Set the LED selector register to enable INTR LED mode (1Ch shadow 01101 or 01110 set bit [7:4]/[3:0] to 0110 depending on the LED).

1000BASE-T/100BASE-TX/10BASE-T Spare Control 3

1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 is enabled by register 1Ch with shadow value in bits [14:10] = 00101.

Table 53: 1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 Register (Address 1Ch, Shadow Value 00101)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	00101 = Spare Control 3 register	00101
9	Reserved	R/W	Write as 0, ignore when read	0
8	TXC/RXC Disable During Auto Power-Down	R/W	1 = Disable TXC/RXC during auto power-down when there is no energy on the cable	0
7	Reserved	R/W	Write as 0h, ignore when read	07
6	TXC Disable	R/W	1 = Disable TXC clock	0
5	Signal Detect/Energy Detect Enable	R/W	1 = Enable Interrupt register for Signal Detect/Energy Detect	0
4:2	Reserved	R/W	Write as 07h, ignore when read	07
1	CLK125 Auto Power-Down	R/W	1 = Auto power down of CLK125 is disabled 0 = Auto power down of CLK125 is enabled	1
0	CLK125 Output	R/W	1 = Enable CLK125 output 0 = Disable CLK125 output	1

Write Enable

During a write to this register, setting bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 register allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow register values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Register bits [14:10] must be set to 00101 to enable a read/write to the 1000BASE-T/100BASE-TX/10BASE-T Spare Control 3 register.

TXC/RXC Disable During Auto Power-Down

A 1 disables TXC/RXC during auto power-down when there is no energy on the cables.

TXC Disable

Setting this bit disables TXC clock.

Signal Detect/Energy Detect Enable

Setting this bit enables the Interrupt register for Signal Detect/Energy detect.

CLK125 Auto Power-Down

Clearing this bit enables the auto power-down mode of the CLK125 output. This feature enables additional power savings. This feature should only be used during auto power-down mode.

CLK125 Output

Setting this bit enables the CLK125 output; clearing this bit disables the CLK125 output.

1000BASE-T/100BASE-TX/10BASE-T LED Status

The LED status is enabled by 1000BASE-T/100BASE-TX/10BASE-T register 1Ch with shadow value in bits [14:10] = 01000.

Table 54: 1000BASE-T/100BASE-TX/10BASE-T LED Status Register (Address 1Ch, Shadow Value 01000)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01000 = LED Status register	01000
9	Reserved	R/O	Write as 0, ignore when read.	0
8	$\overline{\text{Slave}}$ Indicator	RO	1 = Master mode 0 = Slave mode	0
7	$\overline{\text{FDX}}$ Indicator	RO	1 = Half-duplex mode 0 = Full-duplex mode	0
6	$\overline{\text{INTR}}$ Indicator	RO	1 = No active Interrupt 0 = Interrupt activated	0
5	Reserved	RO	Write as 0, ignore when read.	0
4:3	$\overline{\text{LINKSPD}}$ Indicator	RO	11 = No link 10 = 10BASE-T LINK 01 = 100BASE-TX LINK 00 = 1000BASE-T LINK	00
2	$\overline{\text{Transmit}}$ Indicator	RO	1 = No transmit activity 0 = Transmit activity	0
1	$\overline{\text{Receive}}$ Indicator	RO	1 = Not receive activity 0 = Receive activity	0
0	$\overline{\text{Quality}}$ Indicator	RO	1 = Quality not good mode 0 = Quality good mode	0

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 15 to 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains in bits [9:0] the preferred shadow register values.

Shadow Register Selector

Bits [14:10] of this register must be set to 01000 to enable a read/write to the 1000BASE-T/100BASE-TX/10BASE-T LED Status register.

Slave Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 8 returns 0, the device is in the slave mode. When this bit returns 1, the device is not in the slave mode.

FDX Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 7 returns 0, the device is in the full-duplex mode. When this bit returns 1, the device is not in the full-duplex mode.

INTR Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 6 returns 0, the device is in interrupt mode. When this bit returns 1, the device is not in interrupt mode.

LINKSPD Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bits [4:3] return 00, the device is in the 1000BASE-TX link mode. When these bits return 01, the device is in the 100BASE-TX link mode. When these bits return 10, the device is in the 10BASE-T link mode. When these bits return an 11, the device is not linked.

Transmit Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 2 returns 0, the device is in the transmit mode. When this bit returns 1, the device is not in the transmit mode.

Receive Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 1 returns 0, the device is in receive mode. When this bit returns 1, the device is not in receive mode.

Quality Indicator

When 1000BASE-T/100BASE-TX/10BASE-T LED Status register bit 0 returns 0, the device is in quality good mode. When this bit returns 1, the device is not in quality good mode.

1000BASE-T/100BASE-TX/10BASE-T LED Control

LED Control is enabled by 1000BASE-T/100BASE-TX/10BASE-T register 1Ch with shadow value in bits [14:10] = 01001.

Table 55: 1000BASE-T/100BASE-TX/10BASE-T LED Control Register (Address 1Ch, Shadow Value 01001)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01001 = LED Control register	01001
9:6	Reserved	R/W	Write as 00000, ignore when read.	00000
5	Override Media Converter LED Mode	R/W	1 = LEDs not remapped in media converter mode. 0 = In media converter mode, LEDs mapped as follows: • LED1: RX_LOSS • LED2: LINK	0
4	Activity/Link LED Enable	R/W	1 = Drive activity/link data on $\overline{\text{ACTIVITY}}$ LED 0 = Drive activity data on $\overline{\text{ACTIVITY}}$ LED	0
3	$\overline{\text{ACTIVITY}}$ LED Enable	R/W	1 = Drive activity data on $\overline{\text{ACTIVITY}}$ LED 0 = Drive receive data on $\overline{\text{ACTIVITY}}$ LED	1
2	Remote Fault LED Enable	R/W	1 = Drive remote fault on quality LED 0 = Normal operation	0
1:0	Link Utilization LED Selector	R/W	00 = Normal activity (fixed blink rate) 01 = Transmit activity with variable blink rate 10 = Receive activity with variable blink rate 11 = Transmit/receive activity with variable blink rate ***Note:*** This mode has higher priority than the activity LED enable mode in bit 3.	00

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED Control register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 01001 to enable a read/write to the register address 1Ch.

Override Media Converter LED Mode

When bit 5 is set to 1, the LEDs following the normal configuration. When bit 5 is set to 0, media converter LED mode is invoked.

Activity/Link LED Enable

Setting 1000BASE-T/100BASE-TX/10BASE-T LED Control register bit 4 drives activity/link data on $\overline{\text{ACTIVITY}}$ LED.

$\overline{\text{ACTIVITY}}$ LED Enable

Setting 1000BASE-T/100BASE-TX/10BASE-T LED Control register bit 3 drives activity data on $\overline{\text{ACTIVITY}}$ LED. Otherwise, it drives receive data on $\overline{\text{ACTIVITY}}$ LED.

Remote Fault LED Enable

Setting 1000BASE-T/100BASE-TX/10BASE-T LED Control register bit 2 drives a Remote Fault on the Quality LED.

Link Utilization LED Selector

These bits apply to the LED programmed to the ACTIVITY mode only. In the activity LED mode, the LED expresses estimated activity in terms of blink rate. The blink rate of the LED increases as the activity duty cycle increases by increments of 10%. For duty cycles of 0.001% to10%, the LED blinks at 3 Hz. for duty cycles of 10% to 20%, at 6 Hz, and for duty cycles of 90% to 96%, at 30 Hz. Even though the frequency of the LED blink increases, the duty cycle of the LED stays at about 50%. The ACTIVITY LED can be programmed to display the following:

- 00 = Normal activity (fixed blink rate)
- 01 = Transmit activity with variable blink rate
- 10 = Receive activity with variable blink rate
- 11 = Transmit/receive activity with variable blink rate

1000BASE-T/100BASE-TX/10BASE-T Auto Power-Down

Auto Power-Down is enabled by 1000BASE-T/100BASE-TX/10BASE-T Auto Power-Down register 1Ch with shadow value in bits [14:10] = 01010.

Table 56: Auto Power-Down Register (Address 1Ch, Shadow Value 01010)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01010 = Auto Power-Down register	01010
9:6	Reserved	R/W	Write as 0h, ignore when read.	0h

Table 56: Auto Power-Down Register (Address 1Ch, Shadow Value 01010) (Cont.)

Bit	Name	R/W	Description	Default
5	Auto Power-Down Mode	R/W	1 = Auto power-down mode enabled 0 = Auto power-down mode disabled	0
4	Sleep Timer Select	R/W	1 = Sleep timer is 5.4s 0 = Sleep timer is 2.7s	0
3:0	Wake-up Timer Select	R/W	Counter for wake-up timer in units of 84 ms. 0001 = 84 ms 0010 = 168 ms ... 1111 = 1.26s	0001

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T Auto Power-Down register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Register bits [14:10] must be set to 01010 to enable a read/write to the 1000BASE-T/100BASE-TX/10BASE-T Auto Power-Down register address 1Ch.

TXC/RXC Disable During Auto Power-Down

A 1 disables TXC/RXC during auto power-down when there is no energy on the cables.

Auto Power-Down Mode

Setting this bit enables the auto power-down mode.

Sleep Timer Select

Setting this bit changes the wake-up time leaving auto power-down mode.

Wake-up Timer Select

The port continues wake-up mode for a time based on the count stored in this register. The minimum value is 84 ms and the maximum value is 1.26 sec. This only applies when the part is in auto power-down mode.

1000BASE-T/100BASE-TX/10BASE-T LED Selector 1

LED Selector 1 is enabled by 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 register 1Ch with shadow value in bits [14:10] = 01101.

External Control 2

Table 57: External Control 2 (Address 1Ch, Shadow Value 01100)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01100 = External Control 2 register	01100
9:7	Reserved	R/W	Write as 00, ignore when read.	000
6	Ultra low power mode	R/W	1 = When set, the device is in ultra low power mode. Ultra low power mode is enable through bit 6 of the port1 registers. Bit 6 in the port2 register is reserved. 0 = in normal mode	0
5:0	Reserved		Write as 00, ignore when read.	000000

Table 58: 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 Register (Address 1Ch, Shadow Value 01101)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01101 = LED Selector 1 register	01101
9:8	Reserved	R/W	Write as 00, ignore when read.	00
7:4	LED3 ($\overline{\text{LINKSPD[2]}}$) Selector	R/W	0000: $\overline{\text{LINKSPD[1]}}$ 0001: $\overline{\text{LINKSPD[2]}}$ 0010: $\overline{\text{XMITLED}}$ 0011: $\overline{\text{ACTIVITYLED}}$ 0100: $\overline{\text{FDXLED}}$ 0101: $\overline{\text{SLAVE}}$ 0110: $\overline{\text{INTR}}$ 0111: $\overline{\text{QUALITY}}$ 1000: RCVLED 1001: $\overline{\text{Reserved}}$ 1010: $\overline{\text{MULTICOLOR}}$[1] 1011: $\overline{\text{OPENSHORT}}$ 1100: Energy/Link 1101: CRS (SGMII Mode) 1110: Off (high)	00001

Table 58: 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 Register (Address 1Ch, Shadow Value 01101)

Bit	Name	R/W	Description	Default
3:0	LED1 ($\overline{\text{LINKSPD[1]}}$) Selector	R/W	0000: $\overline{\text{LINKSPD[1]}}$ 0001: $\overline{\text{LINKSPD[2]}}$ 0010: $\overline{\text{XMITLED}}$ 0011: $\overline{\text{ACTIVITYLED}}$ 0100: $\overline{\text{FDXLED}}$ 0101: $\overline{\text{SLAVE}}$ 0110: $\overline{\text{INTR}}$ 0111: $\overline{\text{QUALITY}}$ 1000: RCVLED 1001: $\overline{\text{Reserved}}$ 1010: $\overline{\text{MULTICOLOR[1]}}$ 1011: OPENSHORT 1100: Energy/LINK 1101: CRS (SGMII MODE) 1110: Off (high)	0000

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED Selector register 1 bit 15 to 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 01101 to enable a read/write to the 1000BASE-T/100BASE-TX/10BASE-T LED Selector register 1 address 1Ch.

LED3 ($\overline{\text{LINKSPD[2]}}$) Selector

Bits [7:4] of 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 register 1Ch with shadow value 01101 select the LED3 mode.

LED1 ($\overline{\text{LINKSPD[1]}}$) Selector

Bits [3:0] of 1000BASE-T/100BASE-TX/10BASE-T LED Selector 1 register 1Ch with shadow value 01101 select the LED1 mode.

1000BASE-T/100BASE-TX/10BASE-T LED Selector 2

LED Selector 2 is enabled by 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 register 1Ch with shadow value in bits [14:10] = 01110.

Table 59: 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 Register (Address 1Ch, Shadow Value 01110)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01110 = LED Selector 2 register	01110
9:8	Reserved	R/W	Write as 00, ignore when read.	00
7:4	LED2 ($\overline{\text{INTR}}$) Selector	R/W	0000: $\overline{\text{LINKSPD[1]}}$ 0001: $\overline{\text{LINKSPD[2]}}$ 0010: $\overline{\text{XMITLED}}$ 0011: $\overline{\text{ACTIVITYLED}}$ 0100: $\overline{\text{FDXLED}}$ 0101: $\overline{\text{SLAVE}}$ 0110: $\overline{\text{INTR}}$ 0111: $\overline{\text{QUALITY}}$ 1000: RCVLED 1001: $\overline{\text{Reserved}}$ 1010: $\overline{\text{MULTICOLOR[2]}}$ 1011: $\overline{\text{OPENSHORT}}$ 1100: EnergyLink 1101: CRS (SGMII Mode) 1110: Off (high)	0110
3:0	LED4 ($\overline{\text{Activity}}$) Selector	R/W	0000: $\overline{\text{LINKSPD[1]}}$ 0001: $\overline{\text{LINKSPD[2]}}$ 0010: $\overline{\text{XMITLED}}$ 0011: $\overline{\text{ACTIVITYLED}}$ 0100: $\overline{\text{FDXLED}}$ 0101: $\overline{\text{SLAVE}}$ 0110: $\overline{\text{INTR}}$ 0111: $\overline{\text{QUALITY}}$ 1000: RCVLED 1001: $\overline{\text{Reserved}}$ 1010: $\overline{\text{MULTICOLOR[2]}}$ 1011: $\overline{\text{OPENSHORT}}$ 1100: EnergyLink 1101: CRS (SGMII Mode) 1110: Off (high)	0011

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 register bit 15 to 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 01110 to enable a read/write to the 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 register address 1Ch.

LED2 ($\overline{\text{INTR}}$) Selector

Bits [7:4] of 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 register 1Ch with shadow value 01110 select the LED2 mode.

LED4 ($\overline{\text{Activity}}$) Selector

Bits [3:0] of 1000BASE-T/100BASE-TX/10BASE-T LED Selector 2 register 1Ch with shadow value 01110 select the LED3 mode.

1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status

1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status is enabled by register 1Ch with shadow value in bits [14:10] = 01111.

Table 60: 1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status Register (Address 1Ch, Shadow Value 01111)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	01111 = LED GPIO Control/Status register	01111
9:8	Reserved	R/W	Write as 00, ignore when read.	00
7:4	LED I/O Status	RO	Bit 7: LED2 pin status Bit 6: Reserved Bit 5: Reserved Bit 4: LED1 pin status 1 = LED pin is an input 0 = LED pin is an output	0h

Table 60: 1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status Register (Address 1Ch, Shadow Value 01111) (Cont.)

Bit	Name	R/W	Description	Default
3:0	Programmable LED I/O Control	R/W	Bit 3: LED2 pin control Bit 2: Reserved Bit 1: Reserved Bit 0: LED1 pin control 1 = Disable LED output 0 = Enable LED output	0h

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register bits [14:10] must be set to 01111 to enable a read/write to the register address 1Ch.

LED I/O Status

The 1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register, bit 7 and bit 4, read back the status of the LED pin.

Programmable LED I/O Control

Setting 1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register, bit 3 and bit 0, sets the LED pin to disable LED output. Clearing LED GPIO Control/Status register, bit 3 and bit 0, sets the LED pin to enable LED output.

SerDes 100BASE-FX Status

Table 61: SerDes 100BASE-FX Status Register (Address 1Ch, Shadow Value = 10001)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0], 0 = Read bits[9:0]	0
15:9	Reserved	RO	Write as 00, ignore when read.	0000h
14:10	Shadow Register Selector	R/W	1001 selects the SerDes 100BASE-FX Status register.	1001
9	Reserved	R/W	Write as 00, ignore when read.	00
8	Bad ESD Detected (Premature End)	RO LH	1 = Bad ESD error detected since last read 0 = No error detected since last read	0
7	False Carrier Detected	RO LH	1 = False carrier detected since last read 0 = No error detected since last read	0
6	Transmit Error Detected	RO LH	1 = Received packet with txer code since last read 0 = No error detected since last read	0
5	Receive Error Detected	RO LH	1 = Receive coding error detected since last read 0 = No error detected since last read	0
4	Lock Timer Expired	RO LH	1 = Unable to lock within 730 µs since last read 0 = Condition not detected occurred since last read	0
3	Lost Lock	RO LH	1 = Lost lock since last read 0 = Lock has not been lost since last read	0
2	Faulting	RO LH	1 = Far end fault detected since last read 0 = No fault detected since last read	0
1	Locked	RO	1 = Enough idles are properly detected to lock 0 = Not locked	0
0	100FX Link (SerDes)	RO	1 = Link is up 0 = Link is down	0

Write Enable

During a write to this register, setting 1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

1000BASE-T/100BASE-TX/10BASE-T LED GPIO Control/Status register bits [14:10] must be set to 01111 to enable a read/write to the register address 1Ch.

Bad ESD Detected (Premature End)

Bit 8 indicates whether a Bad ESD error has been detected since last read.

False Carrier Detected

Bit 7 indicates whether a False carrier has been detected since last read.

Transmit Error Detected

Bit 6 indicates whether a packet with txer code has been received since last read.

Receive Error Detected

Bit 5 indicates whether a Receive coding error has been detected since last read.

Lock Timer Expired

Bit 4 indicates whether there has been an inability to lock within 730 µs of the last read.

Lost Lock

Bit 3 indicates whether there has been a Lost lock since last read.

Faulting

Bit 2 indicates whether there has been a Far end fault detected since last read.

Locked

Bit 1 indicates whether enough idles are properly detected to lock.

100FX Link (SerDes)

Bit 0 indicates whether the Link is up.

SerDes 100BASE-FX Extend Register

SerDes 100BASE-FX Extend is enabled by register 1C with shadow values in bits [14:10] = 10010.

Table 62: SerDes 100BASE-FX Extend Register

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits[9:0]	0
14:10	Shadow Register Selector	R/W	1001 selects the SerDes 100BASE-FX status register.	1001
9:4	Reserved	R/W	Write as 0, ignore when read	000
3:2	Unidirectional	R/W	11 = 100BASE-FX unidirectional enable. 00 = Normal operation	00
1:0	Reserved	R/W	Write as 0, ignore when read	00

When bit 3:2 is set to 11, the device is able to transmit without a receive section to which to link.

SerDes 100BASE-FX Control is enabled by register 1Ch with shadow value in bits [14:10] = 10011.

Table 63: SerDes 100BASE-FX Control Register (Address 1Ch, Shadow Value 10011)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	Shadow register selector.	10011
9:4	Reserved	R/W	Write as 0, ignore when read.	000
3	Far End Fault Enable	R/W	1 = Enable far-end fault 0 = Disable far-end fault	0
2	Reserved	R/W	Write as 0, ignore when read.	0
1	100BASE-FX SerDes Full-Duplex	R/W	1 = 100BASE-FX SerDes full-duplex 0 = 100BASE-FX SerDes half-duplex	1
0	100BASE-FX SerDes Enable	R/W	1 = Select RGMII-to-100BASE-FX (SerDes) 0 = Select RGMII-to-1000BASE-X	0

Write Enable

During a write to this register, setting bit 15 of the 100BASE-FX SerDes Control register allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

100BASE-FX SerDes Control register bits [14:10] must be set to 10011 to enable a read/write to the register address 1Ch.

Far End Fault Enable

Bit 3 of the 100BASE-FX SerDes Control register disables far-end fault reporting.

100BASE-FX SerDes Full-Duplex

Bit 1 of the 100BASE-FX SerDes Control register enables full-duplex when set to 1 and half-duplex when set to 0.

100BASE-FX SerDes Enable

Bit 0 of the 100BASE-FX SerDes Control register enables 100BASE-FX through the SerDes interface. Setting this bit should follow by write to 00h bit 15 = 1 and 00h bit 11 = 0. Clearing this bit should also follow by write to 00h bit 15 = 1 and 00h bit 11 = 0 to change the mode back to 1000-X/SGMII slave

Secondary SerDes Control

Secondary SerDes Control is enabled by register 1Ch with shadow value in bits [14:10] = 10100.

Table 64: Secondary SerDes Control Register (Address 1Ch, Shadow Value 10100)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	Shadow register selector	10100
9	Secondary SerDes Link Status Change	RO, LH	1 = Link status change detected since last read 0 = Link status change not detected since last read	0
8	Secondary SerDes Link	RO	1 = Link is up 0 = Link is down	0
7	Secondary SerDes Duplex	RO	1 = SerDes full-duplex 0 = SerDes half-duplex or auto-negotiating in progress	0
6	Reserved	R/W	Write as 0, ignore when read.	0
5	Secondary SerDes 100BASE-FX Full-Duplex	R/W	1 = Secondary SerDes 100BASE-FX full-duplex 0 = Secondary SerDes 100BASE-FX half-duplex	0
4	Secondary SerDes 100BASE-FX Mode	R/W	1 = Operate secondary SerDes in 100BASE-FX mode 0 = Operate secondary SerDes in 1000BASE-X mode	0
3	Secondary SerDes LED Mode	R/W	1 = Use secondary SerDes transmit, receive, and link for LEDs whenever secondary SerDes is selected via bit 0 of this register 0 = Disable secondary SerDes LED mode	0

Table 64: Secondary SerDes Control Register (Address 1Ch, Shadow Value 10100) (Cont.)

Bit	Name	R/W	Description	Default
2	Select Sync Status	R/W	1 = Use sync status from secondary SerDes for dual SerDes auto-medium detection. In 100BASE-FX mode, use secondary SerDes link status (see register 1Ch shadow 11110 [9]) 0 = Use sync status from internal SerDes for auto-medium detection. In 100BASE-FX mode, use internal SerDes link status (see register 1Ch shadow 11110 [0])	0
1	Select SD	R/W	1 = Use signal detect from pin for Secondary SerDes fiber auto-power down and PCS synchronization. 0 = Use signal detect from pin for Primary SerDes fiber auto-power down and PCS synchronization.	0
0	Secondary SerDes Select	R/W	1 = Enable the Secondary SerDes 0 = Disable the Secondary SerDes	0

Write Enable

During a write to this register, setting Secondary SerDes Control register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Register bits [14:10] of this register must be set to 10100 to enable a read/write to the Secondary SerDes Control register address 1Ch.

Secondary SerDes Link Status Change

Bit 9 of the Secondary SerDes Control register detects a link status change since last read.

Secondary SerDes Link

Bit 8 of the Secondary SerDes Control register is set to 1 when the link is up and the BCM5482S is configured in SGMII, Fiber, or 1000BASE-FX mode.

Secondary SerDes Duplex

Bit 7 of the Secondary SerDes Control register indicates the status of the full-duplex/half/duplex:

1 = SerDes full-duplex

0 = SerDes half-duplex or auto-negotiating in progress

Secondary SerDes 100BASE-FX Full-Duplex

Bit 5 of the Secondary SerDes Control register provides the status of the full-duplex/half/duplex:

1 = SerDes full-duplex

0 = SerDes half-duplex or auto-negotiating in progress

Secondary SerDes 100BASE-FX Mode

Bit 4 of the Secondary SerDes Control register enables 100BASE-FX through the SerDes interface. Setting this bit should be followed by a write to the secondary SerDes register 00h, bit 15 = 0, and the secondary SerDes register 00h, bit 11 = 0, to change the speed to 100BASE-FX. Clearing this bit should also be followed by a write to the secondary SerDes register 00h, bit 15 = 0, and the secondary SerDes register 00h, bit 11 = 0, to change the speed to 1000BASE-X (SGMII-slave).

Secondary SerDes LED Mode

Bit 3 enables the Secondary SerDes Control register transmit, receiver, and link for LEDS when the BCM5482S Secondary SerDes is enabled.

Select Sync Status

When this bit is set to 1, the device uses the sync function of the secondary SerDes for auto-detection function. When this bit is set to 0, the device uses the sync function of the primary SerDes for auto-detection function.

Select SD

When this bit is set to 1, the device uses signal detect from the pin for the secondary SerDes auto-detection function. When this bit is set to 0, the device uses signal detect from the pin for the primary SerDes auto-detection function.

Secondary SerDes Select

Bit 0 enables the secondary SerDes when the BCM5482S is configured for SGMII-to-fiber mode.

SGMII Slave

SGMII Slave is enabled by register 1Ch with shadow value in bits [14:10] = 10101.

Table 65: SGMII Slave Register (Address 1Ch, Shadow Value 10101)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	Shadow register selector	10101
9	SerDes Link	RO	1 = Link up in fiber, SGMII, or media Converter modes 0 = Link down	0
8	SerDes Duplex	RO	1 = SerDes full-duplex 0 = SerDes half-duplex or auto-negotiating in progress	1
7:6	SerDes Speed	RO	10 = SerDes speed 1000 (SGMII 1000BASE or 1000BASE-X) 01 = SerDes speed 100 (SGMII 100BASE or 100BASE-FX) 00 = SerDes speed 10 (SGMII 10) 11 = Reserved	10
5	SerDes Link Status Change	RO LH	1 = Link status change detected since last read 0 = Link status change not detected since last read	0
4:3	Mode Select	RO	00 = Copper 01 = Fiber 10 = SGMII 11 = Media converter	intf_sel[1:0]
2	RGMII-to-SGMII Slave 10/100BASE-TX FIFO Frequency Lock Mode	R/W	1 = SGMII slave 10/100 speeds transmit FIFO is frequency-locked to RGMII 0 = Normal operation	0
1	SGMII Slave Mode	R/W	1 = Enable RGMII-to-SGMII slave mode 0 = Disable SGMII slave mode	0
0	SGMII Slave Auto-Detection	R/W	1 = Enable SGMII slave auto-detection 0 = Normal operation	0

Write Enable

During a write to this register, setting bit 15 of the SGMII Slave register allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

SGMII Slave register bits [14:10] must be set to 10101 to enable a read/write to the register address 1Ch.

SerDes Link

Bit 9 of the SGMII Slave register is 1 when the link is up and the BCM5482S is in SGMII or media converter modes.

SerDes Duplex

Bit 8 of the SGMII Slave register provides the status of the full-duplex/half-duplex:

1 = SerDes full-duplex

0 = SerDes half-duplex or auto-negotiating in progress

SerDes Speed

Bits [7:6] of the SGMII Slave register provide the status of SerDes speeds:

00 = SerDes speed 10 (SGMII 10)

01 = SerDes speed 100 (SGMII 100BASE or 100BASE-FX)

10 = SerDes speed 1000 (SGMII 1000BASE or 1000BASE-X)

11 = Reserved

SerDes Link Status Change

Bit 5 of the SGMII Slave register detects a SerDes link status change since the last read.

Mode Select

Bits [4:3] of the SGMII Slave register select one of the four available interfaces:

00 = Copper

01 = Fiber

10 = SGMII

11 = Media Converter

RGMII-to-SGMII Slave 10/100 TX FIFO Frequency Lock Mode

Bit 2 of the SGMII Slave register enables the RGMII-to-SGMII slave 10/100BASE-TX FIFO frequency lock mode modes when the BCM5482S is in fiber mode.

SGMII Slave Mode

Bit 1 of the SGMII Slave register enables the SGMII slave modes when the BCM5482S is in fiber mode.

SGMII Slave Auto-Detection

Bit 0 of the SGMII Slave Auto-Detection register enables auto-detection between 1000BASE-X and SGMII slave modes based on SerDes-received auto-negotiation code word when the BCM5482S is in fiber mode.

Primary SerDes Control

Primary SerDes Control is enabled by register 1Ch with shadow value in bits [14:10] = 10110.

Table 66: Primary SerDes Control Register (Address 1C, Shadow Value = 10110)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	10110 = Secondary SerDes Control register	10110
6:9	Reserved	R/W	Write as 0, ignore on read	00h
5	Signal Detect Enable	R/W	1 = Force synchronization to fail if signal detect is not active. 0 = Synchronization will not fail by Signal Detect	1
2:4	Reserved	R/W	Write as 0, ignore on read	00h
1	SerDes Auto-Negotiation Parallel Detect Enable	R/W	11 = Turn auto-negotiation on/off to link up with link partner. Algorithm based on received code words. 00 = Disable parallel detection	1
0	Reserved	R/W	Write as 0, ignore on read	0

Write Enable

During a write to this register, setting 1000BASE-X auto-detect SGMII/Media Converter register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Register bits [14:10] must be set to 10110 to enable a read/write to the Primary SerDes Control register address 1Ch. When bit 5 is enabled, forces synchronization to fail if signal detect is not active. Disabled if register 1ch shadow 10100[1] = 0.

Signal Detect Enable

Setting this bit to 1 will force synchronization to fail if signal detect pin is not active.

SerDes Auto-Negotiation Parallel Detect Enable

Setting this bit enables parallel detection. When the Auto_Negotation bit 12 of the primary SerDes register 00h is disabled, the parallel detect function looks for a valid incoming code word on the SerDes inputs. When it receives a valid
A/N code word, it enables the Auto_Neg function of the device to attempt to link.

If Parallel Detect bit and Auto_Neg bit 12 of primary SerDes register 00h is enabled, but there is no link, the parallel detect function will turn off the A/N function and attempt to link to the link partner which is in the force mode 1000-X.

Misc 1000BASE-X Control 2

Register address [7:0] = 17h.

Table 67: Misc 1000BASE-X Control 2 Register (Address 1C, Shadow Value = 10111)

Bit	*Name*	*R/W*	*Description*	*Default*
15:7	Reserved	RO	Write as 0, ignore on read	000h
6	SerDes Transmit Disable	R/W	1 = Force all SerDes transmit data to 0 0 = Normal operation	0
5	Signal Detect Enable	R/W	1 = Force synchronization to fail if signal detect is not active. Disabled if register 1ch shadow 10100[1] = 0. 0 = Ignore signal detect pin ***Note:*** When the device is in media converter mode, the signal detect does not get disabled by this bit.	1
4	Disable Media Converter Updates From GPHY SerDes	R/W	1 = Use register 4 for SerDes auto-negotiation. Do not allow media converter updates from GPHY SerDes. 0 = Allow register 4 to update when GPHY SerDes is in GBIC mode.	0
3	Force XMIT = Data	R/W	1 = Force XMIT = data regardless of state of receive channel 0 = Normal operation	0
2:0	Reserved	RO	Write as 0, ignore on read	000

SerDes Transmit Disable

When set, bit 6 of the Misc 1000BASE-X Control 2 register forces all SerDes transmit data to 0.

Signal Detect Enable

When set, bit 5 of the Misc 1000BASE-X Control 2 register forces synchronization to fail if the signal detect is not active and is disabled if register 1ch shadow 10100[1] = 0.

Disable Media Converter Updates From GPHY SerDes

Use register 4 of the Misc 1000BASE-X Control 2 register for SerDes auto-negotiation. Do not allow media converter updates from GPHY SerDes. 0 allows register 4 to update when GPHY SerDes is in Media Converter mode.

Force XMIT = Data

Bit 3 of the Misc 1000BASE-X Control 2 register forces XMIT = data regardless of state of receive channel. For normal operation, bit 3 must be 0.

1000BASE-X Auto-Detect SGMII/Media Converter

The 1000BASE-X auto-detect SGMII/media converter is enabled by register 1Ch with shadow value in bits [14:10] = 11000.

Table 68: 1000BASE-X Auto-Detect SGMII/Media Converter Register (Address 1Ch, Shadow Value 11000)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	11000 = Auto-detect SGMII/Media Converter register	11000
9	SerDes Resolution Fault	RO	1 = Selected field mismatch 0 = No mismatch or SGMII/media Converter auto-detect mode is disabled	0
8:3	Reserved	RO	Write as 00h, ignore when read.	00h
2	1000BASE-T PCS Transmit FIFO Elasticity (SGMII/ Media Converter mode)	R/W	1= Enable jumbo packets 0= Normal Ethernet packets	1
1	SGMII 10/100BASE-T RX FIFO Frequency Lock mode	R/W	1= Enable mode 0 = No operation	0
0	SGMII/Media Converter Auto-Detect Mode Enable	R/W	1 = Enable SGMII/media converter auto-detect mode 0 = Normal operation	INTF_SEL[1]

Write Enable

During a write to this register, setting 1000BASE-X auto-detect SGMII/Media Converter register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Register bits [14:10] must be set to 11000 to enable a read/write to the 1000BASE-X auto-detect SGMII/Media Converter address 1Ch.

SerDes Resolution Fault

Bit 9 of the 1000BASE-X Auto-detect SGMII/Media Converter register indicates there is a selected field mismatch on bit 0 of the auto-negotiation base page code-word. Otherwise, it reads 0.

1000BASE-T PCS Transmit FIFO Elasticity (SGMII/Media Converter Mode)

For the SGMII/Media Converter 1000T PCS transmit FIFO:

- 0 = Supports normal packets
- 1 = Supports 10k packets in gigabit mode

SGMII 10/100BASE-T RX FIFO Frequency Lock Mode

- 0 = Normal operation
- 1 = Uses phase-delay receive FIFO instead of the frequency offset FIFO to reduce latency (switch/MAC and PHY must use same crystal.)

SGMII/Media Converter Auto-Detect Mode Enable

Setting bit 0 of the 1000BASE-X auto-detect SGMII/Media Converter register enables the SGMII/media converter auto-detect mode. This is an algorithm to detect and change the mode of operation (register 1Ch, shadow 11111, bits 2:1) to match the MAC/switch link partner automatically. When bit 0 is cleared, it is disabled.

1000BASE-X Auto-negotiation Debug

1000BASE-X Auto-negotiation Debug is enabled by register 1Ch with shadow value in bits [14:10] = 11010.

Table 69: 1000BASE-X Auto-negotiation Debug Register (Address 1Ch, Shadow Value 11010)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	11010 = 1000BASE-X Auto-negotiation Debug register	11010
9	Consistency Mismatch	RO LH	1 = Consistency mismatch occurred since last read 0 = No consistency mismatch occurred since last read	0
8	RUDI Invalid	RO LH	1 = RUDI invalid detected since last read 0 = No RUDI invalid detected since last read	0
7	Sync Status Detected	RO LH	1 = Sync status detected since last read 0 = No sync status detected since last read	0

Table 69: 1000BASE-X Auto-negotiation Debug Register (Address 1Ch, Shadow Value 11010) (Cont.)

Bit	Name	R/W	Description	Default
6	AN_Sync_Status	RO LH	1 = AN_Sync_Status has not failed since last read 0 = AN_sync_status failed since last read	0
5	Idle Detect State	RO LH	1 = Idle detect state entered since last read 0 = Idle detect state has not been entered since last read	0
4	Complete Acknowledge State	RO LH	1 = Complete acknowledge state entered since last read 0 = Complete acknowledge state has not been entered since last read	0
3	Acknowledge Detect State	RO LH	1 = Acknowledge detect state entered since last read 0 = Acknowledge detect state has not been entered since last read	0
2	Ability Detect State	RO LH	1 = Ability detect state entered since last read 0 = Ability detect state has not been entered since last read	0
1	Sync Status Failed	RO LH	1 = Sync status failed since last read 0 = Sync status has not failed since last read	0
0	AN_Enable State	RO LH	1 = AN_Enable state entered since last read 0 = AN_Enable state has not been entered since last read	0

Write Enable

During a write to this register, setting 1000BASE-X Auto-negotiation Debug register 1 bit 15 to 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] must be set to 11010 to enable a read/write to the 1000BASE-X Auto-negotiation Debug register.

Consistency Mismatch

Bit 9 of 1000BASE-X Auto-negotiation Debug register indicates a consistency mismatch occurred since last read.

RUDI Invalid

Bit 8 of 1000BASE-X Auto-negotiation Debug register indicates a RUDI (Rx_UnitData Indicate, specified in IEEE 36.2.5.1.6) invalid detected since last read.

Sync Status Detected

Bit 7 of 1000BASE-X Auto-negotiation Debug register indicates a sync status was detected since last read.

AN_Sync_Status

Bit 6 of 1000BASE-X Auto-negotiation Debug register indicates the AN_Sync_Status has not failed since last read.

Idle Detect State

Bit 5 of 1000BASE-X Auto-negotiation Debug register indicates the idle detect state entered since last read.

Complete Acknowledge State

Bit 4 of 1000BASE-X Auto-negotiation Debug register indicates the complete acknowledge state entered since last read.

Acknowledge Detect State

Bit 3 of 1000BASE-X Auto-negotiation Debug register indicates the acknowledge detect state entered since last read.

Ability Detect State

Bit 2 of 1000BASE-X Auto-negotiation Debug register indicates the ability detect state entered since last read.

Sync Status Failed

Bit 1 of 1000BASE-X Auto-negotiation Debug register indicates the sync status has failed since last read.

AN_Enable State

Bit 0 of 1000BASE-X Auto-negotiation Debug register indicates the AN_Enable state entered since last read.

Auxiliary 1000BASE-X Control

Auxiliary 1000BASE-X Control is enabled by register 1Ch with shadow value in bits [14:10] = 11011.

Table 70: Auxiliary 1000BASE-X Control Register (Address 1Ch, Shadow Value 11011)

Bit	Name	R/W	Description	Default
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	11011 = Auxiliary 1000BASE-X Control register	11011
9	Use SerDes Mode Counters	R/W	1 = Use registers 12–14h for SerDes data 0 = Normal operation	0
8:5	Reserved	R/W	Write as 04h, ignore when read	04h
4	Disable Remote Fault Sensing	R/W	1 = Disable automatic remote fault sensing of auto-negotiation resolution error and offline errors in media converter mode 0 = Normal operation	0
3	Auto-neg. Error Timer Enable	R/W	Enables auto-neg; error timer	0
2	Comma Detect Enable	R/W	1 = Enable comma detection 0 = Disable comma detection	1
1	1000BASE-X PCS Transmit, SGMII 10/100BASE-T Transmit and Receive FIFO Elasticity	R/W	1 = High elasticity to support jumbo packets (supports 10/100/1000 jumbo packets) 0 = Low elasticity (low latency)	1
0	Disable CRC Checker	R/W	1 = Disable CRC checker 0 = Enable CRC checker	1

Write Enable

During a write to this register, setting 1000BASE-X Control register bit 15 to 1 allows writing to bits [7:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 set to 0 and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 11011 to enable a read/write to the Auxiliary 1000BASE-X Control register.

Use SerDes Mode Counters

Setting bit 9 of the Auxiliary 1000BASE-X Control register enables SerDes data to be presented on register 12h–14h.

Disable Remote Fault Sensing

Setting bit 4 of the Auxiliary 1000BASE-X Control register disables automatic remote fault sensing of an auto-negotiation resolution error.

Auto-negotiation Error Timer Enable

Enables auto-negotiation error timer.

Comma Detect Enable

Setting bit 2 of Auxiliary 1000BASE-X Control register enables comma detection.

1000BASE-X PCS Transmit, SGMII 10/100BASE-T Transmit and Receive FIFO Elasticity

Setting bit 1 of Auxiliary 1000BASE-X Control register enables jumbo packet reception.

Disable CRC Checker

Setting bit 0 of Auxiliary 1000BASE-X Control register disables the CRC checker.

Auxiliary 1000BASE-X Status

Auxiliary 1000BASE-X Status is enabled by register 1Ch with shadow value in bits [14:10] = 11100.

Table 71: Auxiliary 1000BASE-X Status Register (Address 1Ch, Shadow Value 11100)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	11100 = Auxiliary 1000BASE-X Status register	11100
9	Link Status Change	RO LH	1 = Link status change has occurred since last read 0 = Link status change has not occurred since last read	0
8	SGMII Selector Mismatch	RO	1 = SGMII selector mismatch in SGMII mode 0 = Fiber, copper, media converter mode, or SGMII selector does not mismatch, or auto-negotiation is disabled	0
7	Auto-negotiation Resolution Error	RO	1 = Auto-negotiation HCD is none (no common half-duplex or full-duplex abilities) 0 = SGMII mode, or auto-negotiation disabled, or no resolution error	0

Table 71: Auxiliary 1000BASE-X Status Register (Address 1Ch, Shadow Value 11100) (Cont.)

Bit	Name	R/W	Description	Default
6:5	Link Partner Remote Fault	RO	Reflects 1000BASE-X register 05h [13:12]: 00 = No remote fault 10 = Off line 01 = Link fault 11 = Auto-negotiation error	00
4	Auto-negotiation Page Received	RO LH	1 = Page has been received since last read 0 = Page has not been received since last read	0
3	Current Operating Duplex Mode	RO	1 = Phy is operating in full-duplex mode 0 = Phy is operating in half-duplex mode (or auto-negotiation has not completed)	0
2	Link Status	RO	1 = Link is up on SerDes side 0 = Link is down on SerDes side	0
1	PAUSE Resolution—Receive Side	RO	1 = Enable pause receive 0 = Disable pause receive	0
0	PAUSE Resolution—Transmit Side	RO	1 = Enable pause transmit 0 = Disable pause transmit	0

Write Enable

During a write to this register, setting Auxiliary 1000BASE-X Status register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Bits [14:10] of this register must be set to 11100 to enable a read/write to the Auxiliary 1000BASE-X Status register

Link Status Change

Bit 9 of Auxiliary 1000BASE-X Status register indicates that the link status has changed since the last register read.

SGMII Selector Mismatch

Bit 8 of Auxiliary 1000BASE-X Status register indicates an SGMII selector mismatch in SGMII mode.

Auto-negotiation Resolution Error

Bit 7 of Auxiliary 1000BASE-X Status register indicates auto-negotiation HCD is none (no common half-duplex or full-duplex abilities).

Link Partner Remote Fault

Bits [6:5] of Auxiliary 1000BASE-X Status register indicates the link partner remote fault status reflected from 1000BASE-X register 05h bits [13:12].

Auto-negotiation Page Received

Bit 4 of Auxiliary 1000BASE-X Status register indicates auto-negotiation page has been received since last read.

Current Operating Duplex Mode

Bit 3 of Auxiliary 1000BASE-X Status register indicates the PHY is operating in full-duplex mode.

Link Status

Bit 2 of Auxiliary 1000BASE-X Status register indicates the PHY link is up on the SerDes side.

PAUSE Resolution—Receive Side

Bit 1 of Auxiliary 1000BASE-X Status register indicates receive pause resolution.

PAUSE Resolution—Transmit Side

Bit 0 of Auxiliary 1000BASE-X Status register indicates transmit pause resolution.

Misc 1000BASE-X Status

Misc 1000BASE-X Status is enabled by register 1Ch with shadow value in bits [14:10] = 11101.

Table 72: Misc 1000BASE-X Status Register (Address 1Ch, Shadow Value 11101)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	11101 = Misc 1000BASE-X Status register	11101
9:6	Reserved	RO LH	Write as 0, ignore when read.	0000
5	False Carrier Detected	RO LH	1 = False carrier detected since last read 0 = No false carriers detected since last read	0
4	CRC Error Detected	RO LH	1 = CRC Error detected since last read 0 = No CRC error detected since last read or mode is disabled via register 1Ch, shadow 11011, bit 0	0
3	Transmit Error Detected	RO LH	1 = Transmit error code detected since last read (rx_data_error state in PCS receive) 0 = No transmit error code detected since last read	0
2	Receive Error Detected	RO LH	1 = Receive error since last read (early_end state in PCS receive) 0 = No receive error since last read	0
1	Carrier Extend Error Detected	RO LH	1 = Carrier extend error since last read (extend_err state in PCS receive) 0 = No carrier extend error since last read	0
0	Early End Extension Detected	RO LH	1 = Early end extension since last read (early_end_ext state in PCS receive) 0 = No early end extension since last read	0

Write Enable

During a write to this register, setting Misc 1000BASE-X Status register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Register bits [14:10] must be set to 11101 to enable a read/write to the Misc 1000BASE-X Status register.

False Carrier Detected

Bit 5 of Misc 1000BASE-X Status register indicates a false carrier detected since the last read.

CRC Error Detected

Bit 4 of Misc 1000BASE-X Status register indicates a CRC error detected since the last read.

Transmit Error Detected

Bit 3 of Misc 1000BASE-X Status register indicates a transmit error code detected since the last read.

Receive Error Detected

Bit 2 of Misc 1000BASE-X Status register indicates a receive error code detected since the last read.

Carrier Extend Error Detected

Bit 1 of Misc 1000BASE-X Status register indicates a carrier extend error since the last read.

Early End Extension Detected

Bit 0 of Misc 1000BASE-X Status register indicates an early end extension since the last read.

Copper/Fiber Auto-Detect Medium

Copper/Fiber Auto-detect Medium is enabled by register 1Ch with shadow value in bits [14:10] = 11110.

Table 73: Copper/Fiber Auto-Detect Medium Register (Address 1Ch, Shadow Value 11110)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	11110 = Auto-detect Medium register	11110
9	Secondary SerDes Auto-detection	R/W	1 = Enable Secondary SerDes auto-detect medium (switch between SGMII-to-Fiber (SGMII Slave) and SGMII-to-Copper of the Secondary SerDes) 0 = Disable Secondary SerDes auto-detect medium	0
8	Invert Fiber Signal Detect from SD pin	R/W	1= Fiber signal detect is active low from pin. 0 =Fiber signal detect is active high from pin.	0
7	Fiber In-Use LED Mode	R/W	1 = Drive transmit LED active low when fiber is selected, inactive when copper selected 0 = Normal transmit LED operation	$\overline{\text{INTF\_SEL[1]}}$
6	Fiber LED mode	R/W	1 = Use SerDes transmit, receive, and link for LEDs whenever fiber mode is selected via register 1Ch, shadow 11111, bits [2:1] 0 = Always use copper transmit, receive, and link for LEDs regardless of the mode selected	(INTF_SEL[0]) AND $\overline{\text{(INTF\_SEL[1])}}$

Table 73: Copper/Fiber Auto-Detect Medium Register (Address 1Ch, Shadow Value 11110) (Cont.)

Bit	Name	R/W	Description	Default
5	Qualify Fiber Signal Detect with Sync Status	R/W	1 = Sync status must be set in order for the fiber signal detect to be active. 0 = Fiber signal detect from pin is used directly.	1
4:3	Reserved	R/W	Write as 0, ignore when read.	00
2	Auto-detect Media Default	R/W	1 = Fiber selected when no medium is active 0 = Copper selected when no medium is active	0
1	Auto-detect Medium Priority	R/W	1 = Fiber selected when both media are active 0 = Copper selected when both media are active	1
0	Auto-detect Medium Enable	R/W	1 = Enable auto-detect medium 0 = Disable auto-detect medium	0

Write Enable

During a write to this register, setting the Copper/Fiber Auto-detect Medium register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Register bits [14:10] of this register must be set to 11110 to enable the drive transmit LED active low when SerDes is selected; inactive when copper is selected.

Secondary SerDes Auto-Detection

Bit 9 of the Copper/Fiber Auto-Detect Medium register enables the Secondary SerDes auto-detect medium (switch between SGMII-to-Fiber (SGMII Slave) and SGMII-to-Copper of the Secondary SerDes).

Invert Fiber Signal Detect from SD Pin

Bit 8 of this register will invert the polarity of SD pin.

Fiber In-Use LED Mode

Bit 7 of the Copper/Fiber Auto-detect Medium register drives the transmit LED active low when fiber mode is selected; inactive when copper mode is selected.

Fiber LED Mode

Bit 6 of the Copper/Fiber Auto-detect Medium register enables the use SerDes transmit, receive, and link for LEDs whenever fiber mode is selected via register 1Ch, shadow 11111, bits [2:1] = 01.

Qualify Fiber Signal Detect with Sync Status

Bit 5 of the Copper/Fiber Auto-detect Medium register qualifies the signal detect pin (SD) with sync status state.

Auto-Detect Media Default

Bit 2 of the Copper/Fiber Auto-Detect Medium register enables the selection of fiber as default medium when no medium is active. Clearing this bit sets copper as the default medium.

Auto-detect Media Priority

Bit 1 of the Copper/Fiber Auto-detect Medium register enables the selection of fiber priority when both media are active. Clearing this bit sets copper as the default medium selection.

Auto-detect Media Enable

Bit 0 of the Copper/Fiber Auto-Detect Medium register enables the auto-detect media function. This function modifies register 1Ch, Shadow 11111, bits [2:1] based on the priority and default settings as well as the copper-energy detect and fiber-signal detect.

Mode Control

Mode control is enabled by register 1Ch with shadow value in bits [14:10] = 11111.

Table 74: Mode Control Register (Address 1Ch, Shadow Value 11111)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Write Enable	R/W	1 = Write bits [9:0] 0 = Read bits [9:0]	0
14:10	Shadow Register Selector	R/W	11111 = Mode Control register	11111
9	Reserved	RO	Write as 0, ignore when read.	0
8	Mode Select Change	RO LH	1 = Interface mode select status changed since last read 0 = Interface mode select status did not change since last read	0
7	Copper Link	RO	1 = Link is good on the copper interface 0 = Copper link is down	0

Table 74: Mode Control Register (Address 1Ch, Shadow Value 11111) (Cont.)

Bit	Name	R/W	Description	Default
6	SerDes Link	RO	1 = Link is good on the SerDes interface 0 = SerDes link is down	0
5	Copper Energy Detect	RO	1 = Energy detected on the copper interface 0 = Energy not detected on the copper interface	0
4	Fiber Signal Detect	RO	1 = Filtered fiber signal detect active 0 = Filtered fiber signal detect inactive	0
3	Reserved	RO	Write as 1, ignore when read.	1
2:1	Mode Select	R/W	00 = Copper 01 = Fiber 10 = SGMII 11 = Media Converter ***Note:*** The INTFSEL[1:0] pins should strap to 01 when the user wants to configure one port to RGMII-copper and the other port to SGMII/Fiber through register 1C shadow 1F.[2:1].	INTF_SEL[1:0]
0	Enable 1000BASE-X Registers	R/W	1 = Select 1000BASE-X registers for addresses 00h–0Fh 0 = Select copper registers for addresses 00h–0Fh	INTF_SEL[1:0] = 01

Write Enable

During a write to this register, setting Mode Control register bit 15 allows writing to bits [9:0] of this register. To read the values of bits [9:0], perform an MDIO write with bit 15 cleared and preferred shadow values in bits [14:10]. The next MDIO read of register address 1Ch contains the preferred shadow register values in bits [9:0].

Shadow Register Selector

Register bits [14:10] of this register must be set to 11111 to enable a read/write to the Mode Control register address 1Ch.

Mode Select Change

Bit 8 of the Mode Control register indicates that there is change in the interface mode selection (bits 2:1). Otherwise, it
reads 0.

Copper Link

Bit 7 of the Mode Control register indicates that the link status of the copper interface is up in copper, SGMII, or media converter mode. Otherwise, it reads 0.

SerDes Link

Bit 6 of the Mode Control register indicates the link status of the SerDes interface is up in fiber, SGMII, or media converter mode. Otherwise, it reads 0.

Copper Energy Detect

Bit 5 of the Mode Control register indicates that energy is detected in the copper interface. Otherwise, it reads 0.

Fiber Signal Detect

Bit 4 of the Mode Control register indicates that fiber signal detect is set. Otherwise, it reads 0.

Mode Select

Bits [2:1] of the Mode Control register select one of four available interfaces. Bit 0, auto-detect media enable, in register 1Ch, shadow 1E should be set to 0 when writing into the Mode Select Control register. The interface logic is as follows:

Copper	00
Fiber	01
SGMII	10
Media Converter	11

Enable 1000BASE-X Registers

Setting bit 0 of the Mode Control register enables the 1000BASE-X register set for addresses 00h–0Fh. Clearing bit 0 of the Mode Control register enables the copper register set for addresses 00h–0Fh.

1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed

Table 75: 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed Register (Address 1Dh) Bit 15=0

Bit	*Name*	*R/W*	*Description*	*Default*
15	Enable Shadow Register	R/W	1 = Select shadow register 0 = Normal operation Writes to the selected register are done on a single cycle.	0
14	Master/Slave Seed Match	RO LH	1 = Seeds match 0 = Seeds do not match	0
13	Link Partner Repeater/DTE Bit	RO	1 = Link partner is a repeater/switch device port 0 = Link partner is a DTE device port	0

Table 75: 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed Register (Address 1Dh) Bit 15=0

Bit	Name	R/W	Description	Default
12	Link Partner Manual Master/ Slave Configuration Value	RO	1 = Link partner is configured as master 0 = Link partner is configured as slave	0
11	Link Partner Manual Master/ Slave Configuration Enable	RO	1 = Link partner manual master/slave configuration enabled 0 = Link partner manual master/slave configuration disabled	0
10:0	Local Master/Slave Seed Value	R/W	Returns the automatically generated M/S random seed.	000h

Enable Shadow Register

When bit 15 of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register is cleared, the Master/Slave Seed register is selected. If bit 15 is set, the shadow register HCD Status register is selected for read/write.

Master/Slave Seed Match

When bit 14 of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register returns 1 when the master/ slave seed matches; otherwise, it returns 0.

Link Partner Repeater/DTE Bit

When read-only bit 13 of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register returns 1, the link partner is configured as a repeater or a switch. If this bit returns 0, the link partner is configured as a DTE port.

Link Partner Manual Master/Slave Configuration Value

When read-only bit 12 of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register returns 1, the link partner is configured as a master. If this bit returns 0, the link partner is configured as a slave.

Link Partner Manual Master/Slave Configuration Enable

When read-only bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register returns 1, the link partner manual master/slave configuration is enabled. If this bit returns 0, the link partner manual master/ slave configuration is disabled.

Local Master/Slave Seed Value

Bits [10:0] of the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register return the automatically generated local master/slave seed value.

1000BASE-T/100BASE-TX/10BASE-T HCD Status

Table 76: 1000BASE-T/100BASE-TX/10BASE-T HCD Status Register (Address 1Dh) Bit 15 = 1

Bit	Name	R/W	Description	Default
15	Enable Shadow Register	R/W	1 = Select Shadow register 0 = Normal operation	0
14	Ethernet@WireSpeed Disable Gigabit Advertising	RO	1 = Disable advertising gigabit 0 = Advertise gigabit based on register 09h	0
13	Ethernet@WireSpeed Disable 100TX Advertising	RO	1 = Disable advertising 100TX 0 = Advertise 100TX based on register 04h	0
12	Ethernet@WireSpeed Downgrade	RO LH	1 = Ethernet@WireSpeed downgrade occurred since last read 0 = Ethernet@WireSpeed downgrade cleared	0
11	HCD 1000BASE-T FDX	RO LH	1 = Gigabit full-duplex occurred since last read 0 = HCD cleared	0
10	HCD 1000BASE-T	RO LH	1 = Gigabit half-duplex occurred since last read 0 = HCD cleared	0
9	HCD 100BASE-TXFDX	RO LH	1 = 100BASE-TX full-duplex occurred since last read 0 = HCD cleared	0
8	HCD 100BASE-T	RO LH	1 = 100BASE-TX half-duplex occurred since last read 0 = HCD cleared	0
7	HCD 10BASE-T FDX	RO LH	1 = 10BASE-T full-duplex occurred since last read 0 = HCD Cleared	0
6	HCD 10BASE-T	RO LH	1 = 10BASE-T half-duplex occurred since last read 0 = HCD cleared	0
5	HCD 1000BASE-T FDX (Link Never Came Up)	RO LH	1 = Gigabit full-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0
4	HCD 1000BASE-T (Link Never Came Up)	RO LH	1 = Gigabit half-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0
3	HCD 100BASE-TX FDX (Link Never Came Up)	RO LH	1 = 100BASE-TX full-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0
2	HCD 100BASE-T (Link Never Came Up)	RO LH	1 = 100BASE-TX half-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0
1	HCD 10BASE-T FDX (Link Never Came Up)	RO LH	1 = 10BASE-T full-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0
0	HCD 10BASE-T (Link Never Came Up)	RO LH	1 = 10BASE-T half-duplex HCD and *link never came up* occurred since the last read 0 = HCD cleared	0

Note: Bits 12:0 are cleared when auto-negotiation is disabled via MII register 0 bit 12 or restarted via MII register 0 bit 9.

Enable Shadow Register

When bit 15 of 1000BASE-T/100BASE-TX/10BASE-T HCD Status register is cleared, the 1000BASE-T/100BASE-TX/10BASE-T Master/Slave Seed register is selected. If bit 15 is set, the shadow register HCD Status register (auto-negotiation highest common denominator resolution), is selected for read/write. This bit must be set to be able to read/write to the HCD Status register.

Ethernet@WireSpeed Disable Gigabit Advertising

When bit 14 = 1, 1000BASE-T half-duplex and 1000BASE-T full-duplex are not advertised.

Ethernet@WireSpeed Disable 100BASE-TX Advertising

When bit 13 = 1, 100BASE-TX half-duplex and 100BASE-TX full-duplex are not advertised.

Ethernet@WireSpeed Downgrade

When bit 12 = 1, an Ethernet@WireSpeed downgrade has occurred since the last read.

HCD 1000BASE-T FDX

When bit 11 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns 1, a Gigabit full-duplex HCD has occurred since the last read.

HCD 1000BASE-T

When bit 10 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns 1, a Gigabit half-duplex HCD has occurred since the last read.

HCD 100BASE-TX FDX

When bit 9 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns 1, a 100BASE-TX full-duplex HCD has occurred since the last read.

HCD 100BASE-T

When bit 8 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns 1, a 100BASE-TX half-duplex HCD has occurred since the last read.

HCD 10BASE-T FDX

When bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns 1, a 10BASE-T full-duplex HCD has occurred since the last read.

HCD 10BASE-T

When bit 6 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns 1, a 10BASE-T half-duplex HCD has occurred since the last read.

HCD 1000BASE-T FDX (Link Never Came Up)

When bit 5 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns 1, a Gigabit full-duplex HCD has occurred, but the link was not established since the last read.

HCD 1000BASE-T (Link Never Came Up)

When bit 4 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns 1, a Gigabit half-duplex HCD has occurred, but the link was not established since the last read.

HCD 100BASE-TX FDX (Link Never Came Up)

When bit 3 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns 1, a 100BASE-TX full-duplex HCD has occurred, but the link was not established since the last read.

HCD 100BASE-TX (Link Never Came Up)

When bit 2 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns 1, a 100BASE-TX half-duplex HCD has occurred, but the link was not established since the last read.

HCD 10BASE-T FDX (Link Never Came Up)

When bit 1 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns 1, a 10BASE-T full-duplex HCD has occurred, but the link was not established since the last read.

HCD 10BASE-T FDX (Link Never Came Up)

When bit 0 of the 1000BASE-T/100BASE-TX/10BASE-T HCD Status register returns 1, a 10BASE-T half-duplex HCD has occurred, but the link was not established since the last read.

1000BASE-T/100BASE-TX/10BASE-T Test Register 1

Table 77: 1000BASE-T/100BASE-TX/10BASE-T Test Register 1 (Address 1Eh)

Bit	Name	R/W	Description	Default
15	CRC Error Counter Selector	R/W	1 = Receiver NOT_OK Counters (register 14h) becomes 16 bit CRC error counter (CRC errors are counted only after this bit is set) 0 = Normal operation	0
14:8	Reserved	R/W	Write as 00h, ignore when read.	00h
7	Manual Swap MDI State	R/W	1 = Manually swap MDI state 0 = Normal operation	0
6:0	Reserved	R/W	Write as 00h, ignore when read.	00h

CRC Error Counter Selector

Setting this bit enables the 1000BASE-T/100BASE-TX/10BASE-T Receiver NOT_OK Counter Register (Address 14h) to start counting CRC errors and store the counts in register 14h.

Manual Swap MDI State

Setting bit 7 of the 1000BASE-T/100BASE-TX/10BASE-T Test register 1 manually swaps the MDI transmit and receive pairs during forced 100BASE-TX and 10BASE-T operation. When this bit is set, the BCM5482S transceiver transmits on pairs TRD± {1} and receives on TRD± {0} when operating in 100BASE-TX and 10BASE-T modes. If this bit is cleared, the BCM5482S transmits on pairs TRD± {0} and receives on TRD± {1} when operating in 100BASE-TX and 10BASE-T modes. This bit is ignored when the auto-negotiation is enabled. (See note below.)

Note: To change the MDI state when in forced 100BASE-TX mode, put the PHY into a non-link condition, set bit 7 = 1, and then set the PHY into force 100BASE-TX mode.

Primary SerDes Register Descriptions

1000BASE-X MII Control

The following 1000BASE-X registers are enabled by writing to Mode Control Register (Address 1Ch, Shadow Value 11111) bit 0 = 1 or when the device is powered up in SerDes mode.

Table 78: 1000BASE-X MII Control Register (Address 00h)

Bit	Name	R/W	Description	Default
15	Reset	R/W SC	1 = PHY reset 0 = Normal operation	0
14	Internal Loopback	R/W	1 = Loopback mode 0 = Normal operation	0
13	Reserved	RO	Write as 0, ignore on read	0
12	Auto-negotiation Enable	R/W	1 = Auto-negotiation enabled 0 = Auto-negotiation disabled	1
11	Power-Down	R/W	1 = Power down 0 = Normal operation	INTF_SEL[1:0]=01
10	Isolate	R/W	1 = Electrically isolate PHY from SGMII/SerDes 0 = Normal operation	0
9	Restart Auto-negotiation	R/W SC	1 = Restarting auto-negotiation 0 = Auto-negotiation restart complete	0
8	Duplex Mode	R/W	1 = Full-duplex 0 = Half-duplex	FDX pin
7	Collision Test Enable	R/W	1 = Enable the collision test mode 0 = Disable the collision test mode	0
6:0	Reserved	R/W	Write as 40h, ignore on read	40h

Reset

To reset the BCM5482S transceiver by software control, 1 must be written to bit 15 of the 1000BASE-X MII Control register. This bit clears itself after the reset process is complete, and does not need to be cleared using a second MII write. Writes to other 1000BASE-X MII Control register bits have no effect until the reset process is completed, which requires approximately 2.0 microseconds. Writing 0 to this bit has no effect. When this bit is read during the reset process, a 1 is returned; otherwise, a 0 is returned.

Internal Loopback

The BCM5482S can be placed into internal loopback mode by setting bit 14 of the 1000BASE-X MII Control register. Loopback mode can be cleared by writing 0 to bit 14 of the 1000BASE-X MII Control register or by resetting the chip. When this bit is read and the chip is in loopback mode, a 1 is returned; otherwise, a 0 is returned.

Auto-negotiation Enable

When bit 12 of the 1000BASE-X MII Control register is set, the BCM5482S mode of operation is controlled by auto-negotiation. When this bit is cleared, the BCM5482S mode of operation is determined by the duplex mode. When this bit is read with auto-negotiation enabled, a 1 is returned; otherwise, a 0 is returned.

Power-Down

When bit 11 of the 1000BASE-X MII Control register is set, the BCM5482S is placed into l/O power standby mode. For more details, see "Standby Power-Down Mode" on page lxix. The 1000BASE-X interface is powered down when the device is in copper mode.

Note: When auto-medium mode detection is enabled, power bit of register 00h bit 11 is controlled by the internal state machine to power down the interface when it is selected. A 1 should not be written to this bit.

Isolate

The BCM5482S can be isolated from the RGMII bus by setting bit 10 of the 1000BASE-X MII Control register. All SGMII/SerDes outputs are tristated, and all SGMII/SerDes inputs are ignored. Because the management interface is still active, isolate mode can be cleared by writing 0 to bit 10 of the 1000BASE-X MII Control register or resetting the chip. When this bit is read and the chip is in isolate mode, a 1 is returned; otherwise, a 0 is returned. The default of this bit is 0.

Restart Auto-negotiation

Setting bit 9 of the 1000BASE-X MII Control register forces the auto-negotiation process to be restarted, regardless of the current state of the auto-negotiation state machine. When auto-negotiation is enabled, setting this bit restarts the auto-negotiation process. Clearing this bit has no effect. This bit is self-clearing. After the auto-negotiation process has restarted, it returns 0.

Duplex Mode

When auto-negotiation is disabled, duplex mode can be controlled by writing to bit 8 of the 1000BASE-X MII Control register. Setting this bit forces the BCM5482S into full-duplex operation while clearing this bit forces the BCM5482S into half-duplex operation. When this bit is read, it returns the last value written. The default value of this bit is determined by the FDX pin at reset.

Collision Test

The BCM5482S can be placed into collision test mode by setting bit 7 of the 1000BASE-X MII Control register. In this mode, the COL pin is asserted whenever the TX_EN pin is driven high. Collision test mode can be cleared by writing 0 to bit 7 of the 1000BASE-X MII Control register or resetting the chip. When this bit is read and the chip is in collision test mode, a 1 is returned; otherwise, a 0 is returned.

1000BASE-X MII Status

The following 1000BASE-X registers are enabled by writing to Mode Control Register (Address 1Ch, Shadow Value 11111) bit 0 = 1.

Table 79: 1000BASE-X MII Status Register (Address 01h)

Bit	Name	R/W	Description	Default
15	100BASE-T4 Capable	RO L	1 = 100BASE-T4 capable 0 = Not 100BASE-T4 capable	0
14	100BASE-X Full-duplex Capable	RO L	1 = 100BASE-X full-duplex capable 0 = Not 100BASE-X full-duplex capable	0
13	100BASE-X Half-duplex Capable	RO L	1 = 100BASE-X half-duplex capable 0 = Not 100BASE-X half-duplex capable	0
12	10BASE-T Full-duplex Capable	RO L	1 = 10BASE-T full-duplex capable 0 = Not 10BASE-T full-duplex capable	0
11	10BASE-T Half-duplex Capable	RO L	1 = 10BASE-T half-duplex capable 0 = Not 10BASE-T half-duplex capable	0
10	100BASE-T2 Full-duplex Capable	RO L	1 = 100BASE-T2 full-duplex capable 0 = Not 100BASE-T2 full-duplex capable	0
9	100BASE-T2 Half-duplex Capable	RO L	1 = 100BASE-T2 half-duplex capable 0 = Not 100BASE-T2 half-duplex capable	0
8	Extended Status	RO H	1 = Extended status information in reg 0Fh 0 = No extended status information in reg 0Fh	1
7	Reserved	RO	Write as 0, ignore on read	0
6	Management Frames Preamble Suppression	RO H	1 = Preamble can be suppressed 0 = Preamble always required	1
5	Auto-negotiation Complete	RO	1 = Auto-negotiation complete 0 = Auto-negotiation in progress	0
4	Remote Fault	RO LH	1 = Remote fault detected 0 = No remote fault detected	0
3	Auto-negotiation Ability	RO H	1 = Auto-negotiation capable 0 = Not auto-negotiation capable	1
2	Link Status	RO LL	1 = Link is up (link pass state) 0 = Link is down (link fail state)	0
1	Jabber Detect	RO L	1 = Jabber condition detected 0 = No jabber condition detected	0
0	Extended Capability	RO H	1 = Extended register capabilities 0 = No extended register capabilities	1

100BASE-T4 Capable

The BCM5482S is not capable of 100BASE-T4 operation and returns 0 when bit 15 of the 1000BASE-X MII Status register is read.

100BASE-X Full-Duplex Capable

The BCM5482S is not capable of 100BASE-X full-duplex operation and returns 0 when bit 14 of the 1000BASE-X MII Status register is read.

100BASE-X Half-Duplex Capable

The BCM5482S is not capable of 100BASE-X half-duplex operation and returns 0 when bit 13 of the 1000BASE-X MII Status register is read.

10BASE-T Full-Duplex Capable

The BCM5482S is not capable of 10BASE-T full-duplex operation and returns 0 when bit 12 of the 1000BASE-X MII Status register is read.

10BASE-T Half-Duplex Capable

The BCM5482S is not capable of 10BASE-T half-duplex operation and returns 0 when bit 11 of the 1000BASE-X MII Status register is read.

100BASE-T2 Full-Duplex Capable

The BCM5482S is not capable of 100BASE-T2 full-duplex operation and returns 0 when bit 10 of the 1000BASE-X MII Status register is read.

100BASE-T2 Half-Duplex Capable

The BCM5482S is not capable of 100BASE-T2 half-duplex operation and returns 0 when bit 9 of the 1000BASE-X MII Status register is read.

Extended Status

The BCM5482S contains an IEEE Extended Status register at address 0Fh and returns 1 when bit 8 of the 1000BASE-X MII Status register is read.

Management Frames Preamble Suppression

The BCM5482S accepts MII management frames whether or not they are preceded by the preamble pattern and returns 1 when bit 6 of the 1000BASE-X MII Status register is read.

Note: Preamble is still required on the first read or write.

Auto-negotiation Complete

The BCM5482S returns 1 in bit 5 of the 1000BASE-X MII Status register when auto-negotiation has completed, and the contents of registers 4, 5, and 6 are valid. This bit returns 0 while auto-negotiation is in progress.

Remote Fault

The BCM5482S returns 1 in bit 4 of the 1000BASE-X MII Status register when its link partner has signaled a remote fault condition. When a remote fault occurs, the bit is set and remains so until the remote fault condition has been cleared and the register is read.

Auto-negotiation Ability

Even if the auto-negotiation function has been disabled, the BCM5482S is capable of performing IEEE auto-negotiation and returns 1 when bit 3 of the 1000BASE-X MII Status register is read.

Link Status

The BCM5482S returns 1 in bit 2 of the 1000BASE-X MII Status register when the link monitor is in the link pass state (indicating that a valid link has been established); otherwise it returns 0. When a link failure occurs, the Link Status bit is latched at 0 and remains so until the bit is read and the BCM5482S is in the link pass state.

Jabber Detect

The jabber detect function is not supported for the 1000BASE-X. This bit always returns 0.

Extended Capability

The BCM5482S supports extended capability registers and returns 1 when bit 0 of the 1000BASE-X MII Status register is read.

1000BASE-X Auto-negotiation Advertisement

The following 1000BASE-X registers are enabled by writing to Mode Control Register (Address 1Ch, Shadow Value 11111) bit 0 = 1.

Table 80: 1000BASE-X Auto-negotiation Advertisement Register (Address 04h)

Bit	Name	R/W	Description	Default
15	Reserved	RO	Write as 0, ignore on read	0
14	Reserved	RO	Write as 0, ignore on read	0
13:12	Remote Fault	R/W	00 = No remote fault 01 = Link fault 10 = Off line 11 = Auto-negotiation error	0
11:9	Reserved	R/W	Write as 000, ignore on read	000
8:7	Pause	R/W	00 = No pause 01 = Symmetric pause 10 = Symmetric pause toward link partner 11 = Both asymmetric and symmetric pause toward local device	Changed by hardware pin settings.
6	Half-duplex capable	R/W	1 = 1000BASE-X half-duplex advertised 0 = 1000BASE-X half-duplex not advertised	Changed by hardware pin settings.
5	Full-duplex capable	R/W	1 = 1000BASE-X full-duplex advertised 0 = 1000BASE-X full-duplex not advertised	Changed by hardware pin settings.
4:0	Reserved	R/W	Write as 00h, ignore on read	00h

Note: When SGMII mode is enabled, reading register 04h reflects the ability sent to the link partner. The values written to the register are stored, but not used.

The SGMII word is sent as follows:

[15] = Copper link

[14] = Acknowledge

[13] = 0

[12] = Copper duplex

[11:10] = Copper speed. 00 = 10BASE-T, 01 = 100BASE-TX, 10 = 1000BASE-T, 11 = Reserved

[9:1] = 000000000

[0] = 1 (SGMII Selector)

Remote Fault

Setting bits 12 and 13 of the 1000BASE-X Auto-negotiation Advertisement register sends a remote fault indication to the link partner during auto-negotiation. Writing 00 to this bit clears the Remote Fault transmission bit. This bit returns a nonzero when advertising remote fault; otherwise, it returns 00.

Pause

When bits [8:7] of the 1000BASE-X Auto-negotiation Advertisement register is set, the BCM5482S advertises full-duplex pause capability. When these bits are 00, the BCM5482S advertises no pause capability. This bit returns 10, 01, or when advertising pause capability; otherwise, it returns 00.

Half-Duplex Capable

When bit 6 of the 1000BASE-X Auto-negotiation Advertisement register is set, the BCM5482S advertises 1000BASE-X half-duplex capability. When the bit is cleared, the BCM5482S advertises no 1000BASE-X half-duplex capability. This bit returns 1 when advertising 1000BASE-X half-duplex capability; otherwise, it returns 0. This bit updates during reset based on configuring the hardware pins in the following way: (INTF_SEL[1] AND INTF_SEL[0] AND ANEN) OR (NOT INTF_SEL[1]) OR (NOT INTF_SEL[0]).

Full-Duplex Capable

When bit 5 of the 1000BASE-X Auto-negotiation Advertisement register is set, the BCM5482S advertises 1000BASE-X full-duplex capability. When the bit is cleared, the BCM5482S advertises no 1000BASE-X full-duplex capability. This bit returns 1 when advertising 1000BASE-X full-duplex capability; otherwise, it returns 0. This bit updates during reset based on configuring the FDX pin.

1000BASE-X Auto-Negotiation Link Partner Ability

The following 1000BASE-X registers are enabled by writing to Mode Control Register (Address 1Ch, Shadow Value 11111) bit 0 = 1.

Table 81: 1000BASE-X Auto-Negotiation Link Partner Ability Register–Base Page (Address 05h)

Bit	Name	R/W	Description	Default
1000BASE-X Mode				
15	Next Page	R/W	1 = Link partner supports Next Page ability 0 = Link partner does not supports Next Page ability	0
14	Acknowledge	RO	1 = Link partner has received link code word 0 = Link partner has not received link code word	0
13:12	Remote Fault	R/W	00 = No remote fault 01 = Link fault 10 = Off line 11 = Auto-negotiation error	0
11:9	Reserved	R/O	Write as 000, ignore on read	000
8:7	Pause	R/O	00 = Link partner sends no pause 01 = Link partner sends symmetric pause 10 = Link partner sends asymmetric pause toward link partners 11 = Link partner sends both asymmetric and symmetric pause toward local device	0
6	Half-duplex Capable	R/O	1 = Link partner is 1000BASE-X half-duplex capable 0 = Link partner is not 1000BASE-X half-duplex capable	0
5	Full-duplex Capable	R/O	1 = Link partner is 1000BASE-X full-duplex capable 0 = Link partner is not 1000BASE-X full-duplex capable	0
4:0	Reserved	R/O	Write as 00h, ignore on read	00h
SGMII Mode				
15	Copper Link	R/O	1 = Link established at copper interface 0 = Link not established at copper interface	0
14	Acknowledge	R/O	1 = Link partner has received link code word 0 = Link partner has not received link code word	0
13	Reserved	R/O	Write as 0, ignore on read	0
12	Copper Duplex	R/O	1 = Copper link partner is full-duplex 0 = Copper link partner is not full-duplex	0
11:10	Copper Speed	R/O	00 = 10BASE-T 01 = 100BASE-TX 10 = 1000BASE-T 11 = Reserved	00

Note: As indicated by bit 5 of the 1000BASE-X MII Status register, the values contained in the Auto-negotiation Link Partner Ability register are guaranteed to be valid only after auto-negotiation has successfully completed.

Table 81: 1000BASE-X Auto-Negotiation Link Partner Ability Register–Base Page (Address 05h) (Cont.)

Bit	Name	R/W	Description	Default
9:1	Reserved	R/O	Write as 00h, ignore on read	00h
0	SGMII Selector	R/O	1 = SGMII mode 0 = 1000BASE-X mode	1

Note: As indicated by bit 5 of the 1000BASE-X MII Status register, the values contained in the Auto-negotiation Link Partner Ability register are guaranteed to be valid only after auto-negotiation has successfully completed.

1000BASE-X Mode

Next Page

The BCM5482S returns 1 in bit 15 of the 1000BASE-X auto-negotiation Link Partner Ability register when the link partner is set to transmit Next Page information.

Acknowledge

The BCM5482S returns 1 in bit 14 of the 1000BASE-X auto-negotiation Link Partner Ability register when the link partner has acknowledged reception of the link code word; otherwise, it returns 0.

Remote Fault

The BCM5482S returns a nonzero value in bits [13:12] of the 1000BASE-X Auto-negotiation Link Partner Ability register when the link partner has advertised detection of a remote fault; otherwise, it returns 00.

Pause

The BCM5482S returns values in bits [8:7] of the 1000BASE-X auto-negotiation Link Partner Ability register when the link partner has advertised pause capability.

Half-Duplex Capable

The BCM5482S returns 1 in bit 6 of the 1000BASE-X auto-negotiation Link Partner Ability register when the link partner has advertised 1000BASE-X half-duplex capability; otherwise, it returns 0.

Full-Duplex Capable

The BCM5482S returns 1 in bit 5 of the 1000BASE-X auto-negotiation Link Partner Ability register when the link partner has advertised 1000BASE-X full-duplex capability; otherwise, it returns 0.

SGMII Mode

Copper Link

This bit indicates the link is established on the copper interface. The MAC sends 0 only.

Acknowledge

This bit indicates the SGMII link partner has received the link code word.

Copper Duplex

This bit indicates the copper link partner is linked up at full-duplex mode. The MAC sends 0 only.

Copper Speed

Bits [11:10] indicate the copper linkup speed. The MAC sends 0 only.

1000BASE-X Auto-negotiation Extended Status

The following 1000BASE-X registers are enabled by writing to Mode Control Register (Address 1Ch, Shadow Value 11111) bit 0 = 1.

Table 82: 1000BASE-X Auto-Negotiation Extended Status Register (Address 06h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:3	Reserved	RO	Write as 000h, ignore on read	000h
2	Next Page Capable	RO L	Write as 0, ignore on read	0
1	Page Received	RO LH	1 = New page has been received from link partner 0 = New page has not been received	0
0	Reserved	RO	Write as 0, ignore on read	0

Next Page Capable

When bit 2 of the 1000BASE-X auto-negotiation Extended Status register is read, the BCM5482S does not support Next Page capability and returns 0.

Page Received

The BCM5482S returns 1 in bit 1 of the 1000BASE-X auto-negotiation Extended Status register when a new link code word has been received from the link partner since the last time this register was read; otherwise, it returns 0.

1000BASE-X IEEE Extended Status

The 1000BASE-X IEEE Extended Status registers are enabled by writing to Mode Control Register (Address 1Ch, Shadow Value 11111) bit 0 = 1.

Table 83: 1000BASE-X IEEE Extended Status Register (Address 0Fh)

Bit	Name	R/W	Description	Default
15	1000BASE-X Full-duplex Capable	RO H	1 = 1000BASE-X full-duplex capable 0 = Not 1000BASE-X full-duplex capable	1
14	1000BASE-X Half-duplex Capable	RO H	1 = 1000BASE-X half-duplex capable 0 = Not 1000BASE-X half-duplex capable	1
13	1000BASE-T Full-duplex Capable	RO L	1 = 1000BASE-T full-duplex capable 0 = Not 1000BASE-T full-duplex capable	0
12	1000BASE-T Half-duplex Capable	RO L	1 = 1000BASE-T half-duplex capable 0 = Not 1000BASE-T half-duplex capable	0
11:0	Reserved	RO	Write as 000h, ignore on read	000h

1000BASE-X Full-Duplex Capable

The BCM5482S is capable of 1000BASE-X full-duplex operation and returns 1 when bit 15 of the 1000BASE-X IEEE Extended Status register is read.

1000BASE-X Half-Duplex Capable

The BCM5482S is capable of 1000BASE-X half-duplex operation and returns 1 when bit 14 of the 1000BASE-X IEEE Extended Status register is read.

1000BASE-T Full-Duplex Capable

The BCM5482S is not capable of 1000BASE-T full-duplex operation and returns 0 when bit 13 of the 1000BASE-X IEEE Extended Status register is read.

1000BASE-T Half-Duplex Capable

The BCM5482S is not capable of 1000BASE-T half-duplex operation and returns 0 when bit 12 of the 1000BASE-X IEEE Extended Status register is read.

Expansion Registers

Expansion Register 00h: Receive/Transmit Packet Counter

Expansion register 00h is enabled by writing to 1000BASE-T/100BASE-TX/10BASE-T Expansion and Secondary SerDes Register Access Register (Address 17h) bits 11:0 = 'F00'h, and read/write access is through register 15h.

Table 84: Receive/Transmit Packet Counter Register (Address 00h)

Bit	Name	R/W	Description	Default
15:0	Packet Counter (Copper Only)	R/W CR	Returns the transmitted and received packet count.	0000h

Packet Counter (Copper Only)

The mode of this counter is set by bit 11 of 1000BASE-T/100BASE-TX/10BASE-T Misc Control Register (Address 18h, Shadow Value 111). Either receive or transmit packets are counted. This counter is cleared on read and freezes at FFFFh.

Expansion Register 01h: Expansion Interrupt Status

Expansion register 01h is enabled by writing to 1000BASE-T/100BASE-TX/10BASE-T Expansion and Secondary SerDes Register Access Register (Address 17h) bits 11:0 = F01h, and read/write access is through register 15h.

Table 85: Expansion Interrupt Status Register (Address 01h)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Write as 00h, ignore on read	00h
7	Mode Select Change	RO LH	1 = Mode select change detected (clears on read) 0 = Mode select change not detected	0
6	SerDes Link Status Change	RO LH	1 = SerDes link status change detected (clears on read) 0 = Mode select change not detected	0
5	RUDI_C detected	RO LH	1 = SerDes auto-negotiation code-word received since last read 0 = SerDes auto-negotiation code-word has not been received	0
4:1	Expansion Interrupt Status	RO LH	1 = Expansion Interrupt condition detected 0 = Expansion Interrupt condition not detected	0000
0	Transmit CRC Error (Copper Only)	RO LH	1= Transmit CRC error detected since last read 0= No Transmit CRC error detected since last read	0

Mode Select Change

This bit indicates that a mode select change is detected.

SerDes Link Status Change

This bit indicates that a SerDes link status change is detected.

RUDI_C Detected

This bit indicates that a SerDes auto-negotiation code word is detected.

Expansion Interrupt Status

These bits corresponds to the Expansion Interrupt Status bits.

Transmit CRC Error (Copper Only)

This bit indicates that a transmit CRC error has occurred since this register was last read.

Expansion Register 02h: Expansion Interrupt Mask

Expansion register 02h is enabled by writing 1000BASE-T/100BASE-TX/10BASE-T Expansion and Secondary SerDes Register Access Register (Address 17h) bits 11:0 = F02h, and read/write access is through register 15.

Table 86: Expansion Interrupt Mask Register (Address 02h)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Write as 00h, ignore on read	00h
7:0	Expansion Interrupt Mask	R/W	1 = Interrupt masked (status bits still operate normally but do not generate interrupt output) 0 = Interrupt enabled	FFh

Expansion Register 04h: Multicolor LED Selector

Expansion register 04h is enabled by writing to 1000BASE-T/100BASE-TX/10BASE-T Expansion and Secondary SerDes Register Access Register (Address 17h) bits 11:0 = F04h, and read/write access is through register 15h.

Table 87: Multicolor LED Selector Register (Address 04h)

Bit	Name	R/W	Description	Default
15:10	Reserved	R/W	Write as 00h, ignore on read	00h
9	Flash Now	R/W SC	1 = Initiate a multicolor LED flash. This works only when the multicolor selector is set to 0111.	0
8	In Phase	R/W	1 = $\overline{\text{MULTICOLOR[1]}}$ and $\overline{\text{MULTICOLOR[2]}}$ are in phase. 0 = $\overline{\text{MULTICOLOR[1]}}$ and $\overline{\text{MULTICOLOR[2]}}$ are in opposite phase. ***Note:*** This is only valid when Multicolor LED Selector bits are set to 0000, 0010, 0011, 0110, 0111, 1000, 1001, 1010.	0
7:4	$\overline{\text{MULTICOLOR[2]}}$ LED Selector	R/W	Selects the multicolor mode for $\overline{\text{MULTICOLOR[2]}}$ LED 0000: Encoded link/activity LED 0001: Encoded speed LED 0010: Activity flash LED 0011: Full-duplex LED 0100: Forced off 0101: Forced on 0110: Alternating LED (toggling between two of the states at 50% duty cycle with a 320 ms period) 0111: Flashing LED (toggling between 2 of the states with an 80 ms period) 1000: Link LED 1001: Activity LED 1010: Programmable blink LED	0h

Table 87: Multicolor LED Selector Register (Address 04h) (Cont.)

Bit	Name	R/W	Description	Default
3:0	MULTICOLOR[1] LED Selector	R/W	Selects the multicolor mode for MULTICOLOR[1] LED 0000: Encoded link/activity LED 0001: Encoded speed LED 0010: Activity flash LED 0011: Full-duplex LED 0100: Forced off 0101: Forced on 0110: Alternating LED (toggling between 2 of the states at 50% duty cycle with a 320 ms period) 0111: Flashing LED (toggling between 2 of the states with an 80 ms period) 1000: Link LED 1001: Activity LED 1010: Programmable blink LED	0h

Flash Now

Asserting this bit causes a single flash to occur on either MULTICOLOR[2:1] LED, as long as its multicolor selector is set to 0111.

In Phase

When both LEDs are selected to the same mode, the MULTICOLOR[2:1] output pins toggle at the same time. This bit determines whether the pins are identical to each other or are inverses of each other. When the two LED pins are attached to a special multicolored LED, the resulting LED colors alternate either between off/amber (in phase) or red/green (out of phase).

MULTICOLOR[2] LED Selector

The bits [7:4] select the multicolor LED mode for MULTICOLOR[2]. The User to determine what functions should appear on the two LED pins.

Example: For a different color toggling operation than the operation previously mentioned (such as red/amber), the user can put one of the selectors to the preferred toggle mode and other selector to forced on.

MULTICOLOR[1] LED Selector

Bits [3:0] select the multicolor LED mode for MULTICOLOR[1].

Expansion Register 05h: Multicolor LED Flash Rate Controls

Expansion register 05h is enabled by writing to 1000BASE-T/100BASE-TX/10BASE-T Expansion and Secondary SerDes Register Access Register (Address 17h) bits 11:0 = F05h, and read/write access is through register 15h.

Table 88: Multicolor LED Flash Rate Controls Register (Address 05h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:12	Reserved	R/W	Write as 0h, ignore on read	0h
11:6	Alternating Rate	R/W	Determines the width and gap for multicolor LED selector 0110 (alternating LED mode). 00h = 21 ms width, 21 ms gap 01h = 42 ms width, 42 ms gap 02h = 63 ms width, 63 ms gap ... 07h = 168 ms width, 168 ms gap ... 3Fh = 1.344s	07h
5:0	Flash Rate	R/W	Determines the width.	01h

Alternating Rate

Setting Bits [11:6] changes the width and gap of the alternating LED modes. These bits are valid only when the MULTICOLOR[1] LED Selector and or the MULTICOLOR[2] LED Selector bits = 0110. The duty cycle of the LEDs is exactly 50%.

Flash Rate

Setting Bits [5:0] determines the width and minimum gap of the flashing pulse. These bits are valid only when the MULTICOLOR[1] LED Selector and or the MULTICOLOR[2] LED Selector bits = 0000, 0010, or 0111. The duty cycle of the flash rate is not exactly 50%.

Expansion Register 06h: Multicolor LED Programmable Blink Controls

Expansion register 06h is enabled by writing to 1000BASE-T/100BASE-TX/10BASE-T Expansion and Secondary SerDes Register Access Register (Address 17h) bits 11:0 = F06h, and read/write access is through register 15h.

Table 89: Multicolor LED Programmable Blink Controls Register (Address 06h)

Bit	Name	R/W	Description	Default
15:6	Reserved	R/W	Write as 000h, ignore on read	000h
5	Blink Update Now	R/W	1 = Change to the new blink rate now. 0 = Wait 1s before changing the blink rate. Controls when a change in the blink rate is actually displayed on the Programmable Blink LED.	0
4:0	Blink Rate	R/W	Programs the number of blinks per second of the Programmable Blink LED 00000 = No blink 00001 = 1 blink per second 00010 = 2 blinks per second 00011 = 3 blinks per second ... 11111 = 31 blinks per second	00000

Blink Update Now

Setting bit 5 updates the blink rate immediately. Clearing this bit causes the blink rate to be updated after the 1s interval timer expires. This bit is only valid when the MULTICOLOR[1] LED Selector and or the MULTICOLOR[2] LED Selector bits = 0000, 0010, or 0111.

Blink Rate

Setting bits [4:0] determines the blink rate of the Programmable Blink LED. These bits are only valid when the MULTICOLOR[1] LED Selector and or the MULTICOLOR[2] LED Selector bits = 0000, 0010, or 0111.

Expansion Register 42h: Operating Mode Status

Expansion register 42h is enabled by writing to 1000BASE-T/100BASE-TX/10BASE-T Expansion bits 11:0 = F42h, and read/write access is through register 15h.

Table 90: Expansion Reg 42h: Operating Mode Status Register

Bit	*Name*	*R/W*	*Description*	*Default*
15	SerDes Link	RO	1 = Link up in fiber, SGMII, or media converter modes (when set in SGMII or media converter mode, the primary SerDes and Copper/Secondary SerDes link must be valid). 0 = Link down	0
14:13	SerDes Speed	RO	10 = SerDes speed 1000 (SGMII 1000BASE or 1000BASE-X) 01 = SerDes speed 100 (SGMII 100BASE or 100BASE-FX) 00 = SerDes speed 10 (SGMII 10BASE)	10
12	SerDes Duplex	RO	1 = SerDes full-duplex 0 = SerDes half-duplex or auto-negotiation in progress	0
11	Copper Link	RO	1 = Link up on copper side (copper, SGMII, or GBIC mode) 0 = Link down	0
10:9	Copper Speed	RO	10 = 1000BASE-T 01 = 100BASE-T 00 = 10BASE-T or auto-negotiation in progress	00
8	Copper Duplex	RO	1 = Full-duplex 0 = Half-duplex or auto-negotiation in progress	0
7	Copper Energy Detect	RO	1 = Copper energy detected 0 = No copper energy detected	0
6	Fiber Signal Detect	RO	1 = Fiber signal detect from pin (filtered) (same as register 1ch shadow 11111 [4]) 0 = No fiber signal detect from pin	0
5	Sync Status	RO	1 = Valid SerDes PCS receive synchronization 0 = Invalid SerDes PCS receive synchronization	0

Table 90: Expansion Reg 42h: Operating Mode Status Register (Cont.)

Bit	Name	R/W	Description	Default
4:0	Operating Mode Status	RO	00000 = Reserved 00001 = Reserved 00010 = Reserved 00011 = Reserved 00100 = Reserved 00101 = Reserved 00110 = RGMII-to-copper 00111 = Reserved 01000 = Reserved 01001 = Reserved 01010 = Reserved 01011 = Reserved 01100 = Reserved 01101 = RGMII-to-100BASE-FX (SerDes) 01110 = RGMII-to-SGMII (10/100/1000) 01111 = RGMII-to-SerDes	00000
4:0	Operating Mode Status (cont.)	–	10000 = Reserved 10001 = Reserved 10010 = SGMII-to-SerDes * 10011 = SGMII-to-100BASE-FX (SerDes) * 10100 = SGMII-to-copper 10101 = Reserved 10110 = SerDes-to-SerDes (media converter) * 10111 = SerDes-to-copper (media converter) * Requires chip with 2 SerDes ports per slice	00000

SerDes Link

Bit 15 of the Operating Mode Status register is 1 when the link is up and the BCM5482S is in fiber, SGMII, or GBIC modes.

SerDes Speed

Bits [14:13] of the Operating Mode Status register provide the status of SerDes speeds:

- 10 = SerDes speed 1000 (SGMII 1000BASE or 1000BASE-X)
- 01 = SerDes speed 100 (SGMII 100BASE or 100BASE-FX)
- 00 = SerDes speed 10 (SGMII 10BASE)

SerDes Duplex

Bit 12 of the Operating Mode Status register provides the status of the full-duplex/half/duplex:

- 1 = SerDes full-duplex
- 0 = SerDes half-duplex or auto-negotiating in progress

Copper Link

Bit 11 of the Operating Mode Status register indicates that there is a link up on the copper side. Otherwise, it reads 0.

Copper Speed

Bits [10:9] of the Operating Mode Status register indicate the copper speed:

- 10 = 1000BASE-T
- 01 = 100BASE-T
- 00 = 10BASE-T or auto-negotiation in progress

Copper Duplex

Bit 8 of the Operating Mode Status register indicates the duplex type of the copper link:

- 1 = Full-duplex
- 0 = Half-duplex or auto-negotiation in progress

Copper Energy Detect

Bit 7 of the Operating Mode Status register indicates that energy is detected in the copper interface. Otherwise, it reads 0.

Fiber Signal Detect

Bit 6 of the Operating Mode Status register indicates that fiber signal detect from the pin is set. Otherwise, it reads 0.

Sync Status

Bit 5 of the Operating Mode Status register indicates valid SerDes PCS receive synchronization. Otherwise, it reads 0.

Operating Mode Status

See Description in Table 90: “Expansion Reg 42h: Operating Mode Status Register,” on page cciv.

Expansion Register 44h: SGMII Recover Control

Table 91: SGMII Recover Control Register (Address 44h)

Bit	Name	R/W	Description	Default
15:5	Reserved	R/W	Write as 00h, ignore on read	00h
4	Select Recovered CLK	R/W	1 = Configures RXD1/2[0] to Recover Clock (RF_CLK1/2) from the fiber interface (When BCM5482S is in SGMII-to-fiber mode). RXC1/2 also becomes the recovered clock from the copper interface when the device is linked up in SGMII-to-copper mode. 0 = Configures RXD1/2[0] to operate as data bit [0] of the RGMII interface	0
3	Reserved	R/W	Write as 00h, ignore on read	00h
2	Primary SerDes	R/W	Lineside Loopback Enable primary SerDes lineside loop 0	
1:0	Reserved	R/W	Write as 00h, ignore on read	00h

Select Recovered CLK

When bit 4 of the SGMII Recover Control register is 1, the RXD1/2[0]/RF_CLK1/2 signals are the recover clock from the fiber interface, and the RXC1/2/RC_CLK1/2 signals are the recover clock from the copper interface. When the bit is 0, these signals are in a normal mode.

Expansion Register 50h: SerDes/SGMII RX Control

Table 92: SerDes/SGMII Control RX Register (Address 50h)

Bit	Name	R/W	Description	Default
15:1	Reserved	R/W	Write as 00h, ignore on read	00h
0	RX Power Down	R/W	SerDes receive power-down	0

RX Power Down

When this bit is set, the receiver SerDes path is power-down.

Expansion Register 52h: SerDes/SGMII Control

Expansion register 52h is enabled by writing to 1000BASE-T/100BASE-TX/10BASE-T Expansion and Secondary SerDes Register Access Register (Address 17h) bits 11:0 = F52h, and read/write access is through register 15h.

Table 93: SerDes/SGMII Control Register (Address 52h)

Bit	Name	R/W	Description	Default
15:3	Reserved	R/W	Write as 00h, ignore on read	00h
2	TX Clock Pad Disable R/W	R/W	1 = Disable SerDes clock pads 0 = Enable SerDes clock pads	1
1:0	Reserved	R/W	Write as 00h, ignore on read	00h

TX Clock Pad Disable R/W

Setting this bit disables SerDes clock pads.

Secondary SerDes Registers

The following registers are applicable when register 15h is accessed, with index addressing filter select = 1110 on bits 11:8 of register 17h. The register address is specified on bits 7:0.

1000BASE-X Control

Register address bits [7:0] = 00h.

Table 94: 1000BASE-X Control Register (Address 00h)

Bit	Name	R/W	Description	Default
15	Secondary SerDes Reset	R/W SC	1 = Secondary SerDes reset (all Secondary SerDes registers, digital and analog, are reset) 0 = Normal operation	0
14	Loopback	R/W	1 = Loopback mode 0 = Normal operation	0
13	Manual Speed [0] (SGMII Slave only)	R/W	Manual speed [1:0]: 1X = SGMII 1000 01 = SGMII 100 00 = SGMII 10 ***Note:*** Register is ignored for 1000BASE-X operation	0
12	Auto-negotiation Enable	R/W	1 = Auto-negotiation enabled 0 = Auto-negotiation disabled (manual mode active)	1

Table 94: 1000BASE-X Control Register (Address 00h) (Cont.)

Bit	Name	R/W	Description	Default
11	Power-Down	R/W	1 = Power-down Secondary SerDes 0 = Normal operation	1
10	Reserved	R/W	Write as 0, ignore on read	0
9	Restart Auto-negotiation	R/W SC	1 = Restart auto-negotiation process 0 = Normal operation	0
8	Manual Full-Duplex Mode (SGMII Slave/ 1000BASE-X)	R/W	1 = Full duplex 0 = Half duplex	1
7	Reserved	R/W	Write as 0, ignore on read	0
6	Manual Speed [1] (SGMII Slave only)	R/W	Manual speed [1:0]: 1X = SGMII 1000 01 = SGMII 100 00 = SGMII 10 ***Note:*** Register is ignored for 1000BASE-X operation	1
5:0	Reserved	RO	Write as 0, ignore on read	000000

Secondary SerDes Reset

To reset the BCM5482S by software control, 1 must be written to bit 15 of the 1000BASE-X Control register. Setting this bit only resets the Secondary SerDes. To reset the primary and copper SerDes, use register MII 00 bit 15. This bit self-clears after the reset process is complete and does not need to be cleared using a second MII write. Writes to other 1000BASE-X Control register bits have no effect until the reset process is completed, which requires approximately 2.0 µs. Writing 0 to this bit has no effect. When this bit is read during the reset process, 1 is returned; otherwise, 0 is returned.

Loopback

The BCM5482S can be placed into loopback mode by setting bit 14 of the 1000BASE-X Control register. Loopback mode can be cleared by writing 0 to bit 14 of the 1000BASE-X Control register or by resetting the chip. When this bit is read and the chip is in loopback mode, a 1 is returned; otherwise, a 0 is returned.

Manual Speed [0]

Bit 13 of the 1000BASE-X Control register provides the status of manual [0] speeds:

Manual speed [1:0]:

- 1X = SGMII 1000
- 01 = SGMII 100
- 00 = SGMII 10

Auto-negotiation Enable

When bit 12 of the 1000BASE-X Control register is set, the BCM5482S mode of operation is controlled by auto-negotiation. When this bit is cleared, the BCM5482S mode of operation is determined by the duplex mode. When this bit is read with auto-negotiation enabled, a 1 is returned; otherwise, it returns 0.

Power-Down

When bit 11 of the Secondary SerDes 1000BASE-X Control register is set, the BCM5482S is placed into l/O power standby mode. For more details, see "Standby Power-Down Mode" on page lxix. The 1000BASE-X interface is powered down when the device is in copper mode.

Note: When auto-medium mode detection is enabled, power bit of register 00h bit 11 is controlled by the internal state machine to power down the interface when it is selected. A 1 should not be written to this bit.

Restart Auto-negotiation

Setting bit 9 of the 1000BASE-X Control register forces the auto-negotiation process to be restarted, regardless of the current state of the auto-negotiation state machine. When auto-negotiation is enabled, setting this bit restarts the auto-negotiation process. Clearing this bit has no effect. This bit is self-clearing. After the auto-negotiation process has restarted, it returns 0.

Manual Full-Duplex Mode

Bit 8 of the 1000BASE-X Control register returns 1 when in full-duplex mode and 0 when in half-duplex mode.

Manual Speed [1]

Bit 6 of the 1000BASE-X Control register provides the status of manual [1] speeds:

Manual speed [1:0]:

- 1X = SGMII 1000
- 01 = SGMII 100
- 00 = SGMII 10

1000BASE-X Auto-Negotiation Advertisement

Register address bits [7:0]= 04h

Table 95: Auto-Negotiation Advertisement Register (Address 04h)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Advertise next page ability 0= Next Page ability is not supported	0
14	Reserved	RO	Write as 0, ignore on read	0
13:12	Remote Fault	R/W	00 = No remote fault 01 = Link failure 10 = Offline 11 = Auto-negotiation error	0
11:9	Reserved	R/W	Write as 0, ignore on read	0
8:7	Pause	R/W	00 = No pause 01 = Symmetric pause 10 = Asymmetric pause toward link partner 11 = Both symmetric pause and asymmetric pause toward local device	Changed by hardware pin settings
6	Half Duplex	R/W	1 = Advertise half duplex 0 = Do not advertise half duplex	Changed by hardware pin settings
5	Full Duplex	R/W	1 = Advertise full duplex 0 = Do not advertise full duplex	Changed by hardware pin settings
4:0	Reserved	RO	Write as 0, ignore on read	00h

Next Page

Bit 15 is used to advertise Next Page ability.

Remote Fault

Bits(13:12) indicate the Remote Fault status: No remote fault, link failure, offline, or auto-negotiation error.

Pause

Bits (8:7) indicate the Pause status: No pause, symmetric pause, asymmetric pause toward link partner, or both symmetric pause and asymmetric pause toward local device.

Half Duplex

When sit, bit 6 advertises half-duplex capability.

Full Duplex

When set, bit 5 advertises full-duplex capability.

1000BASE-X Auto-Negotiation Link Partner Ability

Register address bits [7:0] = 05h.

Table 96: 1000BASE-X Auto-Negotiation Link Partner Ability Register (Address 05h)

Bit	Name	R/W	Description	Default
			1000BASE-X Mode	
15	Next Page	RO	1 = Link partner is Next Page able 0 = Link partner is not Next Page able	0
14	Acknowledge	RO	1 = Link partner has received link codeword 0 = Link partner has not received link codeword	0
13:12	Remote Fault	RO	00 = No remote fault 01 = Link failure 10 = Offline 11 = Auto-negotiation error	00
11:9	Reserved	RO	Ignore on read	000
8:7	Pause	RO	00 = No pause 01 = Symmetric pause 10 = Asymmetric pause toward link partner 11 = Both symmetric pause and asymmetric pause toward local device	00
6	Half-Duplex Capable	RO	1 = Link partner is half-duplex capable 0 = Link partner is not half-duplex capable	0
5	Full-Duplex Capable	RO	1 = Link partner is full-duplex capable 0 = Link partner is not full-duplex capable	0
4:0	Reserved	RO	Ignore on read	00000
			SGMII Slave Mode	
When SGMII slave mode is enabled, then reading the registers will reflect values sent from the link partner. The SGMII word received is:				
15	Copper Link	RO	1 = There is a copper link 0 = There is no copper link	0
14	Acknowledge	RO	1 = Link partner has received link codeword 0 = Link partner has not received link codeword	0
13	Reserved	RO	Write as 0, ignore on read	0
12	Copper Duplex	RO	1 = Duplex 0 = Half-duplex	0
11:10	Copper Speed	RO	00 = 10BASE-T 01 = 100BASE-TX 10 = 1000BASE-T 11 = Reserved	00
9:1	Reserved	RO	Write as 0, ignore on read	00h

Table 96: 1000BASE-X Auto-Negotiation Link Partner Ability Register (Address 05h) (Cont.)

Bit	Name	R/W	Description	Default
0	SGMII Selector	RO	1 = SGMII selected 0 = 1000BASE-X selected	0

Next Page

This bit indicates whether the link partner is Next Page able:

- 1 = Link partner is Next Page able
- 0 = Link partner is not Next Page able

Acknowledge

This bit indicates whether the link partner has received the link codeword:

- 1 = Link partner has received link codeword
- 0 = Link partner has not received link codeword

Remote Fault

This bit indicates the remote fault status:

- 00 = No remote fault
- 01 = Link failure
- 10 = Offline
- 11 = Auto-negotiation error

Pause

This bit defines the pause-type:

- 00 = No pause
- 01 = Symmetric pause
- 10 = Asymmetric pause toward link partner
- 11 = Both symmetric pause and asymmetric pause toward local device

Half-Duplex Capable

This bit indicates whether the link partner is half-duplex capable:

- 1 = Link partner is half-duplex capable
- 0 = Link partner is not half-duplex capable

Full-Duplex Capable

This bit indicates whether the link partner is full-duplex capable:

- 1 = Link partner is full-duplex capable
- 0 = Link partner is not full-duplex capable

Copper Link

This bit indicates whether there is a copper link:

- 1 = There is a copper link
- 0 = There is no copper link

Acknowledge

This bit indicates whether the link partner has received the link codeword:

- 1 = Link partner has received link codeword
- 0 = Link partner has not received link codeword

Copper Duplex

This bit indicates the duplex-type of the copper link:

- 1 = Duplex
- 0 = Half-duplex

Copper Speed

This bit indicates the copper speed:

- 00 = 10BASE-T
- 01 = 100BASE-TX
- 10 = 1000BASE-T
- 11 = Reserved

SGMII Selector

This bit indicates the status of SGMII selection:

- 1 = SGMII selected
- 0 = 1000BASE-X selected

1000BASE-X Auto-Negotiation Secondary SerDes Register

Register address bit [7:0] = 6.

Table 97: 1000BASE-X Auto-Negotiation Secondary SerDes Register

Bit	*Name*	*R/W*	*Description*	*Default*
15:7	Reserved	RO	Ignore on read	000h
6	Next Page Receive Location Able	RO H	1 = Register 6.5 determines next page receive location 0 = Register 6.5 does not determine next page receive location	1
5	Next Page Receive Location	RO H	1 = Next pages stored in register 8 0 = Next pages stored in register 5	1
4:3	Reserved	RO	Ignore on read	00
2	Next Page Ability	RO H	1 = Local device is next page able 0 = Local device is not next page able	1
1	Page Received	RO LH	1 = New link code word has been received 0 = New link code word has not been received	0
0	Reserved	RO	Ignore on read	0

Next Page Receive Location Able

The BCM5482S returns 1 when Register 6.5 determines next page receive location; otherwise, it returns 0.

Next Page Receive Location

The BCM5482S returns 1 when next pages are stored in register 8. It returns 0 when next pages are stored in register 5.

Next Page Ability

The BCM5482S returns 1 if the local device is next page able; otherwise, it returns 0.

Page Received

The BCM5482S returns 1 when a new link code word has been received from the link partner since the last time this register was read; otherwise, it returns 0.

1000BASE-X Auto-Negotiation Next Page Transmit

Register address bit [7:0] = 07h.

Table 98: 1000BASE-X Auto-Negotiation Next Page Transmit Register

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Additional next pages follow 0 = No more next pages to send	0
14	Reserved	RO	Write as 0, ignore on read	0
13	Message Page	R/W	1 = Message page 0 = Unformatted page	1
12	Acknowledge2	R/W	1 = Will comply with message 0 = Cannot comply with message	0
11	Toggle	RO	Toggled by arbitration state machine during next page exchange — write as 0, ignore on read	0
10:0	Code Field	R/W	Message code field or unformatted code field	00 0000 0001

Next Page

Bit 15 of the 1000BASE-X Auto-Negotiation Next Page Transmit register must be set to indicate that more next pages are to be sent. This bit must be cleared to indicate that this is the last next page to be transmitted. When this bit is read, it returns the last value written.

Message Page

Bit 13 of the 1000BASE-X Auto-Negotiation Next Page Transmit register must be set to indicate that a formatted message page is being sent. This bit must be cleared to indicate that an unformatted page is being sent. When this bit is read, it returns the last value written.

Acknowledge2

When this bit is set, the BCM5482S indicates compliance with the next page request. When this bit is cleared, the BCM5482S indicates that it cannot comply with the next page request. When this bit is read, it returns the last value written.

Toggle

This bit toggles between different next page exchanges to ensure a functional synchronization to the link partner.

Code Field

These 11 bits make up the code field defined by IEEE 802.3, Clause 28, Annex C, when sending formatted pages. When sending unformatted next pages, these 11 bits contain an arbitrary data value.

1000BASE-X Auto-Negotiation Link Partner Next Page

Register address bit [7:0] = 08h.

Table 99: 1000BASE-X Auto-Negotiation Link Partner Next Page Register

Bit	Name	R/W	Description	Default
15	Next Page	RO	1 = Additional next pages follow 0 = Sending last page	0

Next Page

Bit 15 of the 1000BASE-X Auto-Negotiation Link Partner Next Page register must be set to indicate that more next pages are to be sent. This bit must be cleared to indicate that this is the last next page to be transmitted. When this bit is read, it returns the last value written.

1000BASE-X Extended Status

Register address bits [7:0] = 0Fh

Table 100: 1000BASE-X Extended Status Register

Bit	Name	R/W	Description	Default
15	1000BASE-X Full-Duplex Capable	RO H	1 = 1000BASE-X full-duplex capable 0 = Not 1000BASE-X full-duplex capable	1
14	1000BASE-X Half-Duplex Capable	RO H	1 = 1000BASE-X half-duplex capable 0 = Not 1000BASE-X half-duplex capable	1
13	1000BASE-T Full-Duplex Capable	RO L	1 = 1000BASE-T full-duplex capable 0 = Not 1000BASE-T full-duplex capable	0
12	1000BASE-T Half-Duplex Capable	RO L	1 = 1000BASE-T half-duplex capable 0 = Not 1000BASE-T half-duplex capable	0
11:0	Reserved	RO	Ignore on read	000h

1000BASE-X Full-Duplex Capable

The BCM5482S is not capable of 1000BASE-X full-duplex operation and returns 0 when bit 15 of the 1000BASE-X Extended Status register is read.

1000BASE-X Half-Duplex Capable

The BCM5482S is not capable of 1000BASE-X half-duplex operation and returns 0 when bit 14 of the 1000BASE-X Extended Status register is read.

1000BASE-T Full-Duplex Capable

The BCM5482S is capable of 1000BASE-T full-duplex operation and returns 1 when bit 13 of the 1000BASE-X Extended Status register is read.

1000BASE-T Half-Duplex Capable

The BCM5482S is capable of 1000BASE-T half-duplex operation and returns 1 when bit 12 of the 1000BASE-X Extended Status register is read.

Misc 1

Register address bit [7:0] = 10h.

Table 101: Misc 1 Register (Address 10h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:8	Reserved	R/W	Write as 0, ignore on read	00
7	Enable Interrupts	R/W	1 = Interrupts are enabled to output pins 0 = Interrupts are disabled to output pins	0
6	Invert Signal Detect Pin	R/W	1 = Invert SD from pin (active low from pin) 0 = Normal operation (active high from pin)	0
5	Reserved	R/W	Write as 0, ignore on read	00
4	Packet Counter Selector (Secondary serdes register 13h)	R/W	1 = count transmitted packets 0 = count received packets	0
3	Reserved	R/W	Write 0, ignore on red	0
2:1	Error Counter Selector (Secondary SerDes register 14h)	R/W	11 = Transmit error codes 10 = Receive error codes 01 = False carriers 00 = CRC errors	00
0	Extended Packet Length (100-FX mode)	R/W	1 = allow reception of extended length packets in 100fx mode 0 = allow normal length Ethernet packets only	0

Enable Interrupts

When this bit is set, the Secondary SerDes interrupt logic is enabled to output pins, otherwise; it is disabled.

Invert Signal Detect

When this bit is set, the signal detect from the pin is inverted (active low) for the Secondary SerDes, otherwise; it is active high from pin.

Extended Packet Length (100-FX Mode)

When this bit is set, it allows reception of extended length packets in 100fx mode (0 = allow normal length Ethernet packets only).

100BASE-FX Status

Register address bit [7:0] = 11h.

Table 102: 100BASE-FX Status Register (Address 11h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:10	Reserved	RO	Write as 0, ignore on read	00h
9	100FX Link Status Change (SerDes)	RO LH	1 = Link status change since last read 0 = Link status has not changed since last read	0
8	Bad ESD Detected (Premature End)	RO LH	1 = Bad ESD error detected since last read 0 = No error detected since last read	0
7	False Carrier Detected	RO LH	1 = False carrier detected since last read 0 = No error detected since last read	0
6	Transmit Error Detected	RO LH	1 = Received packet with transfer code since last read 0 = No error detected since last read	0
5	Receive Error Detected	RO LH	1 = Receive coding error detected since last read 0 = No error detected since last read	0
4	Lock Timer Expired	RO LH	1 = Unable to lock within 730 µs since last read 0 = Condition not detected occurred since last read	0
3	Lost Lock	RO LH	1 = Lost lock since last read 0 = Lock has not been lost since last read	0
2	Faulting	RO LH	1 = Far end fault detected since last read 0 = No fault detected since last read	0
1	Locked	RO	1 = Enough idles are properly detected to lock 0 = Not locked	0
0	100FX Link (SerDes)	RO	1 = Link is up 0 = Link is down	0

100FX Link Status Change (SerDes)

Bit 9 indicates whether the link status has changed since last read.

Bad ESD Detected (Premature End)

Bit 8 indicates whether a Bad ESD error has been detected since last read.

False Carrier Detected

Bit 7 indicates whether a False carrier has been detected since last read.

Transmit Error Detected

Bit 6 indicates whether a packet with transfer code has been received since last read.

Receive Error Detected

Bit 5 indicates whether a receive coding error has been detected since last read.

Lock Timer Expired

Bit 4 indicates whether there has been an inability to lock within 730 µs of the last read.

Lost Lock

Bit 3 indicates whether there has been a Lost lock since last read.

Faulting

Bit 2 indicates whether a Far end fault has been detected since last read.

Locked

Bit 1 indicates whether enough idles are properly detected to lock.

100FX Link (SerDes)

Bit 0 indicates whether the Link is up.

100BASE-FX Test

Register address bit [7:0] = 12h.

Table 103: 100BASE-FX Test Register (Address 12h)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Write as 0, ignore on read	00h
7	Far End Fault Enable	R/W	1 = Enable f ar-end fault 0 = Disable far-end fault	1
6:0	Reserved	R/W	Write as 0, ignore on read	00h
3:2	Unidirectional	R/W	11 = 100BASE-FX unidirectional enable 00 = Normal operation	00

Far End Fault Enable

When this bit is set, the far end fault is enabled.

Unidirectional

When bit 3:2 is set to 11, the device is able to transmit without a receive section to which to link.

Packet Counter

Register address bit [7:0] = 13h.

Table 104: Packet Counter Register

Bit	Name	R/W	Description	Default
15:0	Packet Counter	R/W CR	Returns the number of packets transmitted/received based on the value of Secondary SerDes register 10h [4]. Freezes at FFFFh. Cleared by read. Increment test mode controlled by Secondary SerDes register 10h [3].	0000h

Packet Counter

When these bits are set in the Packet Counter register, either receive or transmit packets are counted. This counter is cleared on read and freezes at FFFFh. Increment test mode is controlled by Secondary SerDes register 10h [3].

Error Counter

Register address bit [7:0] = 14h.

Table 105: Error Counter Register

Bit	Name	R/W	Description	Default
15:0	Error Counter	R/W CR	Returns the number of errors selected by Secondary SerDes register 10h [2:1]. Freezes at FFFFh. Cleared by read. Increment test mode controlled by Secondary SerDes register 10h [3].	0000h

Error Counter

When these bits are set, the Error Counter register returns the number of errors selected by Secondary SerDes register 10h [2:1]. This counter is cleared on read and freezes at FFFFh. Increment test mode is controlled by Secondary SerDes register 10h [3].

SGMII Slave

Register address bits [7:0] = 15h.

Table 106: SGMII Slave Register (Address 15h)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	Write as 0, ignore on read	00h
9	SerDes Link	RO	1 = Link up in fiber, SGMII slave, or 100BASE-FX modes 0 = Link down	0
8	SerDes Duplex	RO	1 = SerDes full-duplex 0 = SerDes half-duplex or auto-negotiation in progress	1
7:6	SerDes Speed	RO	10 = SerDes speed 1000 (SGMII 1000 or 1000BASE-X) 01 = SerDes speed 100 (SGMII 100 or 100BASE-FX) 00 = SerDes speed 10 (SGMII 10) 11 = Reserved	10
5	SerDes Link Status Change	RO LH	1 = Link status change detected since last read 0 = Link status change not detected since last read	0
4:2	Reserved	RO	Write as 0, ignore on read	010
1	SGMII Slave Mode	R/W	1 = Enable SGMII slave mode 0 = Disable SGMII slave mode	0
0	SGMII Slave Auto-Detection	R/W	1 = Enable SGMII slave auto-detection. Switch between 1000BASE-X and SGMII slave modes based on SerDes-received auto-negotiation code word. 0 = Normal operation	0

SerDes Link

Bit 9 of the SGMII Slave register is 1 when the link is up and the BCM5482S is in SGMII or media converter modes.

SerDes Duplex

Bit 8 of the SGMII Slave register provides the status of the full-duplex/half/duplex:

- 1 = SerDes full-duplex
- 0 = SerDes half-duplex or auto-negotiating in progress

SerDes Speed

Bits [7:6] of the SGMII Slave register provide the status of SerDes speeds:

- 10 = SerDes speed 1000 (SGMII 1000BASE or 1000BASE-X)
- 01 = SerDes speed 100 (SGMII 100BASE or 100BASE-FX)
- 00 = SerDes speed 10 (SGMII 10)
- 11 = Reserved

SerDes Link Status Change

Bit 5 of the SGMII Slave register detects a SerDes link status change since the last read.

SGMII Slave Mode

Bit 1 of the SGMII Slave register enables the SGMII slave modes when the BCM5482S is in fiber mode.

SGMII Slave Auto-Detection

Bit 0 of the SGMII Slave Auto-Detection register enables auto-detection between 1000BASE-X and SGMII slave modes based on SerDes-received auto-negotiation code word when the BCM5482S is in fiber mode.

Note: Follow the steps described in register 1Ch, shadow 14, bit 4 when switching between 100BASE-FX and 1000BASE-X/SGMII slave.

Secondary SerDes Control

Register address [7:0] = 16h.

Table 107: Secondary SerDes Control Register

Bit	Name	R/W	Description	Default
15:6	Reserved	R/W	Write as 0, ignore on read	00h
5	SerDes Detect Enable	R/W	1 = Forces synchronization to fail if signal detect is not active. Disabled if register 1ch shadow 10100[1] = 0. 0 = Ignore signal detect pin	1
2:4	Reserved	R/W	Write as 0, ignore on read	0
1	SerDes Auto-Negotiation Parallel Detect Enable	R/W	1 = Turn auto-negotiation on/off to link up with link partner. Algorithm based on received code words 0 = Disable parallel detection	1
0	Reserved	R/W	Write as 0, ignore on read	0

SerDes Detect Enable

Setting this bit to 1 will force synchronization to fail if the signal detect pin is not active.

SerDes Auto-Negotiation Parallel Detect Enable

Setting this bit enables parallel detection. When the Auto_Negotation bit 12 of the Secondary SerDes register 00h is disabled, the parallel detect function looks for a valid incoming code word on the SerDes inputs. When it receives a valid
A/N code word, it enables the Auto_Neg function to attempt to link.

If Parallel Detect bit and Auto_Neg bit 12 of Secondary SerDes register 00h is enabled, but there is no link, the parallel detect function will turn off the A/N function and attempt to link to the link partner in force mode 1000-X.

Misc 1000BASE-X Control 2

Register address [7:0] = 17h.

Table 108: Misc 1000BASE-X Control 2 Register

Bit	Name	R/W	Description	Default
15:7	Reserved	RO	Write as 0, ignore on read	000h
6	SerDes Transmit Disable	R/W	1 = Force all SerDes transmit data to 0 0 = Normal operation	0
5	Signal Detect Enable	R/W	1 = Force synchronization to fail if signal detect is not active. Disabled if register 1ch shadow 10100[1] = 0. 0 = Ignore signal detect pin	1

Table 108: Misc 1000BASE-X Control 2 Register (Cont.)

Bit	Name	R/W	Description	Default
4	Disable GBIC Updates From GPHY SerDes	R/W	1 = Use register 4 for SerDes auto-negotiation. Do not allow GBIC updates from GPHY SerDes. 0 = Allow register 4 to update when GPHY SerDes is in GBIC mode.	0
3	Force XMIT = Data	R/W	1 = Force XMIT = data regardless of state of receive channel 0 = Normal operation	0
2:0	Reserved	RO	Write as 0, ignore on read	000

SerDes Transmit Disable

When set, bit 6 of the Misc 1000BASE-X Control 2 register forces all SerDes transmit data to 0.

Signal Detect Enable

When set, bit 5 of the Misc 1000BASE-X Control 2 register forces synchronization to fail if the signal detect is not active and is disabled if register 1ch shadow 10100[1] = 0.

Disable GBIC Updates from GPHY SerDes

Use register 4 of the Misc 1000BASE-X Control 2 register for SerDes auto-negotiation. Do not allow GBIC updates from GPHY SerDes. 0 allows register 4 to update when GPHY SerDes is in GBIC mode.

Force XMIT = Data

Bit 3 of the Misc 1000BASE-X Control 2 register forces XMIT = data regardless of state of receive channel. For normal operation, bit 3 must be 0.

Misc 1000-X Control 3

Register address [7:0] = 18h.

Table 109: Misc 1000-X Control 3 Register

Bit	Name	R/W	Description	Default
15:9	Reserved	RO	Write as 0, ignore on read	00h
8	XMIT = Data	RO	1 = SerDes is in the XMIT = data state 0 = SerDes is in the XMIT = config or idle state	0
7	Fiber SD (directly from pin, no inversion or filtering)	RO	1 = Fiber signal detect from pin is high 0 = Fiber signal detect from pin is low	0

Table 109: Misc 1000-X Control 3 Register (Cont.)

Bit	Name	R/W	Description	Default
6	SD Amplitude Status	RO	1 = Signal detect amplitude is above the minimum threshold 0 = Signal detect amplitude is below the minimum threshold	0
5	SD Amplitude Status Changed	RO LH	1 = Signal detect amplitude status has changed since last read 0 = Signal detect amplitude status has not changed since last read	0
4:1	Reserved	RO	Write as 0, ignore on read	0000
0	Enable CRC Fragment Errors	R/W	1 = Enable SerDes CRC checker to count fragments ASCRC errors 0 = Normal operation	0

XMIT = Data

Bit 8 of the Misc 1000-X Control 3 register returns 1 when SerDes is in the XMIT = data state; it returns 0 when SerDes is in the XMIT = config or idle state.

Fiber SD

Bit 7 of the Misc 1000-X Control 3 register returns 1 when the fiber signal detect from pin is high; it returns 0 when the fiber signal detect from pin is low.

SD Amplitude Status

Bit 6 of the Misc 1000-X Control 3 register returns 1 when the signal detect amplitude is above the minimum threshold. It returns 0 when the signal detect amplitude is below the minimum threshold.

SD Amplitude Status Changed

Bit 5 of the Misc 1000-X Control 3 register returns 1 when signal detect amplitude status has changed since last read; otherwise, it returns 0.

Enable CRC Fragment Errors

When set, bit 0 of the Misc 1000-X Control 3 register enables the SerDes CRC checker to count fragments ASCRC errors.

Auto-Negotiation 1000BASE-X Debug

Register address [7:0] = 1Ah.

Table 110: Auto-Negotiation 1000BASE-X Debug Register

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	Write as 0, ignore on read	00h
9	Consistency Mismatch	RO LH	1 = Consistency mismatch occurred since last read 0 = No consistency mismatch occurred since last read	0
8	RUDI Invalid	RO LH	1 = RUDI invalid detected since last read 0 = No RUDI invalid detected since last read	0
7	Sync_Status Detected	RO LH	1 = Sync_Status detected since last read 0 = No Sync_Status detected since last read	0
6	Link Went Down From Loss Of Sync	RO LH	1 = A valid link went down from a loss of synchronization for over 10 ms 0 = Failure condition has not been detected since last read	0
5	Idle Detect State	RO LH	1 = Idle detect state entered since last read 0 = Idle detect state has not been entered since last read	0
4	Complete Acknowledge State	RO LH	1 = Complete acknowledge state entered since last read 0 = Complete acknowledge state has not been entered since last read	0
3	Acknowledge Detect State	RO LH	1 = Acknowledge detect state entered since last read 0 = Acknowledge detect state has not been entered since last read	0
2	Ability Detect State	RO LH	1 = Ability detect state entered since last read 0 = Ability detect state has not been entered since last read	0
1	Error State (external reg 1b [3] = 1)	RO LH	1 = Error state entered since last read 0 = Error state has not been entered since last read	0
	Sync_Status Failed (external reg 1b [3] = 0)	RO LH	1 = Sync_Status failed since last read 0 = Sync_Status has not failed since last read	
0	AN_Enable State	RO LH	1 = AN_Enable state entered since last read 0 = AN_Enable state has not been entered since last read	0

Consistency Mismatch

Bit 9 of the Auto-Negotiation 1000BASE-X Debug register indicates a consistency mismatch occurred since last read.

RUDI Invalid

Bit 8 of the Auto-Negotiation 1000BASE-X Debug register indicates a RUDI (Rx_UnitData Indicate, specified in IEEE 36.2.5.1.6) invalid detected since last read.

Sync Status Detected

Bit 7 of the Auto-Negotiation 1000BASE-X Debug register indicates a sync status was detected since last read.

AN_Sync_Status

Bit 6 of the Auto-Negotiation 1000BASE-X Debug register indicates the AN_Sync_Status has not failed since last read.

Idle Detect State

Bit 5 of the Auto-Negotiation 1000BASE-X Debug register indicates the idle detect state entered since last read.

Complete Acknowledge State

Bit 4 of the Auto-Negotiation 1000BASE-X Debug register indicates the complete acknowledge state entered since last read.

Acknowledge Detect State

Bit 3 of the Auto-Negotiation 1000BASE-X Debug register indicates the acknowledge detect state entered since last read.

Ability Detect State

Bit 2 of the Auto-Negotiation 1000BASE-X Debug register indicates the ability detect state entered since last read.

Error State

Bit 1 of the Auto-Negotiation 1000BASE-X Debug register indicates an error state entered since last read.

Sync Status Failed

Bit 1 of the Auto-Negotiation 1000BASE-X Debug register also indicates the sync status has failed since last read.

AN_Enable State

Bit 0 of the Auto-Negotiation 1000BASE-X Debug register indicates the AN_Enable state entered since last read.

Secondary SerDes Auxiliary 1000BASE-X Control Register

Register address bits[7:0] = 1Bh.

Table 111: Secondary SerDes Auxiliary 1000BASE-X Control Register (Address 1Bh)

Bit	Name	R/W	Description	Default
15:5	Reserved	R/W	Write as 0, ignore on read	000h
4	Disable Remote Fault Sensing	R/W	1 = Disable automatic remote fault sensing of auto-negotiation resolution error and offline errors in media converter mode 0 = Normal operation	0
3	Auto-negotiation Error Timer Enable	R/W	Enables auto-negotiation error timer	0
2	Comma Detect Enable	R/W	1 = Enable comma detection 0 = Disable comma detection	1
1	1000BASE-X PCS Transmit, SGMII 10/100BASE-T Transmit, and Receive FIFO Elasticity	R/W	1 = High elasticity to support jumbo packets (supports 10/100/1000 jumbo packets) 0 = Low elasticity (low latency)	1
0	Disable CRC Checker	R/W	1 = Disable CRC checker 0 = Enable CRC checker	1

Disable Remote Fault Sensing

When set, bit 4 disables automatic remote fault sensing of auto-negotiation resolution error and offline errors in media converter mode.

Auto-negotiation Error Timer Enable

When set, bit 3 enables the auto-negotiation error timer.

Comma Detect Enable

When set, bit 2 enables comma detection.

1000BASE-X PCS Transmit, SGMII 10/100BASE-T Transmit, and Receive FIFO Elasticity

When set, bit 1 enables high elasticity to support 10/100/1000 jumbo packets.

Disable CRC Checker

When set, bit 0 disables the CRC checker.

Auxiliary 1000BASE-X Status

Register address [7:0] = 1Ch.

Table 112: Auxiliary 1000BASE-X Status Register

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	Write as 0, ignore on read	00h
9	SerDes Link Status Change	RO LH	1 = Link status change has occurred since last read 0 = Link status change has not occurred since last read	0
8	SGMII Selector Mismatch	RO LH	1 = SGMII selector mismatch in SGMII slave mode 0 = Fiber or 100BASE-FX mode, or SGMII selector does not mismatch, or auto-negotiation disabled	0
7	Auto-Negotiation Resolution Error	RO LH	1 = Auto-negotiation HCD is none (no common half or full-duplex abilities) 0 = SGMII slave mode, or auto-negotiation disabled, or no resolution error	0
6:5	Link Partner Remote Fault	RO LH	1000BASE-X register 5 [13:12]	00
4	Auto-Negotiation Page Received	RO LH	1 = Page has been received since last read 0 = Page has not been received since last read	0
3	Current Operating Duplex Mode	RO LH	1 = PHY is operating in full-duplex mode 0 = PHY is operating in half-duplex mode (or auto-negotiation has not completed)	0
2	SerDes Link	RO LH	1 = Link is up for SerDes applications 0 = Link is down for SerDes applications	0
1	PAUSE Resolution—Receive Side	RO LH	1 = Enable PAUSE receive 0 = Disable PAUSE receive	0
0	PAUSE Resolution—Transmit Side	RO LH	1 = Enable PAUSE transmit 0 = Disable PAUSE transmit	0

Secondary SerDes Link Status Change

Bit 9 of the Auxiliary 1000BASE-X Status register detects a link status change since last read.

SGMII Selector Mismatch

Bit 8 of the Auxiliary 1000BASE-X Status register indicates an SGMII selector mismatch in SGMII mode.

Auto-negotiation Resolution Error

Bit 7 of the Auxiliary 1000BASE-X Status register indicates auto-negotiation HCD is none (no common half-duplex or full-duplex abilities).

Link Partner Remote Fault

Bits [6:5] of the Auxiliary 1000BASE-X Status register indicates the link partner remote fault status reflected from
1000BASE-X register 05h bits [13:12].

Auto-negotiation Page Received

Bit 4 of the Auxiliary 1000BASE-X Status register indicates auto-negotiation page has been received since last read.

Current Operating Duplex Mode

Bit 3 of the Auxiliary 1000BASE-X Status register indicates the PHY is operating in full-duplex mode.

SerDes Link

Bit 2 of the Auxiliary 1000BASE-X Status register indicates that the link is up for SerDes applications.

PAUSE Resolution—Receive Side

Bit 1 of the Auxiliary 1000BASE-X Status register indicates receive pause resolution.

PAUSE Resolution—Transmit Side

Bit 0 of the Auxiliary 1000BASE-X Status register indicates transmit pause resolution.

Misc 1000BASE-X Status

Register address [7:0] = 1Dh.

Table 113: Misc 1000BASE-X Status Register

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	Write as 0, ignore on read	00h
9	Transmit FIFO Error	RO LH	1 = Transmit FIFO error since last read 0 = No transmit FIFO error since last read	0
8	Receive FIFO Error	RO LH	1 = Receive FIFO error since last read 0 = No receive FIFO error since last read	0
7	Bad FIFO Pointer	RO LH	1 = FIFO pointer all 0s since last read 0 = Bad FIFO pointer has not occurred since last read	0
6	Reserved	RO	Ignore on read	0
5	False Carrier Detected (RX Side)	RO LH	1 = False carrier detected on SerDes receiver since last read 0 = No false carriers detected since last read	0
4	CRC Error Detected	RO LH	1 = CRC error detected since last read 0 = No CRC error detected since last read or mode is disabled via register 1ch shadow 27 [0]	0
3	Transmit Error Detected	RO LH	1 = Transmit error code detected since last read (rx_data_error state in PCS receive) 0 = No transmit error code detected since last read	0
2	Receive Error Detected	RO LH	1 = Receive error since last read (early_end state in PCS receive) 0 = No receive error since last read	0
1	Carrier Extend Error Detected	RO LH	1 = Carrier extend error since last read (extend_err state in PCS receive) 0 = No carrier extend error since last read	0
0	Early End Extension Detected	RO LH	1 = Early end extension since last read (early_end_ext state in PCS receive) 0 = No early end extension since last read	0

Transmit FIFO Error

Bit 9 of the Misc 1000BASE-X Status register indicates a FIFO transmit error since the last read.

Receive FIFO Error

Bit 8 of the Misc 1000BASE-X Status register indicates a FIFO receive error since the last read.

Bad FIFO Pointer

Bit 7 of the Misc 1000BASE-X Status register indicates that the FIFO pointer is all 0s since the last read.

False Carrier Detected

Bit 5 of the Misc 1000BASE-X Status register indicates a false carrier detected since the last read.

CRC Error Detected

Bit 4 of the Misc 1000BASE-X Status register indicates a CRC error detected since the last read.

Transmit Error Detected

Bit 3 of the Misc 1000BASE-X Status register indicates a transmit error code detected since the last read.

Receive Error Detected

Bit 2 of the Misc 1000BASE-X Status register indicates a receive error code detected since the last read.

Carrier Extend Error Detected

Bit 1 of the Misc 1000BASE-X Status register indicates a carrier extend error since the last read.

Early End Extension Detected

Bit 0 of the Misc 1000BASE-X Status register indicates an early end extension since the last read.

Spare Register

Register address [7:0] = 21h.

Table 114: Spare Register

Bit	*Name*	*R/W*	*Description*	*Default*
15:8	Reserved	R/W	Write as 1, ignore on read	FFh
7:1	Reserved	R/W	Write as 0, ignore on read	00h
0	Invert Interrupt	R/W	1 = Active high interrupt on output pin 0 = Active low interrupt on output pin	0

Invert Interrupt

Bit 0 of the Spare register returns 1 when there is an active high interrupt on the output pin; it returns 0 when there is an active low interrupt on the output pin.

Secondary SerDes Interrupt Status

Register address bits [7:0] = 30h.

Table 115: Secondary SerDes Interrupt Status Register (Address 30h)

Bit	Name	R/W	Description	Default
15:13	Reserved	RO	Write as 0, ignore on read	000
12	SerDes CRC Error	RO LH	1 = SerDes CRC error detected since last read 0 = No SerDes CRC error detected since last read	0
11	SGMII Slave Mode Change	RO LH	1 = SGMII slave mode changed since last read 0 = No SGMII slave mode changes since last read	0
10	100BASE-FX SerDes Mode Change	RO LH	1 = 100BASE-FX SerDes mode changed since last read 0 = No 100BASE-FX SerDes mode changes since last read	0
9	SerDes Auto-negotiation Page Received	RO LH	1 = SerDes auto-negotiation page received 0 = No SerDes auto-negotiation pages received	0
8	Secondary SerDes Select Change (SGMII: fiber enabled or disabled)	RO LH	1 = Secondary SerDes select changed since last read 0= No Secondary SerDes select changes since last read	0
7	Signal Detect Amplitude Change	RO LH	1 = Signal detect amplitude changed since last read 0 = No signal detect amplitude changes since last read	0
6	SerDes Link Status Change	RO LH	1 = SerDes link status changed since last read 0 = No SerDes link status changes since last read	0
5	Lost Sync Status	RO LH	1 = Loss of synchronization since last read 0 = No loss of synchronization since last read	0
4	Rudi-C Detected (auto-negotiation codeword received)	RO LH	1 = Rudi-C detected since last read 0 = No Rudi-C detected since last read	0
3	SerDes Auto-negotiation Error	RO LH	1 = SerDes auto-negotiation error detected since last read (SGMII or 1000BASE-X selector mismatch, no HCD, or remote fault detected from link partner) 0 = No SerDes auto-negotiation detected since last read	0
2	Idle Codeword Detected	RO LH	1 = Idle codeword is detected since last read 0 = Idle codeword was not detected since last read	0
1	Reserved	RO LH	Write as 0, ignore on read	0
0	Reserved	RO LH	Write as 0, ignore on read	0

SerDes CRC Error

This bit indicates a transmit CRC error has occurred since this register was last read:

- 1 = SerDes CRC error detected since last read
- 0 = No SerDes CRC error detected since last read

SGMII Slave Mode Change

This bit indicates SGMII slave mode changed since this register was last read:

- 1 = SGMII slave mode changed since last read
- 0 = No SGMII slave mode changes since last read

100BASE-FX SerDes Mode Change

This bit indicates 100BASE-FX mode changed since this register was last read:

- 1 = 100BASE-FX SerDes mode changed since last read
- 0 = No 100BASE-FX SerDes mode changes since last read

SerDes Auto-negotiation Page Received

This bit indicates the auto-negotiation page received:

- 1 = SerDes auto-negotiation page received
- 0 = No SerDes auto-negotiation pages received

Secondary SerDes Select Change

This bit indicates Secondary SerDes mode select changes since this register was last read:

- 1 = Secondary SerDes select changed since last read
- 0= No Secondary SerDes select changes since last read

Signal Detect Amplitude Change

This bit indicates a change in the signal amplitude detector logic since this register was last read:

- 1 = Signal detect amplitude changed since last read
- 0 = No signal detect amplitude changes since last read

SerDes Link Status Change

This bit indicates there is a change in the link status since this register was last read:

- 1 = SerDes link status changed since last read
- 0 = No SerDes link status changes since last read

Lost Sync Status

This bit indicates loss of synchronization since this register was last read:

- 1 = Loss of synchronization since last read
- 0 = No loss of synchronization since last read

Rudi-C Detected

This bit indicate a SerDes auto-negotiation code word is detected since this register was last read:

- 1 = Rudi-C detected since last read
- 0 = No Rudi-C detected since last read

SerDes Auto-negotiation Error

This bit indicates an error detected since last read during auto-negotiation error when the device is in the 1000BASE-x or SGMII mode (selector mismatch, no HCD, or remote fault was detected):

- 1 = SerDes auto-negotiation error detected since last read (SGMII or 1000BASE-X selector mismatch, no HCD, or remote fault detected from link partner)
- 0 = No SerDes auto-negotiation detected since last read

Idle Codeword Detected

This bit indicates idle codeword is detected since this register was last read:

- 1 = Idle codeword is detected since last read
- 0 = Idle codeword was not detected since last read

Secondary SerDes Interrupt MASK

Register address bits [7:0] = 31h.

Table 116: Secondary SerDes Interrupt MASK Register (Address 31h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:13	Reserved	RO	Write as 00h, ignore on read	00h
12:0	Secondary SerDes Interrupt Mask	R/W	1 = Interrupt masked (status bits still operate normally but do not generate interrupt output) 0 = Interrupt enabled	FFh

Secondary SerDes Interrupt Mask

These bits indicate a masked interrupt; however, status bits still operate normally but do not generate interrupt output.

Secondary SerDes Lineside Loopback Control

Register address bits[7:0] = 44h.

Table 117: Secondary SerDes Lineside Loopback Control Register

Bit	*Name*	*R/W*	*Description*	*Default*
15:3	Reserved	R/W	Write as 0, ignore on read	00h
2	Secondary SerDes Lineside Loopback	R/W	Enable secondary SerDes lineside loop	0
1:0	Reserved	R/W	Write as 0, ignore on read	00

Secondary SerDes Lineside Loopback

This bit indicates that secondary SerDes lineside loop is enabled.

Section 6: Timing and AC Characteristics

Table 118: Reset Timing

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
Power up to $\overline{\text{RESET}}$ deassertion	RESET_PU	10	–	–	ms
$\overline{\text{RESET}}$ deassertion to normal PHY operation	RESET_WAIT	20	–	–	µs
$\overline{\text{RESET}}$ pulse length	RESET_LEN	2	–	–	µs

Note:

a. When $\overline{\text{RESET}}$ is low, there must be a valid clock signal at the XTALI input and all external power supplies need to be stable.

b. Internal regulator outputs REGSEN{1} and REGSEN{2} need approximately 1 ms to stabilize after the voltage to the regulator input pins REGSUP{1} and REGSUP{2} is stable.

c. MII register read/write access and normal PHY operation can start at the end of the RESET_WAIT time.

d. RESET_PU must be performed when the device is first powered up. Software reset or RESET_LEN do not need to be performed after RESET_PU.

e. Software reset or RESET_LEN should not be performed until after RESET_PU and RESET_WAIT have been completed. After issuing a software reset or a RESET_LEN, normal PHY operation can begin after waiting RESET_WAIT time of 20 µs.

f. Software reset behaves the same as hardware reset (all hardware configuration pins are relatched). CLK125 output remains active and stable during hardware and software reset.

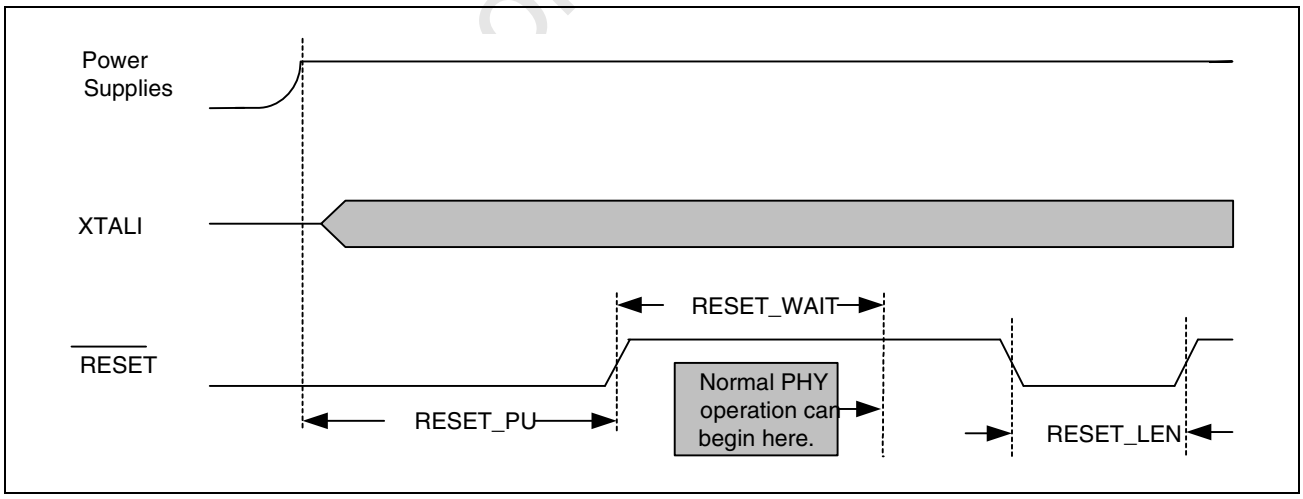


Figure 12: Reset Timing

Table 119: Clock Input Timing

Parameter	Symbol	Minimum	Typical	Maximum	Unit
XTALI cycle time (1/frequency)	X_CT	39.998	40	40.002	ns
XTALI input clock jitter tolerance[a] (Jitter in 12 kHz to 20 MHz range)	–	–	–	1.5	ps RMS
Internal circuitry jitter[b]	–	–	–	200	ppm
XTALI rise/fall time	X_RISE/X_FALL	–	–	5 rise/7 fall	ns
Clock Duty Cycle	X_P_H/X_P_L	45	50	55	%

Note: Do not use PLL-based oscillators or zero-delay buffers as a source for XTALI because this introduces excessive jitter that may result in unacceptable bit error rate performance.

a. Jitter tolerance applies to jitter frequencies between 12 kHz and 20 MHz.
b. Internal circuitry jitter is additive to the input reference clock jitter.

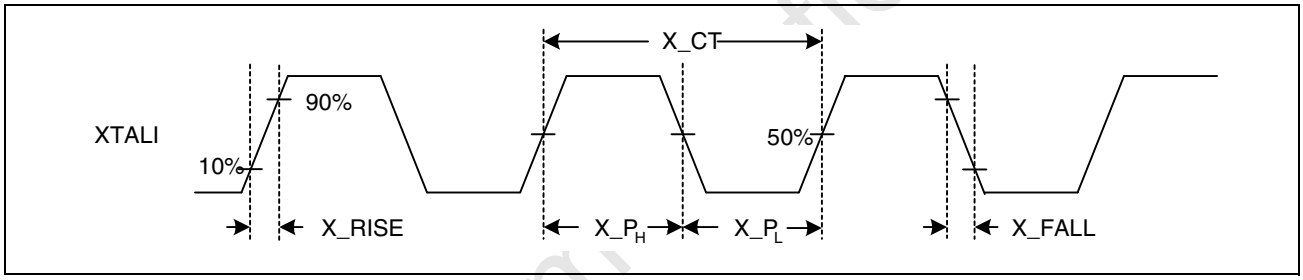


Figure 13: Clock Input Timing

Table 120: Management Interface Timing

Parameter	Symbol	Minimum	Typical	Maximum	Unit
MDC cycle time	MDC_CYCLE	80	–	–	ns
MDC high/low	–	30	–	–	ns
MDIO input setup time to MDC rising	MDIO_SETUP	1	–	–	ns
MDIO input hold time from MDC rising	MDIO_HOLD	1	–	–	ns
MDIO output delay from MDC rising	MDIO_DELAY	0	–	5	ns

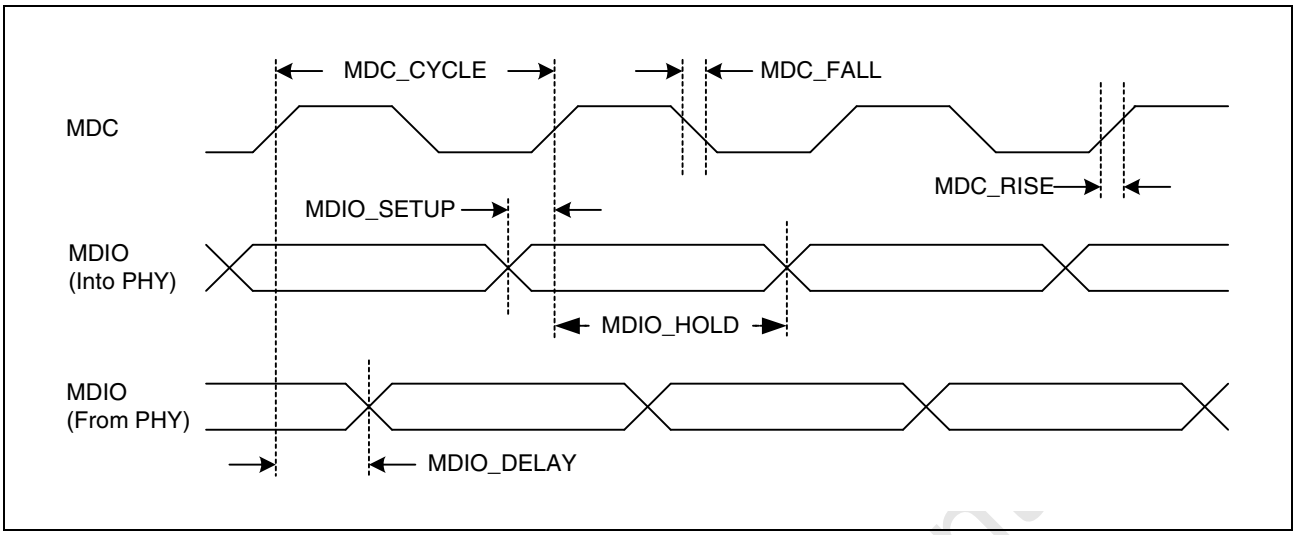


Figure 14: Management Interface Timing

Table 121: RGMII Input Timing (Normal Mode): GTXCLK and TXD[3:0]

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
GTXCLK clock period	–	–	8	–	ns
GTXCLK pulse width	–	3600	–	–	ps
Input setup time	T_setuWp	1000 (normal mode)	–	–	ps
Input hold time	T_hold	1000 (normal mode)	–	–	ps
Required data window at the input	T_setup+T_hold	2000	–	–	ps

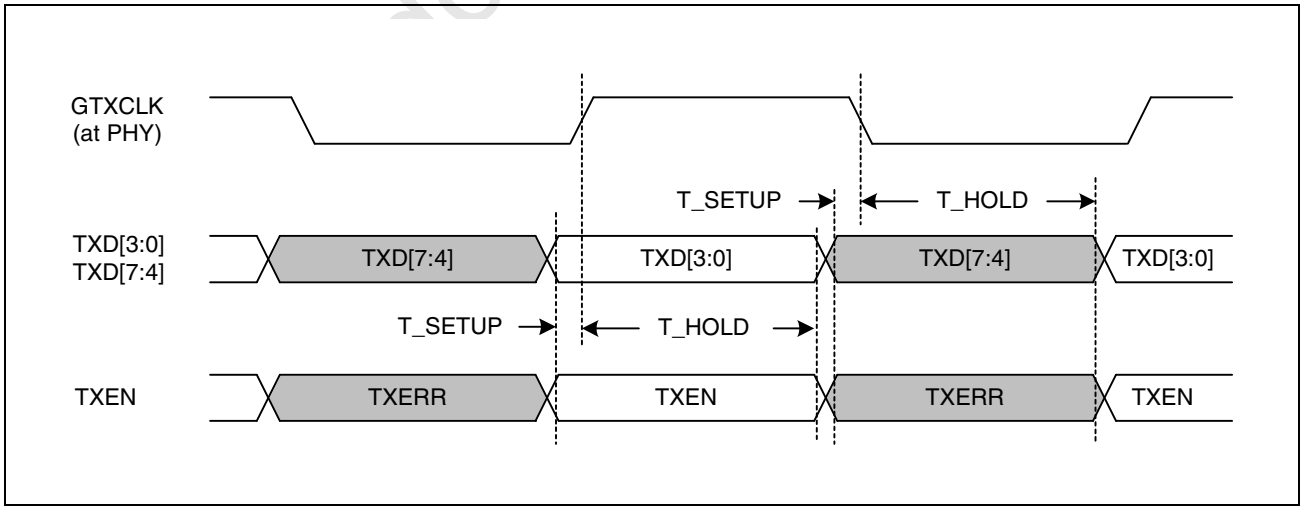


Figure 15: RGMII Input Timing (Normal Mode): GTXCLK and TXD[3:0]

Table 122: RGMII Input Timing (Delayed Mode): GTXCLK and TXD[3:0]

Parameter	Symbol	Minimum	Typical	Maximum	Unit
GTXCLK clock period	–	–	8	–	ns
GTXCLK pulse width	–	3600	–	–	ps
Input setup time	T_setup_{DLY}	–1700 (delayed mode)	–	–	ps
Input hold time	T_hold_{DLY}	2900 (delayed mode)	–	–	ps
Required data window at the input	T_setup_{DLY} + T_hold_{DLY}	1200	–	–	ps

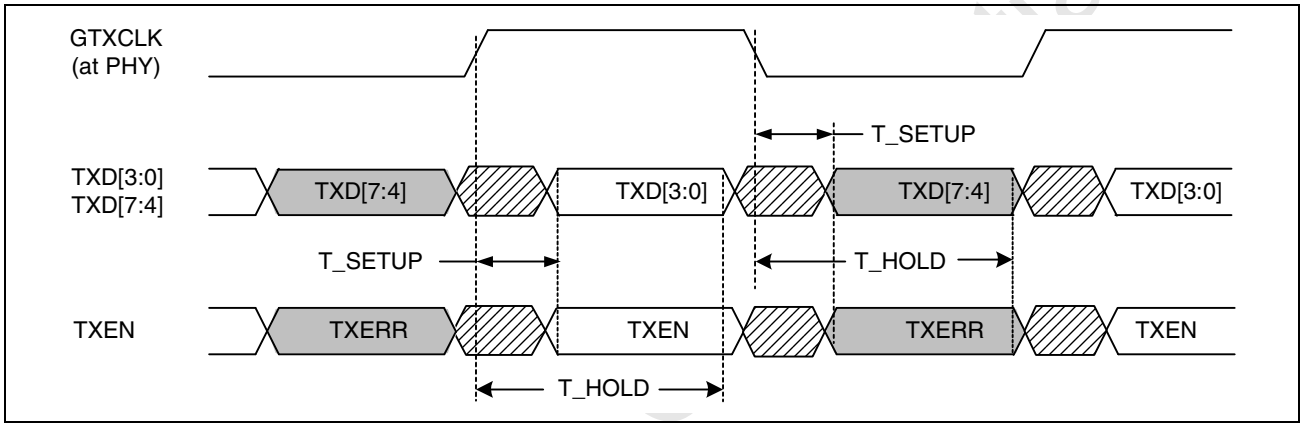


Figure 16: RGMII Input Timing (Delayed Mode): GTXCLK and TXD[3:0]

Table 123: RGMII Output Timing (Normal Mode): RXC and RXD[3:0]

Parameter	Symbol	Minimum	Typical	Maximum	Unit
RXC clock period	T_clk	–	8.0	–	ns
RXC clock pulse width	T_cw	3.6	–	–	ns
Data valid to clock transition: Available setup time at the output source	T_suav	–500 (normal mode)	–	+500 (normal mode)	ps
Clock transition to data valid: Available hold time at the output source	T_hav	3.1	–	–	ns
Data valid window	T_suav + T_hav	2.6	–	–	ns

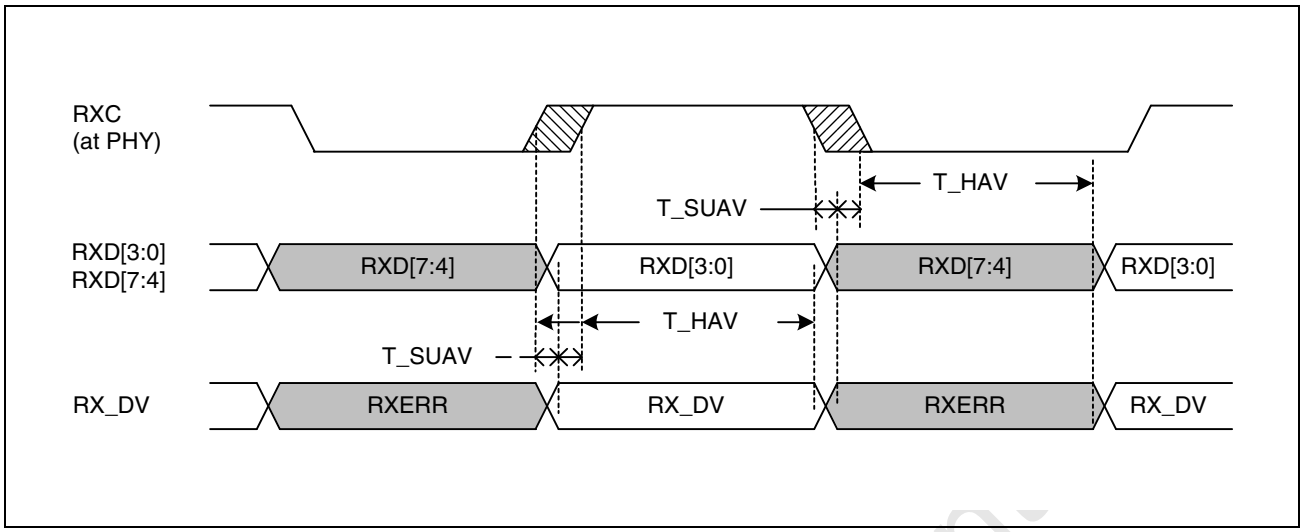


Figure 17: RGMII Output Timing (Normal Mode): RXC and RXD[3:0]

Table 124: RGMII Output Timing (Delayed Mode): RXC and RXD[3:0]

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
RXC clock period	T_clk	–	8.0	–	ns
RXC clock pulse width	T_cw	3.6	–	–	ns
Data valid to clock transition: Available setup time at the output source	T_suav_{DLY}	1400 (delayed mode)	–	2400 (delayed mode)	ps
Clock transition to data valid: Available hold time at the output source	T_hav	1.2	–	–	ns
Data valid window	T_suav + T_hav	2.6	–	–	ns

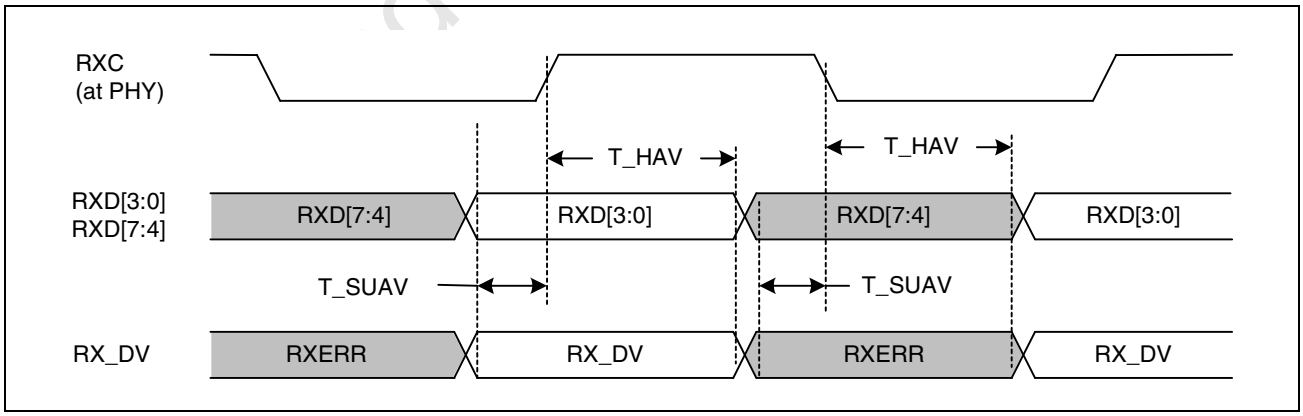


Figure 18: RGMII Output Timing (Delayed Mode): RXC and RXD[3:0]

Table 125: SGMII Timing

Parameter	Symbol	Minimum	Maximum	Unit
Clock Signal Duty Cycle SCLK±	Duty_C	48	52	%
Maximum Pk-PK Clock Jitter SCLK±	T_{JIT}		192	ps pk-pk
Fall Time (20% to 80%) SGOUT_Px±, SCLK±	T_F	100	200	ps
Rise Time (20% to 80%) SGOUT_Px±, SCLK±	T_R	100	200	ps
Skew Between Two Members of a Differential Pair SGOUT_Px±, SCLK±	T_{SKEW}[a]		20	ps
Clock to Data Relationship From Either Edge of the Clock to Valid Data	$T_{CLOCK2Q}$[b]	250	550	ps

a. Measured at 50% transition
b. Measured at 0V differential

Table 126: HSTL Interface AC Timing

Parameter	Symbol	Minimum	Typical	Maximum	Unit
AC differential voltage	V_{Diff}	0.4	–	OVDD1 + 0.60	V
Differential cross-point voltage	V_X	0.69	–	0.90	V
Input signal swing	–	–	1.0	–	V
Differential input signal crossing point	–	–	0.75	–	V
Input signal edge rate	–	10	+1.0	–	V/ns

Section 7: Electrical Characteristics

Table 127: Absolute Maximum Ratings

Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*
Supply voltage (OVDD2)	–	GND – 0.3	3.63	V
Supply voltage (AVDD, PVDD, BIASVDD, XTALVDD, OVDD1)	–	GND – 0.3	2.75	V
Supply voltage (AVDDL, DVDD)	–	GND – 0.3	1.50	V
Storage temperature	T_{STG}	–40	+125	°C
ESD protection	V_{ESD}	–	1000	V

Note: These specifications indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 128: DC Characteristics

Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Condition*
Power Supply					
Supply current 3.3/2.5V	I_{OVDD}	–	See the *5482S Design Guide*	mA	–
Supply voltage 3.3/2.5V	V_{OVDD1}	2.25	3.63	V	–
Supply voltage 3.3/2.5V	V_{OVDD2}	2.25	3.63	V	–
Supply current 2.5V	$I_{AVDD, PVDD, BIASVDD, XTALVDD}$	–	See the *5482S Design Guide*	mA	–
Supply voltage 2.5V	$V_{AVDD, PVDD, BIASVDD, XTALVDD}$	2.37	2.63	V	–
Supply current 1.2V	$I_{AVDDL, DVDD, PLLVDD1, PLLVDD2}$	–	See the *5482S Design Guide*	mA	–
Supply voltage 1.2V	$V_{AVDDL, DVDD, PLLVDD1, PLLVDD2}$	1.14	1.29	V	–
XTALI Pin					
Input low voltage (XTALI)	V_{IL}	–0.30	0.80	V	XTALI Pin
Input high voltage (XTALI)	V_{IH}	1.70	XTALVDD + 0.5	V	XTALI Pin
Digital Pin Operating @ 3.3V OVDD2					
Input high voltage, digital (D) pin	V_{IH}	2.0	OVDD	V	–
Input low voltage, digital (D) pin	V_{IL}	–0.30	0.80	V	–

Table 128: DC Characteristics (Cont.)

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage, digital (D) pin	V_{OH}	OVDD	–	V	I_{OH} = –8 mA
Output low voltage, digital (D) pin	V_{OL}	–	0.40	V	I_{OL} = 8 mA
Digital Pin Operating @ 2.5V OVDD2					
Input high voltage, digital (D) pin	OVDD	1.78	OVDD	V	–
Input low voltage, digital (D) pin	V_{IL}	–0.30	0.70	V	–
Output high voltage, digital (D) pin	V_{OH}	OVDD	–	V	I_{OH} = –8 mA
Output low voltage, digital (D) pin	V_{OL}	–	0.40	V	I_{OL} = 8 mA
RGMII Pin Operating @ 2.5V OVDD1					
Input high voltage, RGMII (G) pin	V_{IH}	1.70	–	V	–
Input low voltage, RGMII (G) pin	V_{IL}	–	0.70	V	–
Output high voltage, RGMII (G) pin	V_{OH}	2.0	OVDD + 0.30	V	I_{OH} = –1 mA
Output low voltage, RGMII (G) pin	V_{OL}	–0.30	00.40	V	I_{OL}= 1 mA
RGMII Pin Operating @ HSTL Levels 1.5V or 1.8V (OVDD1)					
Input high voltage	V_{IH}	OVDD1/2 + 0.10	OVDD1 + 0.30	V	HSTL
Input low voltage	V_{IL}	–0.30	OVDD1/2 – 0.10	V	HSTL
Output high voltage	V_{OH}	OVDD1 – 0.40	–	V	HSTL
Output low voltage	V_{OL}	–	0.40	V	HSTL
SGMII (SerDes) Pin *(see Figure 19 on page ccxlvii)*					
Output High Voltage SGOUT_Px±, SCLK±	V_{OH}	–	1525	mV	Rload = 100Ω ± 1%
Output Low Voltage SGOUT_Px±, SCLK±	V_{OL}	875	–	mV	Rload = 100Ω ± 1%
Output Ringing SGOUT_Px±, SCLK±	V_{ring}	–	10	%	Rload = 100Ω ± 1%
SGMII Output Differential Voltage SGOUT_Px±, SCLK±	$\lvert V_{OD\_SGMII} \rvert$	150	400	mV	$V_{OD} = V_{OA} - V_{OB}$ Rload = 100Ω ± 1%
Output Offset Voltage SGOUT±, SCLK±	V_{OS}	1075	1325	mV	$V_{OS} = (V_{OA} - V_{OB})/2$ Rload = 100Ω ± 1%
Output Impedance (single-ended) SGOUT_Px±, SCLK±	Ro	40	60	Ω	–

Table 128: DC Characteristics (Cont.)

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Mismatch in Pair SGOUT_Px±, SCLK±	DRo	–	10	%	–
Change in V_{OD} between 0 and 1 SGOUT_Px±, SCLK±	$\Delta\|V_{OD}\|$	–	25	mV	–
Change in V_{OS} between 0 and 1 SGOUT_Px±, SCLK±	ΔV_{OS}	–	25	mV	–
Output Current on Short to Ground SGOUT_Px±, SCLK±	I_{SA}, I_{SB}	–	40	mA	–
Power Off Leakage Current SGOUT_Px±, SCLK±	I_{XA}, I_{XB}	–	10	mA	–
Input Voltage range for SGIN_Px+ or SGIN_Px–	V_I	675	1725	mV	–
Input Differential Threshold SGIN_Px±	V_{ID}	–50	50	mV	–
Receiver Differential Input Impedance SGIN_Px±	R_{IN}	80	120	Ω	–
Fiber (SerDes) (AC-Coupled) Pin					
Maximum Input Differential Voltage SGIN_Px±	V_{IDMAX}	–	2000	mV	–
Output Impedance (differential) SGOUT_Px±	Ro	80	120	Ω	–
Output High Voltage SGOUT_Px±	V_{OH}	–	1525	mV	Rload = 100Ω ± 1%
SerDes Output Differential (pk-pk) Voltage SGOUT_Px±	V_{OD_SerDes}	750	1100	mV	$V_{OD} = V_{OA} – V_{OB}$ Rload = 100Ω ± 1%
Receiver Differential Input Impedance SGIN_Px±	R_{IN}	80	120	Ω	–
Total Output Jitter	J_{tpk-pk}	–	192	ps	–
Input Differential Threshold SGIN_Px±	V_{ID}	-50	50	mV	–
TRD Pin					
Output high voltage, analog TRD±[3:0]{4:1}	V_{OH}	–	AVDD + 1.5	V	(A) Pin loaded by transformer and termination
Output low voltage, analog TRD±[3:0]{4:1}	V_{OL}	AVDD – 1.5	–	V	(A) Pin loaded by transformer and termination
RESET MDIO (SDA), MDC (SLC) Pin					
Positive edge threshold	VT+	1.29	1.78	V	$\overline{\text{RESET}}$, MDC(SLC), MDIO(SDA) pins
Negative edge threshold	VT–	1.13	1.60	V	$\overline{\text{RESET}}$, MDC(SLC), MDIO(SDA) pins

Table 128: DC Characteristics (Cont.)

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Hysteresis	V_{HYST}	120	337	mV	$\overline{\text{RESET}}$, MDC(SLC), MDIO(SDA) pins
REGSUP Pin					
Regulator input voltage, REGSUP[2:1] pin	VI_{REGSUP}	1.71	2.62	V	REGSUP
RDAC Pin					
Bias current set	V_{BIAS}	1.15	1.35	V	Voltage across RDAC resistor

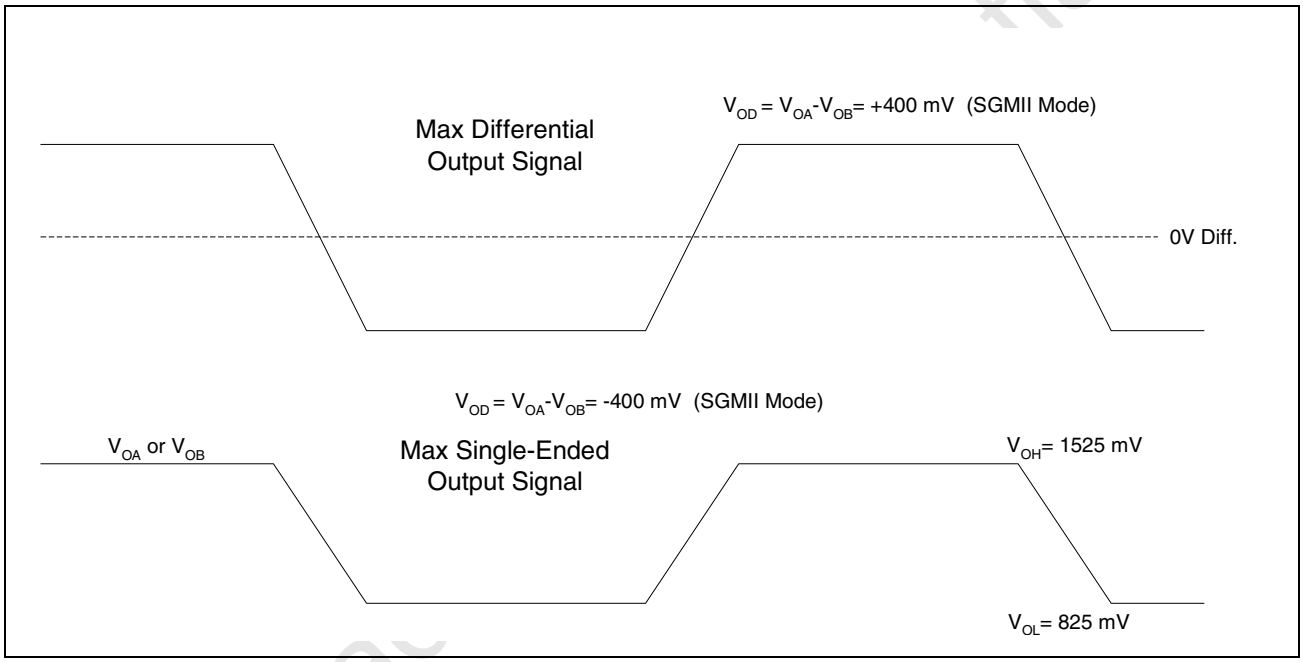


Figure 19: SGMII (SerDes) DC Parameters

Section 8: Mechanical and Thermal Data

RoHS-Compliant Packaging

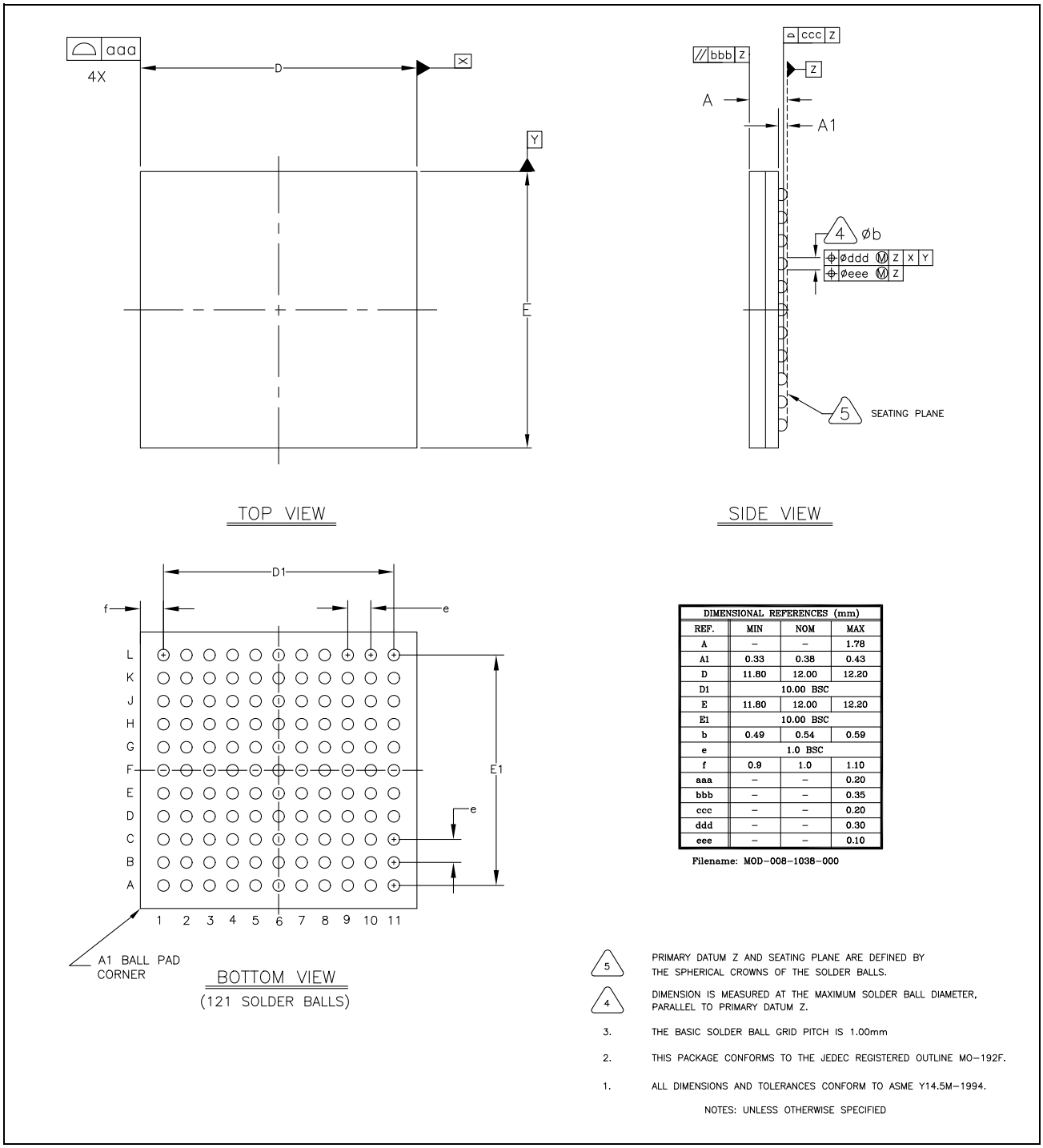
Broadcom offers both a standard package and an RoHS package that is compliant with RoHS and WEEE directives. Standard parts are also compliant with these directives, except for Pb (>1000 ppm). Table 129 shows the main differences between standard and RoHS-compliant parts.

RoHS-compliant parts have the letter G added to the top line of the part marking. Standard parts (non Pb-free parts) are NOT compatible with the Pb-free surface-mount process. Refer to *Reflow Process Guidelines for Surface Mount Assemblies* application note for more details.

Table 129: Main Differences Between Standard and RoHS-Compliant Packages

Part Number	*Solder Ball Composition*	*Maximum Reflow Temperature (°C)*
BCM5482SKFB (standard package)	63%Sn/37%Pb	225
BCM5482SKFBG (RoHS-compliant package)	95.5%Sn/3%Ag/0.5%Cu	260
BCM5482SIFB	63%Sn/37%Pb	225
BCM5482SIFBG	95.5%Sn/3%Ag/0.5%Cu	260

Mechanical Drawings



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.78
A1	0.33	0.38	0.43
D	11.80	12.00	12.20
D1		10.00 BSC	
E	11.80	12.00	12.20
E1		10.00 BSC	
b	0.49	0.54	0.59
e		1.0 BSC	
f	0.9	1.0	1.10
aaa	–	–	0.20
bbb	–	–	0.35
ccc	–	–	0.20
ddd	–	–	0.30
eee	–	–	0.10

Filename: MOD–008–1038–000

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–192F.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 20: 121-Pin FBGA Package

Thermal Information

This section includes basic thermal information pertaining to the BCM5482S 121-pin FBGA package. Table 130 provides a comparison of Theta-J_A versus airflow for the FBGA package. The BCM5482S is designed and rated for a maximum junction temperature of 125°C.

Table 130: Theta-J_A vs. Airflow for the FBGA Package

	Airflow (Feet Per Minute)				
121 FBGA Package	***0***	***100***	***200***	***400***	***600***
Theta-J_A (°C/W)	33.68	31.31	30.10	28.66	27.68

Table 131 provides a comparison of Theta-J_A versus airflow when using the FBGA package with a heat sink (VEF14-14-10B).

Table 131: Theta-J_A vs. Airflow for the FBGA Package with Heat Sink

	Airflow (Feet Per Minute)				
121 FBGA Package	***0***	***100***	***200***	***400***	***600***
Theta-J_A (°C/W)	27.73	23.14	21.37	19.89	19.16

Table 132: Theta-J_B and Theta-J_C

121 FBGA Package	***(°C/W)***
Theta-J_B	15.35
Theta-J_C	12.32

Junction Temperature Estimation and Ψ_{JT} vs. θ_{JC}

Package thermal characterization parameter Psi-J_T (Ψ_{JT}) yields a better estimation of actual device junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta-J_C (θ_{JC}). The reason for this is, θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom and sides of the package. The equation for calculating the device junction temperature is as $T_J = T_T + P \bullet x \Psi_{JT.}$

Where:

- T_J = junction temperature at steady-state condition, °C
- T_T = package case top center temperature at steady-state condition, °C
- P = device power dissipation, Watts
- Ψ_{JT} = package thermal characteristics (no airflow), °C/W

Table 133: 121-FPBGA Psi-Junction Temperature

121 FBGA Package	*°C/W*
Psi-J_T[a]	0.31

a. This package thermal parameter assumes no airflow and no external heat sink.

Section 9: Ordering Information

Part Number	*Package*	*Ambient Temperature*
BCM5482SA2KFB	121-pin FBGA	0°C to 70°C
BCM5482SA2KFBG	121-pin RoHS-compliant FBGA	0°C to 70°C
BCM5482SA2IFB	121-pin FBGA	–40°C to 85°C
BCM5482SA2IFBG	121-pin RoHS-compliant FBGA	–40°C to 85°C
BCM5482SEA2KFB *	121-pin FBGA	0°C to 70°C
BCM5482SEA2KFBG *	121-pin RoHS-compliant FBGA	0°C to 70°C
BCM5482SEA2IFB *	121-pin FBGA	–40°C to 85°C
BCM5482SEA2IFBG *	121-pin RoHS-compliant FBGA	–40°C to 85°C
BCM5482SHA2KFB	121-pin FBGA	0°C to 70°C
BCM5482SHEA2KFB *	121-pin FBGA	0°C to 70°C
BCM5482SHEA2KFBG *	121-pin RoHS-compliant FBGA	0°C to 70°C
BCM5482SHA2KFBG	121-pin RoHS-compliant FBGA	0°C to 70°C
BCM5482SHEA2IFB *	121-pin FBGA	–40°C to 85°C
BCM5482SHEA2IFBG *	121-pin RoHS-compliant FBGA	–40°C to 85°C

***** This device supports Synchronous Ethernet applications.

Note: Use of the internal regulators supplying 1.2V may require a heat sink or airflow. Industrial temperature versions require a heat sink and airflow, and cannot use the internal regulators supplying 1.2V. Please see your Broadcom representative for additional information.

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