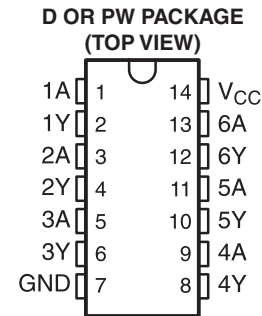


HEX BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

Check for Samples: [SN74LVC07A-Q1](#)

FEATURES

- Qualified for Automotive Applications
- Operates From 1.65 V to 5 V
- Inputs and Open-Drain Outputs Accept Voltages up to 5.5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17



DESCRIPTION/ORDERING INFORMATION

This hex buffer/driver is designed for 1.65-V to 5.5-V V_{CC} operation.

The outputs of the SN74LVC07A device are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

Inputs can be driven from 1.8-V, 2.5-V, 3.3-V (LVTTTL), or 5-V (CMOS) devices. This feature allows the use of this device as a translator in a mixed-system environment.

ORDERING INFORMATION⁽¹⁾

| T_A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| –40°C to 125°C | SOIC – D | Reel of 2500 | SN74LVC07AQDRQ1 | LVC07AQ |
| | TSSOP – PW | Reel of 2000 | SN74LVC07AQPWRQ1 | LVC07AQ |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

**Table 1. FUNCTION TABLE
(EACH BUFFER/DRIVER)**

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | H |
| L | L |

LOGIC DIAGRAM, EACH BUFFER/DRIVER (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|--|--------------------|-----|---------|
| V _{CC} | Supply voltage range | –0.5 | 6.5 | V |
| V _I | Input voltage range ⁽²⁾ | –0.5 | 6.5 | V |
| V _O | Output voltage range | –0.5 | 6.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | | –50 mA |
| I _{OK} | Output clamp current | V _O < 0 | | –50 mA |
| I _O | Continuous output current | | | ±50 mA |
| Continuous current through V _{CC} or GND | | | | ±100 mA |
| θ _{JA} | Package thermal impedance ⁽³⁾ | D package | | 86 °C/W |
| | | PW package | | 113 |
| T _{stg} | Storage temperature range | –65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------|--------------------------------|------------------------------------|------------------------|------|
| V _{CC} | Supply voltage | 1.65 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | |
| | | V _{CC} = 2.7 V to 3.6 V | 2 | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | |
| | | V _{CC} = 2.7 V to 3.6 V | 0.8 | |
| V _I | Input voltage | 0 | 5.5 | V |
| V _O | Output voltage | 0 | 5.5 | V |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | 4 | mA |
| | | V _{CC} = 2.3 V | 12 | |
| | | V _{CC} = 2.7 V | 12 | |
| | | V _{CC} = 3 V | 24 | |
| T _A | Operating free-air temperature | –40 | 125 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|--|-----------------|-----|--------------------|------|------|
| V _{OL} | I _{OL} = 100 µA | 1.65 V to 3.6 V | | | 0.2 | V |
| | I _{OL} = 4 mA | 1.65 V | | | 0.45 | |
| | I _{OL} = 12 mA | 2.3 V | | | 0.7 | |
| | | 2.7 V | | | 0.4 | |
| | I _{OL} = 24 mA | 3 V | | | 0.65 | |
| I _I | V _I = 5.5 V or GND | 3.6 V | | | ±5 | µA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | | | 10 | µA |
| ΔI _{CC} | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | | | 500 | µA |
| C _i | V _I = V _{CC} or GND | 3.3 V | | | 5 | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#) through [Figure 3](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|-----------------|-----------------|----------------|-------------------------------------|-----|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | 1 | 3.5 | 1 | 2.8 | | 3 | 1 | 2.9 | ns |

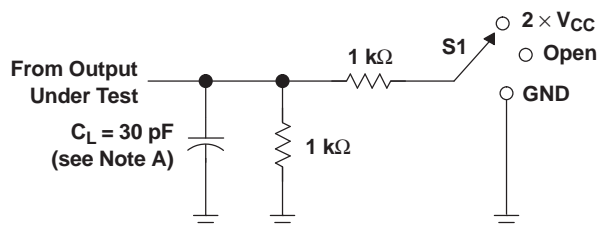
Operating Characteristics

T_A = 25°C

| PARAMETER | | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | UNIT |
|-----------------|---|--------------------|-------------------------|-------------------------|-------------------------|------|
| | | | TYP | TYP | TYP | |
| C _{pd} | Power dissipation capacitance per buffer/driver | f = 10 MHz | 1.8 | 2 | 2.5 | pF |

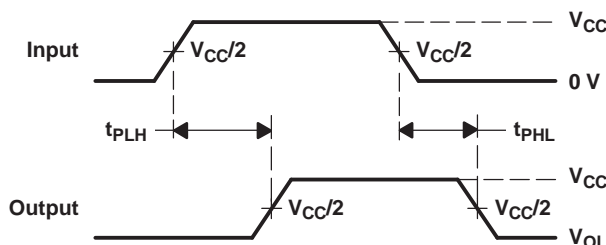
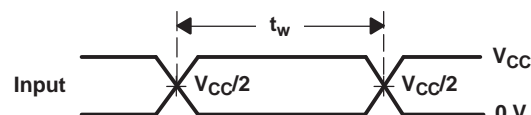
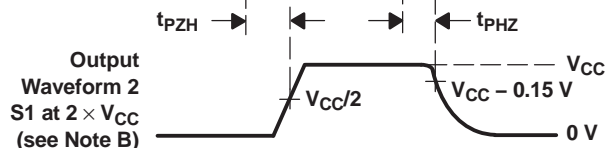
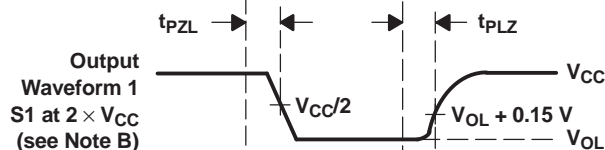
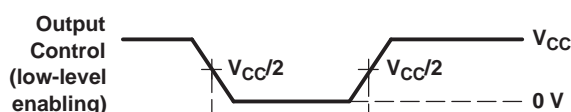
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$$



LOAD CIRCUIT

| TEST | S1 |
|------------------------|---------------------|
| t_{PZL} (see Note F) | 2 \times V_{CC} |
| t_{PLZ} (see Note G) | 2 \times V_{CC} |
| t_{PHZ}/t_{PZH} | 2 \times V_{CC} |

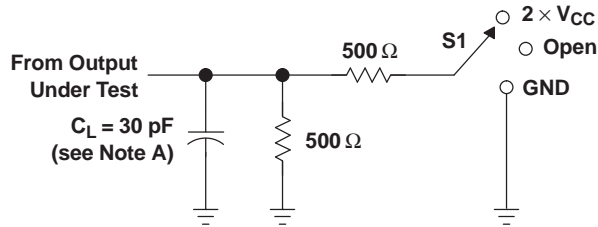
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMESVOLTAGE WAVEFORMS
PROPAGATION DELAY TIMESVOLTAGE WAVEFORMS
PULSE DURATIONVOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
- F. t_{PZL} is measured at $V_{CC}/2$.
- G. t_{PLZ} is measured at $V_{OL} + 0.15\text{ V}$.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

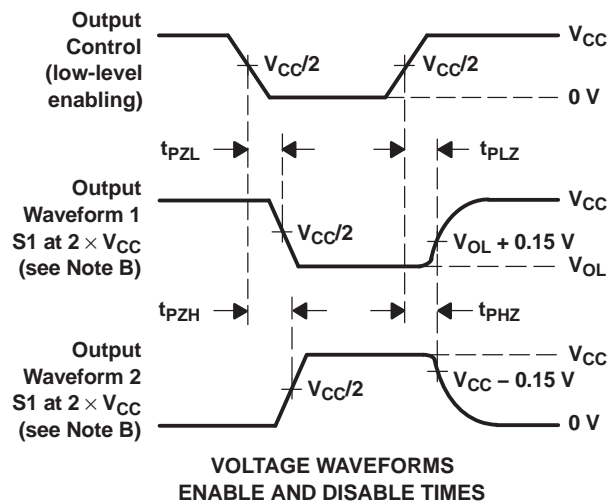
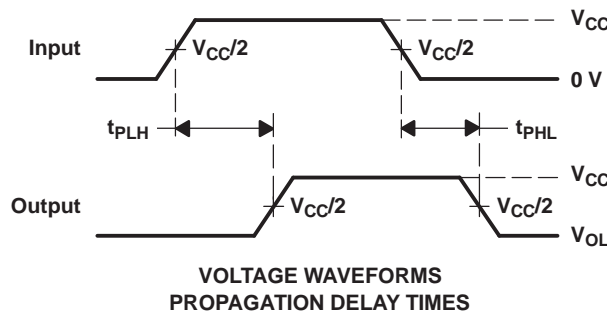
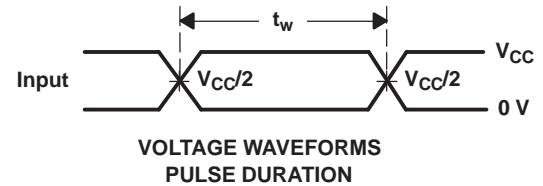
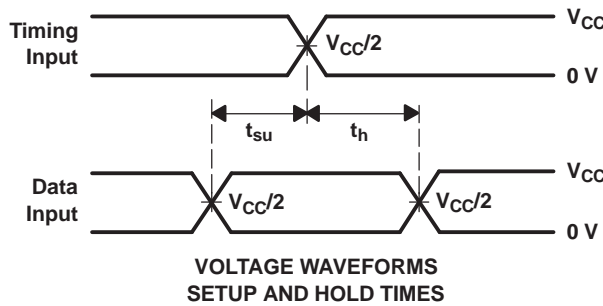
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



LOAD CIRCUIT

| TEST | S1 |
|------------------------|-------------------|
| t_{PZL} (see Note F) | 2 $\times V_{CC}$ |
| t_{PLZ} (see Note G) | 2 $\times V_{CC}$ |
| t_{PHZ}/t_{PZH} | 2 $\times V_{CC}$ |

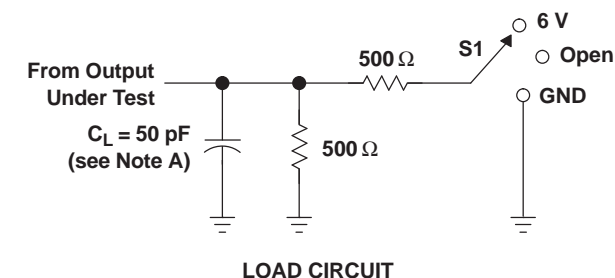


- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
- F. t_{PZL} is measured at $V_{CC}/2$.
- G. t_{PLZ} is measured at $V_{OL} + 0.15 \text{ V}$.
- H. All parameters and waveforms are not applicable to all devices.

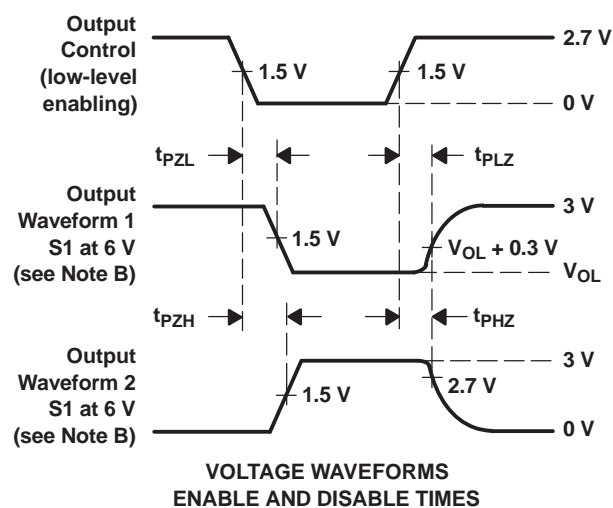
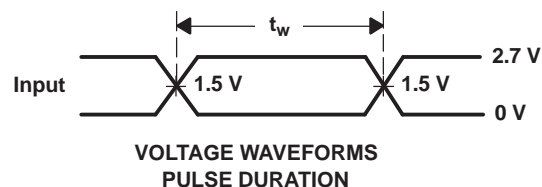
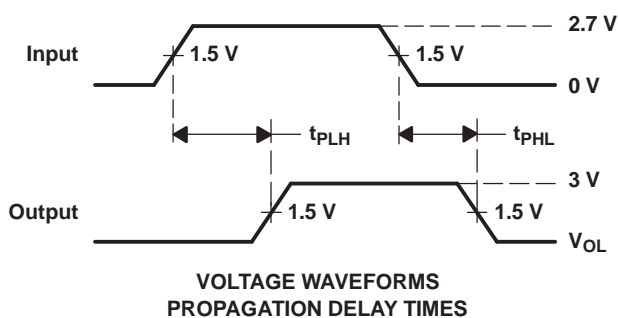
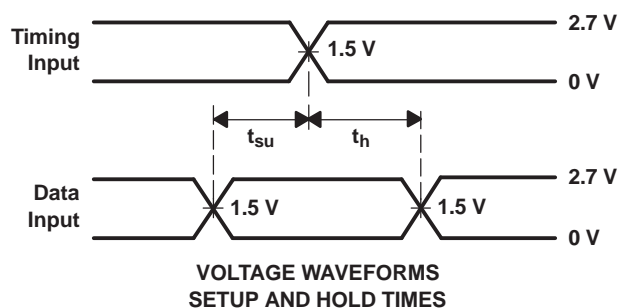
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.7 \text{ and } 3.3 \text{ V} \pm 0.3 \text{ V}$$



| TEST | S1 |
|------------------------|-----|
| t_{pZL} (see Note F) | 6 V |
| t_{pLZ} (see Note G) | 6 V |
| t_{PHZ}/t_{PZH} | 6 V |

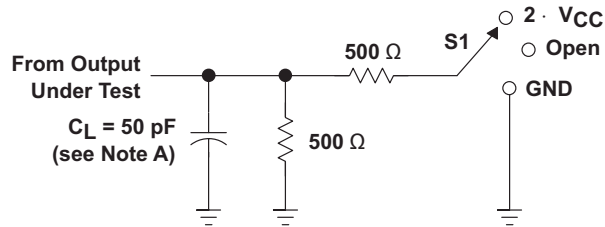


- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pD} .
- F. t_{pZL} is measured at 1.5 V.
- G. t_{pLZ} is measured at $V_{OL} + 0.3 \text{ V}$.
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

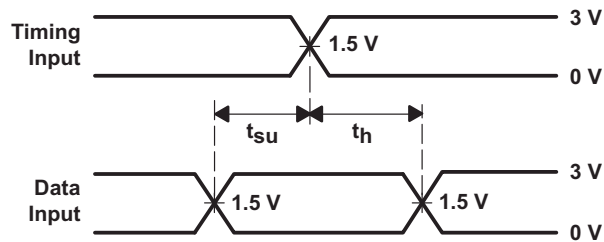
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$$

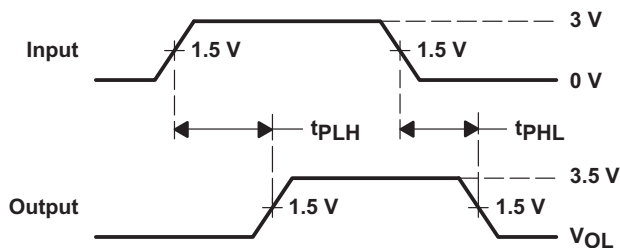


LOAD CIRCUIT

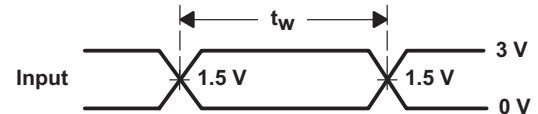
| TEST | S1 |
|------------------------|--------------|
| t_{pZL} (see Note F) | 2 · V_{CC} |
| t_{pLZ} (see Note G) | 2 · V_{CC} |
| t_{PHZ}/t_{PZH} | 7 V |



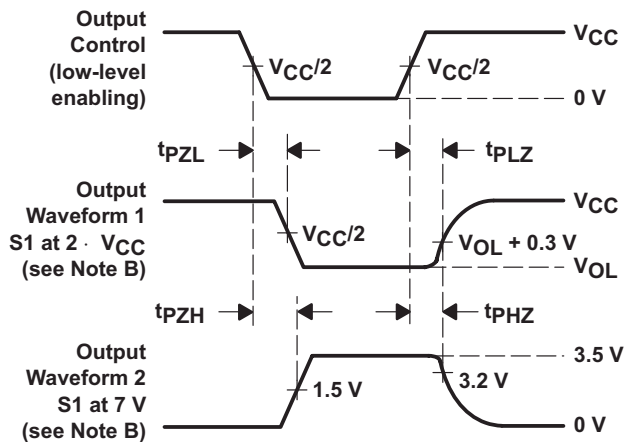
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pd} .
- F. t_{pZL} is measured at $V_{CC}/2$.
- G. t_{pLZ} is measured at $V_{OL} + 0.3\text{ V}$.
- H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

REVISION HISTORY

| Changes from Revision C (December, 2007) to Revision D | Page |
|---|-------------------------------------|
| <ul style="list-style-type: none"> Changed from "Operates From 1.65 V to 3.6 V" to "Operates From 1.65 V to 5 V" Changed from "This hex buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation" to "This hex buffer/driver is designed for 1.65-V to 5.5-V V_{CC} operation" Changed supply voltage max value from 3.6 to 5.5 Added 4th PMI image | <p>1</p> <p>1</p> <p>2</p> <p>7</p> |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVC07AQPWRG4Q1 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC07AQ | Samples |
| SN74LVC07AQPWRQ1 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC07AQ | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC07A-Q1 :

- Catalog: [SN74LVC07A](#)
- Enhanced Product: [SN74LVC07A-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC07AQPWRG4Q1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC07AQPWRQ1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

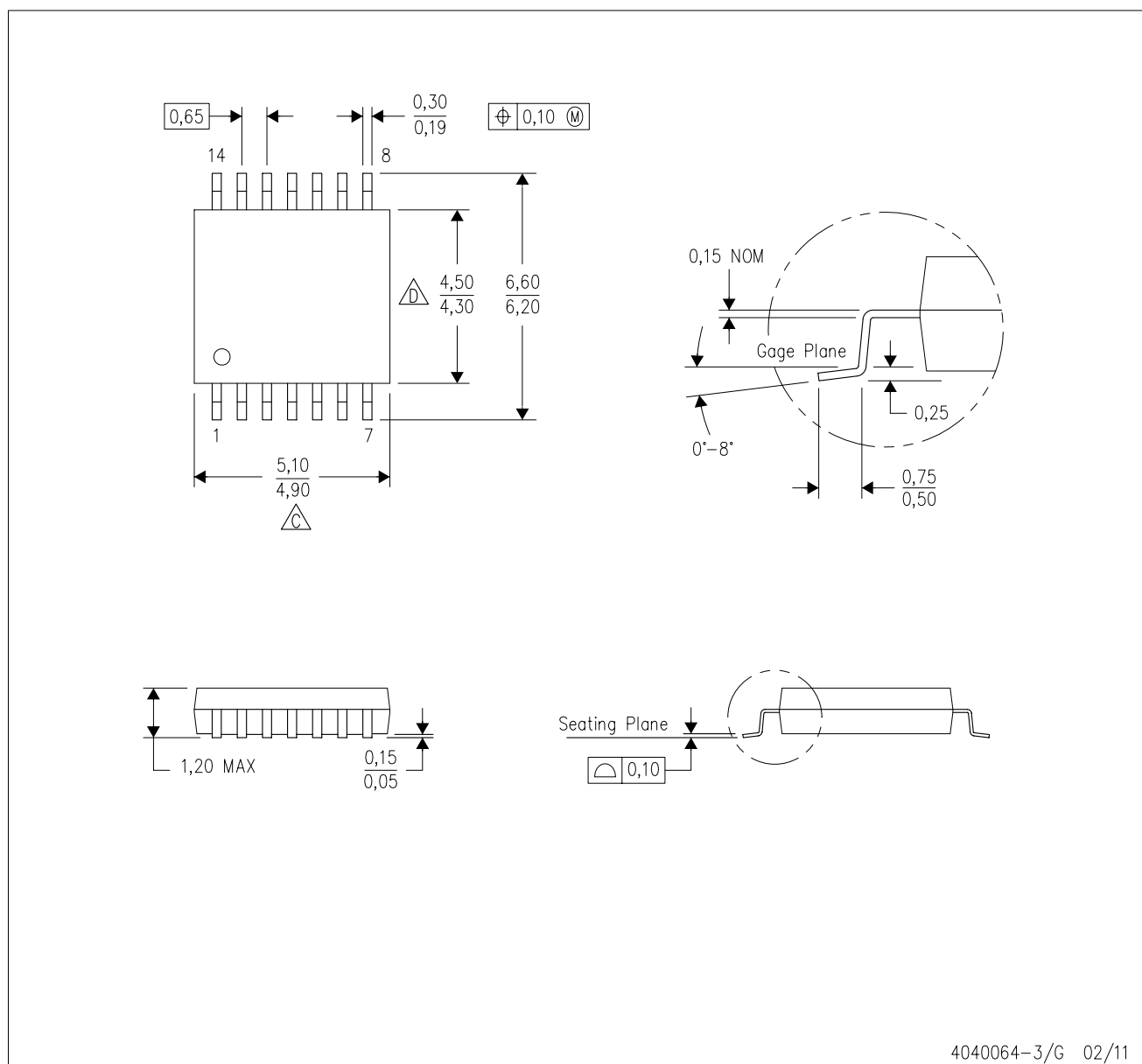


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC07AQPWRG4Q1 | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74LVC07AQPWRQ1 | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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