Si5395/94/92 Reference Manual

Any-frequency, Any-output Jitter-Attenuators/Clock Multipliers Si5395/94/92 Family Reference Manual

This Family Reference Manual is intended to provide system, PCB design, signal integrity, and software engineers the necessary technical information to successfully use the Si5395/94/92 devices in end applications. The official device specifications and ordering information can be found in the Si5395/94/92 data sheets.

The Si5395/94/92 jitter attenuating clock multipliers combine 4th generation DSPLL and MultiSynth™ technologies to enable any-frequency clock generation for applications that require the highest level of jitter performance. These devices are programmable via a serial interface with in-circuit programmable non-volatile memory (NVM) ensuring power up with a known frequency configuration. Freerun, synchronous, and holdover modes of operation are supported offering both automatic and manual input clock switching. The loop filter is fully integrated on-chip eliminating the risk of potential noise coupling associated with discrete solutions. Further, the jitter attenuation bandwidth is digitally programmable providing jitter performance optimization at the application level. These devices are capable of generating any combination of output frequency from any input frequency within the specified input and output range.

All devices of the 9x family offer the option of an external reference or an internal reference. Please refer to the datasheet for the different device ordering options and restrictions.

RELATED DOCUMENTS

- Si5395/94/92 Data Sheet
- UG335: Si5395 Evaluation Board User's Guide
- UG334: Si5394 Evaluation Board User's Guide
- UG387: Si5392 Evaluation Board User's Guide
- Recommended Crystal, TCXO and OCXO Reference Manual for High-Performance Jitter Attenuators and Clock Generators
- AN947: Implementing Zero Delay Mode Using the Si5340/41/42/44/45/80
- AN1178: Frequency-On-the-Fly for Silicon Labs Jitter Attenuators and Clock Generators
- AN1155: Differences between Si5342-47 and Si5392-97

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1. Work Flow Using ClockBuilder Pro and the Register Map

This reference manual is to be used to describe all the functions and features of the parts in the product family with register map details on how to implement them. It is important to understand that the intent is for customers to use the ClockBuilder Pro software to provide the initial configuration for the device. Although the register map is documented, all the details of the algorithms to implement a valid frequency plan are fairly complex and are beyond the scope of this document. Real-time changes to the frequency plan and other operating settings are supported by the devices. However, describing all the possible changes is not a primary purpose of this document. Refer to the applications notes and Knowledge Base articles within the ClockBuilder Pro GUI for information on how to implement the most common, real-time frequency plan changes.

The primary purpose of the software is to enable use of the device without an in-depth understanding of its complexities. The software abstracts the details from the user to allow focus on the high level input and output configuration, making it intuitive to understand and configure for the end application. The software walks the user through each step, with explanations about each configuration step in the process to explain the different options available. The software will restrict the user from entering an invalid combination of selections. The final configuration settings can be saved, written to an EVB and a custom part number can be created for customers who prefer to order a factory preprogrammed device. The final register maps can be exported to text files, and comparisons can be done by viewing the settings in the register map described in this document.

1.1 Field Programming

To simplify design and software development of systems using the Si5395/94/92, a field programmer is available in addition to the evaluation board. The ClockBuilder Pro Field Programmer supports both “in-system” programming (for devices already mounted on a PCB), as well as “in-socket” programming of Si5395/94/92 sample devices. Refer to www.silabs.com/CBProgrammer for information about this kit.

2. Family Product Comparison

The following table is a comparison of the different parts in the product family showing the differences in the inputs, MultiSynths, outputs and package type.

Table 2.1. Family Feature Comparison

Part Number	Internal/ External Reference	Number of Inputs	Number of Multi-Synths	Number of Outputs	Package Type
Si5392 A/B/C/D/P	External	4	2	2	44-QFN
Si5392 J/K/L/M/E	Internal	4	2	2	44-LGA
Si5394 A/B/C/D/P	External	4	4	4	44-QFN
Si5394 J/K/L/M/E	Internal	4	4	4	44-LGA
Si5395 A/B/C/D/P	External	4	5	12	64-QFN
Si5395 J/K/L/M/E	Internal	4	5	12	64-LGA

2.1 Grade P/E Restrictions and Requirements

Some applications like 56G PAM4 SERDES require even higher performance than is already provided by standard jitter attenuators. The Si539xP/E internally calibrates out linearity errors to deliver even better jitter performance for 56G SerDes applications that require 156.25MHz and 312.5MHz clocks. For optimal performance, the device input clocks should be traceable back to a Stratum 3 primary reference clock. If frequencies other than the restricted set mentioned are required, grades A/J will provide the most flexibility.
For performance devices with external reference (Grade P), the XA/XB input is XTAL only. The XTAL frequency is fixed at 48MHz and variation must be within ±100 ppm across temperature and aging. The CLKIN inputs must be within ±4.6 ppm across temperature and aging. If this is violated, the grade P device will not work. It is tuned specifically for high performance and must meet these input requirements. The performance devices with integrated reference (Grade E) have a high quality Japanese crystal that has been prescreened for activity dips inside the package which meets the above specifications. The CLKIN inputs must still be within ±4.6 ppm across temperature and aging for the grade E devices.

Grade P/E parts require a 625 ms wait time after the pre-amble when changing a frequency plan. This is also noted in the Dynamic PLL Changes section.

2.2 Si5395/94/92-P/E Grade Part Frequency Plan Rules

The P/E grade parts have various restrictions compared to the highly flexible A/J grade device. These restrictions are required to guarantee the 100-fs integrated jitter specification in the 12 kHz-20 MHz frequency band for 156.25 MHz, 312.5 MHz, and 625 MHz output frequencies. This section is intended to capture the rules required for the frequency planning of the P/E grade parts. The intention is to use the guidance from CBPro and these rules to create a P/E grade frequency plan. These rules may be updated in the future to allow more flexibility as further validation can be done.

2.2.1 Input Rules

The following are the allowable input frequencies for the P/E grade part.

2M, 25M, 19.2M, 19.44M, 38.88M, 156.25M, 312.5M

Note that not all combinations of these frequencies can be used at the same time and not all formats are allowed on every input. The following input rules apply.

1. The P/E grade part limits the input P dividers to integer only. This means that the greatest common divisor (which is the phase detector frequency) among the different inputs must be found using integer P dividers on the inputs.
2. The phase detector frequency (Fpfd) must be 200 kHz or greater.
3. IN0 and IN1 will allow Standard AC-coupled differential, Standard AC-coupled single ended, Standard DC-coupled CMOS, and Non-Standard DC-coupled CMOS input formats, but not Pulsed CMOS.
4. Only Standard AC-coupled differential input format mode is supported on IN2/IN3 (no Standard AC-coupled single ended, no Standard CMOS, no Non-Standard CMOS and no Pulsed CMOS. No single ended DC coupled or AC coupled of any type).

2.2.2 Output Rules

The outputs are divided into different “domains” which are combinations of frequencies. There are rules for where certain domains which can be placed among the (up to) 12 outputs. All of these rules are built into CBPro with warnings and guidance to assist in optimizing the frequency plans for performance.

These are the frequencies for the different domains:

- **Domain1:** 156.25/312.5/625 MHz
- **Domain2:** 25/50/100/125/200 MHz
- **Domain3:** 322.265625/644.53125 MHz

Si5392P/E

The Si5392 Performance grades have 2 outputs both of which are tuned to operate with one time domain and delivers less than 100 fs of jitter on the PHY clock. The rules for placement of the output clocks are shown below.

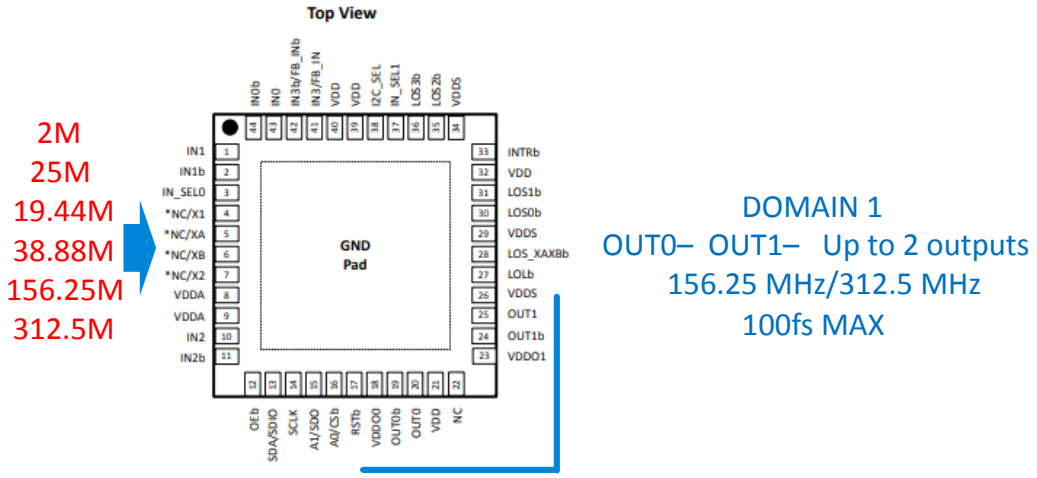


Figure 2.1. Si5392P/E Outputs with Single Time Domain

Domain 1 rules are the following:

- OUT0-OUT1: 156.25/312.5/625 MHz
- No Gap needed
- No CMOS output clocks allowed anywhere

Si5394P/E

The Si5394 Performance grades have 4 outputs and are able to deliver up to 2 time domains at the same time and still deliver less than 100fs of jitter on the PHY clock. The rules for placement of output clocks are as shown below.

- OUT0-OUT1: 125/156.25/312.5/625 MHz
- OUT2-OUT3: 25/50/100/125/200, 156.25/312.5 MHz/625 MHz

Special Note on Input Restrictions: If domain 2 clocks are not present and a 25/156.25/312.5 MHz differential input clock is present on IN0,1,2 (IN3 is not allowed for 25 Mhz input but ok for 156.25/312.5 MHz input), OUT0-OUT3 are 100 fs capable for domain 1 clocks.

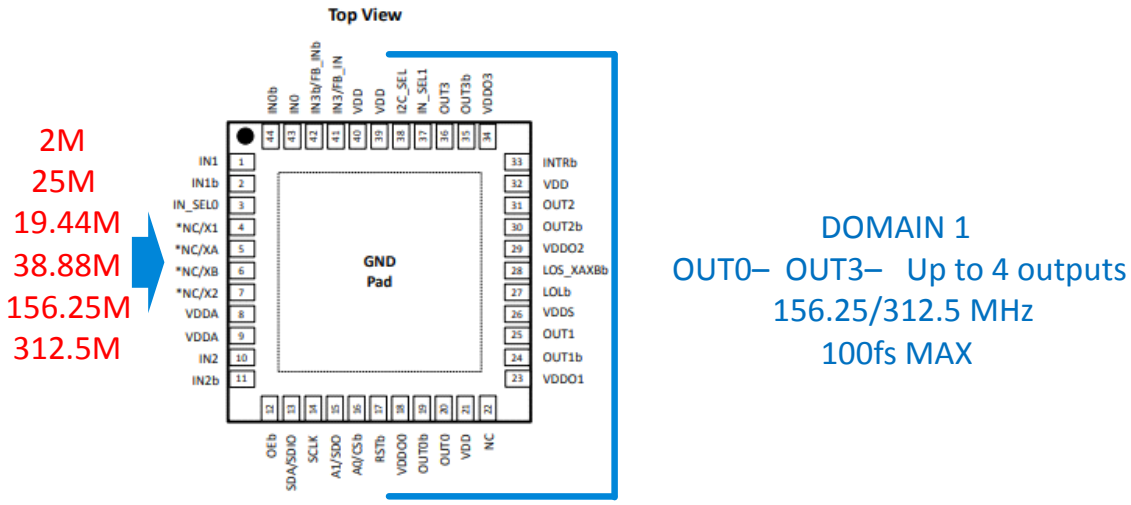


Figure 2.2. Si5394P/E Outputs with Single Time Domain

Domain 1 rules are the following:

- OUT0-OUT3: 156.25/312.5/625 MHz
- No Gap Needed
- No CMOS output clocks allowed anywhere

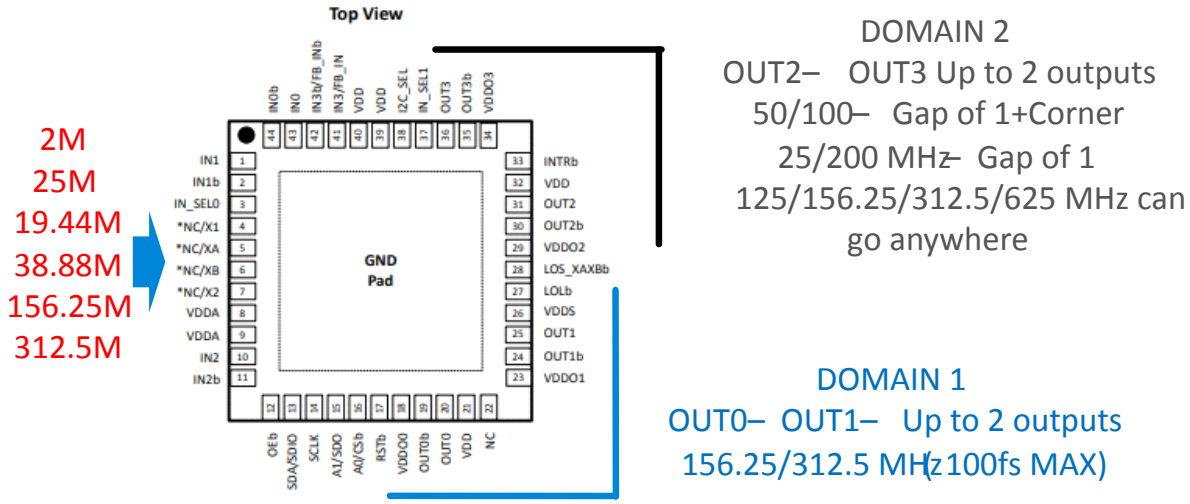


Figure 2.3. Si5394P/E Outputs with Two Time Domains

Domain 2 rules are the following:

- 1 corner of isolation must be present between domain 1 and domain 2
- Between domain 1 and 2, 1-2 outputs must be empty or have benign clocks (156.25/312.5MHz) on which higher jitter is acceptable
- If ANY domain 2 clocks are LVPECL then ALL domain 1 clocks must be LVPECL
- If ALL domain 2 clocks are LVDS then ANY domain 1 clocks can be LVDS or LVPECL
- No CMOS output clocks allowed anywhere
- The voltage regulator powering domain 1 drivers must be independent of the regulator powering domain 2 drivers

Si5395P/E

The Si5395 P and E grade performance calibrated versions have 12 ouputs and are able to deliver up to 3 time domains at the same time and still have less than 100fs of jitter on the PHY clock. The rules for placement of output clocks are as shown below.

- OUT0A-OUT1: 125/156.25/312.5/625 MHz
- OUT2: 25/125/200 MHz, 156.25/312.5/625 MHz
- OUT3-OUT6: 25/50/100/125/200 MHz, 156.25/312.5 MHz/625 MHz
- OUT7 – OUT9A: 25/50/100/125/200 MHz, 156.25/312.5 MHz/625 MHz, 322.265625/644.53125 MHz

Note: Only OUT0A ,0,1,2,3,4, and 5 are 100 fs capable if any domain 2 or domain 3 clocks are present.

Special Note on Input Restrictions: If no domain 2 or 3 clocks are present and a 25/156.25/312.5 MHz differential input clock is present on IN0, IN1, or IN2, (IN3 is not allowed to use 25 MHz input but ok to use 156.25 MHz or 312.5 MHz input). Then, OUT0A-OUT9A are 100fs capable for domain 1 clocks. **No CMOS input clocks** are supported when OUT6-9A are rated for 100 fs.

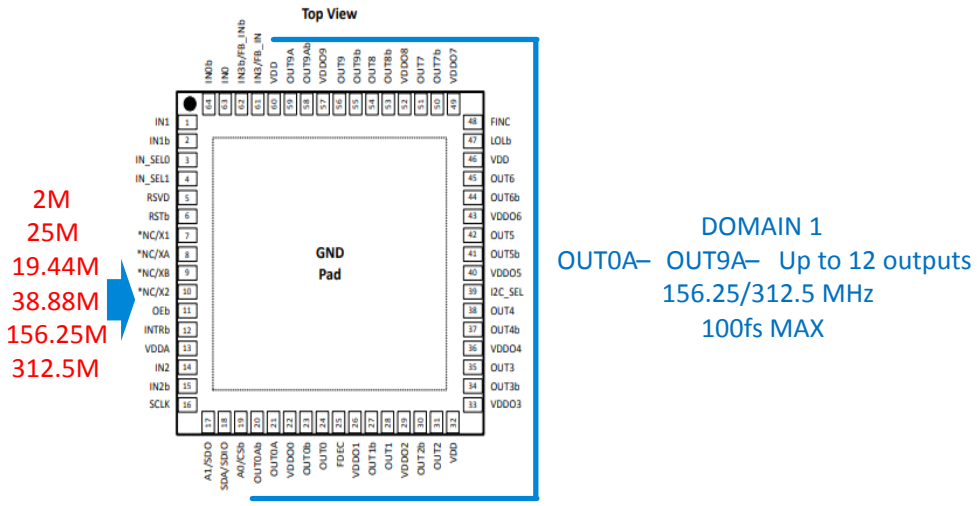


Figure 2.4. Si5395P/E Outputs with Single Time Domain

Domain 1 rules are the following:

- No Gap Needed
- No CMOS output clocks allowed anywhere

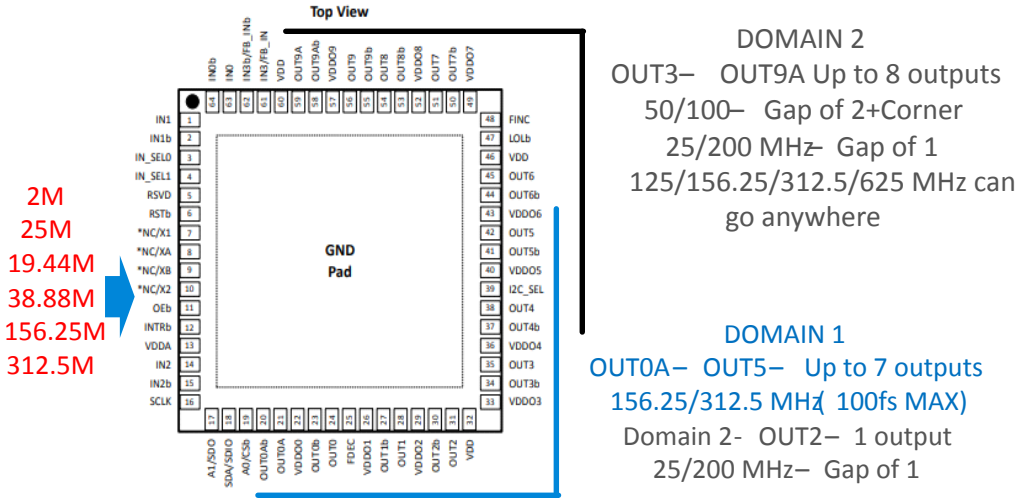


Figure 2.5. Si5395P/E Outputs with Two Time Domains

Domain 2 rules are the following:

- 1 corner of isolation must be present between domain 1 and domain 2
- Between domain 1 and 2, 1-2 outputs must be empty or have benign clocks (156.25/312.5MHz) on which higher jitter is acceptable
- If ANY domain 2 clocks are LVPECL then ALL domain 1 clocks must be LVPECL
- If ALL domain 2 clocks are LVDS then ANY domain 1 clocks can be LVDS or LVPECL
- No CMOS output clocks allowed anywhere
- The voltage regulator powering domain 1 drivers must be independent of the regulator powering domain 2 drivers

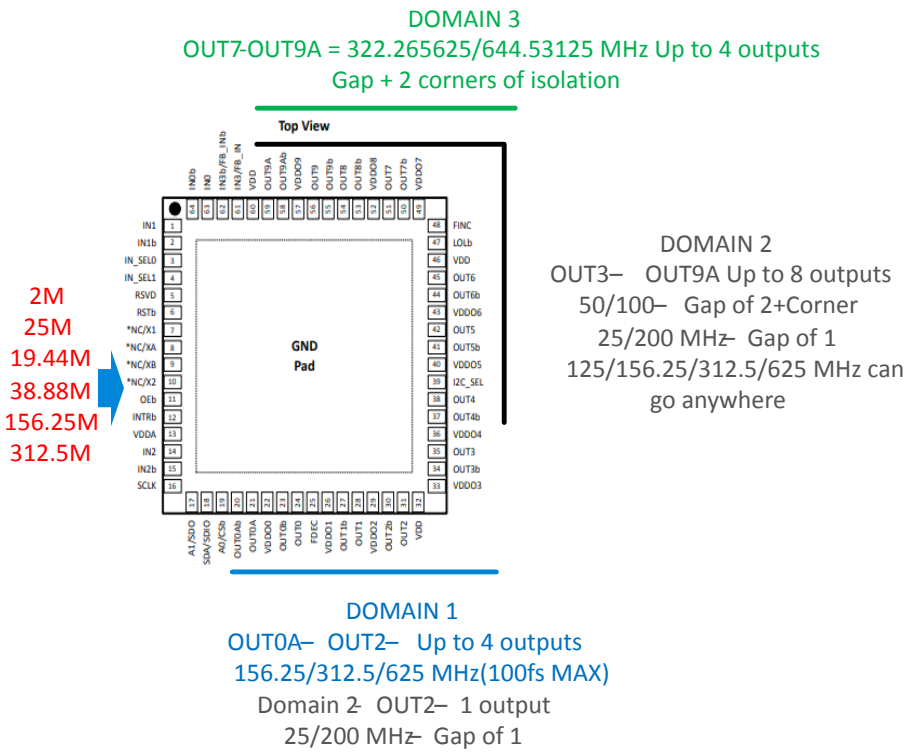


Figure 2.6. Si5395P/E Outputs with Three Time Domains

Domain 3 rules are the following:

- One corner of isolation must be present between domain 1 and domain 2
- Two corner of isolation must be present between domain 1 and domain 3
- Between domain 1 and 2, 1-2 Outputs must be empty or have benign clocks (156.25/312.5 MHz) on which higher jitter is acceptable
- If ANY domain 2 clocks are LVPECL then ALL domain 1 clocks must be LVPECL
- If ALL domain 2 clocks are LVDS then ANY domain 1 clocks can be LVDS or LVPECL
- No CMOS output clocks allowed anywhere
- The VDDO powering domain 1 drivers must be independent of the VDDO for domain 2 outputs

2.2.3 Output Formats

- LVPECL and LVDS are supported for all outputs.
- HCSL is supported only for 25/50/125/200 MHz outputs.
- If any Domain 2/3 clocks are LVPECL/HCSL, all Domain 1 100 fs capable outputs must be LVPECL.

2.2.4 Multi-Synth Assignment

The following table provides the output frequency and the N divider that is used in each case.

Output Frequency (MHz)	N Divider/Value	Notes
156.25	N0 = 43	Integer N
312.5 / 625	N1 = 21.5 / 10.75	Fractional N required if both 625 MHz and 312.5 MHz enabled on same plan CBPro uses N1 = 10.75
25/50/100/125/200	N2 (94P/E) N4 (95P/E)	Fractional N value chosen by CBPro
322.265625/644.53125	N2	Fractional N value chosen by CBPro

From CBPro, the design report defines which outputs are guaranteed to meet the 100 fs integrated jitter specification in the 12 kHz-20 MHz frequency band.

3. DSPLL and MultiSynth

The DSPLL is responsible for input frequency translation, jitter attenuation and wander filtering. Fractional input dividers (Pxn/Pxd) allow for integer or fractional division of the input frequency, but the input frequencies must be integer related to allow the DSPLL to perform hitless switching between input clocks (INx). Input switching is controlled manually or automatically using an internal state machine. The oscillator circuit (OSC) provides a frequency reference which determines output frequency stability and accuracy while the device is in free-run or holdover mode. Note that a XTAL (or suitable XO reference on XA/XB) is always required and is the jitter reference for the device. The high-performance MultiSynth dividers (Nxn/Nxd) generate integer or fractionally related output frequencies for the output stage. A crosspoint switch connects any of the generated frequencies to any of the outputs. A single MultiSynth output can connect to one or more output drivers. Additional integer division (R) determines the final output frequency. Grade J/K/L/M and Grade E devices would have reference integrated in the package, so no external XTAL is needed. The specs for the integrated reference can be found in the data sheet.

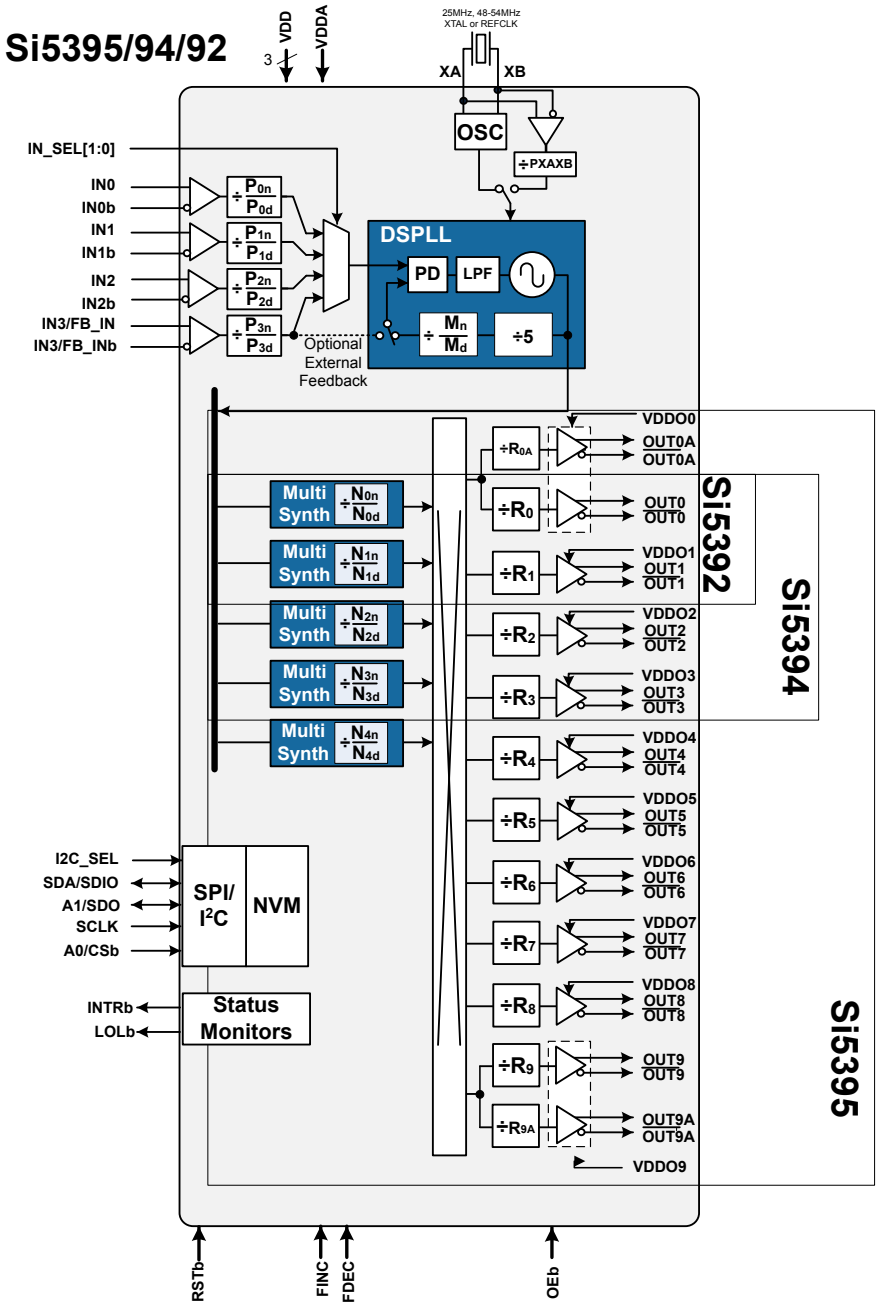


Figure 3.1. DSPLL and Multisynth System Flow Diagram

The frequency configuration of the DSPLL is programmable through the SPI or I^2C serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (Pn/Pd), fractional frequency multiplication (Mn/Md), fractional output MultiSynth division (Nn/Nd), and integer output division (Rn) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro software.

3.1 Dividers

There are five divider classes within the Si5395/94/92. See Figure 3.1 DSPLL and Multisynth System Flow Diagram on page 13 which shows all of these dividers.

1. P-dividers: Wide range input dividers P3, P2, P1, P0
   - Divider: 48 bit numerator, 32 bit denominator, min value is 1
   - Practical range limited by phase detector and VCO range
   - Each divider has an update bit that must be written to cause a newly written divider value to take effect.

2. Narrow range input divider: Pxaxb
   - Only divides by 1, 2, 4, 8

3. Feedback M divider
   - Integer or fractional divide values
   - 56 bit numerator, 32-bit denominator
   - Practical range limited by phase detector
   - Each divider has an update bit that must be written to cause a newly written divider value to take effect.

4. Output N divider
   - MultiSynth divider
   - Integer or fractional divide values
   - 44-bit numerator, 32 bit denominator
   - Each divider has an update bit that must be written to cause a newly written divider value to take effect.

5. Output R divider
   - Only even integer divide values
   - Min value is 2
   - Maximum value is $2^{25} – 2$

3.2 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation and wander filtering. Register configurable DSPLL loop bandwidth settings in the range of 0.1 Hz to 4 kHz are available for selection. The loop bandwidth is controlled digitally and remains stable with less than 0.1 dB of peaking for the loop bandwidth selected. The DSPLL loop bandwidth is set in registers 0x0508-0x050D and are determined using ClockBuilder Pro.

The higher the PLL bandwidth is set relative to the phase detector frequency (f_{pfd}), the more chance that f_{pfd} will cause a spur in the Phase Noise plot of the output clock and increase the output jitter. To guarantee the best phase noise/jitter it is recommended that the normal PLL bandwidth be kept less than $f_{pfd}/160$ although ratios of $f_{pfd}/100$ will typically work fine.

Note: After changing the bandwidth parameters, the appropriate BW_UPDATE_PLL bit (0x514) must be set high to latch the new values into operation. The update bits will latch both nominal and fastlock bandwidths.

Table 3.1. PLL Bandwidth Registers

Register Name	Hex Address [Bit Field]	Function
BWx_PLL	0x0508[7:0]–0x050D[7:0]	Determines the loop BW for the DSPLL. This is set by CBPro. See CBPro for a correlation of bandwidths and values.

3.2.1 Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The Fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process to reduce lock time. Higher Fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Once lock acquisition has completed, the DSPLL's loop bandwidth will automatically revert to the nominal DSPLL Loop Bandwidth setting. The Fastlock feature can be enabled or disabled independently by register control. If enabled, when LOL is asserted Fastlock will be automatically enabled. When LOL is no longer asserted, Fastlock will be automatically disabled. The loss of lock (LOL) feature is a fault monitoring mechanism. Details of the LOL feature can be found in the fault monitoring section.

Note: After changing the bandwidth parameters, the appropriate BW_UPDATE_PLL bit (0x514) must be set hight to latch the new values into operation. This update bit will latch new values for Loop, Fastlock, and Holdover bandwidths simultaneously.

Table 3.2. PLL Fastlock Registers

Register Name	Hex Address [Bit Field]	Function
FASTLOCK_AUTO_EN	0x052B[0]	Auto Fastlock Enable/Disable
FASTLOCK_MAN	0x052B[1]	0 for normal operation, 1 to force fast lock
FASTLOCK_BW_PLL	0x050E[7:0]–0x0513[7:0]	Fastlock BW selection. Parameters are generated by ClockBuilder Pro. See CBPro for the generated values and corresponding bandwidths.

3.2.2 Holdover Exit Bandwidth

In addition to the operating loop and fastlock bandwidths, there is also a user-selectable bandwidth when exiting holdover and locking or relocking to an input clock, available when ramping is disabled (HOLD_RAMP_BYP = 1). CBPro sets this value equal to the loop bandwidth by default.

Note: The BW_UPDATE_PLL bit bit will latch new values for Loop, Fastlock, and Holdover bandwidths simultaneously.

Table 3.3. DSPLL Holdover Exit Bandwidth Registers

Register Name	Hex Address	Function
HOLDEXIT_BW	0x059D–0x05A2	Determines the Holdover Exit BW for the DSPLL. Parameters are generated by ClockBuilder Pro. See CBPro for the generated values and corresponding bandwidths.

4. Modes of Operation

Once initialization is complete, the DSPLL operates independently in one of four modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in the figure below. The following sections describe each of these modes in greater detail.

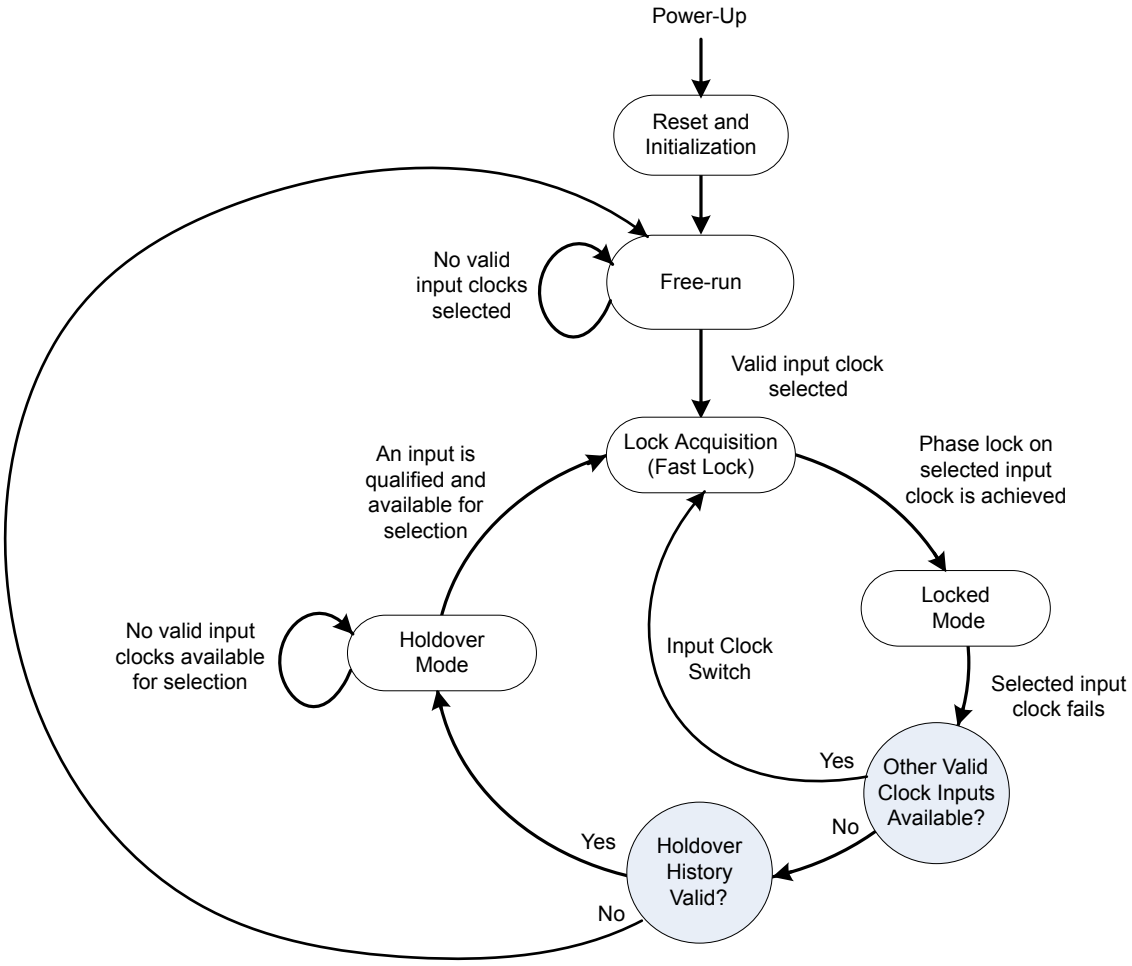


Figure 4.1. Modes of Operation

4.1 Reset and Initialization

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from internal non-volatile memory (NVM) and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete.

There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the RST pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes.

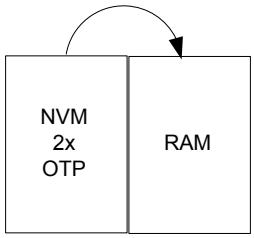


Figure 4.2. Si5395/94/92 Memory Configuration

Table 4.1. Reset Control Registers

Register Name	Hex Address [Bit Field]	Function
HARD_RST	0x001E[1]	Performs the same function as power cycling the device. All registers will be restored to their default values.
SOFT_RST	0x001C[0]	Performs a soft reset. Initiates register configuration changes.

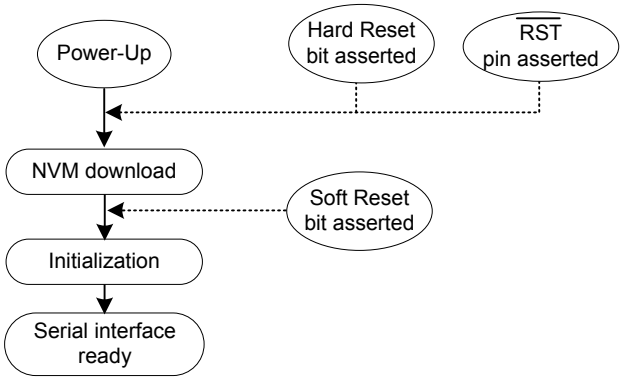


Figure 4.3. Initialization from Hard Reset and Soft Reset

The Si5395/94/92 is fully configurable using the serial interface (I^2C or SPI). At power up the device downloads its default register values from NVM. Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its VDD (1.8 V) and VDDA (3.3 V) pins. Neither VDDOx or VDDS supplies are required to write the NVM.

4.2 Dynamic PLL Changes

It is possible for a PLL to become unresponsive (i.e., lose lock indefinitely) when it is dynamically reprogrammed or changed via the serial port. Reprogramming/changing the N divider does not affect the PLL. Any change that causes the VCO frequency to change by more than 250 ppm since Power-up, NVM download, or SOFT_RST requires the following special sequence of writes. Changes to the following registers require the following special sequence of writes:

- PXAXB
- PX_NUM
- PX_DEN
- MXAXB_NUM
- MXAXB_DEN
- M_NUM
- M_DEN

1. First, write in the preamble

   Write 0x0B24 = 0xC0

   Write 0x0B25 = 0x00

   Write 0x0540 = 0x01 (NOTE: for all new designs it is recommend that this register be written as part of the preamble. In some rare cases, omitting this write may result in a one-time LOL occurrence. However, if this issue has not occurred with your current frequency plan it is not likely to occur)
2. Wait 300 ms for Grade A/B/C/D/J/K/L/M, Wait 625ms for Grade P/E
3. Then perform the desired register modifications
4. Write SOFT_RST 0x001C[0] = 1
5. Write the post-amble

   Write 0x0540 = 0x00 (NOTE: for all new designs it is recommend that this register be written as part of the post-amble. In some rare cases, omitting this write may result in a one-time LOL occurrence. However, if this issue has not occurred with your current frequency plan it is not likely to occur)

   Write 0x0B24 = 0xC3

   Write 0x0B25 = 0x02

Note: Please check for the latest information online. This information is subject to updates.

4.3 NVM Programming

Devices have two categories of non-volatile memory: user NVM and Factory (Silabs) NVM. Each type is segmented into NVM banks. There are three user NVM banks, one of which is used for factory programming (whether a base part or an Orderable Part Number). User NVM can be therefore be burned in the field up to two times. Factory NVM cannot be modified, and contains fixed configuration information for the device.

The ACTIVE_NVM_BANK device setting can be used to determine which user NVM bank is currently being used and therefore how many banks, if any, are available to burn. The following table describes possible values:

Table 4.2. NVM Bank Burning Values

Active NVM BANK Value (Decimal)	Number of User Banks Burned	Number of User Banks Available to Burn
3 (factory state)	1	2
15	2	1
63	3	0

Note: While polling DEVICE_READY during the procedure below, the following conditions must be met in order to ensure that the correct values are written into the NVM:

- VDD and VDDA power must both be stable throughout the process.
- No additional registers may be written or read during DEVICE_READY polling. This includes the PAGE register at address 0x01. DEVICE_READY is available on every register page, so no page change is needed to read it.
- Only the DEVICE_READY register (0xFE) should be read during this time.

The procedure for writing registers into NVM is as follows:

1. Write all registers as needed. Verify device operation before writing registers to NVM.
2. You may write to the user scratch space (Registers 0x026B to 0x0272 DESIGN_ID0-DESIGN_ID7) to identify the contents of the NVM bank.
3. Write 0xC7 to NVM_WRITE register.
4. Poll DEVICE_READY until DEVICE_READY=0x0F.
5. Set NVM_READ_BANK 0x00E4[0]=1. This will load the NVM contents into non-volatile memory.
6. Poll DEVICE_READY until DEVICE_READY=0x0F.
7. Read ACTIVE_NVM_BANK and verify that the value is the next highest value in the table above. For example, from the factory it will be a 3. After NVM_WRITE, the value will be 15.

Alternatively, steps 5 and 6 can be replaced with a Hard Reset, either by RSTb pin, HARD_RST register bit, or power cycling the device to generate a POR. All of these actions will load the new NVM contents back into the device registers.

The ClockBuilder Pro Field Programmer kit is a USB attached device to program supported devices either in-system (wired to your PCB) or in-socket (by purchasing the appropriate field programmer socket). ClockBuilder Pro software is then used to burn a device configuration (project file). Learn more at https://www.silabs.com/products/development-tools/timing/cbprogrammer.

Table 4.3. NVM Programming Registers

Register Name	Hex Address [Bit Field]	Function
ACTIVE_NVM_BANK	0x00E2[7:0]	Identifies the active NVM bank.
NVM_WRITE	0x00E3[7:0]	Initiates an NVM write when written with value 0xC7.
NVM_READ_BANK	0x00E4[0]	Download register values with content stored in NVM.
DEVICE_READY	0x00FE[7:0]	Indicates that the device is ready to accept commands when value = 0x0F.

Warning: Any attempt to read or write any register other than DEVICE_READY before DEVICE_READY reads as 0x0F may corrupt the NVM programming and may corrupt the register contents, as they are read from NVM. Note that this includes accesses to the PAGE register.

4.4 Free Run Mode

Once power is applied to the Si5395/94/92 and initialization is complete, if valid input is not present, the DSPLL will automatically enter freerun mode, generating the frequencies determined by the NVM. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the crystal or reference clock on the XA/XB pins. For example, if the crystal frequency is ±100 ppm, then all the output clocks will be generated at their configured frequency ±100 ppm in freerun mode. Any drift of the crystal frequency will be tracked at the output clock frequencies. A TCXO or OCXO is recommended for applications that need better frequency accuracy and stability while in freerun or holdover modes. Because there is little or no jitter attenuation from the XAXB pins to the clock outputs, a low-jitter XAXB source will be needed for low-jitter clock outputs.

4.5 Acquisition Mode

The device monitors all inputs for a valid clock. If at least one valid clock is available for synchronization, the DSPLL will automatically start the lock acquisition process. If the fast lock feature is enabled, the DSPLL will acquire lock using the Fastlock Loop bandwidth setting and then transition to the normal DSPLL Loop bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

4.6 Locked Mode

Once locked, a DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point any XTAL frequency drift will not affect the output frequency. DSPLL has its LOL pin and status bit to indicate when lock is achieved. See Section 5.3.3 Loss of Lock (LOL) Fault Monitoring for more details on the operation of the loss of lock circuit.

4.7 Holdover Mode

The DSPLL programmed for holdover mode automatically enters holdover when the selected input clock becomes invalid (i.e. when either OOF or LOS are asserted) and no other valid input clocks are available for selection. The DSPLL calculates a historical average of the input frequency while in locked mode to minimize the initial frequency offset when entering the holdover mode.

The averaging circuit for the DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window with the stored historical frequency data. The window size determines the amount of holdover frequency averaging. The delay value is used to ignore frequency data that may be corrupt just before the input clock failure. Both the window size and the delay are programmable as shown in the figure below.

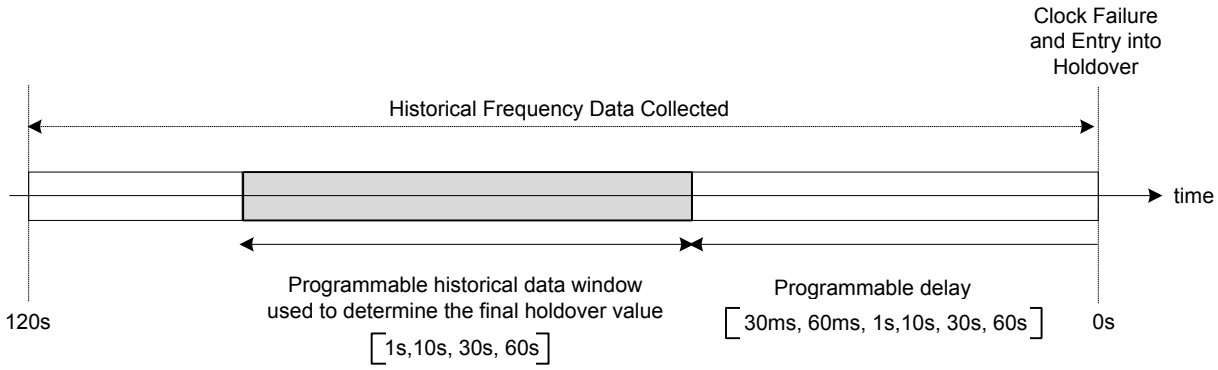


Figure 4.4. Programmable Holdover Window

When entering Holdover, the DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in Holdover, the output frequency drift is entirely dependent on the external crystal or external reference clock connected to the XAXB pins. If the clock input becomes valid, the DSPLL will automatically exit the Holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. These options are register programmable.

The recommended mode of exit from holdover is a ramp in frequency. Just before the exit begins, the frequency difference between the output frequency while in holdover and the desired, new output frequency is measured. It is likely that the new output clock frequency will not be the same as the holdover output frequency because the new input clock frequency might have changed and the XTAL drift might have changed the output frequency. The ramp logic calculates the difference in frequency between the holdover frequency and the new, desired output frequency. Using the user selected ramp rate, the correct ramp time is calculated. The output ramp rate is then applied for the correct amount of time so that when the ramp ends, the output frequency will be the desired new frequency. Using the ramp, the transition between the two frequencies is smooth and linear. The ramp rate can be selected to be very slow (0.2 ppm/sec), very fast (40,000 ppm/sec) or any of approximately 40 values that are in between. The loop bandwidth values do not limit or affect the ramp rate selections and vice versa. CBPro defaults to ramped exit from holdover. Ramped exit from holdover is also used for ramped input clock switching. See Section 5.2.4 Ramped Input Switching for more information.

As shown in Figure 4.1 Modes of Operation on page 16, the Holdover and Freerun modes are closely related. The device will only enter Holdover if a valid clock has been selected long enough for the holdover history to become valid. If the clock fails before the combined holdover history length and holdover history delay time has been met, then holdover history won't be valid and the device will enter Freerun mode instead. Reducing the holdover history length and holdover history delay times will allow Holdover in less time, limited by the source clock failure and wander characteristics. Note that the Holdover history accumulation is suspended when the input clock is removed and resumes accumulating when a valid input clock is again presented to the DSPLL.

Table 4.4. Holdover Mode Control Registers

Register Name	Hex Address [Bit Field]	Function
Holdover Status		
HOLD	0x000E[5]	DSPLL Holdover status indicator. 0: Normal Operation 1: In Holdover/Freerun Mode: HOLD_HIST_VALID = 0 Freerun Mode HOLD_HIST_VALID = 1 Holdover Mode
HOLD_FLG	0x0013[5]	Holdover indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.
HOLD_INTR_MSK	0x0019[5]	Masks Holdover/Freerun from generating INTR interrupt. 0: Allow Holdover/Freerun interrupt (default) 1: Mask (ignore) Holdover/Freerun for interrupt
HOLD_HIST_VALID	0x053F[1]	Holdover historical frequency data valid. 0: Incomplete Holdover history, Freerun mode available 1: Valid Holdover history, Holdover mode available
Holdover Control and Settings		
HOLD_HIST_LEN	0x052E[4:0]	Window Length time for historical average frequency used in Holdover mode. Window Length in seconds (s): Window Length = $((2^{LEN}) – 1) \times 268$ ns
HOLD_HIST_DELAY	0x052F[4:0]	Delay Time to ignore data for historical average frequency in Holdover mode. Delay Time in seconds (s): Delay Time (s) = $(2^{DELAY}) \times 268$ ns
FORCE_HOLD	0x0535[0]	Force the device into Holdover mode. Used to hold the device output clocks while retraining an upstream input clock. 0: Normal Operation 1: Force Holdover/Freerun Mode: HOLD_HIST_VALID = 0 ? Freerun Mode HOLD_HIST_VALID = 1 ? Holdover Mode
Holdover Exit Control		
HOLD_RAMP_BYP	0x052C[3]	Holdover Exit Ramp Bypass 0: Use Ramp when exiting from Holdover (default) 1: Use Holdover/Fastlock Loop bandwidth when exiting from Holdover
HOLDEXIT_BW_SEL0	0x059B[6]	Forces holdover bandwidth when exiting holdover (HOLDEXIT_BW_SEL1=0 fastlock mode) 0: normal operation 1: Use Holdover Exit bandwidth on Holdover exit (default)

Register Name	Hex Address [Bit Field]	Function
HOLDEXIT_BW_SEL1	0x052C[4]	Select the exit bandwidth from Holdover when ramped exit is not selected (HOLD_RAMP_BYP = 1). 0: Use Fastlock bandwidth on Holdover exit 1: Use Normal Loop bandwidth on Holdover exit
RAMP_STEP_INTERVAL	0x052C[7:5]	Time Interval of the frequency ramp steps when ramping between inputs or exiting holdover.
RAMP_STEP_SIZE	0x05A6[2:0]	Size of the frequency ramp steps when ramping between inputs or exiting holdover.

5. Clock Inputs

The Si5395/94/92 supports 4 inputs that can be used to synchronize to the DSPLL .

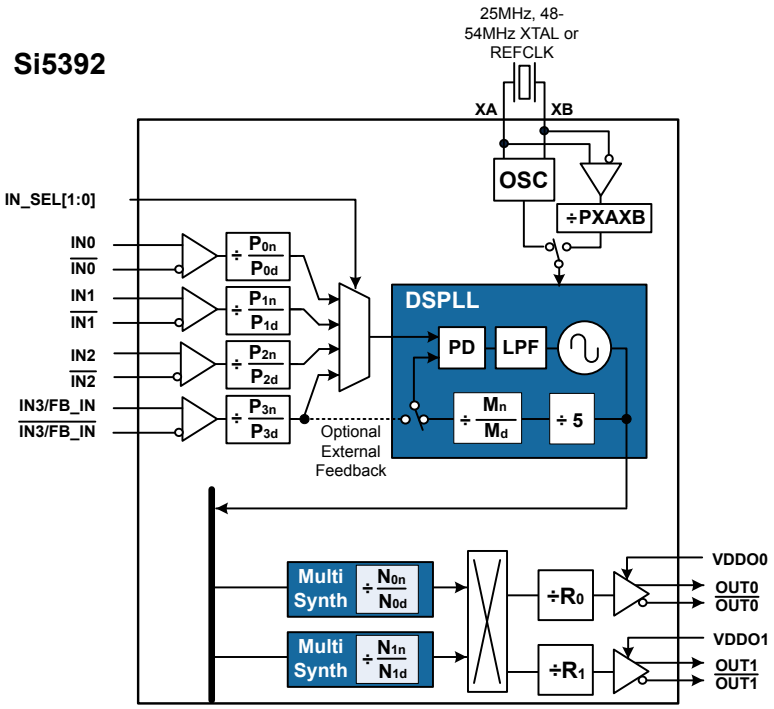


Figure 5.1. Clock Inputs Example Si5392

5.1 Input Source Selection

The inputs accept AC coupled clocks that are differential or singled ended such as LVCMOS. In addition, the inputs also accept DC coupled CMOS type inputs with 50% or very low input duty cycle. Input selection can be manual (pin or register controlled) or automatic with user definable priorities. There is a register to select pin or register control, and to configure the input as shown below.

Table 5.1. Input Selection Configuration

Register Name	Hex Address [Bit Field]	Function
CLK_SWITCH_MODE	0x0536[1:0]	Selects manual or automatic switching modes. Automatic mode can be revertive or non-revertive. Selections are the following: 00 Manual,01 Automatic non-revertive 02 Automatic revertive, 03 Reserved
IN_SEL_REGCTRL	0x052A [0]	0 for pin controlled clock selection 1 for register controlled clock selection
IN_SEL	0x052A [2:1]	0 for IN0, 1 for IN1, 2 for IN2, 3 for IN3 (or FB_IN)

5.1.1 Manual Input Switching

In manual mode, CLK_SWITCH_MODE=0x00.

Input switching can be done manually using the IN_SEL[1:0] device pins from the package or through register 0x052A IN_SEL[2:1]. Bit 0 of register 0x052A determines if the input selection is pin selectable or register selectable. The default is pin selectable. The following table describes the input selection on the pins. Note that when Zero Delay Mode is enabled, the FB_IN pins will become the feedback input and IN3 therefore is not available as a clock input. Note, in Zero Delay Mode, register based input clock selection must be done with IN_SEL (0x052A). If there is no clock signal on the selected input, the device will automatically enter free-run or holdover mode.

Table 5.2. Manual Input Selection using IN_SEL[1:0] Pins

IN_SEL[1:0] DEVICE PINS	Zero Delay Mode Disabled	Zero Delay Mode Enabled
00	IN0	IN0
01	IN1	IN1
10	IN2	IN2
11	IN3	Reserved

5.1.2 Automatic Input Switching

In automatic mode CLK_SWITCH_MODE = 0x01 (non-revertive) or 0x02 (revertive)

An automatic input switch is available in addition to the above mentioned manual switching option described in 5.1.1 Manual Input Switching. In automatic mode, the selection criteria is based on input clock qualification, input priority and the revertive option. The IN_SEL[1:0] pins or IN_SEL[2:1] register bits are not used in automatic input selection. Also, only input clocks that are valid (i.e., with no active alarms) can be selected by the automatic clock selection. If there are no valid input clocks available the DSPLL will enter the holdover mode. With revertive switching enabled, the highest priority input with a valid input clock is always selected. If an input with a higher priority becomes valid then an automatic switchover to that input will be initiated. With non-revertive switching, the active input will always remain selected while it is valid. If it becomes invalid an automatic switchover to a valid input with the highest priority will be initiated.

Table 5.3. Registers for Automatic Input Selection

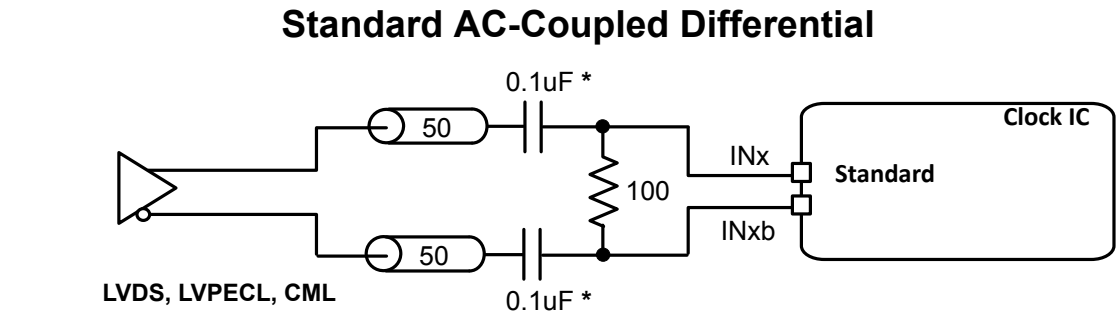
Register Name	Hex Address [Bit Field]	Function
CLK_SWITCH_MODE	0x0536[1:0]	Selects manual or automatic switching modes. Automatic mode can be revertive or non-revertive. Selections are the following: 00 Manual,01 Automatic non-revertive 02 Automatic revertive, 03 Reserved
ZDM_EN	0x0487[0]	0: disable zero delay mode 1: enable zero delay mode
ZDM_AUTOSW_EN	0x0487[4]	0: automatic switching disabled for zero-delay mode 1: automatic input switching enabled and input clock selection governed by automatic input switching engine
IN0_PRIORITY	0x0538[2:0]	IN0, IN1, IN2, IN3 priority select for the automatic selection state machine. Priority selections are 1,2,3,4, or zero for not selected.
IN1_PRIORITY	0x0538[6:4]	
IN2_PRIORITY	0x0539[2:0]	
IN3_PRIORITY	0x0539[6:4]	
IN_LOS_MSK	0x0537[3:0]	Determines the LOS status for IN3,2,1,0 and is used in determining a valid clock for automatic input selection 0 to use LOS in clock selection logic, 1 to mask LOS from the clock selection logic
IN_OOF_MSK	0x0537[7:4]	Determines the OOF status for IN3,2,1,0 and is used in determining a valid clock for the automatic input selection 0 to use OOF in the clock selection logic, 1 to mask the OOF from the clock selection logic

When in zero delay mode (ZDM_EN (0x0487[0]) the phase difference between the output, which is connected to the selected input, will be nulled to zero. However the IO delay variation will substantially increase in ZDM mode if the Fpfd is below 128 kHz. Phase buildout is not supported in Zero Delay Mode. See 5.2 Types of Inputs.

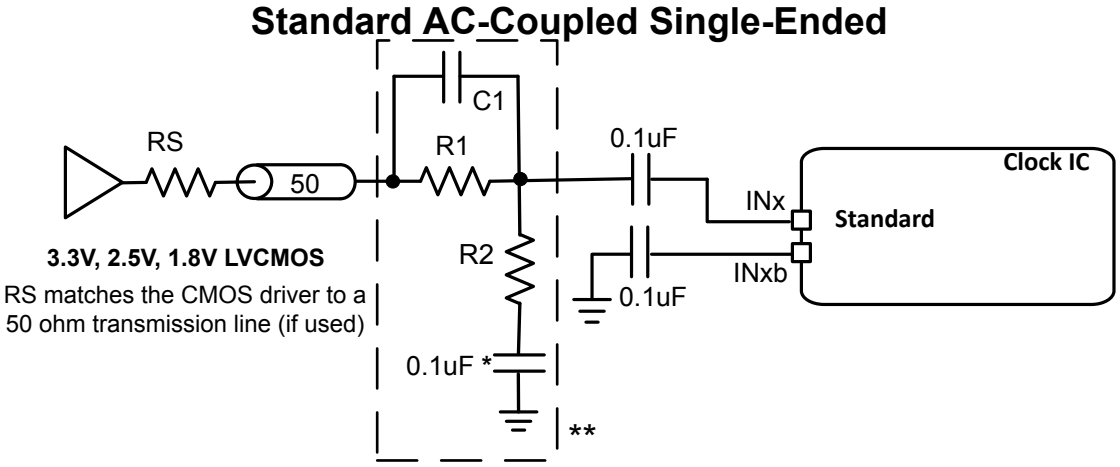
5.2 Types of Inputs

Each of the four different inputs IN0-IN3 can be configured as ac coupled differential formats such as LVDS, LVPECL, HCSL, CML, and ac-coupled single-ended CMOS formats. The standard format inputs have a nominal 50% duty cycle, must be ac-coupled and use the “Standard” input buffer selection as these pins are internally dc-biased to approximately 0.83 V.

Floating clock inputs are noise sensitive. Add a cap to ground for all non-CMOS unused clock inputs. To place the input into Standard Mode make sure IN_PULSED_CMOS_EN 0x949 [7:4] = 0. Bit 7 = IN3, Bit 6 = IN2, Bit 5 = IN1 and Bit 4 = IN0. Make sure the corresponding input bit is set to 0 for Standard Mode. If this bit is 1 this will turn on dc coupled CMOS Mode. Although the name is PULSED_CMOS_EN this setting actually corresponds to enable all dc coupled CMOS modes described further below for the Standard CMOS and Non-Standard/Pulsed CMOS inputs, which are all dc coupled inputs.



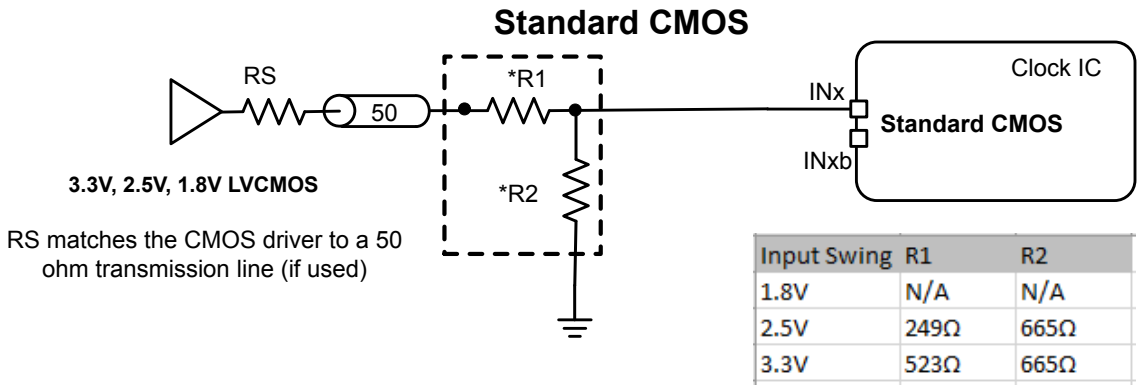
* These caps should have < ~5 ohms capacitive reactance at the clock input frequency.



*This cap should have less than ~20 ohms of capacitive reactance at the clock input frequency.
** Only when 3.3V LVCMOS driver is present, use R2 = 845 ohm and R1 = 267 ohm if needed to keep the signal at INx < 3.6 Vpp_se. Including C1 = 6 pf may improve the output jitter due to faster input slew rate at INx. If attenuation is not needed for Inx<3.6Vppse, make R1 = 0 ohm and omit C1, R2 and the capacitor below R2. C1, R1, and R2 should be physically placed as close as practicle to the device input pins.

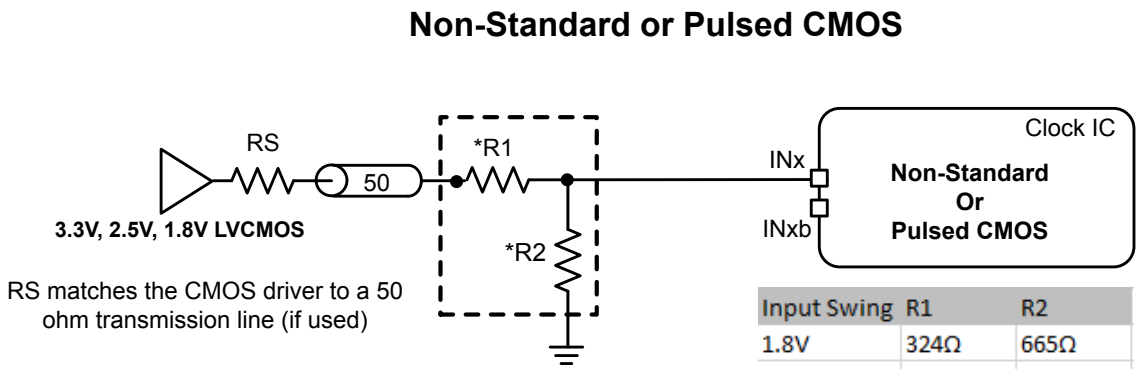
Figure 5.2. AC Coupled Standard Input Termination Diagrams

Each of the four different inputs IN0-IN3 can be configured as single ended **DC**-coupled standard CMOS, non-standard CMOS or pulsed CMOS inputs. In all cases, the inputs should be terminated near the device input pins. In these configurations CMOS mode is enabled via register setting "IN_PULSED_CMOS_EN" = 1 for each input. Note from the datasheet that the Standard CMOS selection has higher VIL and VIH settings than the non-standard/ pulsed CMOS Input buffer selection. Please see the datasheet for the max VIL and min VIH values for both Standard CMOS vs Non-standard CMOS & Pulsed CMOS selection. In general, following the “Standard **AC** Coupled Single Ended” arrangement shown above will give superior jitter performance than the **DC**-coupled arrangements below.



Input Swing	R1	R2
1.8V	N/A	N/A
2.5V	249Ω	665Ω
3.3V	523Ω	665Ω

* Attenuation circuit not required for 1.8V input or if all input specifications in datasheet are met.



Input Swing	R1	R2
1.8V	324Ω	665Ω
2.5V	665Ω	665Ω
3.3V	1.1kΩ	665Ω

* Attenuation circuit recommended but not required if input specifications in datasheet are met.

Figure 5.3. Input Terminations for DC Coupled Standard CMOS and Non-Standard/Pulsed CMOS Inputs

Standard CMOS refers to a signal with a swing of (1.8V, 2.5V or 3.3V) +/- 5% that complies with the specified maximum VIL and minimum VIH specifications in the datasheet. Please refer to the datasheet for the VIL and VIH specifications. For non-compliant inputs, a resistive attenuator is required as shown. It is not recommended to add the attenuation circuit for compliant inputs as it adversely affects the signal integrity at the input pins. Note that maximum input frequency cannot be guaranteed with the attenuator circuit. If an input exceeds 3.3V +5% then the input must be attenuated before going into the chip.

Non-standard CMOS refers to to a signal with a swing of (1.8V, 2.5V or 3.3 V) +/-5% that has been attenuated/level-shifted in order to comply with the specified non-standard maximum VIL and minimum VIH specifications. Please refer to the datasheet for the VIL and VIH specifications. For non-compliant inputs, a resistive attenuator is required as shown. It is not recommended to add the attenuation circuit for compliant inputs as it adversely affects the signal integrity at the input pins. Note that maximum input frequency cannot be guaranteed with the attenuator circuit. If an input exceeds 3.3V +5% then the input must be attenuated before going into the chip.

The pulsed CMOS input format allows pulse-based inputs, such as frame-sync and other synchronization signals having a duty cycle much less than 50%. These pulsed CMOS signals are DC-coupled and use the “Pulsed CMOS” Input Buffer selection. The resistor divider values given in the diagram will work with up to 1 MHz pulsed inputs. Pulsed CMOS refers to a low-frequency (up to 1 MHz), low/high duty cycle signal with a swing of (1.8 V, 2.5 V or 3.3 V) +/-5% that has been attenuated/level-shifted in order to comply with the specified non-standard maximum VIL and minimum VIH specifications. Please refer to the datasheet for the VIL and VIH specifications. Make sure to not violate the max and min specifications or use the attenuator circuit to ensure the specifications.

Input clock buffers are enabled by setting the IN_EN 0x0949[3:0] bits appropriately for IN3 through IN0. Unused clock inputs may be powered down and left unconnected at the system level. For standard mode inputs, both input pins must be properly connected, as shown in the above figure, including the “Standard AC Coupled Single Ended” case. In any of the CMOS modes, it is not necessary to connect the inverting INx input pin. To place the input buffer into any one of the CMOS modes, the corresponding bit must be set in IN_PULSED_CMOS_EN 0x0949[7:4]. Make sure the corresponding input bit is set to 1 for DC Coupled CMOS Mode. Although the name is PULSED_CMOS_EN this setting actually corresponds to enable all DC coupled CMOS modes. IN_CMOS_USE1P8 0x094F[7:4] determines Standard CMOS mode when the input bit is high and Non-Standard or Pulsed CMOS Mode when the input bit is low. The difference between Standard CMOS and Non-Standard/ Pulsed CMOS is the VIL/VIH settings, which should be reviewed carefully from the datasheet.

Table 5.4. Input Clock Control and Configuration Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5395/94/92	
IN_EN	0x0949[3:0]	Enable each of the input clock buffers for IN3 through IN0.
IN_PULSED_CMOS_EN	0x0949[7:4]	Enable CMOS mode for each input 1 = DC Coupled CMOS Mode either Standard or Non-Standard/Pulsed CMOS 0 = Standard AC Coupled Mode 7: IN3 6: IN2 5: IN1 4: IN0
IN_CMOS_USE1P8	0x094F[7:4]	1 = Standard DC-Coupled CMOS mode 0 = Non-Standard or Pulsed DC-Coupled CMOS Mode 7: IN3 6: IN2 5: IN1 4: IN0 Review datasheet for max and min VIL/VIH thresholds

5.2.1 Unused Inputs

Unused inputs can be disabled and left unconnected. Register 0x0949[3:0] defaults the input clocks to being enabled. Clearing the unused input bits will disable them. Enabled inputs not actively being driven by a clock may benefit from pull up or pull down resistors to avoid them responding to system noise.

5.2.2 Hitless Input Switching with Phase Buildout

Phase buildout, also referred to as hitless switching, prevents a phase change from propagating to the output when switching between two clock inputs with an integer related frequency and a fixed phase relationship (i.e., they are phase/frequency locked, but with a non-zero phase difference). When phase buildout is enabled, the DSPLL absorbs the phase difference between the two input clocks during a clock switch. When phase buildout is disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL loop bandwidth. Lower PLL loop bandwidth provides more filtering.

Hitless Switching with Phase Buildout should be used for applications where the input clocks are all locked to a common upstream clock, as in most synchronization systems. Hitless switching is supported for input frequencies down to 8 kHz. Gapped clocks are not recommended for use with Hitless Switching, as this may increase the phase transient on the outputs.

Table 5.5. Hitless Switching Enable Bit

Register Name	Hex Address [Bit Field]	Function
HSW_EN	0x0536[2]	Hitless switching is enabled = 1, or disabled = 0.

5.2.3 Use Case Scenario: Using More Than Two Inputs

When a DSPLL uses more than two inputs there is a rare but small chance that if two of the inputs are lost at the exact same time (within 1 PFD clock period) the switch to the 3rd available input will not occur correctly, and the state machine will be stuck pointing to a lost clock causing the PLL to lose lock. It won't recover unless manually switched to an available input.

Workaround: For designs using more than two inputs with hitless switching enabled follow the below guidance.

1. Do not disable two inputs at the exact same time. If both inputs must be shut off then leave at least one clock period of delay between shutting off one input and then shut off the other input.
2. Also consider including a LOS ISR (Interrupt Service Routine) that always checks for a LOS event with the active input pointing to an input that is LOS.

Outside the ISR make sure the device is already configured for input register control mode if this is an available feature for the device. Set IN_SEL_REGCTRL[0] = 1 for devices that have the option of both pin or register control.

LOS Interrupt Service Routine Pseudocode Example:

```
Step 1. If a LOS event occurs – read and store the LOS flags LOS_FLG 0x0012[0:3]

Step 2. Read the Input Active Register. This is named IN_ACTV 0x0507[7:6]. Compare this to the LOS flags
asserted in step 1. This is done to determine if the device is pointing to an input that is LOS asserted.

Step 3. If the input points to a LOS input, then set the input switch to manual mode.
Set CLK_SWITCH_MODE 0x0536[1:0] = 0

Step 4. Change the input to an available active input.
Set IN_SEL 0x052A[2:1]  Set to 0, 1, 2 or 3 whichever is the available active input.

Step 5. Verify IN_ACTV 0x0507[7:6] to make sure the input is pointing to the active input as expected.

Step 6. Go back to automatic mode
Set CLK_SWITCH_MODE 0x0536[1:0] = 1 for Automatic non revertive, or 2 for automatic revertive
```

For further guidance and workarounds please contact Silicon Labs.

5.2.4 Ramped Input Switching

When switching between input clocks that are not synchronized to the same upstream clock source (i.e. are plesiochronous) there will be differences in frequency between clocks. Ramped switching should be enabled in these cases to ensure a smooth frequency transition on the outputs. In this situation, it is also advisable to enable phase buildout, as discussed in the previous section to minimize the input-to-output clock skew after the frequency ramp has completed.

When ramped clock switching is enabled, the Si5395/94/92 will enter into holdover and then exit from holdover when the exit ramp has been calculated. This means that ramped switching behaves like an exit from holdover. This is particularly important when switching between two input clocks that are not the same frequency so that the transition between the two frequencies will be smooth and linear. Ramped switching is not needed for cases where the input clocks are locked to the same upstream clock source. The CBPro 'DSPLL Configure' page defaults to enable 'Ramped Exit from Holdover', but the user needs to select the 'Ramped Input Switching & Exit from Holdover' option when switching between non-synchronized input clocks.The same ramp rate settings are used for both exit from holdover and clock switching. For more information on ramped exit from holdover including the ramp rate, see Section 4.7 Holdover Mode.

Table 5.6. Ramped Switching Decision Matrix

Frequency Difference between Input Frequencies	f_{Pfd} > 500 kHz	f_{Pfd} < 500 kHz
Zero PPM	Select "Ramped Exit from Holdover"	
Non-Zero PPM	If difference is: • Less than 10 ppm, select "Ramped Exit from Holdover". • More than 10 ppm, select "Ramped input switching and Ramped Exit from Holdover".	Select "Ramped input switching and Ramped Exit from Holdover".

Table 5.7. Ramped Input Switching Control Registers

Setting Name	Hex Address [Bit Field]	Function
RAMP_STEP_INTERVAL	0x052C[7:5]	Calculated by CBPro based on the selected ramp rate.
RAMP_STEP_SIZE	0x05A5[2:0]	Calculated by CBPro based on the selected ramp rate.
RAMP_SWITCH_EN	0x05A6[3]	Enable frequency ramping on an input switch.
HSW_MODE	0x053A[1:0]	Input switching mode select.

5.2.5 Hitless Switching, LOL (Loss of Lock) and Fastlock

When doing a clock switch between clock inputs that are frequency locked, LOL may be momentarily asserted. In such cases, the assertion of LOL will invoke Fastlock. Because Fastlock temporarily increases the loop BW by asynchronously inserting new filter parameters into the DSPLL's closed loop, there may be transients at the clock outputs when Fastlock is entered or exited. For this reason, it is suggested that automatic entry into Fastlock be disabled by writing a zero to FASTLOCK_AUTO_EN whenever a clock switch might occur.

5.2.6 Glitchless Input Switching

The DSPLL has the ability to switch between two input clock frequencies that are up to ±500 ppm apart. The DSPLL will pull-in to the new frequency at a rate determined by the DSPLL loop bandwidth. The DSPLL loop bandwidth is set using registers 0x0508–0x050D. Note that if "Fastlock" is enabled then the DSPLL will pull-in to the new frequency using the Fastlock Loop Bandwidth. Depending on the LOL configuration settings, the loss of lock (LOL) indicator may assert while the DSPLL is pulling-in to the new clock frequency. Outputs will never generate runt pulses during input clock transitions.

5.2.7 External Clock Switching

When applications require an external switch, it is difficult for the the PLL to predict when that switch will occur. The Si5395/94/92 will temporarily go into holdover and then exit in a controlled manner to have a minimum phase/frequency transient. If expansion beyond the maximum number of inputs is required, please see AN1111: DSPLL Input Clock Expander which describes how an external FPGA can be used for this purpose.

5.2.8 Synchronizing to Gapped Input Clocks

The DSPLL supports locking to an input clock with missing clock edges. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its edges. Gapping a clock significantly increases its jitter so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter, periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock. A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of 2 missing cycles out of every 8. Gapped input clocks are not recommended for use with Hitless Switching, as the output phase transients may be significantly higher.

When properly configured, locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification for a maximum phase transient, when the switch occurs during a gap in either input clocks. The following figure shows a 100 MHz clock with one cycle removed every 10 cycles, which results in a 90 MHz periodic non-gapped output clock.

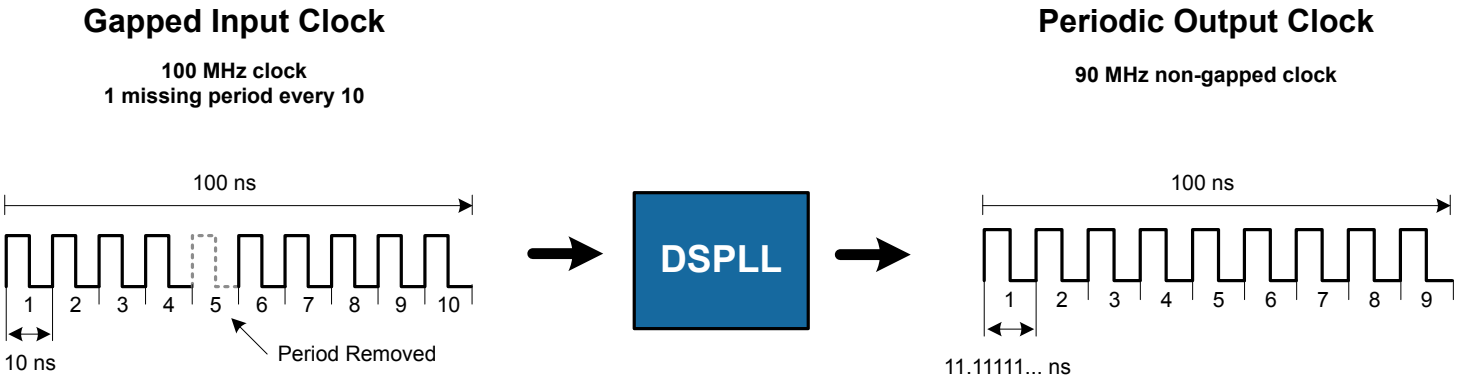


Figure 5.4. Gapped Input Clock Use

5.2.9 Rise Time Considerations

It is well known that slow rise time signals with low slew rates are a cause of increased jitter. In spite of the fact that the low loop BW of the Si5395/94/92 will attenuate a good portion of the jitter that is associated with a slow rise time clock input, if the slew rate is low enough, the output jitter will increase. The following figure shows the effect of a low slew rate on RMS jitter for a differential clock input. It shows the relative increase in the amount of RMS jitter due to slow rise time and is not intended to show absolute jitter values.

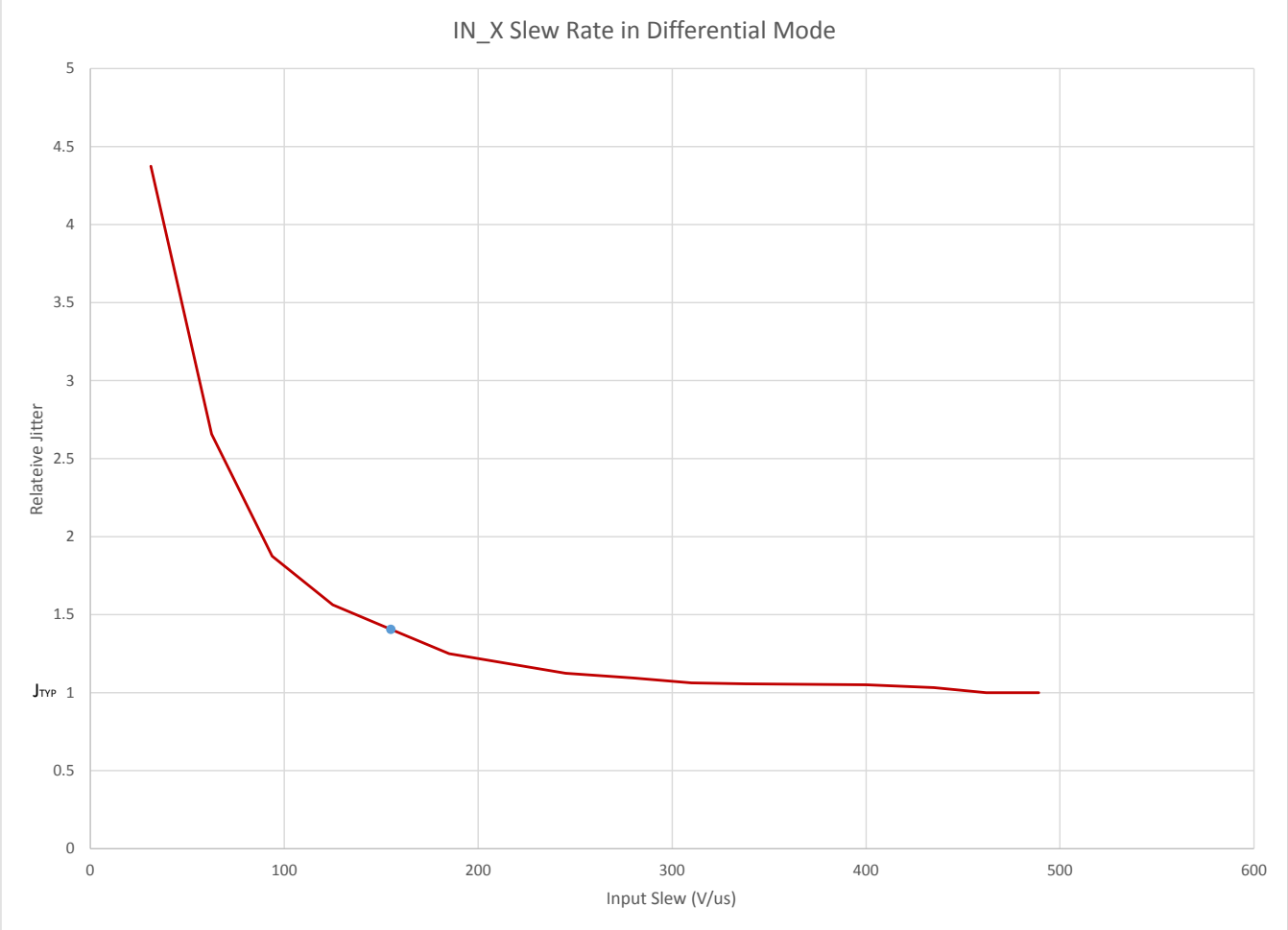


Figure 5.5. Effect of Low Slew Rate on RMS Jitter

5.3 Fault Monitoring

All four input clocks (IN0, IN1, IN2, IN3) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown below. The reference at the XA/XB pins (grades A/B/C/D/P) or the integrated reference (grade J/K/L/M/E) are monitored for LOS since it provides a critical reference clock for the DSPLLs. There is a Loss Of Lock (LOL) indicator asserted when the DSPLL loses synchronization with its reference input.

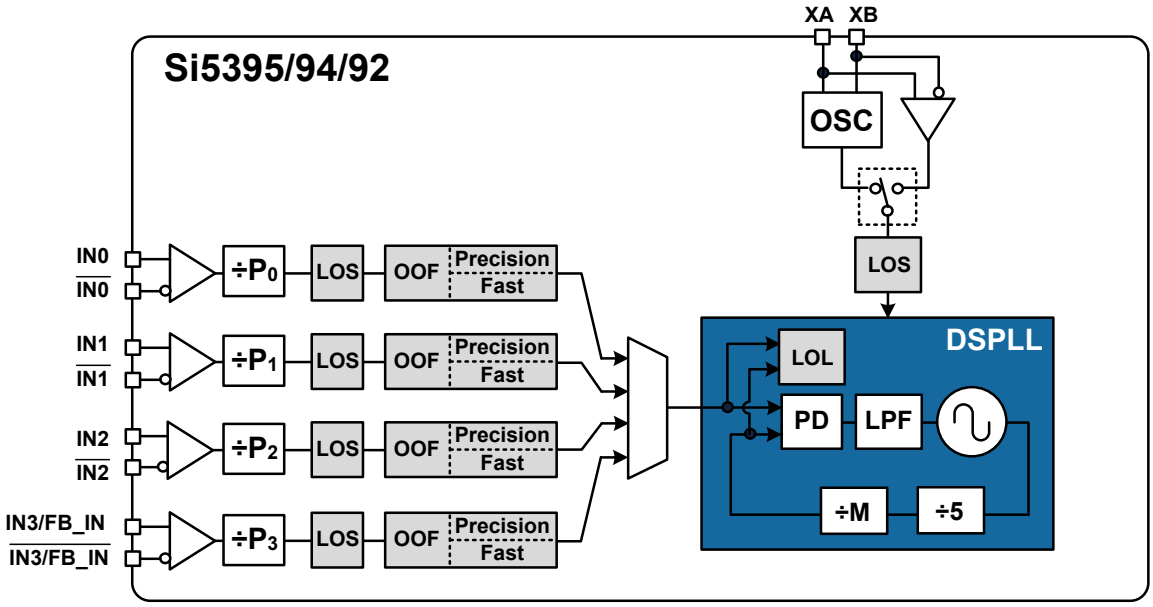


Figure 5.6. Fault Monitors

5.3.1 Input Loss of Signal (LOS) Fault Detection

The loss of signal monitor qualifies the input signal with the following criteria to determine if a valid signal is present. The loss of signal monitor measures the period of each phase detector input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits compares the measured phase detector input period to a maximum (set) and minimum (clear) period thresholds. LOS asserts if the maximum input period threshold is exceeded or if the input period is less than the minimum input period threshold. The thresholds for assert and de-assert of LOS are specified in a number of corresponding clock cycles at the input to the phase detector which is the input clock divided by it's corresponding P divider. This is translated to a time based on the frequency of the corresponding phase detetor input clock. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility.

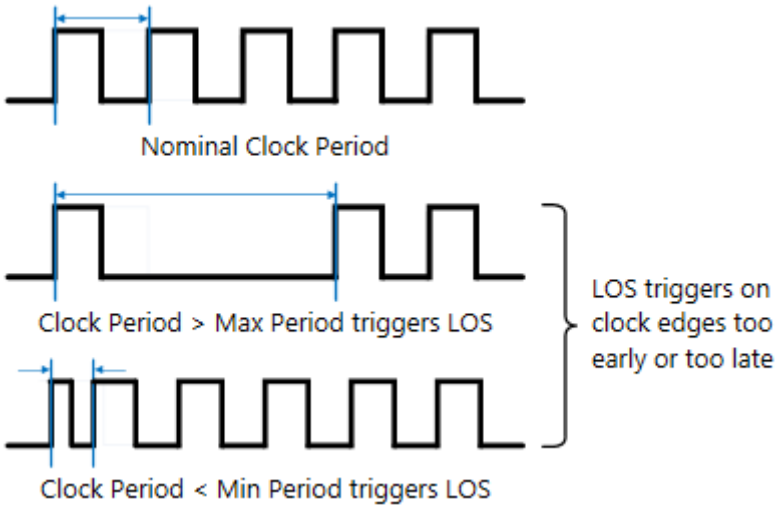


Figure 5.7. LOS Clock Maximum (Trigger) and Minimum (Clear) Period Thresholds

The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register when set, always stays asserted until cleared by the user.

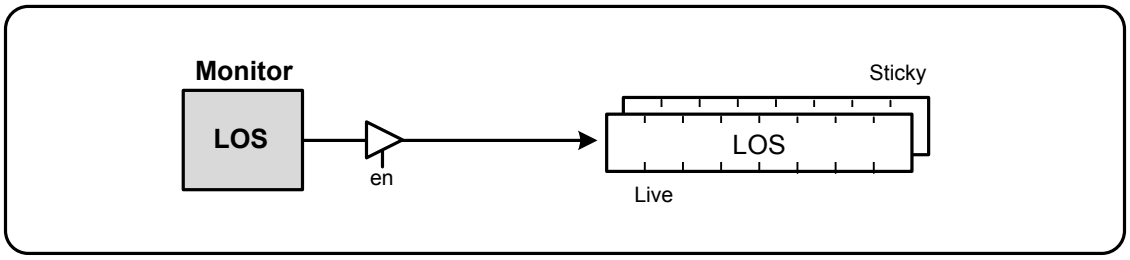


Figure 5.8. LOS Status Indicators

A LOS monitor is also available to ensure that the external crystal or reference clock is valid. By default the output clocks are disabled when LOSXAXB is detected. This feature can be disabled such that the device will continue to produce output clocks even when LOSXAXB is detected. Single-ended inputs must be connected to the XA input pin with the XB pin terminated properly for LOSXAXB to function correctly. The table below lists the loss of signal status indicators and fault monitoring control registers.

Table 5.8. Loss of Signal Status Monitoring and Control Registers

Register Name	Hex Address [Bit Field]	Function
LOS	0x000D[3:0]	LOS status monitor for IN3 (bit3), IN2 (bit2), IN1(bit1), IN0 (bit0) indicates if a valid clock is detected. A set bit indicates the input is LOS.
SYSINCAL	0x000C[0]	Asserted when in calibration
LOSXAXB	0x000C[1]	LOS status monitor for the XTAL or REFCLK at the XA/XB pins

Register Name	Hex Address [Bit Field]	Function
LOS_FLG	0x0012[3:0]	LOS status monitor sticky bits for IN3, IN2, IN1, IN0. Sticky bits will remain asserted when a LOS event occurs until manually cleared. Writing zero to the bit will clear it.
SYSINCAL_FLG	0x0011[0]	SYSINCAL sticky bit. Sticky bits will remain asserted until written with a zero to clear.
LOSXAXB_FLG	0x0011[1]	LOS status monitor sticky bits for XAXB. Sticky bits will remain asserted when a LOS event occurs until cleared. Writing zero to the bit will clear it.
LOS_EN	0x002C[3:0]	LOS monitor enable for IN3, IN2, IN1, IN0. Allows disabling the monitor if unused. 0: Disable LOS Detection 1: Enable LOS Detection (default)
LOSXAXB_DIS	0x002C[4]	Enable LOS detection on the XAXB inputs. 0: Enable LOS Detection (default) 1: Disable LOS Detection
LOS_TRG_THR	0x002E[7:0]-0x0035[7:0]	Sets the LOS trigger threshold and clear sensitivity for IN3, IN2, IN1, IN0. These 16- bit values are determined by ClockBuilder Pro. The trigger threshold sets the maximum period and the clear threshold sets the minimum period.
LOS_CLR_THR	0x0036[7:0]-0x003D[7:0]	
LOS_INTR_MSK	0x0018[3:0]	This is the LOS interrupt mask, which can be cleared to trigger an interrupt on the INTR pin if an LOS occurs for IN0-3.

5.3.2 Out of Frequency (OOF) Fault Detection

Each input clock is monitored for frequency accuracy with respect to an OOF reference which it considers as its 0 ppm reference. This OOF reference can be selected as either:

- XA/XB pins
- Any input clock (IN0, IN1, IN2, IN3)

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure directly below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state and its sticky register bit stays asserted until cleared.

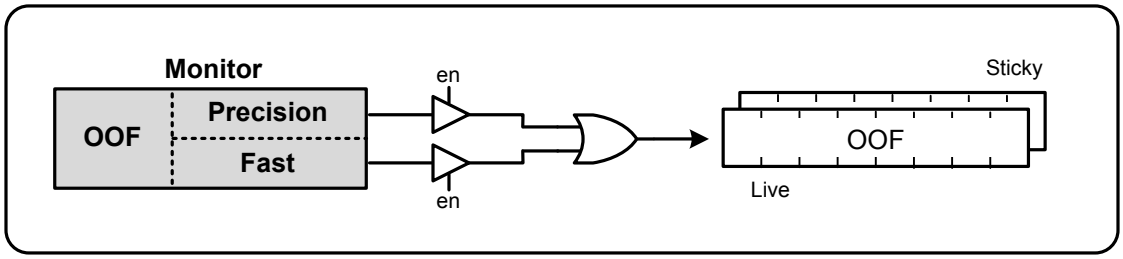


Figure 5.9. OOF Status Indicator

The Precision OOF monitor circuit measures the frequency of all input clocks to within up to ±0.0625 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the register-programmable OOF frequency range of from ±0.0625 ppm to ±512 ppm in steps of 1/16 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0–IN3) as the 0 ppm OOF reference instead of the XAXB pins is available. These options are all register configurable.

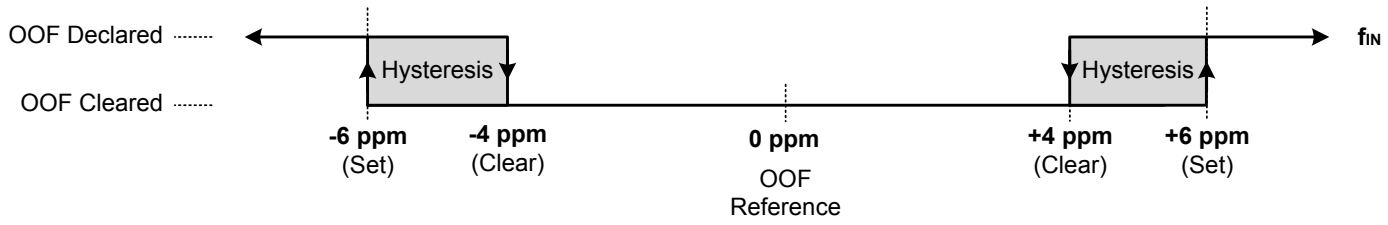


Figure 5.10. Example of Precise OOF Monitor Assertion and De-assertion Triggers

The table below lists the OOF monitoring and control registers. Because the precision OOF monitor needs to provide 1/16 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF responds more quickly and has larger thresholds.

Table 5.9. Out-of-Frequency Status Monitoring and Control Registers

Register Name	Hex Address [Bit Field]	Function
OOF	0x000D[7:4]	OOF status monitor for IN3, IN2, IN1, IN0. Indicates if a valid clock is detected or if a OOF condition is detected.
OOF_FLG	0x0012[7:4]	OOF status monitor sticky bits for IN3, IN2, IN1, IN0. Stick bits will remain asserted when an OOF event occurs until cleared. Writing zero to the bit will clear it.
OOF_INTR_MSK	0x0018[7:4]	Masks OOF from generating INTR interrupt for IN3 – IN0. 0: Allow OOF interrupt (default) 1: Mask (ignore) OOF for interrupt
OOF_REF_SEL	0x0040[2:0]	This selects the clock that the OOF monitors use as the 0 ppm reference. Selections are XA/XB, IN0, IN1, IN2, IN3. Default is XAXB.
OOF_EN	0x003F[3:0]	This allows to enable/disable the precision OOF monitor for IN3, IN2, IN1, IN0
FAST_OOF_EN	0x003F[7:4]	This allows to enable/disable the fast OOF monitor for IN3, IN2, IN1, IN0
OOF_SET_THR	0x0046[7:0]-0x0049[7:0]	OOF Set threshold. Range is up to ±500 ppm in steps of 1/16 ppm
OOF_CLR_THR	0x004A[7:0]-0x004D[7:0]	OOF Clear threshold. Range is up to ±500 ppm in steps of 1/16 ppm
FAST_OOF_SET_THR	0x0051[7:0]-0x0054[7:0]	Determines the fast OOF alarm set threshold for IN3, IN2, IN1, IN0.
FAST_OOF_CLR_THR	0x0055[7:0]-0x0058[7:0]	Determines the fast OOF alarm clear threshold for IN3, IN2, IN1, IN0.

5.3.3 Loss of Lock (LOL) Fault Monitoring

The Loss of Lock (LOL) monitor asserts a LOL register bit when the DSPLL has lost synchronization with its selected input clock. There is also a dedicated loss of lock pin that reflects the loss of lock condition. The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are four parameters that control the LOL monitor. First, there is an **assert threshold** which sets the LOL assertion threshold. The user sets this threshold in ppm in CBPro. Then, there is a **fast assert threshold**. CBPro sets this to ~100 times the assert threshold. Then there is a **de-assert threshold** to clear the LOL, which is set in ppm in CBPro. Then, there is a **clear delay**, which CBPro sets based upon the project plan.

Note: A very large ppm error in a short time will assert LOL.

A block diagram of the LOL monitor is shown below. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOL pin reflects the current state of the LOL monitor.

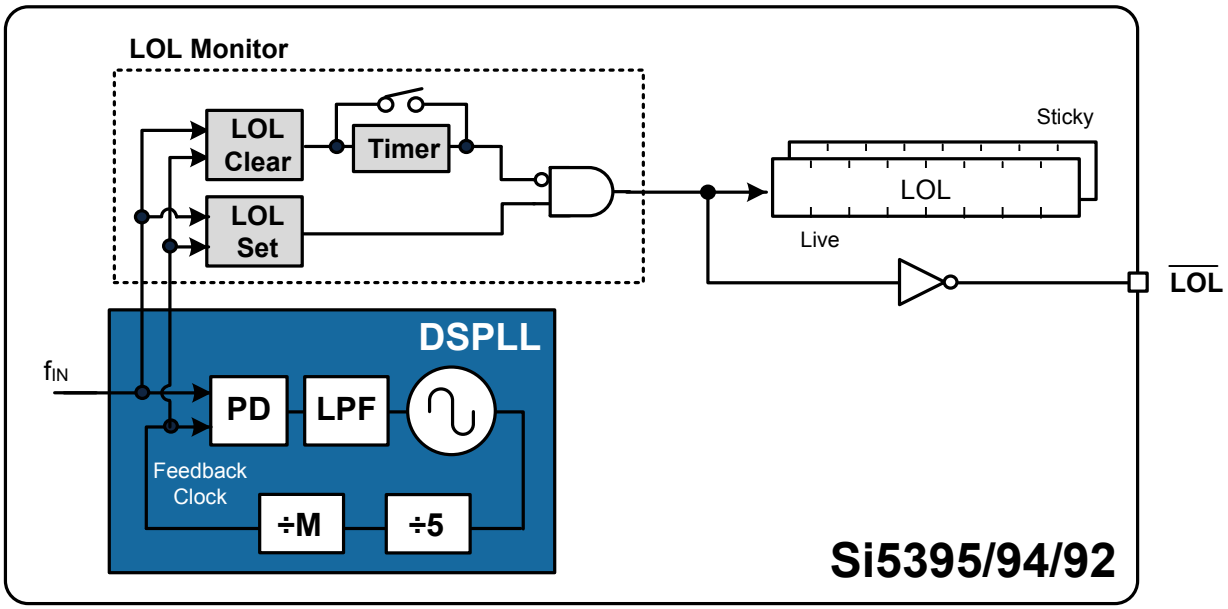


Figure 5.11. LOL Status Indicators

The LOL frequency monitors have an adjustable sensitivity which is register configurable from 0.1 ppm to 10000 ppm. CBPro provides a wide range of set and clear thresholds for the LOL function. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration of the LOL set and clear thresholds is shown below.

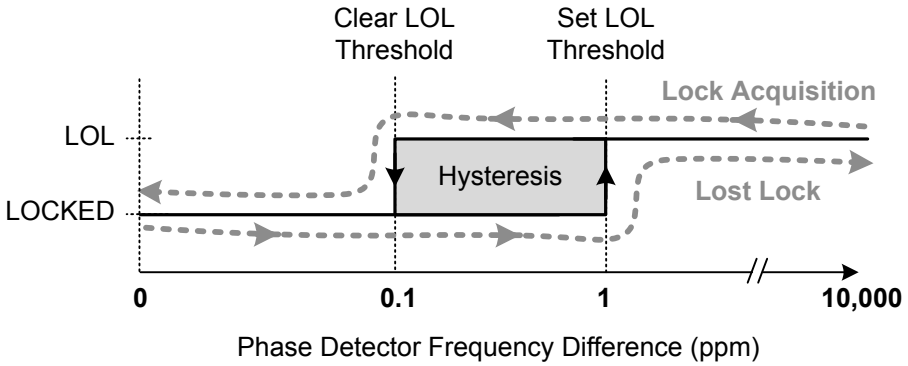


Figure 5.12. LOL Set and Clear Thresholds

Table 5.10. Loss of Lock Status Monitor and Control Registers

Register Name	Hex Address [Bit Field]	Function
LOL	0x000E[1]	Status bit that indicates if the DSPLL is locked to an input clock
LOL_FLG	0x0013[1]	Sticky bits for LOL register. Writing 0 to a sticky bit will clear it.
LOL_SET_THR	0x009E[7:4]	Configures the loss of lock set threshold in ppm.
LOL_CLR_THR	0x00A0[7:4]	Configures the loss of lock clear threshold in ppm.
LOL_TIMER_EN	0x00A2[1]	Allows bypassing the LOL clear delay timer. 0-bypassed, 1-enabled. Set by CBPro.
LOL_NOSIG_TIME	0x02B7[3:2]	Sets 417 µs as time without an input to assert LOL. Set by CBPro.
LOL_CLR_DELAY_DIV256	[0x00AC[4:0] 0x00AB[7:0] 0x00AA[7:0] 0x00A9[7:0]]	This 29 bit timer sets the delay value for the LOL clear delay timer. Set by CBPro.
FASTLOCK_EXTEND_EN	0x00E5[5]	Enables FASTLOCK_EXTEND.
FASTLOCK_EXTEND	[0x00ED[4:0] 0x00EC[7:0] 0x00EB[7:0] 0x00EA[7:0]]	Set by CBPro to minimize phase transients when switching the PLL bandwidth.
FASTLOCK_EXTEND_SCL	0x0294[7:4]	Set by CBPro.
LOL_SLW_VALWIN_SELX	0x0296[1]	Set by CBPro.
FASTLOCK_DLY_ONSW_EN	0x0297[1]	Set by CBPro.
FASTLOCK_DLY_ONSW	0x02A9[19:0]	Set by CBPro.
FASTLOCK_DLY_ONLOL_EN	0x0299[1]	Set by CBPro.
FASTLOCK_DLY_ONLOL	0x029D[19:0]	Set by CBPro.

The settings in the table above are handled by ClockBuilder Pro. Manual settings should be avoided.

5.3.4 Interrupt Pin (INTR)

An interrupt pin (INTR) indicates a change in state with any of the status indicators for any of the DSPLLs. All status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTR pin is reset by clearing the sticky status registers.

Table 5.11. Interrupt Mask Registers

Register Name	Hex Address [Bit Field]	Function
LOS(3, 2, 1, 0)_INTR_MSK	0018[3:0]	Prevents IN3, IN2, IN1, IN0 LOS from asserting the INTR pin
OOF(3, 2, 1, 0)_INTR_MSK	0018[7:4]	Prevents IN3, IN2, IN1, IN0 OOF from asserting the INTR pin
LOSXAXB_INTR_MSK	0017[1]	Prevents XAXB LOS from asserting the INTR pin
LOL_INTR_MSK	0019[1]	Prevents the DSPLL from asserting the INTR pin
HOLD_INTR_MSK	0019[5]	Prevents the DSPLL HOLD from asserting the INTR pin

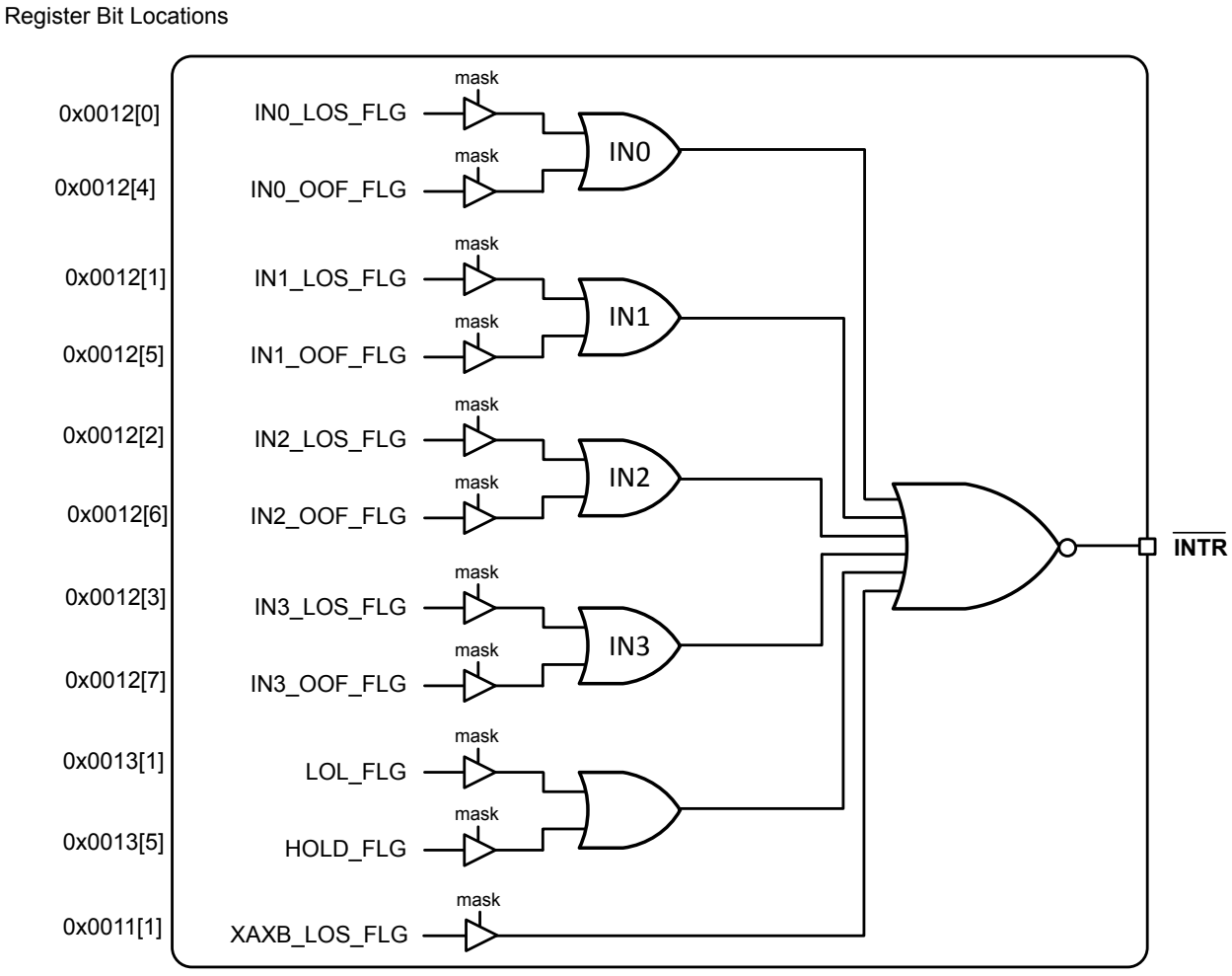


Figure 5.13. Interrupt Triggers and Masks

The _FLG bits are “sticky” versions of the alarm bits and will stay high until cleared. A _FLG bit can be cleared by writing a zero to the _FLG bit. When a _FLG bit is high and its corresponding alarm bit is low, the _FLG bit can be cleared.

During run time, the source of an interrupt can be determined by reading the _FLG register values and logically ANDing them with the corresponding _MSK register bits (after inverting the _MSK bit values). If the result is a logic one, then the _FLG bit will cause an interrupt.

For example, if LOS_FLG[0] is high and LOS_INTR_MSK[0] is low, then the INTR pin will be active (low) and cause an interrupt. If LOS[0] is zero and LOS_MSK[0] is one, writing a zero to LOS_MSK[0] will clear the interrupt (assuming that there are no other interrupt sources). If LOS[0] is high, then LOS_FLG[0] and the interrupt cannot be cleared.

Note: The INTR pin may toggle during reset.

6. Outputs

The Si5395 supports up to 12 differential output drivers. The Si5394 supports up to four differential outputs and the Si5392 supports two. Each driver has a configurable voltage amplitude and common mode voltage covering a wide variety of differential signal formats including LVPECL, LVDS, HCSL, with CML-compatible amplitudes. In addition to supporting differential signals, any of the outputs can be configured as dual single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 24 single-ended outputs for the Si5395, 8 single-ended outputs for the Si5394 and up to 4 single-ended outputs for the Si5392. There can be any combination of differential and single-ended outputs.

6.1 Output Crosspoint Switch

A crosspoint switch allows any of the output drivers to connect with any of the MultiSynths as shown in Figure 6.1 MultiSynth to Output Driver Crosspoint on page 43. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up. Any MultiSynth output can connect to multiple output drivers.

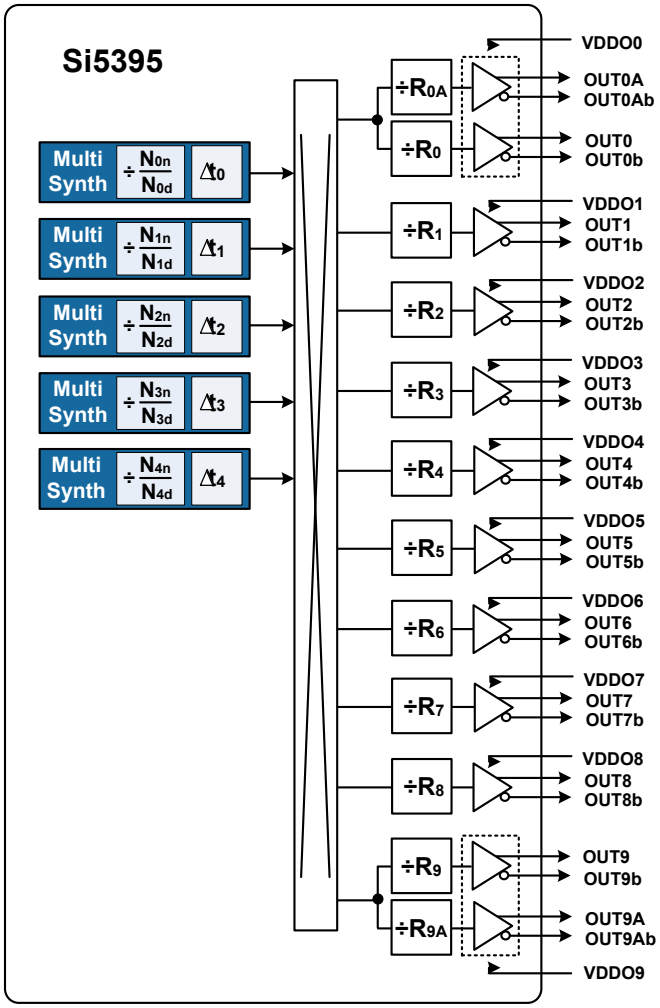


Figure 6.1. MultiSynth to Output Driver Crosspoint

The figure above is used to set up the routing from the MultiSynth frequency selection to the output.

Table 6.1. Output Driver Crosspoint Configuration Registers

Register Name	Hex Address [Bit Field]			Function
	Si5395	Si5394	Si5392	
OUT0A_MUX_SEL	0x106[2:0]	—	—	Connects the output drivers to one of the N dividers. Selections are N0, N1, N2, N3, N4 for each output divider.
OUT0_MUX_SEL	0x010B[2:0]	0x0115[2:0]	0x0115[2:0]	
OUT1_MUX_SEL	0x0110[2:0]	0x011A[2:0]	0x011A[2:0]	
OUT2_MUX_SEL	0x0115[2:0]	0x0129[2:0]	—	
OUT3_MUX_SEL	0x011A[2:0]	0x012E[2:0]	—	
OUT4_MUX_SEL	0x011F[2:0]	—	—	
OUT5_MUX_SEL	0x0124[2:0]	—	—	
OUT6_MUX_SEL	0x0129[2:0]	—	—	
OUT7_MUX_SEL	0x012E[2:0]	—	—	
OUT8_MUX_SEL	0x0133[2:0]	—	—	
OUT9_MUX_SEL	0x0138[2:0]	—	—	
OUT9A_MUX_SEL	0x013D[2:0]	—	—	

6.2 Performance Guidelines for Outputs

Whenever a number of high frequency, fast rise time, large amplitude signals are all close to one another there will be some amount of crosstalk. The jitter generation of the Si5395/94/92 is so low that crosstalk can become a significant portion of the final measured output jitter. Some of the crosstalk will come from the Si5395/94/92, and some will be introduced by the PCB. It is difficult (and possibly irrelevant) to allocate the jitter portions between these two sources since the Si5395/94/92 must be attached to a board in order to measure jitter.

For extra fine tuning and optimization in addition to following the usual PCB layout guidelines, crosstalk can be minimized by modifying the arrangements of different output clocks. For example, consider the following lineup of output clocks in following table.

Table 6.2. Example of Output Clock Placement

Output	Not Recommended (Frequency MHz)	Recommended (Frequency MHz)
0	155.52	155.52
1	156.25	155.52
2	155.52	622.08
3	156.25	Not used
4	200	156.25
5	100	156.25
6	622.08	625
7	625	Not used
8	Not used	200
9	Not used	100

Using this example, a few guidelines are illustrated:

1. Avoid adjacent frequency values that are close. For example, a 155.52 MHz clock should not be placed next to a 156.25 MHz clock. If the jitter integration bandwidth goes up to 20 MHz then keep adjacent frequencies at least 20 MHz apart.
2. Adjacent frequency values that are integer multiples of one another are allowed, and these outputs should be grouped together when possible. Noting that because 155.52 MHz x 4 = 622.08 MHz, it is okay to place the pair of these frequency values close to one another.
3. Unused outputs can be used to separate clock outputs that might otherwise interfere with one another.

If some outputs have tight jitter requirements while others are relatively loose, rearrange the clock outputs so that the critical outputs are the least susceptible to crosstalk. These guidelines need to be followed by those applications that wish to achieve the highest possible levels of jitter performance. Because CMOS outputs have large pk-pk swings, are single ended, and do not present a balanced load to the VDDO supplies, they generate much more crosstalk than differential outputs. For this reason, CMOS outputs should be avoided in jitter-sensitive applications. When CMOS clocks are unavoidable, even greater care must be taken with respect to the above guidelines. For more information on these issues, see application note, "AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems."

The ClockBuilder Pro Clock Placement Wizard is an easy way to reduce crosstalk for a given frequency plan. This feature can be accessed on the “Define Output Frequencies” page of ClockBuilder Pro in the lower left hand corner of the GUI. It is recommended to use this tool after each project frequency plan change.

6.3 Output Signal Format

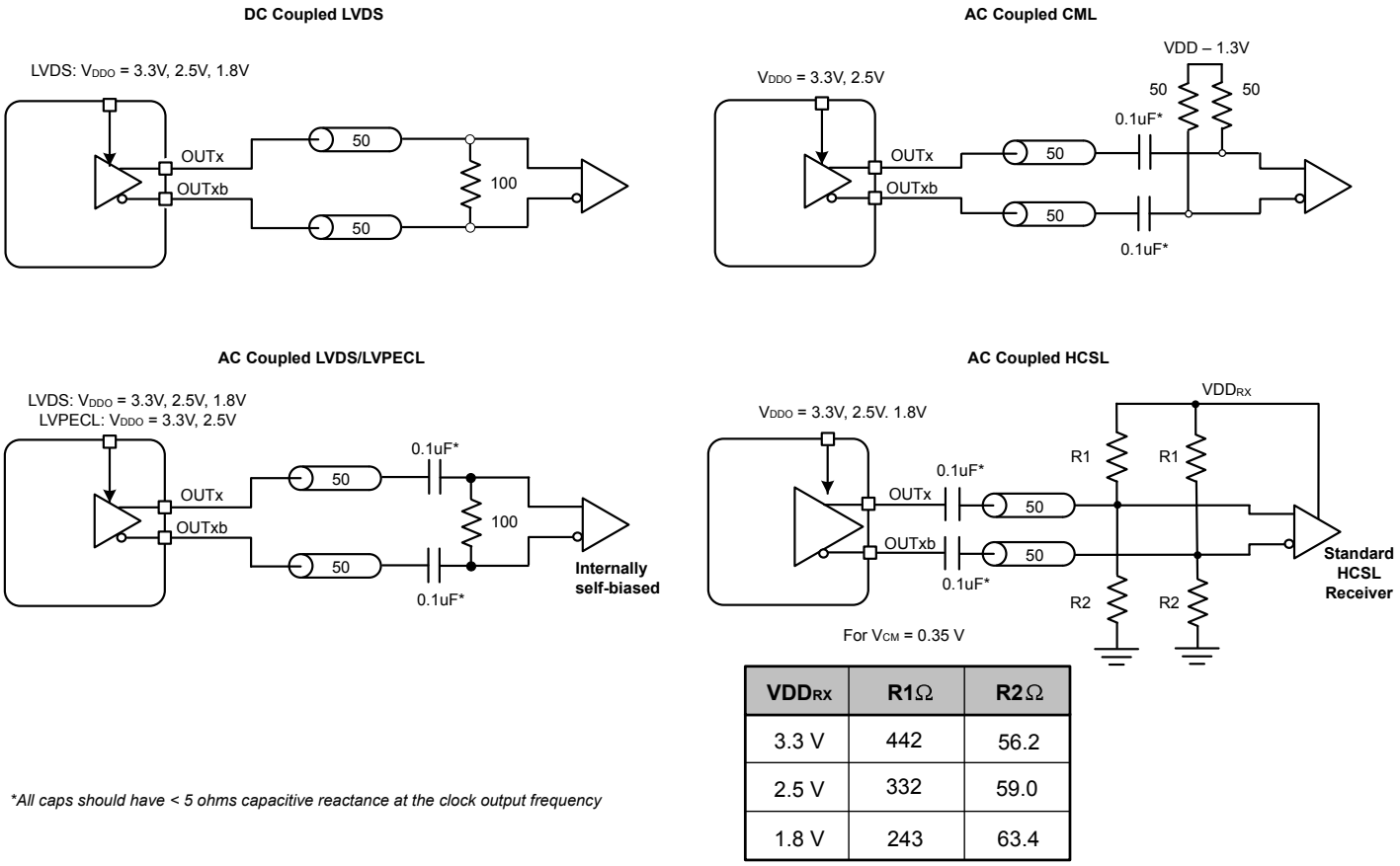
The differential output swing and common mode voltage are both fully programmable covering a wide variety of signal formats including LVDS, LVPECL, and HCSL. For CML applications, see Section 6.3.9 Setting the Differential Output Driver to Non-Standard Amplitudes. The differential formats can be either normal or low power. Low power format uses less power for the same amplitude but has the drawback of slower rise/fall times. The source impedance in low power format is much higher than 100 Ω. See Section 6.3.9 Setting the Differential Output Driver to Non-Standard Amplitudes for register settings to implement variable amplitude differential outputs. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3, 2.5, or 1.8 V) drivers providing up to 8 (for the Si5394) single-ended outputs, or any combination of differential and single-ended outputs. Note also that CMOS output can create much more crosstalk than differential outputs so extra care must be taken in their pin replacement so that other clocks that need the lowest jitter are not on nearby pins. See AN862: Optimizing Jitter Performance in Next Generation Internet Infrastructure Systems for additional information.

Table 6.3. Output Signal Format Control Registers

Register Name	Hex Address [Bit Field]			Function
	Si5395	Si5394	Si5392	
OUT0A_FORMAT	0x0104[2:0]	—	—	Selects the output signal format as differential or LVCMOS mode.
OUT0_FORMAT	0x0109[2:0]	0x0113[2:0]	0x0113[2:0]	
OUT1_ FORMAT	0x010E[2:0]	0x0118[2:0]	0x0118[2:0]	
OUT2_ FORMAT	0x0113[2:0]	0x0127[2:0]	—	
OUT3_ FORMAT	0x0118[2:0]	0x012C[2:0]	—	
OUT4_ FORMAT	0x011D[2:0]	—	—	
OUT5_ FORMAT	0x0122[2:0]	—	—	
OUT6_ FORMAT	0x0127[2:0]	—	—	
OUT7_ FORMAT	0x012C[2:0]	—	—	
OUT8_ FORMAT	0x0131[2:0]	—	—	
OUT9_ FORMAT	0x0136[2:0]	—	—	
OUT9A_ FORMAT	0x013B[2:0]	—	—	

6.3.1 Differential Output Terminations

The differential output drivers support both ac and dc-coupled terminations as shown in the following figure.



VDDRX	R1Ω	R2Ω
3.3 V	442	56.2
2.5 V	332	59.0
1.8 V	243	63.4

*All caps should have < 5 ohms capacitive reactance at the clock output frequency

Figure 6.2. Supported Differential Output Terminations

6.3.2 Differential Output Swing Modes

There are two selectable differential output swing modes: Normal and High (also called low power mode). Each output can support a unique mode.

Differential Normal Swing Mode—This is the usual selection for differential outputs and should be used, unless there is a specific reason to do otherwise. When an output driver is configured in normal swing mode, its output swing is selectable as one of 7 settings ranging from 200 mVpp_se to 800 mVpp_se in increments of 100 mV. Differential Output Voltage Swing Control Registers lists the registers that control the output voltage swing. The output impedance in the Normal Swing Mode is 100 Ω differential. Any of the terminations shown in Figure 6.2 Supported Differential Output Terminations on page 47 are supported in this mode.

Differential High Swing Mode—When an output driver is configured in high swing mode, its output swing is configurable as one of 7 settings ranging from 400 mVpp_se to 1600 mVpp_se in increments of 200 mV. The output driver is in high impedance mode and supports standard 50 Ω PCB traces. Any of the terminations shown in Figure 6.2 Supported Differential Output Terminations on page 47 are supported. The use of High Swing mode will result in larger pk-pk output swings that draw less power. The trade off will be slower rise and fall times.

Vpp_diff is 2 x Vpp_se as shown below.

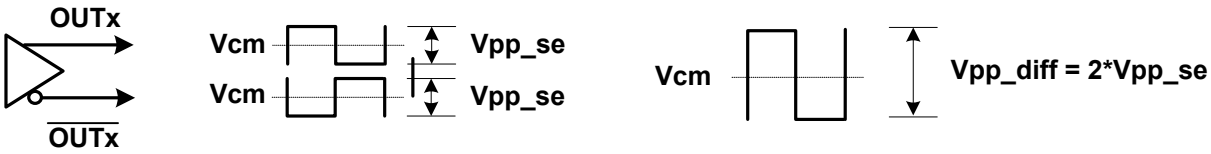


Figure 6.3. Vpp_se and Vpp_diff

Table 6.4. Differential Output Voltage Swing Control Registers

Register Name	Hex Address [Bit Field]			Function
	Si5395	Si5394	Si5392	
OUT0A_AMPL	0x0105[6:4]	—	—	Sets the voltage swing for the differential output drivers for both normal and high swing modes.
OUT0_AMPL	0x010A[6:4]	0x0114[6:4]	0x0114[6:4]	
OUT1_ AMPL	0x010F[6:4]	0x0119[6:4]	0x0119[6:4]	
OUT2_ AMPL	0x0114[6:4]	0x0128[6:4]	—	
OUT3_ AMPL	0x0119[6:4]	0x012D[6:4]	—	
OUT4_ AMPL	0x011E[6:4]	—	—	
OUT5_ AMPL	0x0123[6:4]	—	—	
OUT6_ AMPL	0x0128[6:4]	—	—	
OUT7_ AMPL	0x012D[6:4]	—	—	
OUT8_ AMPL	0x0132[6:4]	—	—	
OUT9_ AMPL	0x0137[6:4]	—	—	
OUT9A_ AMPL	0x013C[6:4]	—	—	

6.3.3 Programmable Common Mode Voltage for Differential Outputs

The common mode voltage (VCM) for the differential Normal and High Swing modes is programmable in 100 mV increments from 0.7 to 2.3 V depending on the voltage available at the output's VDDO pin. Setting the common mode voltage is useful when dc coupling the output drivers. High swing mode may also cause an increase in the rise/fall time.

Table 6.5. Differential Output Common Mode Voltage Control Registers

Register Name	Hex Address [Bit Field]			Function
	Si5395	Si5394	Si5392	
OUT0A_CM	0x0105[3:0]	—	—	Sets the common mode voltage for the differential output driver.
OUT0_CM	0x010A[3:0]	0x0114[3:0]	0x0114[3:0]	
OUT1_ CM	0x010F[3:0]	0x0119[3:0]	0x0119[3:0]	
OUT2_ CM	0x0114[3:0]	0x0128[3:0]	—	
OUT3_ CM	0x0119[3:0]	0x012D[3:0]	—	
OUT4_ CM	0x011E[3:0]	—	—	
OUT5_ CM	0x0123[3:0]	—	—	
OUT6_ CM	0x0128[3:0]	—	—	
OUT7_ CM	0x012D[3:0]	—	—	
OUT8_ CM	0x0132[3:0]	—	—	
OUT9_ CM	0x0137[3:0]	—	—	
OUT9A_ CM	0x013C[3:0]	—	—	

6.3.4 LVCMOS Output Terminations

LVCMOS outputs are dc-coupled as shown in Figure 6.4 LVCMOS Output Terminations on page 49.

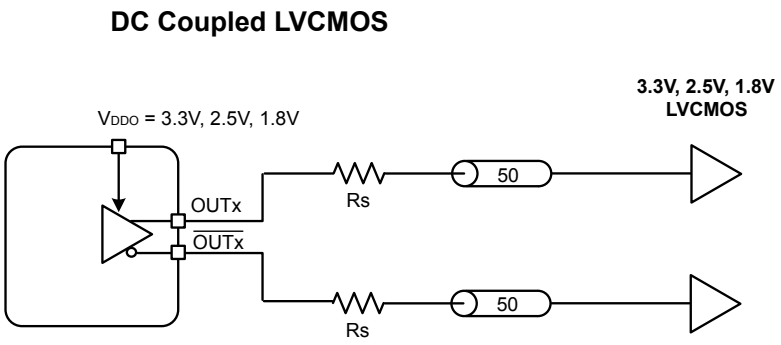


Figure 6.4. LVCMOS Output Terminations

6.3.5 LVCMOS Output Impedance and Drive Strength Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A source termination resistor is recommended to help match the selected output impedance to the trace impedance. There are three programmable output impedance selections for each VDDO option as shown below. The value for the OUTx_CMOS_DRIVE bits are given.

Table 6.6. Output Impedance and Drive Strength Selections

VDDO	OUTx_CMOS_DRV	Source Impedance (Rs)	Drive Strength (Iol/Ioh)
3.3 V	0x01	38 Ω	10 mA
	0x02	30 Ω	12 mA
	0x03[1]	22 Ω	17 mA
2.5 V	0x01	43 Ω	6 mA
	0x02	35 Ω	8 mA
	0x03[1]	24 Ω	11 mA
1.8 V	0x03[1]	31 Ω	5 mA

1. Use of the lowest impedance setting is recommended for all supply voltages.

Table 6.7. LVCMOS Drive Strength Control Registers

Register Name	Hex Address [Bit Field]			Function
	Si5395	Si5394	Si5392	
OUT0A_CMOS_DRV	0x0104[7:6]	—	—	LVCMOS output impedance.
OUT0_CMOS_DRV	0x0109[7:6]	0x0113[7:6]	0x0113[7:6]	
OUT1_ CMOS_DRV	0x010E[7:6]	0x0118[7:6]	0x0118[7:6]	
OUT2_ CMOS_DRV	0x0113[7:6]	0x0127[7:6]	—	
OUT3_ CMOS_DRV	0x0118[7:6]	0x012C[7:6]	—	
OUT4_ CMOS_DRV	0x011D[7:6]	—	—	
OUT5_ CMOS_DRV	0x0122[7:6]	—	—	
OUT6_ CMOS_DRV	0x0127[7:6]	—	—	
OUT7_ CMOS_DRV	0x012C[7:6]	—	—	
OUT8_ CMOS_DRV	0x0131[7:6]	—	—	
OUT9_ CMOS_DRV	0x0136[7:6]	—	—	
OUT9A_ CMOS_DRV	0x013B[7:6]	—	—	

6.3.6 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

6.3.7 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and OUTxb). By default the clock on the OUTx pin is generated with the same polarity (in phase) with the clock on the OUTxb pin. The polarity of these clocks is configurable enabling complimentary clock generation and/or inverted polarity with respect to other output drivers.

Table 6.8. LVCMOS Output Polarity Control Registers

Register Name	Hex Address [Bit Field]			Function
	Si5395	Si5394	Si5392	
OUT0A_INV	0x0106[7:6]	—	—	Controls the output polarity of the OUTx and OUTx pins when in LVCMOS mode. Selections are below in the Output Polarity Registers.
OUT0_INV	0x010B[7:6]	0x0115[7:6]	0x0115 [7:6]	
OUT1_ INV	0x0110[7:6]	0x011A[7:6]	0x011A [7:6]	
OUT2_ INV	0x0115[7:6]	0x0129[7:6]	—	
OUT3_ INV	0x011A[7:6]	0x012E[7:6]	—	
OUT4_ INV	0x011F[7:6]	—	—	
OUT5_ INV	0x0124[7:6]	—	—	
OUT6_ INV	0x0129[7:6]	—	—	
OUT7_ INV	0x012E[7:6]	—	—	
OUT8_ INV	0x0133[7:6]	—	—	
OUT9_ INV	0x0138[7:6]	—	—	
OUT9A_ INV	0x013D[7:6]	—	—	

Table 6.9. Output Polarity of OUTx and OUTxb Pins in LVCMOS Mode

OUTx_INV Register Settings	OUTx	OUTxb	Comment
00	CLK	CLK	Both in phase (default)
01	CLK	CLKb	OUTxb inverted
10	CLKb	CLK	OUTx and OUTxb inverted
11	CLKb	CLKb	OUTx inverted

6.3.8 Output Driver Settings for LVPECL, LVDS, HCSL, and CML

Each differential output has four settings for control:

- Normal or Low Power Format
- Amplitude (sometimes called Swing)
- Common Mode Voltage
- Stop High or Stop Low

The normal Format setting has a 100 Ω internal resistor between the plus and minus output pins. The Low Power Format setting removes this 100 Ω internal resistor and then the differential output resistance will be > 500 Ω. However as long as the termination impedance matches the differential impedance of the pcb traces the signal integrity across the termination impedance will be good. For the same output amplitude the Low Power Format will use less power than the Normal Format. The Low Power Format also has a lower rise/fall time than the Normal Format. See the Si5395/94/92 data sheet for the rise/fall time specifications. For LVPECL and LVDS standards, ClockBuilder Pro does not support the Low Power Differential Format. Stop High means that when the output driver is disabled the plus output will be high and the minus output will be low. Stop Low means that when the output driver is disabled the plus output will be low and the minus output will be high.

The Format, Amplitude and Common Mode settings for the various supported standards are shown in Table 6.10 Settings for LVDS, LVPECL, and HCSL on page 52.

Table 6.10. Settings for LVDS, LVPECL, and HCSL

OUTx_FORMAT[1]	Standard	VDDO Volts	OUTx_CM (Decimal)	OUTx_AMPL (Decimal)
001 = Normal Differential	LVPECL	3.3	11	6
001 = Normal Differential	LVPECL	2.5	11	6
002 = Low Power Differential	LVPECL	3.3	11	3
002 = Low Power Differential	LVPECL	2.5	11	3
001 = Normal Differential	LVDS	3.3	3	3
001 = Normal Differential	LVDS	2.5	11	3
001 = Normal Differential	Sub-LVDS[2]	1.8	13	3
002 = Low Power Differential	LVDS	3.3	3	1
002 = Low Power Differential	LVDS	2.5	11	1
002 = Low Power Differential	Sub-LVDS[2]	1.8	13	1
002 = Low Power Differential	HCSL[3]	3.3	11	3
002 = Low Power Differential	HCSL[3]	2.5	11	3
002 = Low Power Differential	HCSL[3]	1.8	13	3

Note:

1. The low-power format will cause the rise/fall time to increase by approximately a factor of two. See the Si5395/94/92 data sheet for more information.
2. The common-mode voltage produced is not compliant with LVDS standards; therefore ac coupling the driver to an LVDS receiver is highly recommended.
3. Creates HCSL compatible signal. See Section 5.3 Fault Monitoring.

The output differential driver can produce a wide range of output amplitudes that includes CML amplitudes. See Section 6.3.9 Setting the Differential Output Driver to Non-Standard Amplitudes for additional information.

6.3.9 Setting the Differential Output Driver to Non-Standard Amplitudes

In some applications, it may be desirable to have larger or smaller differential amplitudes than those produced by the standard LVPECL and LVDS settings, as selected by CBPro. In these cases, the following information describes how to implement these amplitudes by writing to the OUTx_CM and OUTx_AMPL setting names. Contact Silicon Labs for assistance if you want your custom configured device to be programmed for any of the settings described here.

The differential output driver has a variable output amplitude capability and two basic formats, normal and low-power format. The difference between these two formats is that the normal format has an output impedance of ~100 Ω differential, and the low-power format has an output impedance of > 500 Ω differential. Note that the rise/fall time is slower when using the Low Power Differential Format. See the Si5395/94/92 data sheet for rise/fall time specifications.

If the standard LVDS or LVPECL compatible output amplitudes will not work for a particular application, the variable amplitude capability can be used to achieve higher or lower amplitudes. For example, a “CML” format is sometimes desired for an application. However, CML is not a defined standard, and hence the amplitude of a CML signal for one receiver may be different than that of another receiver.

When the output amplitude needs to be different than standard LVDS or LVPECL, the Common Mode Voltage settings must be set as shown in Table 6.11 Output Differential Common Mode Voltage Settings on page 53. No settings other than these are supported as the signal integrity could be compromised. In addition, the output driver should be ac-coupled to the load so that the common-mode voltage of the driver is not affected by the load.

Table 6.11. Output Differential Common Mode Voltage Settings

VDDOx (Volts)	Differential Format	OUTx_FORMAT	Common Mode Voltage (Volts)	OUTx_CM
3.3	Normal	0x1	2.0	0xB
3.3	Low Power	0x2	1.6	0x7
2.5	Normal	0x1	1.3	0xC
2.5	Low Power	0x2	1.1	0xA
1.8	Normal	0x1	0.8	0xD
1.8	Low Power	0x2	0.8	0xD

The differential amplitude can be set as shown in the following table.

Table 6.12. Typical Differential Amplitudes[1]

OUTx_AMPL	Normal Differential Format (Vpp SE mV – Typical)	Low-Power Differential Format (Vpp SE mV – Typical)
0	130	200
1	230	400
2	350	620
3	450	820
4	575	1010
5	700	1200
6	810	1350[2]
7	920	1600[2]

Note:
1. These amplitudes are based upon a 100 Ω differential termination.
2. In low-power mode and VDDOx = 1.8 V, OUTx_AMPL may not be set to 6 or 7.

Note: High-Speed Differential Mode in ClockBuilder Pro output setting page sets OUTx_AMP to 7 in order to compensate for channel loss at high frequency.

See the register map portion of this document for additional information about OUTx_FORMAT, OUTx_CM and OUTx_AMPL. Contact Silicon Labs for assistance if you require a factory-programmed device to be configured for any of the output driver settings listed above.

6.4 Output Enable/Disable

The OEb pin provides a convenient method of disabling or enabling the output drivers. When the OEb pin is held high all outputs will be disabled. When the pin is not driven, the device defaults to all outputs on. Outputs in the enabled state can be individually disabled through register control. If the pin is high register control is disabled and all outputs will be disabled.

Table 6.13. Output Enable/Disable Control Registers

Register Name	Hex Address [Bit Field]			Function
	Si5395	Si5394	Si5392	
OUTALL_ DISABLE_LOW	0x0102[0]	0x0102[0]	0x0102[0]	Disables all output drivers: 0 - all outputs disabled, 1 – all outputs enabled. This bit essentially has the same function as the OE pin if the OE pin is held low. If the OE pin is held high, then all outputs will be disabled regardless of the state of this register bit.
OUT0A_OE	0x0103[1]	—	—	Allows enabling/disabling individual output drivers. Note that the OE pin must be held low in order to enable an output.
OUT0_OE	0x0108[1]	0x0112[1]	0x0112[1]	
OUT1_ OE	0x010D[1]	0x0117[1]	0x0117[1]	
OUT2_ OE	0x0112[1]	0x0126[1]	—	
OUT3_ OE	0x0117[1]	0x012B[1]	—	
OUT4_ OE	0x011C[1]	—	—	
OUT5_ OE	0x0121[1]	—	—	
OUT6_ OE	0x0126[1]	—	—	
OUT7_ OE	0x012B[1]	—	—	
OUT8_ OE	0x0130[1]	—	—	
OUT9_ OE	0x0135[1]	—	—	
OUT9A_ OE	0x013A[1]	—	—	

6.4.1 Output Driver State When Disabled

The disabled state of an output driver is configurable as disable low or disable high. When the output driver is disabled, the outputs will drive either logic high or logic low, selectable by the user. The output common mode voltage is maintained while the driver is disabled, reducing enable/disable transients. By contrast, powering down the driver rather than disabling it increases output impedance and shuts off the output common mode voltage. For all output drivers connected in the system, it is recommended to use Disable rather than Powerdown to reduce enable/disable common mode transients. Unused outputs may be left unconnected, powered down to reduce current draw, and, with the corresponding VDDOx, left unconnected.

Table 6.14. Output Driver State Control Registers

Register Name	Hex Address [Bit Field]			Function
	Si5395	Si5394	Si5392	
OUT0A_DIS_STATE	0x0104[5:4]	—	—	Determines the state of an output driver when disabled. Selectable as: Disable logic low Disable logic high
OUT0_DIS_STATE	0x0109[5:4]	0x0113[5:4]	0x0113[5:4]	
OUT1_ DIS_STATE	0x010E[5:4]	0x0118[5:4]	0x0118[5:4]	
OUT2_ DIS_STATE	0x0113[5:4]	0x0127[5:4]	—	
OUT3_ DIS_STATE	0x0118[5:4]	0x012C[5:4]	—	
OUT4_ DIS_STATE	0x011D[5:4]	—	—	
OUT5_ DIS_STATE	0x0122[5:4]	—	—	
OUT6_ DIS_STATE	0x0127[5:4]	—	—	
OUT7_ DIS_STATE	0x012C[5:4]	—	—	
OUT8_ DIS_STATE	0x0131[5:4]	—	—	
OUT9_ DIS_STATE	0x0136[5:4]	—	—	
OUT9A_ DIS_STATE	0x013B[5:4]	—	—	

6.4.2 Synchronous Output Enable/Disable Feature

The output drivers provide a selectable synchronous enable/disable feature when OUTx_SYNC_EN = 1. Output drivers with this feature turned on will wait until a clock period has completed before the driver is disabled or enabled. This prevents unwanted runt pulses from occurring when disabling an output. When this feature is turned off OUTx_SYNC_EN = 0, the output clock will disable immediately without waiting for the period to complete and will enable immediately without waiting a period to complete. The default state is for the synchronous output disable/enable to be turned on OUTx_SYNC_EN = 1 .

Table 6.15. Synchronous Disable Control Registers

Register Name	Hex Address [Bit Field]			Function
	Si5395	Si5394	Si5392	
OUT0A_SYNC_EN	0x0104[3]	—	—	Synchronous output disable/enable. When this feature is set high, the output clock will always finish a complete period before disabling/enabling. When this feature is cleared (low), the output clock will disable immediately without waiting for the period to complete. This feature is set (high) by default.
OUT0_SYNC_EN	0x0109[3]	0x0113[3]	0x0113[3]	
OUT1_ SYNC_EN	0x010E[3]	0x0118[3]	0x0118[3]	
OUT2_ SYNC_EN	0x0113[3]	0x0127[3]	—	
OUT3_ SYNC_EN	0x0118[3]	0x012C[3]	—	
OUT4_ SYNC_EN	0x011D[3]	—	—	
OUT5_ SYNC_EN	0x0122[3]	—	—	
OUT6_ SYNC_EN	0x0127[3]	—	—	
OUT7_ SYNC_EN	0x012C[3]	—	—	
OUT8_ SYNC_EN	0x0131[3]	—	—	
OUT9_ SYNC_EN	0x0136[3]	—	—	
OUT9A_ SYNC_EN	0x013B[3]	—	—	

6.5 Input-Output Skew Control

The input to output skew can be adjusted dynamically. This involves changing the output phase of the N divider; so the phase for all outputs that are driven by a given Nx will change together.The dynamic phase adjust can be initiated at any time under register control. This adjustment can change the output phase by up to 360 degrees (i.e. one UI). The resolution values listed in the table below assume a VCO frequency of 14 GHz for a Tvco of 71.43 psec. The skew value may change after each reset or power cycle.

Table 6.16. Input-Output Skew Control Registers

Type	Setting Names	Setting Address Start	Typical Resolution
Dynamic	Nx_PHASE_STEP, Nx_PHASE_COUNT	0x0A38	T_{VCO} = 71.43 ps

For more details on how these registers are enabled and programmed, see the appropriate register map section toward the end of this reference manual.

6.6 Output Buffer Supply Voltage Selection

These power supply settings must match the actual VDDOx voltage so that the output driver operates properly.

Table 6.17. OUTx VDD Settings

Setting Name	Description
OUTx_VDD_SEL_EN	These bits are set to 1 and should not be changed
OUTx_VDD_SEL	These bits are set by CBPro to match the expected VDDOx voltage. 0: 3.3 V; 1: 1.8 V; 2: 2.5 V; 3: Reserved

7. Zero Delay Mode

A zero delay mode is available for applications that require fixed and consistent minimum delay between the selected input and outputs. The zero delay mode is configured by opening the internal feedback loop through software configuration and closing the loop externally as shown in Figure 7.1 Si5395 Zero Delay Mode Setup on page 58. This helps to cancel out the internal delay introduced by the dividers, the crosspoint, the input, and the output drivers. Any one of the outputs can be fed back to the FB_IN pins, although using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay. The OUT9A and FB_IN pins are recommended for the external feedback connection in the Si5395. OUT3 and FB_IN pins are recommended for the external feedback in the Si5394. OUT1 or OUT2 are recommended with FB_IN in the Si5392 . The FB_IN input pins must be terminated and ac-coupled when zero delay mode is used. A differential external feedback path connection is necessary for best performance. For this reason, customers should avoid using CMOS outputs for driving the external feedback path. Zero Delay Mode performance will degrade with low values of phase detector frequency (Fpfd). For this reason, ClockBuilder Pro will not enable Zero Delay Mode with an Fpfd of less than 128 kHz.

When the DSPLL is set for Zero-Delay Mode (ZDM), a hard reset request from either the RSTb pin or RST_REG register bit will have a delay of ~750 ms before executing. Any subsequent register writes to the device should be made after this time expires or they will be overwritten with the NVM values. Please contact Silicon Labs technical support for information on reducing this ZDM hard reset time.

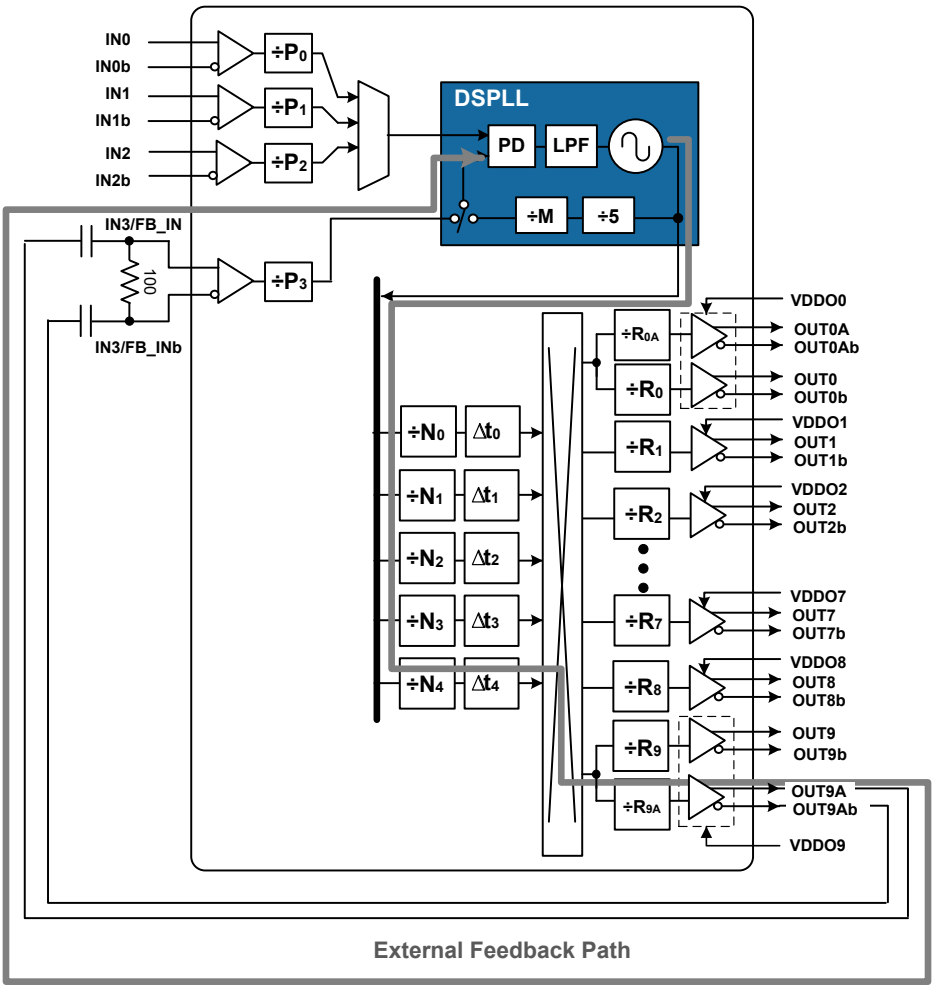


Figure 7.1. Si5395 Zero Delay Mode Setup

The following table lists the registers used for the Zero Delay mode.

Table 7.1. Zero Delay Mode Registers

Register Name	Hex Address [Bit Field]	Function
ZDM_EN	0x0487[0]	0: Disable zero delay mode. 1: Enable zero delay mode.
ZDM_AUTOSW_EN	0x0487[4]	0: Automatic switching disabled for zero-delay mode 1: Automatic input switching enabled and input clock selection governed by automatic input switching engine

Table 7.2. Input Clock Selection in Zero Delay Mode

ZDM_AUTO_SW_EN	ZDM_EN	IN_SEL_REGCTRL	Input Clock Selection Governed by
0	0	0	IN_SEL[1:0] Pins
0	0	1	IN_SEL Register
0	1	0	IN_SEL[1:0] Pins
1	X	X	Input clock selection governed by automatic input switching engine (see 5.1.2 Automatic Input Switching)

8. Digitally-Controlled Oscillator (DCO) Mode

An output that is controlled as a DCO is useful for simple tasks, such as frequency margining, CPU speed control, or just changing the output frequency. The output can also be used for more sophisticated tasks, such as FIFO management, by adjusting the frequency of the read or write clock to the FIFO or using the output as a variable Local Oscillator in a radio application.

The N dividers can be digitally controlled so that all outputs connected to the N divider change frequency in real time without any transition glitches. There are two ways to control the N divider to accomplish this task:

Use the Frequency Increment/Decrement Pins or register bits.

Write directly to the numerator or denominator of the N divider.

The output N divider can be changed from its minimum value to its maximum value in very small fractional increments or in a single large increment. Each N divider has a value of Nx_NUM/Nx_DEN. Nx_NUM is a 44-bit word, and Nx_DEN is a 32-bit word. Clockbuilder Pro left-shifts these values as far as possible before writing them to the actual Nx_NUM and Nx_DEN registers. For example, an integer Nx divider of 30/1, when left shifted, becomes Nx_NUM=64424509440 (decimal) and Nx_DEN=2147483648 (decimal). By adjusting the size of the Nx_NUM and Nx_DEN but keeping the ratio the same, the resolution of the LSB of numerator or denominator can be controlled.

When changing the N divider(s) to fractional values, the setting name, N_PIBYP[4:0], must be a 0 for the N divider that is being changed. This applies when using FINC/FDEC or when directly writing to the N divider. After changing N_PIBYP a soft reset must occur to update the part.

8.1 DCO with Frequency Increment/Decrement Pins/Bits

The Nx_FSTEPW (Frequency STEP Word) is a 44-bit word that is used to change the value of the Nx_NUM word. Whenever an FINC or FDEC is asserted, the Nx_FSTEPW will automatically add or subtract from the Nx_NUM word so that the output frequency will, respectively, increment (FINC) or decrement (FDEC).

Each of the N dividers can be independently stepped up or down in numerical, predefined steps with a maximum resolution that varies from ~ 0.05 ppb to a ~0.004 ppb depending upon the frequency plan. One or more N dividers can be controlled by FINC/FDEC at the same time by use of the N_FSTEP_MSK bits. Any N divider that is masked by its corresponding bit in the N_FSTEP_MSK field will not change when FINC or FDEC is asserted. The magnitude of the frequency change caused by FINC or FDEC is determined by the value of the Nx_FSTEPW word and the magnitude of the word in Nx_NUM. For a specific frequency step size, it may be necessary to adjust the Nx_NUM value while keeping the ratio of Nx_NUM/Nx_DEN the same. When the FINC or FDEC pin or register bit is asserted, the selected N dividers will have their numerator changed by the addition or subtraction of the Nx_FSTEPW so that an FINC will increase the output frequency, and an FDEC will decrease the output frequency. A FINC or FDEC can be followed by another FINC or FDEC with a minimum time interval of 1 µs.

Because the output frequency = FVCO*Nx_DEN/(Rx*Nx_NUM), subsequent changes to Nx_NUM by the Nx_FSTEPW will not produce exactly the same output frequency change. The amount of error in the frequency step is extremely small and, in a vast number of applications, will not cause a problem. When consecutive frequency steps must be exactly the same, it is possible to set FINC and FDEC to change the Nx_DEN instead of Nx_NUM, and then, consecutive FINCs or FDECs will be exactly the same frequency change. However, there are some special setups that are necessary to achieve this. For more information, contact Silicon Labs athttps://www.silabs.com/support/pages/contacttechnicalsupport.aspx .

Table 8.1. Frequency Increment/Decrement Control Registers

Register Name	Hex Address [Bit Field]			Function
	Si5395	Si5394	Si5392	
FINC	0x001D[0]	0x001D[0]	0x001D[0]	Asserting this bit will increase the DSPLL output frequency by the frequency step word.
FDEC	0x001D[1]	0x001D[1]	0x001D[1]	Asserting this bit will decrease the DSPLL output frequency by the frequency step word.
N0_FSTEPW	0x033B[7:0]–0x0340[7:0]	0x033B[7:0]–0x0340[7:0]	0x033B[7:0]-0x0340[7:0]	This is a 44-bit frequency step word for each of the MultiSynths. The Nx_FSTEPW will be added or subtracted to the output frequency during assertion of the FINC/FDEC bits or pins. The Nx_FSTEPW is calculated based on the frequency configuration and is easily determined using the ClockBuilder Pro
N1_FSTEPW	0x0341[7:0]–0x0346[7:0]	0x0341[7:0]–0x0346[7:0]	0x0341[7:0]-0x0346[7:0]	
N2_FSTEPW	0x0347[7:0]–0x034C[7:0]	0x0347[7:0]–0x034C[7:0]	—	
N3_FSTEPW	0x034D[7:0]–0x0352[7:0]	0x034D[7:0]–0x0352[7:0]	—	
N4_FSTEPW	0x0353[7:0]–0x0358[7:0]	—	—	
N_FSTEP_MSK	0x0339[4:0]	0x0339[3:0]	0x0339[1:0]	This mask bit determines if a FINC or FDEC affects N0, N1, N2, N3, N4. 0 = FINC/FDEC will Increment/decrement the Nx_FSTEPW to the selected MultiSynth(s), 1 = Ignores FINC/FDEC.

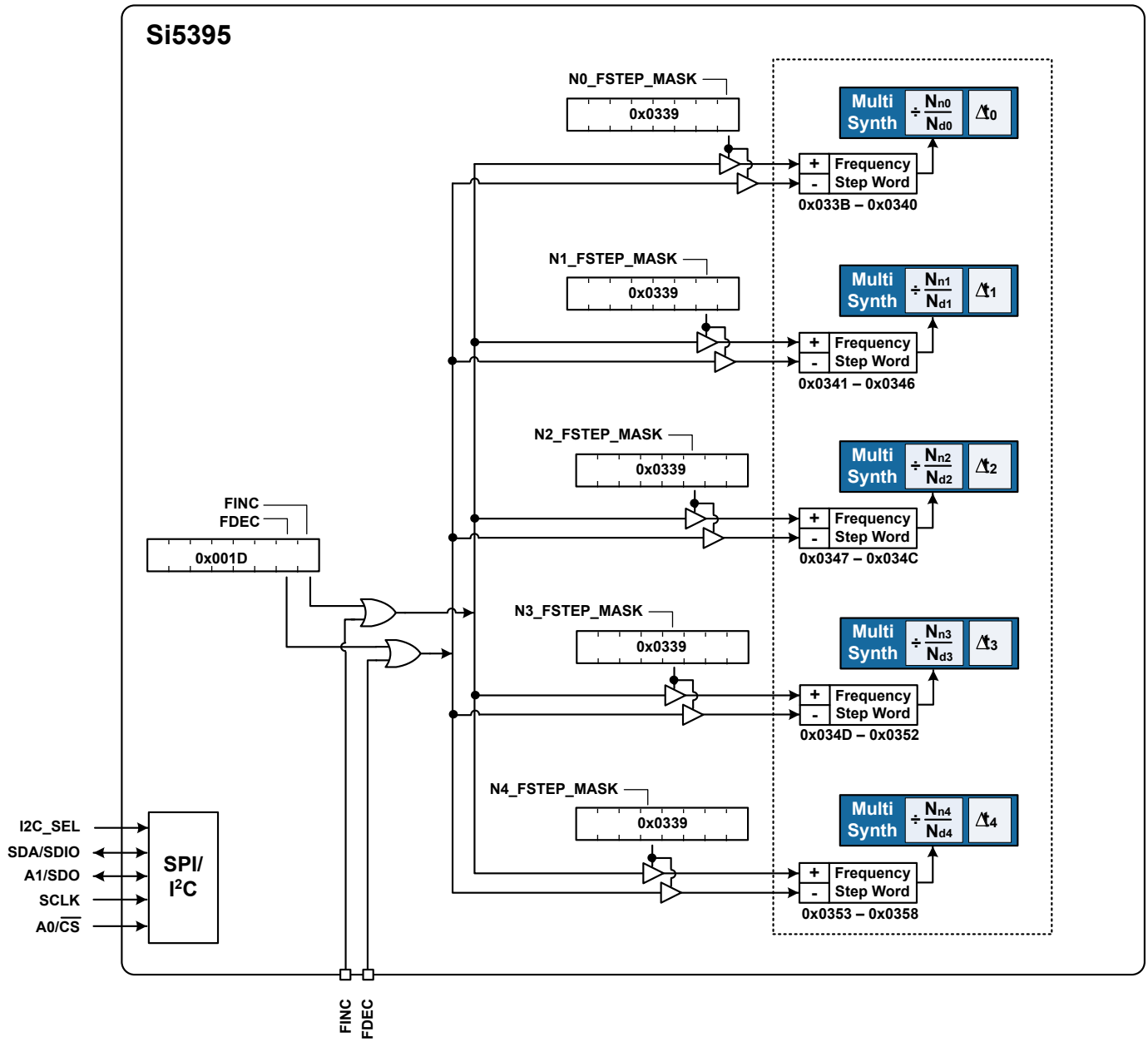


Figure 8.1. DCO with FINC/FDEC Pins or Bits

8.2 DCO with Direct Register Writes

When an N divider numerator (Nx_NUM) and its corresponding update bit (Nx_UPDATE) are written, the new numerator value will take effect, and the output frequency will change without any glitches. The N divider numerator and denominator terms (Nx_NUM and Nx_DEN) can be left- and right-shifted so that the least significant bit of the numerator word represents the exact step resolution that is needed for your application. Each N divider has an update bit (Nx_UPDATE) that must be written to cause the written values to take effect. All N dividers can be updated at the same time by writing the N_UPDATE_ALL bit. Writing this bit will NOT cause any output glitching on an N divider that did not have its numerator or denominator changed.

When changing the N divider denominator (Nx_DEN), it is remotely possible that a small phase shift may occur at the exact time of the frequency change. However, with the proper setup, it is possible to change Nx_DEN and never have a phase shift. If your application requires changing an N divider denominator, contact Silicon Labs at https://www.silabs.com/support/pages/contacttechnicalsupport.aspx for support.

9. Frequency-On-The-Fly for Si5395/94/92

In some applications it is desirable to modify the output frequency of a certain output, while maintaining other outputs unaffected. This Frequency-On-The-Fly functionality is fully supported by the Si5395/94/92 hardware with the help of CBPro Command Line Interface (CLI) tool.
Frequency-On-The-Fly allows the user to:

- Reconfigure the output frequency(s) on a given MultiSynth.
- Outputs on other MultiSynths will not be disturbed during the reconfiguration process. There will be no impact on phase noise.

Detailed explanation on how to set up Frequency-On-The-Fly with CLI tool is included in these two documents: “CBPro Tools & Support for In-System Programming” & “CLI User’s Guide”

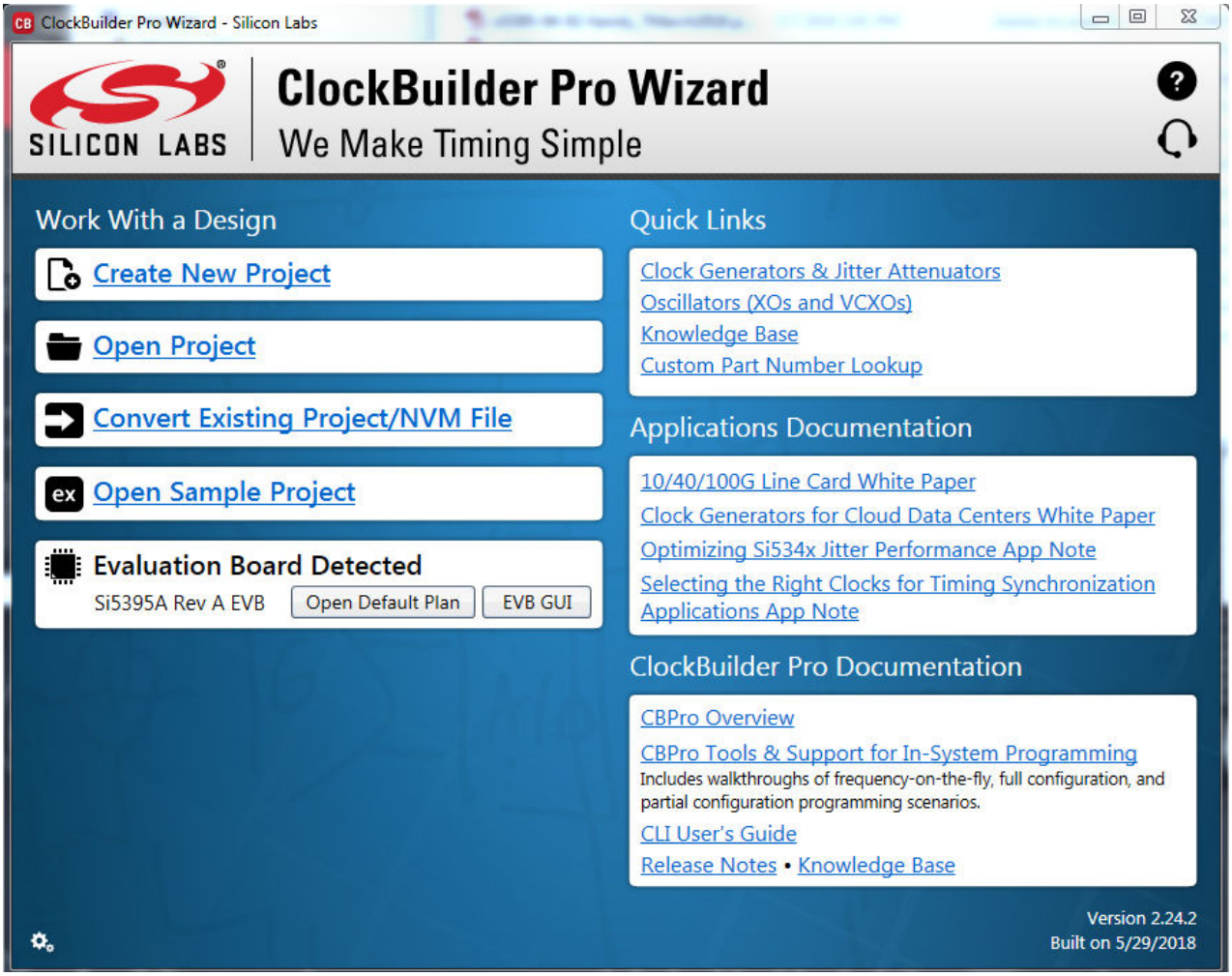


Figure 9.1. CBPro Tools & Support for In-System Programming

“CBPro Tools & Support for In-System Programming” has a section called “Si539x/8x/4x Frequency-On-The-Fly” that walks the user through each of the steps.

1. Create CBPro project as base frequency plan.

2. Create text files detailing the output frequency of new plans; plans are defined independently for each MultiSynth.

3. Use CLI FOTF tool (create a batch script) to auto generate register files for switching among different plans.

The CLI FOTF tool optimizes the VCO frequency for all of the plans “CLI User’s Guide” includes more in-depth and detailed syntax explanation and function definition. Example files are bundled in CBPro at C:\Program Files (x86)\Silicon Laboratories\ClockBuilder Pro \CLI\Samples\Single-PLL-FOTF.
Refer to AN1178: Frequency-On-the-Fly for Silicon Labs Jitter Attenuators and Clock Generators.

10. Serial Interface

Configuration and operation of the Si5395/94/92 is controlled by reading and writing registers using the I²C or SPI serial interface. The I2C_SEL pin selects between I²C or SPI operation. The Si5395/94/92 supports communication with either a 3.3 V or 1.8 V host by setting the IO_VDD_SEL (0x0943[0]) configuration bit. The SPI mode supports 4-wire or 3-wire by setting the SPI_3WIRE configuration bit. See the figure below for supported modes of operation and settings. The I²C pins are open drain and are ESD clamped to 3.3 V, regardless of the host supply level. The I²C pins are clamped to 3.3 V so that they may be externally pulled up to 3.3 V regardless of IO_VDD_SEL (in register 0x0943).

The table below lists register settings of interest for the I²C/SPI.

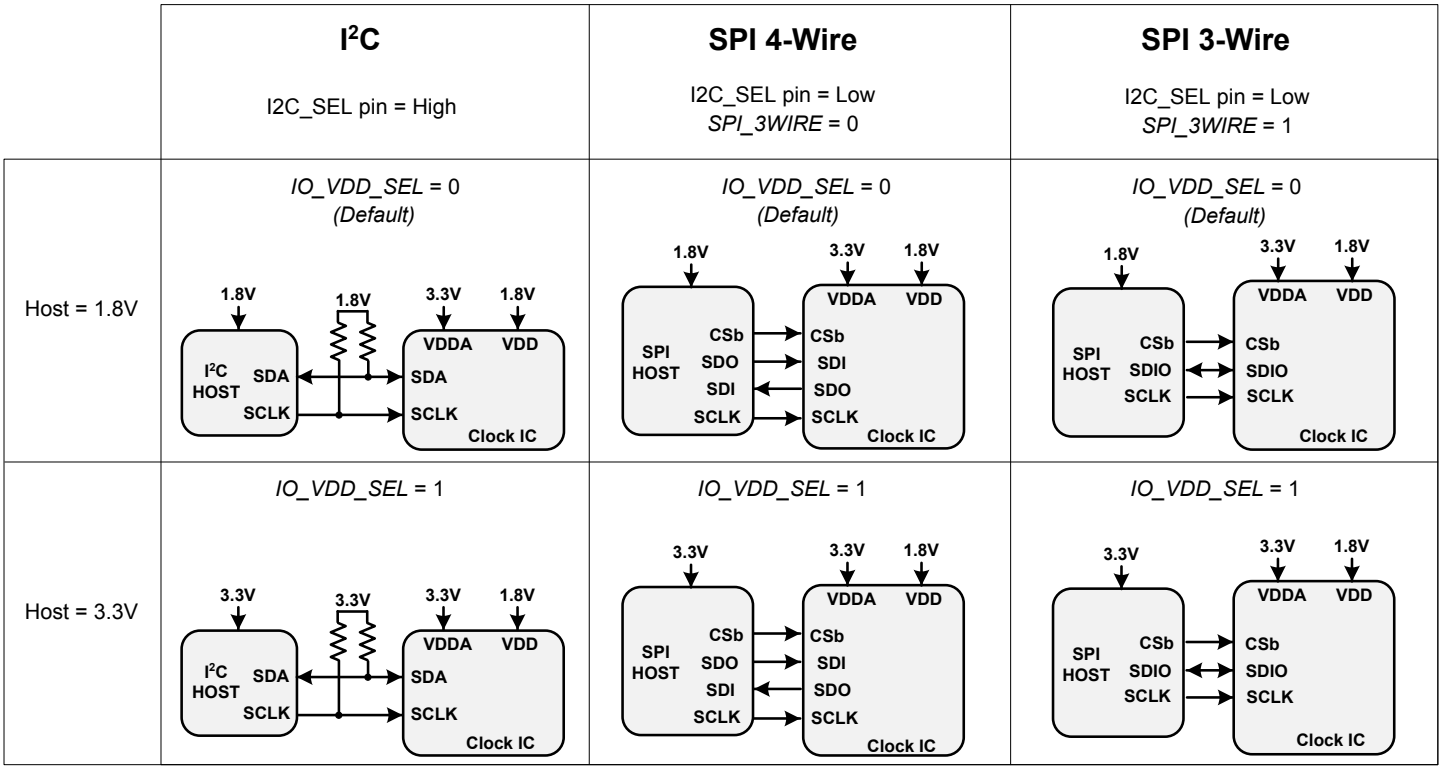


Figure 10.1. I²C/SPI Device Connectivity Configurations

If neither serial interface is used, leave I2C_SEL unconnected. Pull pins SDA/SDIO, SCLK, A1/SDO, and A0/CS all low.

Note that the Si5395/94/92 is not I²C fail-safe upon loss of power. Applications that require fail-safe operation should isolate the device from a shared I²C bus.

Table 10.1. I^2C/SPI Register Settings

Setting Name	Hex Address [Bit Field]	Function
	Si5395/94/92	
IO_VDD_SEL	0x0943[0]	The IO_VDD_SEL configuration bit optimizes the V_{IL}, V_{IH}, V_{OL}, and V_{OH} thresholds to match the VDDS voltage. By default the IO_VDD_SEL bit is set to the VDD option. The serial interface pins are always 3.3 V tolerant even when the device's VDD pin is supplied from a 1.8 V source. When the I^2C or SPI host is operating at 3.3 V and the Si5395/94/92 at VDD = 1.8 V, the host must write the IO_VDD_SEL configuration bit to the VDDA option. This will ensure that both the host and the serial interface are operating at the optimum voltage thresholds.
SPI_3WIRE	0x002B[3]	The SPI_3WIRE configuration bit selects the option of 4-wire or 3-wire SPI communication. By default, this configuration bit is set to the 4-wire option. In this mode the Si5395/94/92 will accept write commands from a 4-wire or 3- wire SPI host allowing configuration of device registers. For full bidirectional communication in 3-wire mode, the host must write the SPI_3WIRE configuration bit to “1”.

10.1 I²C Interface

When in I²C mode, the serial interface operates in slave mode with 7-bit addressing and can operate in Standard-Mode (100 kbps) or Fast-Mode (400 kbps) and supports burst data transfer with auto address increments. The I²C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL) as shown in the figure below. Both the SDA and SCL pins must be connected to a supply via an external pull-up (4.7 kΩ) as recommended by the I²C specification as shown in the figure below. Two address select bits (A0, A1) are provided allowing up to four Si5395/94/92 devices to communicate on the same bus. This also allows four choices in the I²C address for systems that may have other overlapping addresses for other I²C devices.

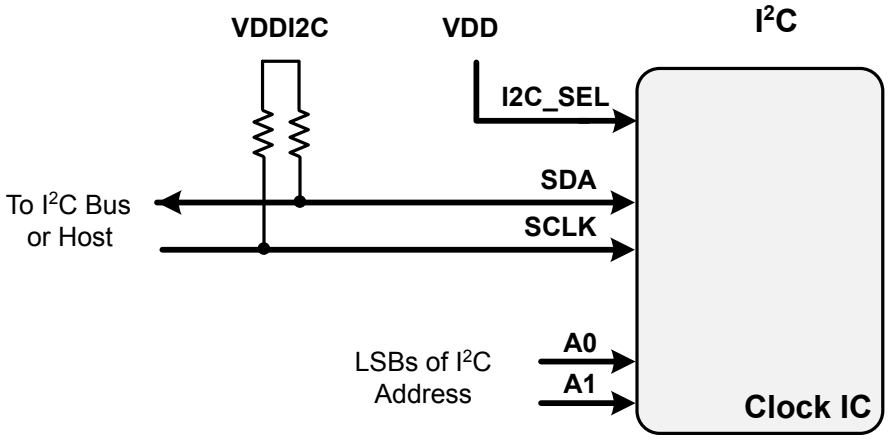


Figure 10.2. I²C Configuration

The 7-bit slave device address of the Si5395/94/92 consists of a 5-bit fixed address plus 2 pins which are selectable for the last two bits, as shown in the following figure.

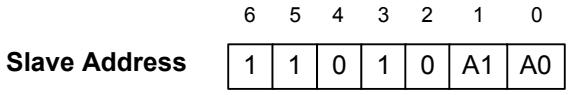


Figure 10.3. 7-bit I²C Slave Address Bit-Configuration

Data is transferred MSB first in 8-bit words as specified by the I²C specification. A write command consists of a 7-bit device (slave) address + a write bit, an 8-bit register address, and 8 bits of data as shown in Figure 10.6 SPI Interface Connections on page 68. A write burst operation is also shown where subsequent data words are written using to an auto-incremented address.

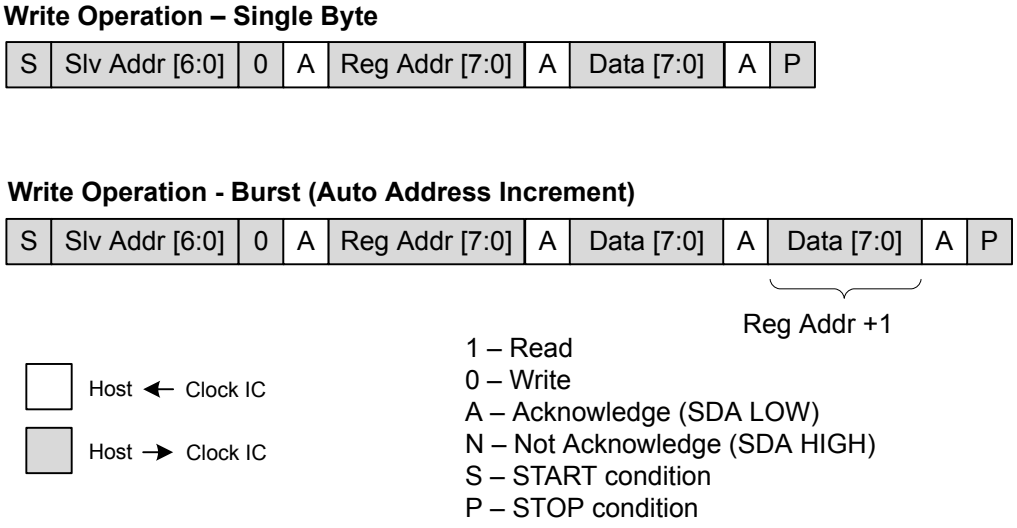


Figure 10.4. I²C Write Operation

A read operation is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. A read burst operation is also supported. This is shown in the following figure.

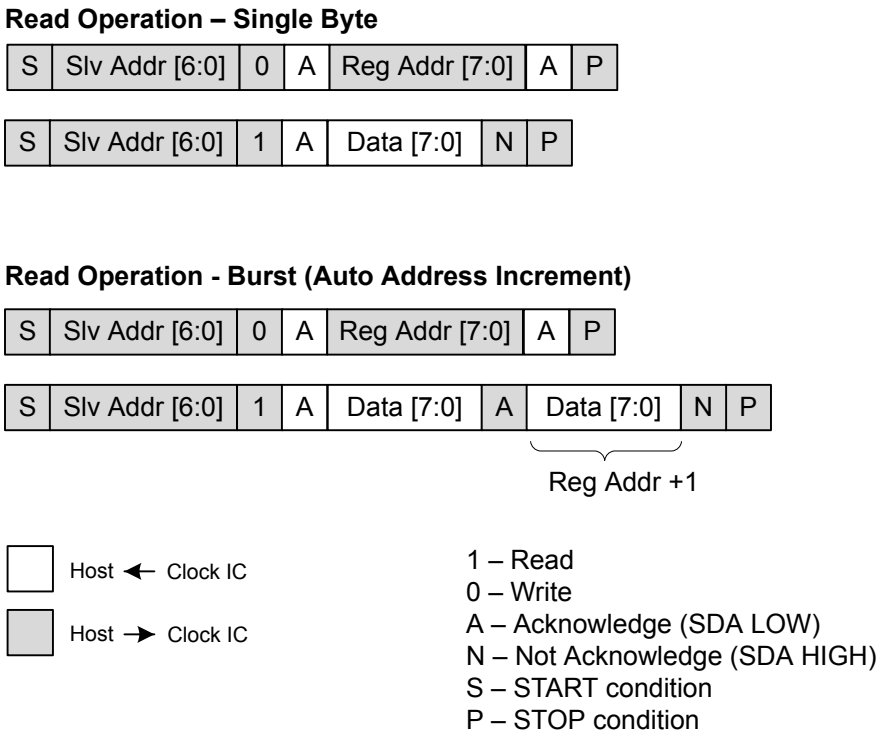


Figure 10.5. I²C Read Operation

The SMBUS interface requires a timeout. The error flags are found in the registers listed below.

Table 10.2. SMBus Timeout Error Bit Indicators

Register Name	Hex Address [Bit Field]	Function
SMBUS_TIMEOUT	0x000C[5]	1 if there is a SMBus timeout error.
SMBUS_TIME-OUT_FLG	0x0011[5]	1 if there is a SMBus timeout error.

10.2 SPI Interface

When in SPI mode, the serial interface operates in 4-wire or 3-wire depending on the state of the SPI_3WIRE configuration bit. The 4-wire interface consists of a clock input (SCLK), a chip select input (CS), serial data input (SDI), and serial data output (SDO). The 3-wire interface combines the SDI and SDO signals into a single bidirectional data pin (SDIO). Both 4-wire and 3-wire interface connections are shown in the following figure.

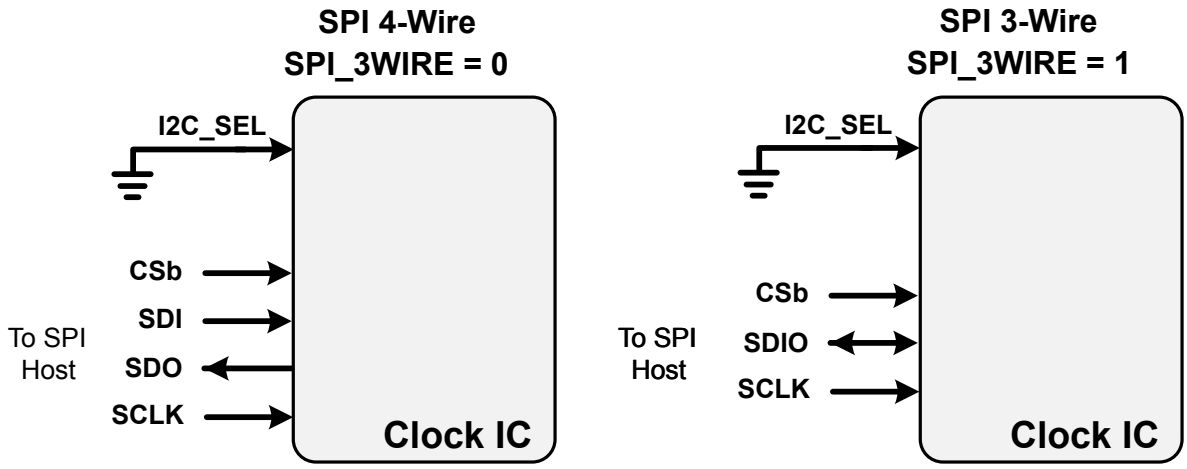


Figure 10.6. SPI Interface Connections

Table 10.3. SPI Command Format

Instruction	1st Byte[1]	2nd Byte	3rd Byte	Nth Byte[2,3]
Set Address	000x xxxx	8-bit Address	—	—
Write Data	010x xxxx	8-bit Data	—	—
Read Data	100x xxxx	8-bit Data	—	—
Write Data + Address Increment	011x xxxx	8-bit Data	—	—
Read Data + Address Increment	101x xxxx	8-bit Data	—	—
Burst Write Data	1110 0000	8-bit Address	8-bit Data	8-bit Data

Note:

1. X = don't care (1 or 0).
2. The Burst Write Command is terminated by de-asserting CSb (CSb = high).
3. There is no limit to the number of data bytes that follow the Burst Write Command, but the address will wrap around to zero in the byte after address 255 is written.

Writing or reading data consist of sending a "Set Address" command followed by a "Write Data" or "Read Data" command. The 'Write Data + Address Increment' or "Read Data + Address Increment" commands are available for cases where multiple byte operations in sequential address locations is necessary. The "Burst Write Data" instruction provides a compact command format for writing data since it uses a single instruction to define starting address and subsequent data bytes. Figure 10.7 Example Writing Three Data Bytes using the SPI Write Commands on page 69 shows an example of writing three bytes of data using the write commands. As can be seen, the "Write Burst Data" command is the most efficient method for writing data to sequential address locations. Figure 10.8 Example of Reading Three Data Bytes Using the SPI Read Commands on page 69 provides a similar comparison for reading data with the read commands. Note that there is no equivalent burst read; the read increment function is used in this case.

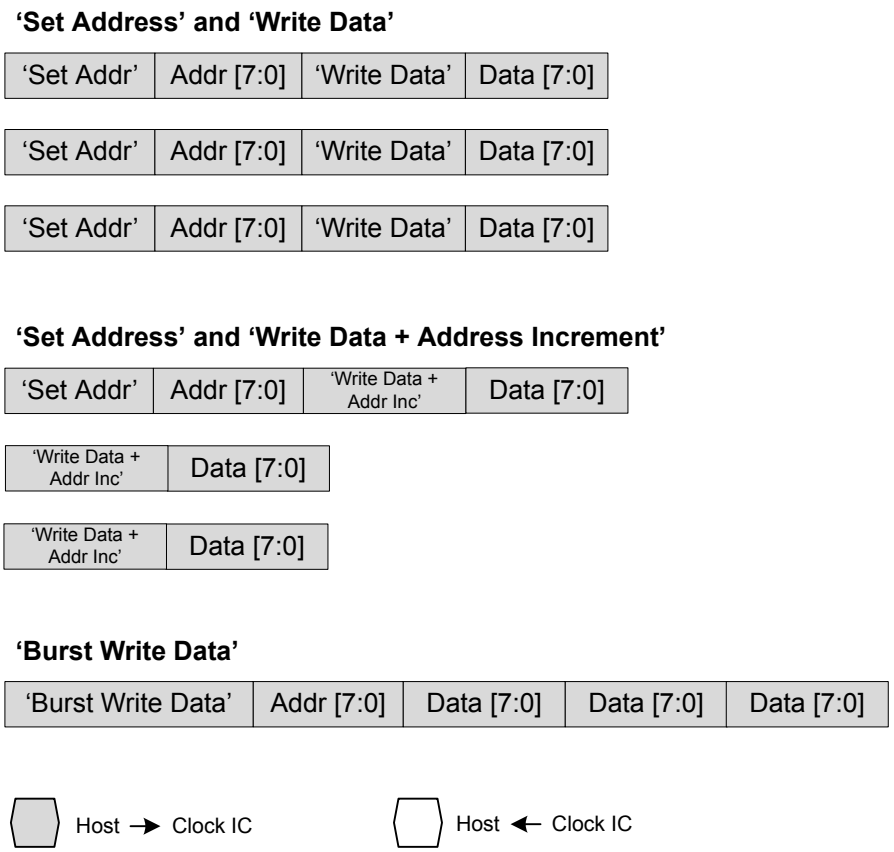


Figure 10.7. Example Writing Three Data Bytes using the SPI Write Commands

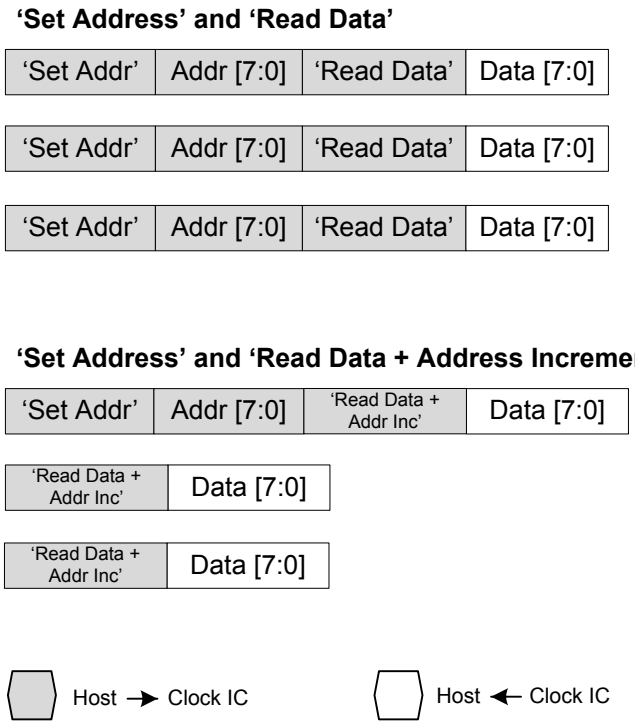


Figure 10.8. Example of Reading Three Data Bytes Using the SPI Read Commands

The timing diagrams for the SPI commands are shown in Figures Figure 10.9 SPI “Set Address” Command Timing on page 70, Figure 10.10 SPI “Write Data” and “Write Data+ Address Increment” Instruction Timing on page 71, Figure 10.11 SPI “Read Data” and “Read Data + Address Increment” Instruction Timing on page 72, and Figure 10.12 SPI “Burst Data Write” Instruction Timing on page 72.

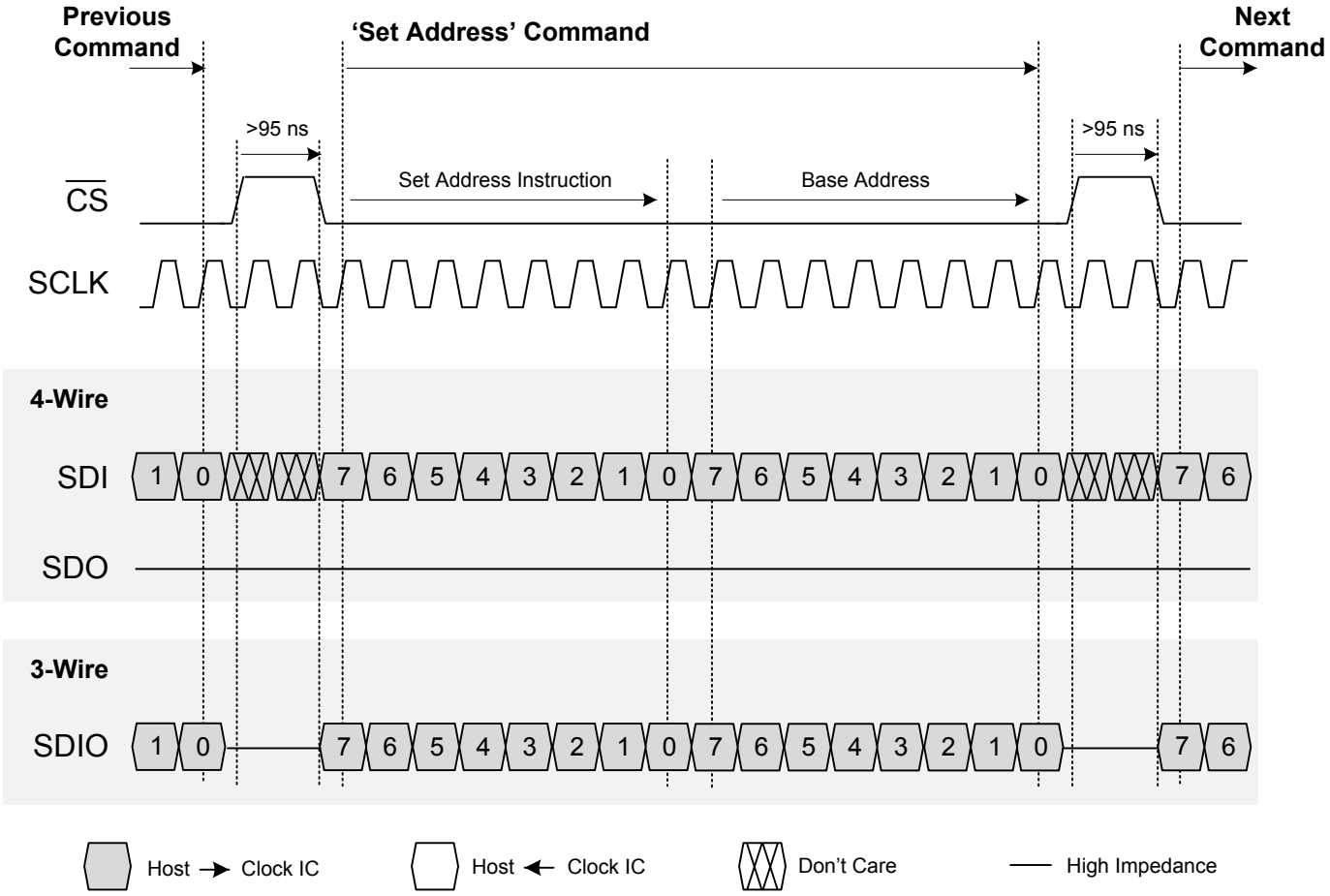


Figure 10.9. SPI “Set Address” Command Timing

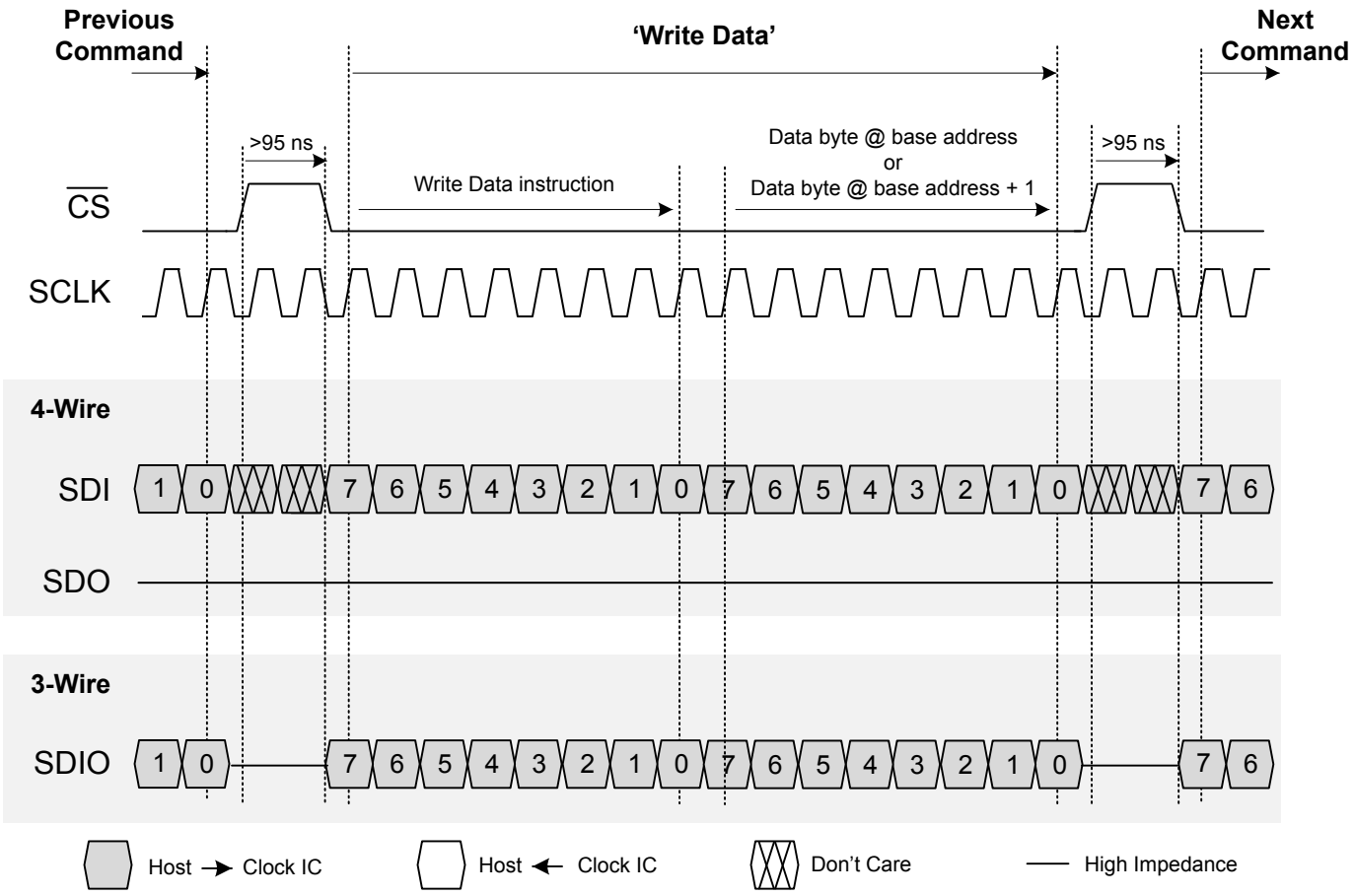


Figure 10.10. SPI "Write Data" and "Write Data+ Address Increment" Instruction Timing

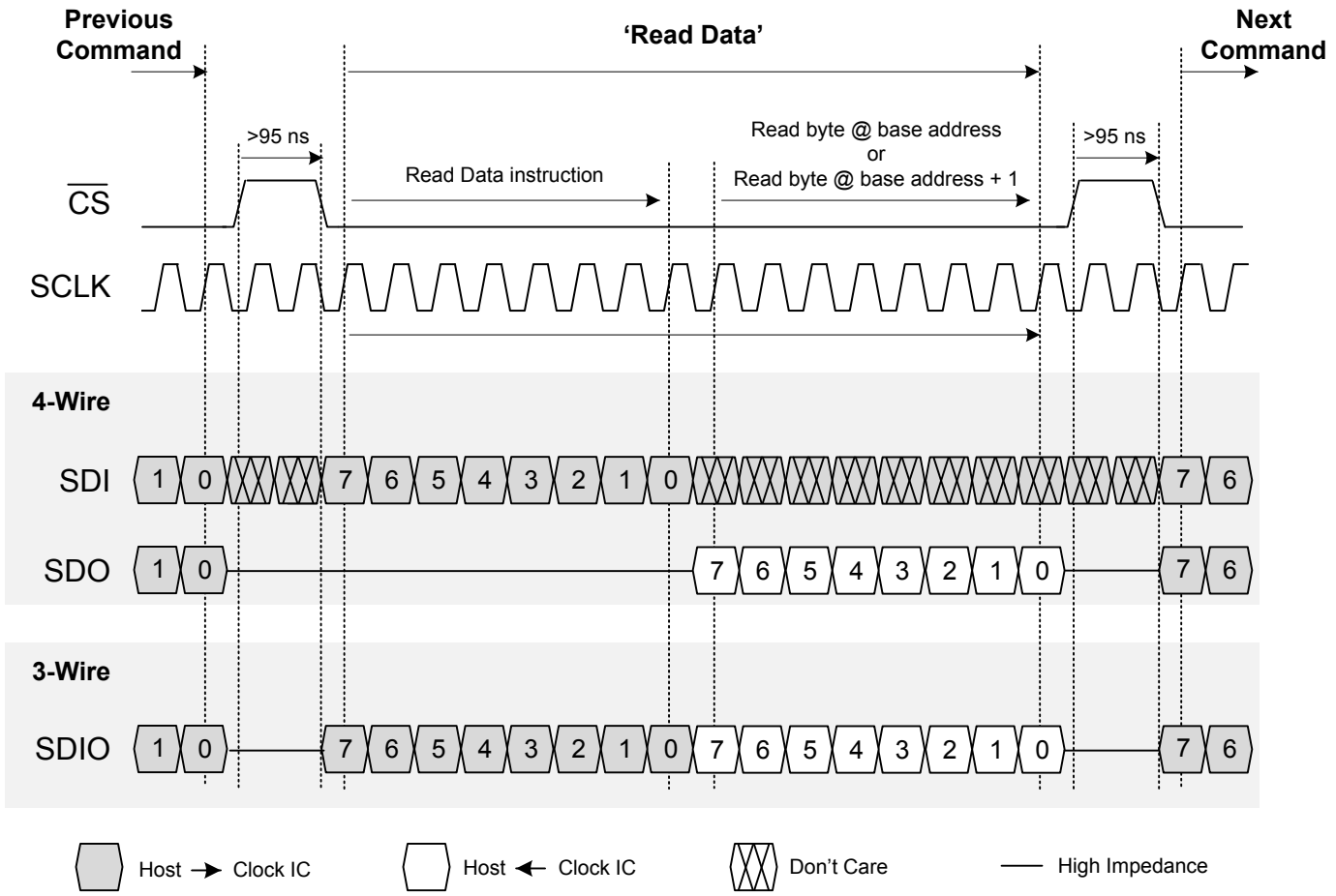


Figure 10.11. SPI "Read Data" and "Read Data + Address Increment" Instruction Timing

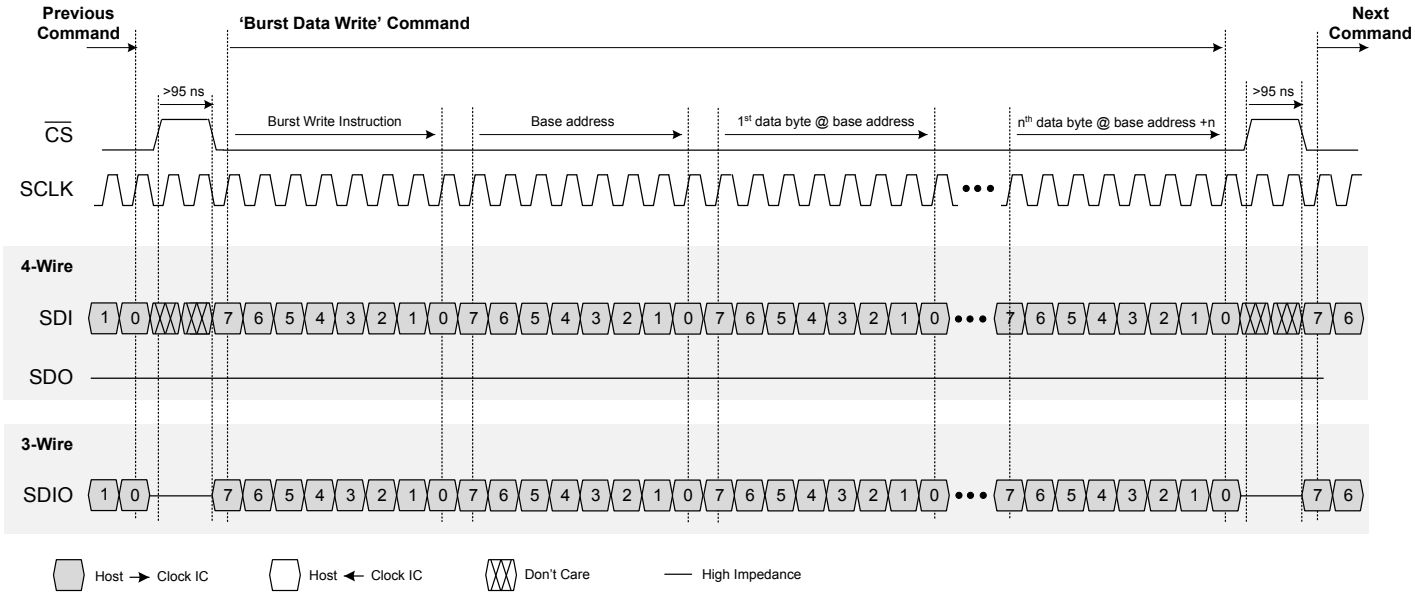


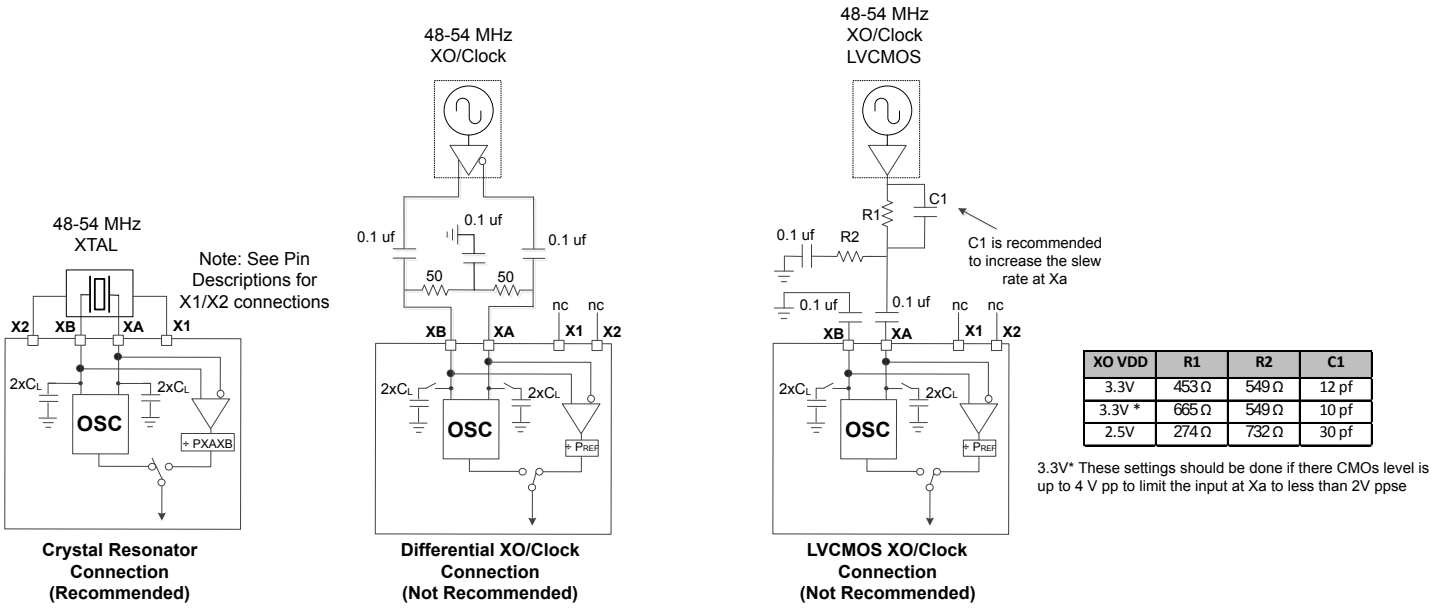
Figure 10.12. SPI "Burst Data Write" Instruction Timing

Note that for all SPI communication the chip select (CS) must be high for the minimum time period between commands. When chip select goes high it indicates the termination of the command. The SCLK can be turned off between commands, particularly if there are very long delays between commands.

11. XAXB References

11.1 External References

An external standard low-pullability crystal (XTAL) is recommended in combination with the internal oscillator (OSC) to produce an ultra low phase noise reference clock for the DSPLL, as well as providing a stable reference for the Freerun and Holdover modes. Simplified connection diagrams are shown below. The device includes internal 8 pF crystal loading capacitors which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. In most applications, using the internal OSC with an external crystal provides the best phase noise performance. See AN905: External References; Optimizing Performance for more information on the performance of various XO's with these devices. The recommended crystal suppliers are listed in the Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual.



XO VDD	R1	R2	C1
3.3V	453 Ω	549 Ω	12 pf
3.3V *	665 Ω	549 Ω	10 pf
2.5V	274 Ω	732 Ω	30 pf

3.3V* These settings should be done if there CMOs level is up to 4 V pp to limit the input at Xa to less than 2V ppse

Note: XA and XB must not exceed the maximum input voltage listed in Si5372-71 Datasheet Table 5.3 Input Clock Specifications.

Figure 11.1. XAXB Crystal Resonator and External Reference Clock Connection Options

In addition to crystal operations, the Si5395/94/92 accepts a clipped sine wave, CMOS, or differential reference clock on the XA/XB interface. Most clipped sine wave and CMOS TCXOs have insufficient drive strength to drive a 100 Ω or 50 Ω load. For this reason, place the TCXO as close to the Si5395/94/92 as possible to minimize PCB trace length. In addition, ensure that both the Si5395/94/92 and the TCXO are both connected directly to the ground plane. Figure 11.1 XAXB Crystal Resonator and External Reference Clock Connection Options on page 73 shows the recommended method of connecting a clipped sine wave TCXO to the Si5395/94/92. Because the Si5395/94/92 provides dc bias at the XA and XB pins, the ~800 mV peak-peak swing can be input directly into the XA interface of the Si5395/94/92 once it has been ac-coupled. Because the signal is single-ended, the XB input is ac-coupled to ground. Figure 11.1 XAXB Crystal Resonator and External Reference Clock Connection Options on page 73 illustrates the recommended method of connecting a CMOS rail-to-rail output to the XA/XB inputs of the Si5395/94/92. The resistor network attenuates the rail-to-rail output swing to ensure that the maximum input voltage swing at the XA pin is less than the data sheet specification. The signal is ac-coupled before connecting it to the Si5395/94/92 XA input. Again, since the signal is single-ended, the XB input should be ac-coupled to ground. For applications with loop BW values less than 10 Hz that require low wander output clocks, using a TCXO as the XAXB reference source should be considered to avoid the wander of a crystal.

If an external oscillator is used as the XAXB reference, it is important to use a low jitter source because there is effectively no jitter attenuation from the XAXB pins to the outputs. To minimize jitter at the XA/XB pins, the rise time of the XA/XB signals should be as fast as possible.

For best jitter performance, use a XAXB frequency above 40 MHz. Also, for XAXB frequencies higher than 125 MHz, the PXAXB control must be used to divide the input frequency down below 125 MHz.

11.2 Recommended Crystals and Oscillators

Refer to the Recommended Crystal, TCXO, and OCXO Reference Manual for High-Performance Jitter Attenuators and Clock Generators for more information.

11.3 Register Settings to Configure for External XTAL Reference

The following registers can be used to control and make adjustments for the external reference source used.

11.3.1 XAXB_EXTCLK_EN Reference Clock Selection Register

Table 11.1. XAXB External Clock Selection Register

Setting Name	Hex Address [Bit Field]	Function
	Si5395/94/92	
XAXB_EXTCLK_EN	090E[0]	Selects between the XTAL or external reference clock on the XA/XB pins. Default is 0, XTAL. Set to 1 to use an external reference oscillator.

The internal crystal loading capacitors (CL) are disabled when an external clock source is selected.

11.3.2 PXAXB Pre-scale Divide Ratio for Reference Clock Register

Table 11.2. XAXB Pre-Scale Divide Ratio Register

Setting Name	Hex Address [Bit Field]	Function
	Si5395/94/92	
PXAXB	0x0206[1:0]	Sets the XAXB input divider value according to the table below.

The following table lists the values, along with the corresponding divider ratio.

Table 11.3. XAXB Pre-Scale Divide Values

Value (Decimal)	PXAXB Divider Value
0	1
1	2
2	4
3	8

12. Internal Reference

Devices with internal reference (J/K/L/M/E) have a 48MHz crystal integrated in the package, to deliver a smaller layout footprint and more immunity to acoustic emissions. This crystal is manufactured by a reliable Japanese crystal manufacturer and has been pre-screened for activity dips before being assembled. It is important to note that connecting an external reference to XA/XB of a device that already has an integrated reference is not allowed. Doing so could lead to internal damage to the circuits. When using this integrated crystal option in a design that has been laid out for an external crystal, simply depopulate the crystal and replace the external crystal device with the internal crystal version. It is important to note that a new CBPro plan is required for the integrated crystal variant. For more information, please contact Silicon Labs support. For specifications of the internal crystal, please refer to the data sheet. During the initial power up, the integrated crystal quickly settles down to a temperature that is slightly higher than ambient temperature due to proximity to the die. If the PLL is locked to an input, the frequency accuracy of the crystal has no impact on the output frequency accuracy; if the PLL is free-running, then the output frequency tracks the crystal frequency which is still well within the spec.

13. Crystal, XO and Device Circuit Layout Recommendations

The following are recommendations for crystal layout (for devices that require an external reference), as well as device layout for all variants. The main layout issues that should be carefully considered include the following:

- Number and size of the ground vias for the Epad
- Output clock trace routing
- Input clock trace routing
- Control and Status signals to input or output clock trace coupling
- Xtal signal coupling (external reference devices)
- Xtal layout (external reference devices)

If the application uses a crystal for the XAXB inputs a shield should be placed underneath the crystal connected to the X1 and X2 pins to provide the best possible performance. The shield should not be connected to the ground plane(s), and the layers underneath should have as little area under the shield as possible. It may be difficult to do this for all the layers, but it is important to do this for the layers that are closest to the shield.

Go to the Silicon Labs Clock Development Tool webpage to obtain Si5395, Si5394, Si5392 evaluation board schematics, layouts, and component BOM files.

13.1 64-Pin QFN Si5395 Layout Recommendations

This section details the recommended guidelines for the external reference layout of the 64-pin Si5395 device using an example 8-layer PCB. The following are the descriptions of each of the eight layers.

- Layer 1: device layer, with low speed CMOS control/status signals
- Layer 2: crystal shield (applies to external reference devices only)
- Layer 3: ground plane
- Layer 4: power distribution
- Layer 5: power routing layer
- Layer 6: input clocks
- Layer 7: output clocks layer
- Layer 8: ground layer

The 64 pin QFN crystal guidelines show the top layer layout of the Si5395 device mounted on the top PCB layer. This particular layout was designed to implement either a crystal or an external oscillator as the XAXB reference. Note this applies only to external reference devices. The crystal/ oscillator area is outlined with the white box around it. In this case, the top layer is flooded with ground. Note that this layout has a resistor in series with each pin of the crystal. In typical applications, these resistors should be removed.

13.1.1 Si5395 XO Guidelines

For devices that use an external reference like an XO, pins X1 and X2 should not be connected to "ground" and should be left as "no-connects". An external reference does not need a crystal shield or the voids underneath the shield. The XA/XB connection should be treated as a high speed critical path that is ac-coupled and terminated at the end of the etch run. The layout should minimize the stray capacitance from the XA pin to the XB pin. Jitter is very critical at the XA/XB pins and therefore split termination and differential signaling should be used whenever possible.

13.1.2 Si5395 Crystal Guidelines

The following are five recommended crystal guidelines used with external reference devices:

1. Place the crystal as close as possible to the XA/XB pins.

2. DO NOT connect the crystal's GND pins to PCB gnd.

3. Connect the crystal's GND pins to the DUT's X1 and X2 pins via a local crystal GND shield placed around and under the crystal. See Figure 13.1 64-pin Si5395 Crystal Layout Recommendations Top Layer (Layer 1) on page 77 at the bottom left for an illustration of how to create a crystal GND shield by placing vias connecting the top layer traces to the shield layer underneath. Note that a zoom view of the crystal shield layer on the next layer down is shown in Figure 13.2 Zoom View Crystal Shield Layer, Below the Top Layer (Layer 2) on page 78.

4. Minimize traces adjacent to the crystal/oscillator area especially if they are clocks or frequently toggling digital signals.

5. In general do not route GND, power planes/traces, or locate components on the other side, below the crystal GND shield. As an exception if it is absolutely necessary to use the area on the other side of the board for layout or routing, then place the next reference plane in the stack-up at least two layers away or at least 0.05 inches away. The Si5395 should have all layers underneath the ground shield removed if possible.

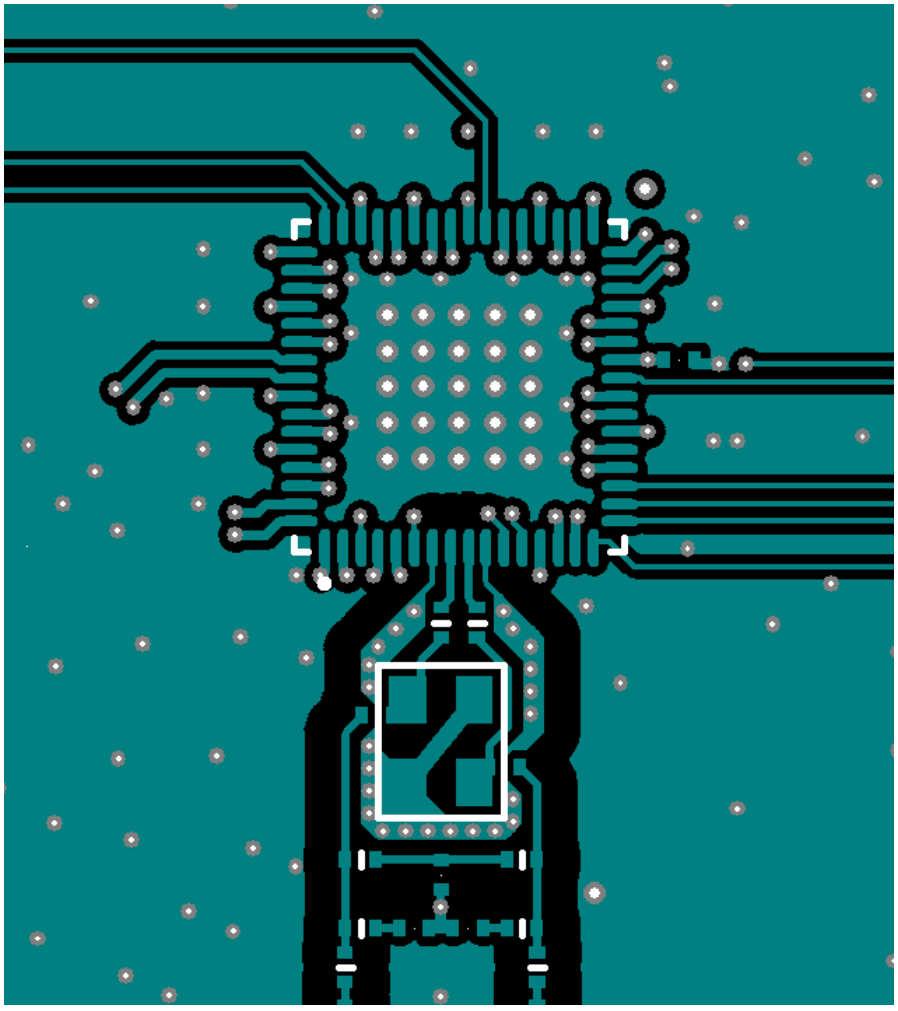


Figure 13.1. 64-pin Si5395 Crystal Layout Recommendations Top Layer (Layer 1)

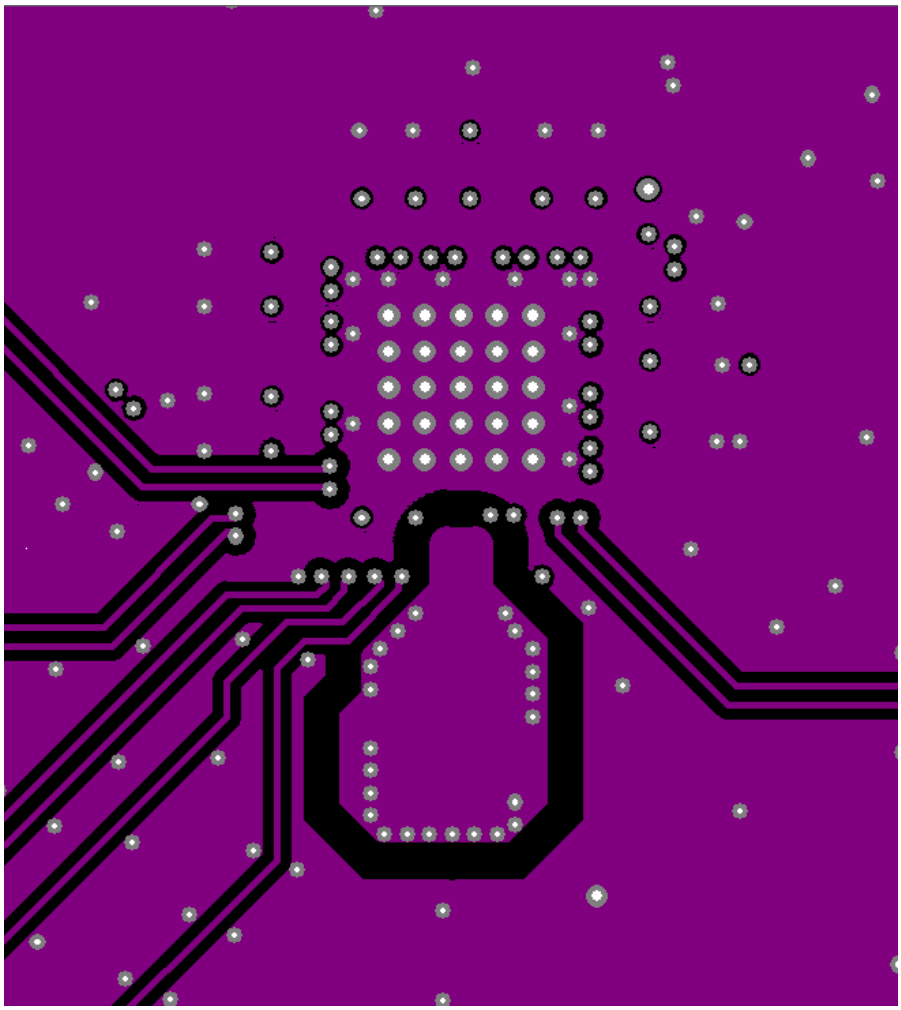


Figure 13.2. Zoom View Crystal Shield Layer, Below the Top Layer (Layer 2)

Figure 13.2 Zoom View Crystal Shield Layer, Below the Top Layer (Layer 2) on page 78 shows the layer that implements the shield underneath the crystal. The shield extends underneath the entire crystal and the X1 and X2 pins. This layer also has the clock input pins. The clock input pins go to layer 2 using vias to avoid crosstalk. As soon as the clock inputs are on layer 2, they have a ground shield above, below, and on the sides for protection.

Figure 13.3 Crystal Ground Plane (Layer 3) on page 79 is the ground plane and shows a void underneath the crystal shield. Figure 13.4 Power Plane (Layer 4) on page 80 is a power plane and shows the clock output power supply traces. The void underneath the crystal shield is continued.

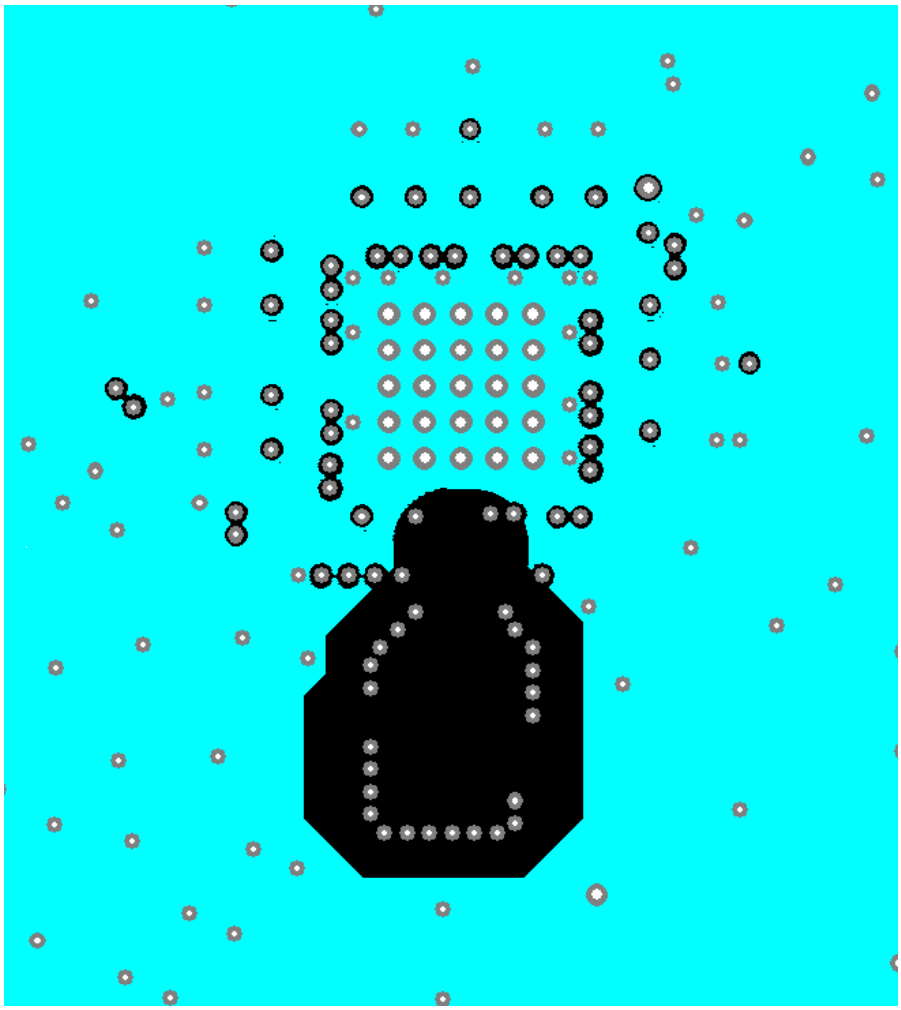


Figure 13.3. Crystal Ground Plane (Layer 3)

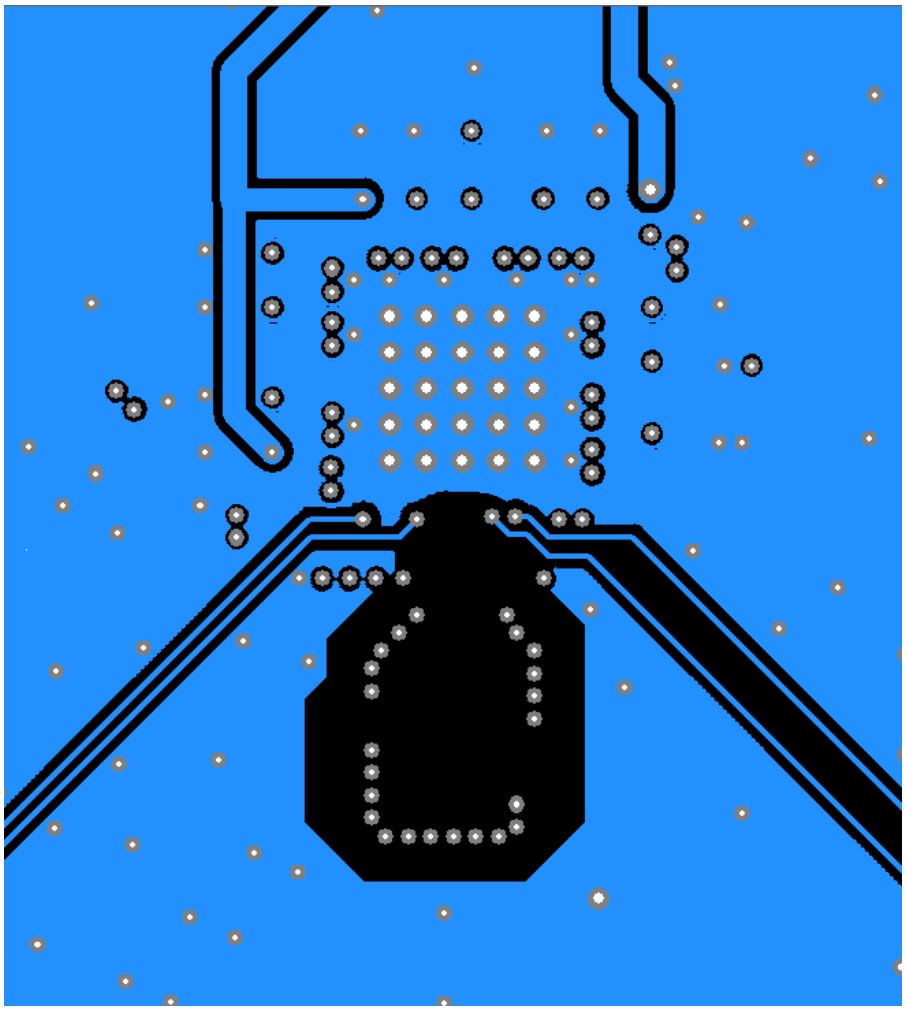


Figure 13.4. Power Plane (Layer 4)

Figure 13.5 Layer 5 Power Routing on Power Plane (Layer 5) on page 81 shows layer 5, which is the power plane with the power routed to the clock output power pins.

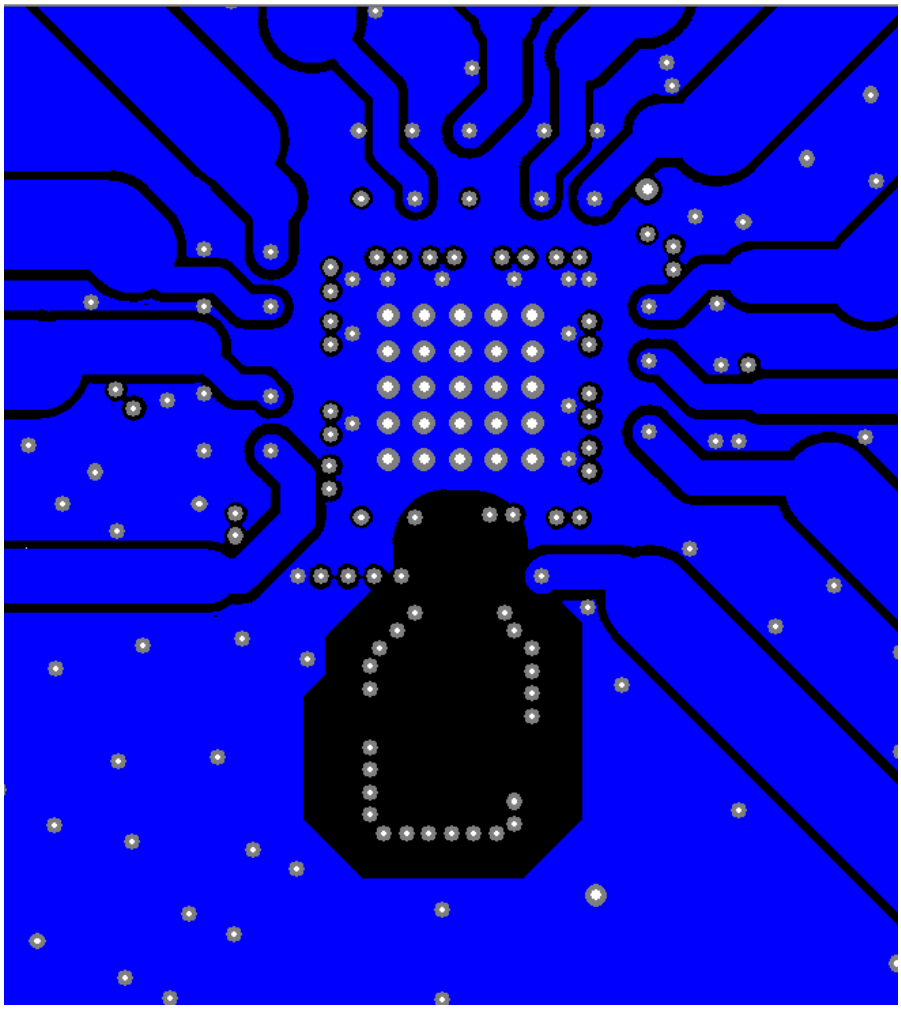


Figure 13.5. Layer 5 Power Routing on Power Plane (Layer 5)

Figure 13.6 Ground Plane (Layer 6) on page 82 is another ground plane similar to layer 3.

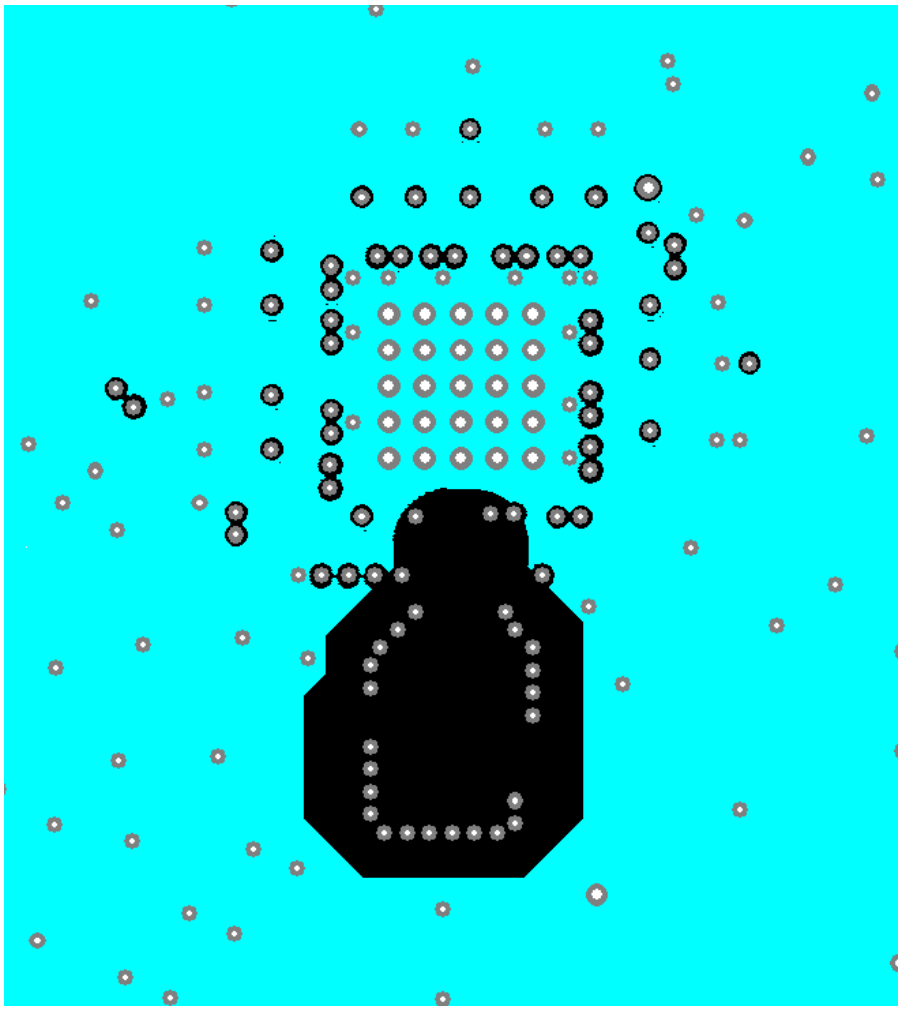


Figure 13.6. Ground Plane (Layer 6)

13.1.3 Si5395 Output Clocks

Figure 13.7 Output Clock Layer (Layer 7) on page 83 shows the output clocks. Similar to the input clocks the output clocks have vias that immediately go to a buried layer with a ground plane above them and a ground flooded bottom layer. There is a ground flooding between the clock output pairs to avoid crosstalk. There should be a line of vias through the ground flood on either side of the output clocks to ensure that the ground flood immediately next to the differential pairs has a low inductance path to the ground plane on layers 3 and 6.

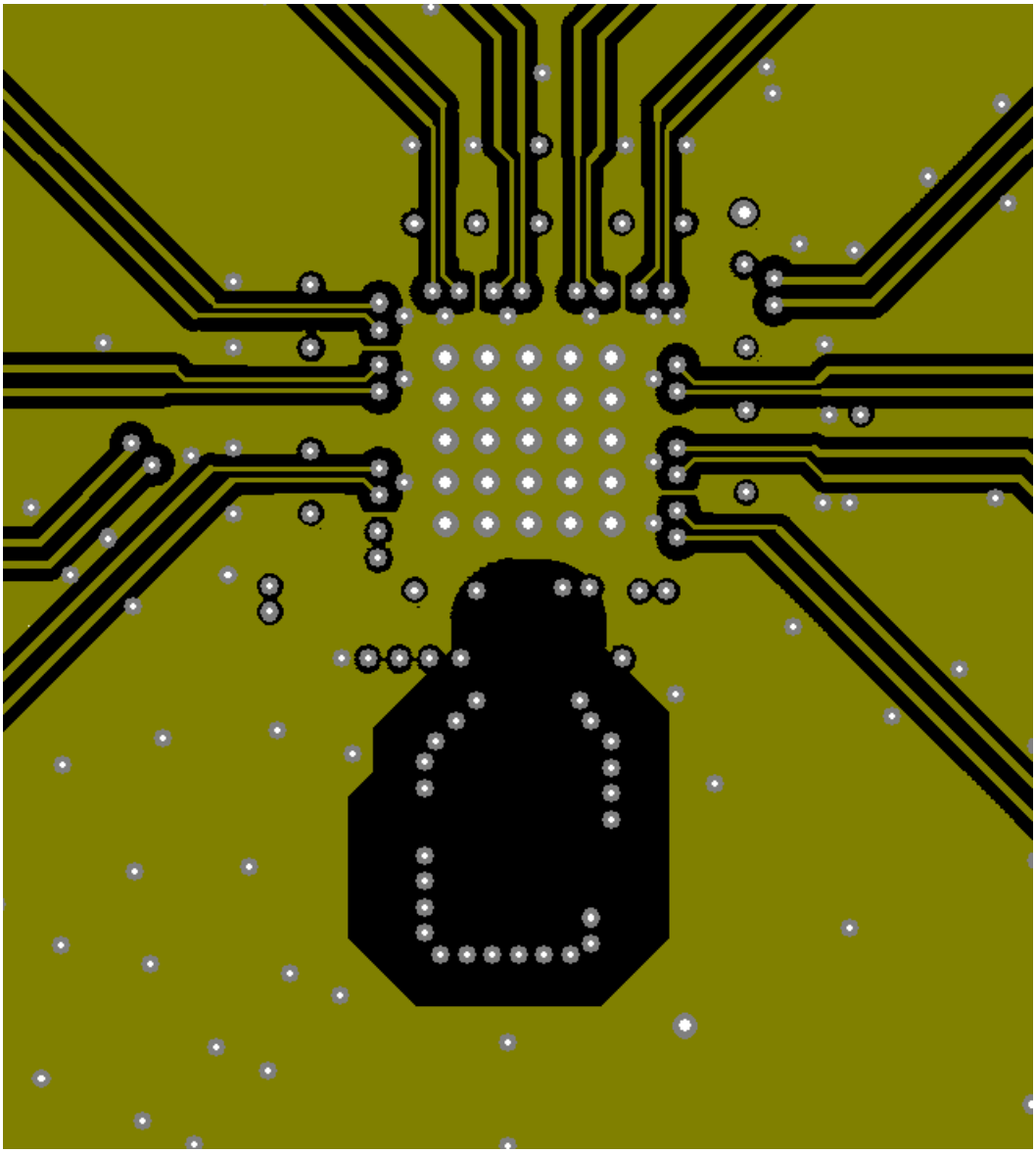


Figure 13.7. Output Clock Layer (Layer 7)

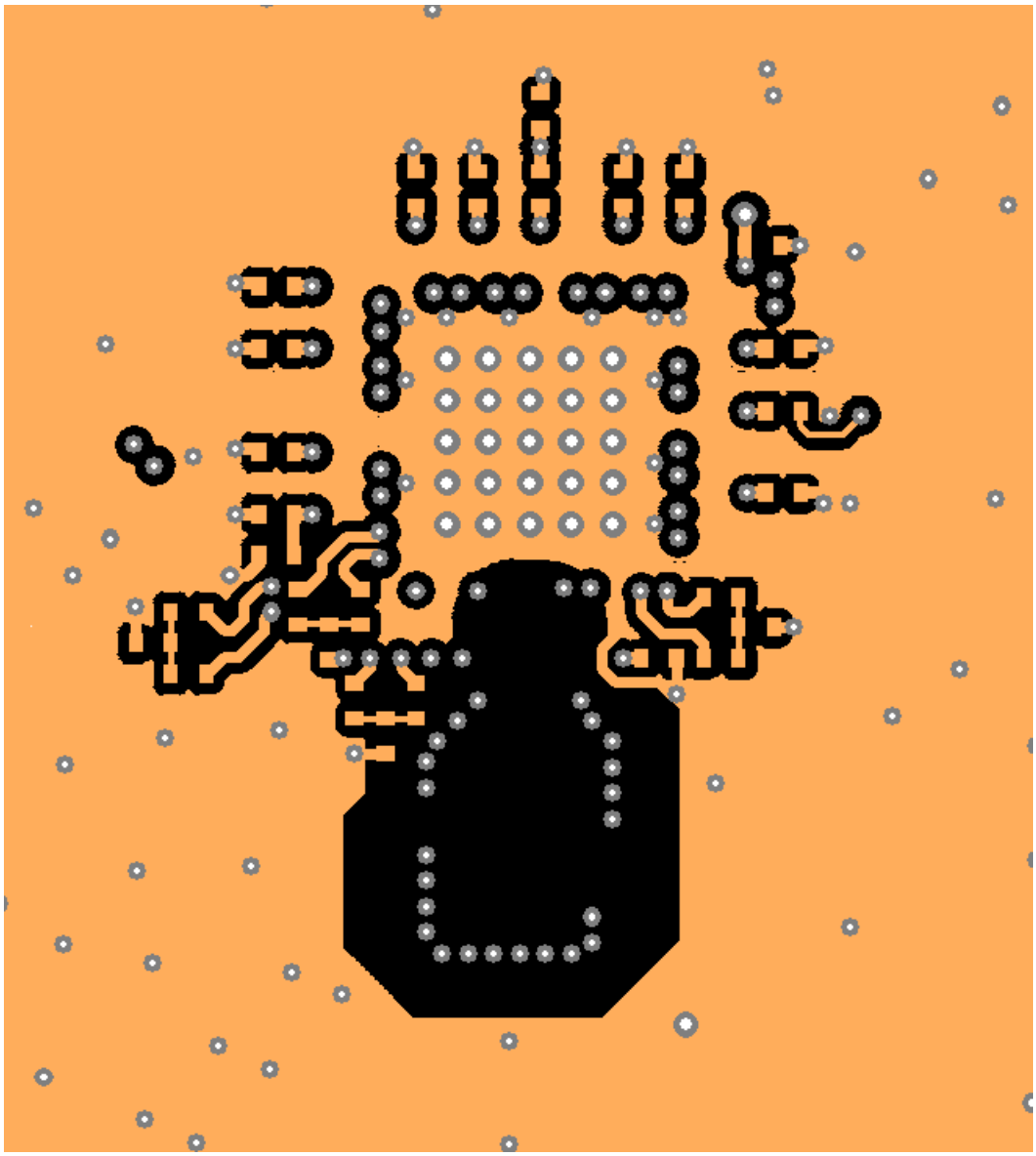


Figure 13.8. Bottom Layer Ground Flooded (Layer 8)

13.2 64-Pin LGA Si5395 Layout Recommendations

This section details the recommended guidelines for the internal reference layout. The crystal is integrated inside the package so leave XA, XB, X1, and X2 unconnected. An additional benefit of the internal crystal is that is does NOT need a crystal shield or voids on the PCB layers beneath the crystal. It is recommended to minimize traces adjacent to the chip especially if there are clocks or frequently toggling digital signals to avoid coupling of these signals into the device.

13.3 44-Pin QFN Si5394/92 Layout Recommendations

This section details the layout recommendations for the 44-pin external reference devices using an example 6-layer PCB.

The following guidelines details images of a six layer board with the following stack:

Layer 1: device layer, with low speed CMOS control/status signals, ground flooded

Layer 2: crystal shield, output clocks, ground flooded

Layer 3: ground plane

Layer 4: power distribution, ground flooded

Layer 5: input clocks, ground flooded

Layer 6: low-speed CMOS control/status signals, ground flooded

This layout was designed to implement either a crystal or an external oscillator as the XAXB reference (used with external reference devics). The top layer is flooded with ground. The clock output pins go to layer 2 using vias to avoid crosstalk during transit. When the clock output signals are on layer 2 there is a ground shield above, below and on all sides for protection. Output clocks should always be routed on an internal layer with ground reference planes directly above and below. The plane that has the routing for the output clocks should have ground flooded near the clock traces to further isolate the clocks from noise and other signals.

13.3.1 Si5394/92 XO Guidelines

For devices that use an external reference like an XO, pins X1 and X2 should not be connected to "ground" and should be left as "no-connects". An external reference does not need a crystal shield or the voids underneath the shield. The XA/XB connection should be treated as a high speed critical path that is ac-coupled and terminated at the end of the etch run. The layout should minimize the stray capacitance from the XA pin to the XB pin. Jitter is very critical at the XA/XB pins and therefore split termination and differential signaling should be used whenever possible. See Recommended Crystal, TCXO and OCXO Reference Manual for High-Performance Jitter Attenuators and Clock Generators for a suggested list of XOs.

13.3.2 Si5394/92 Crystal Guidelines

The following are five recommended crystal guidelines:

1. Place the crystal as close as possible to the XA/XB pins.
2. DO NOT connect the crystal's GND pins to PCB gnd.
3. Connect the crystal's GND pins to the DUT's X1 and X2 pins via a local crystal GND shield placed around and under the crystal. See Figure 13.9 Device Layer (Layer 1) on page 86 at the bottom left for an illustration of how to create a crystal GND shield by placing vias connecting the top layer traces to the shield layer underneath. Note that a zoom view of the crystal shield layer on the next layer down is shown in Figure 13.10 Crystal Shield Layer 2 on page 87.
4. Minimize traces adjacent to the crystal/oscillator area especially if they are clocks or frequently toggling digital signals.
5. In general do not route GND, power planes/traces, or locate components on the other side, below the crystal GND shield. As an exception if it is absolutely necessary to use the area on the other side of the board for layout or routing, then place the next reference plane in the stack-up at least two layers away or at least 0.05 inches away. The Si5394/92 should have all layers underneath the ground shield removed if possible.

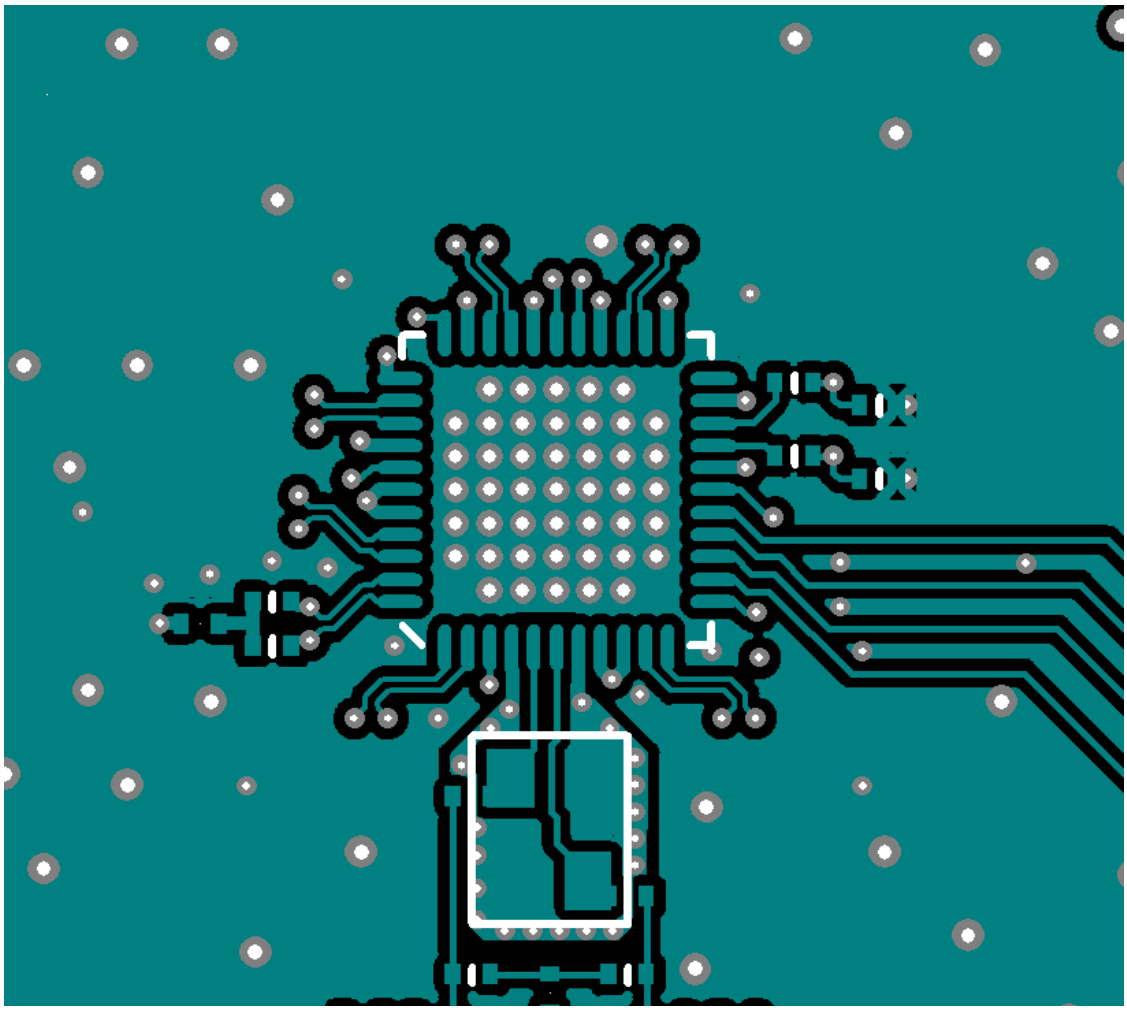


Figure 13.9. Device Layer (Layer 1)

Figure 13.10 Crystal Shield Layer 2 on page 87 is the second layer. The second layer implements the shield underneath the crystal. The shield extends underneath the entire crystal and the X1 and X2 pins. There should be no less than 12 vias to connect the X1 and X2 planes on layers 1 and 2. These vias are not shown in any other figures. All traces with signals that are not static must be kept well away from the crystal and the X1 and X2 plane.

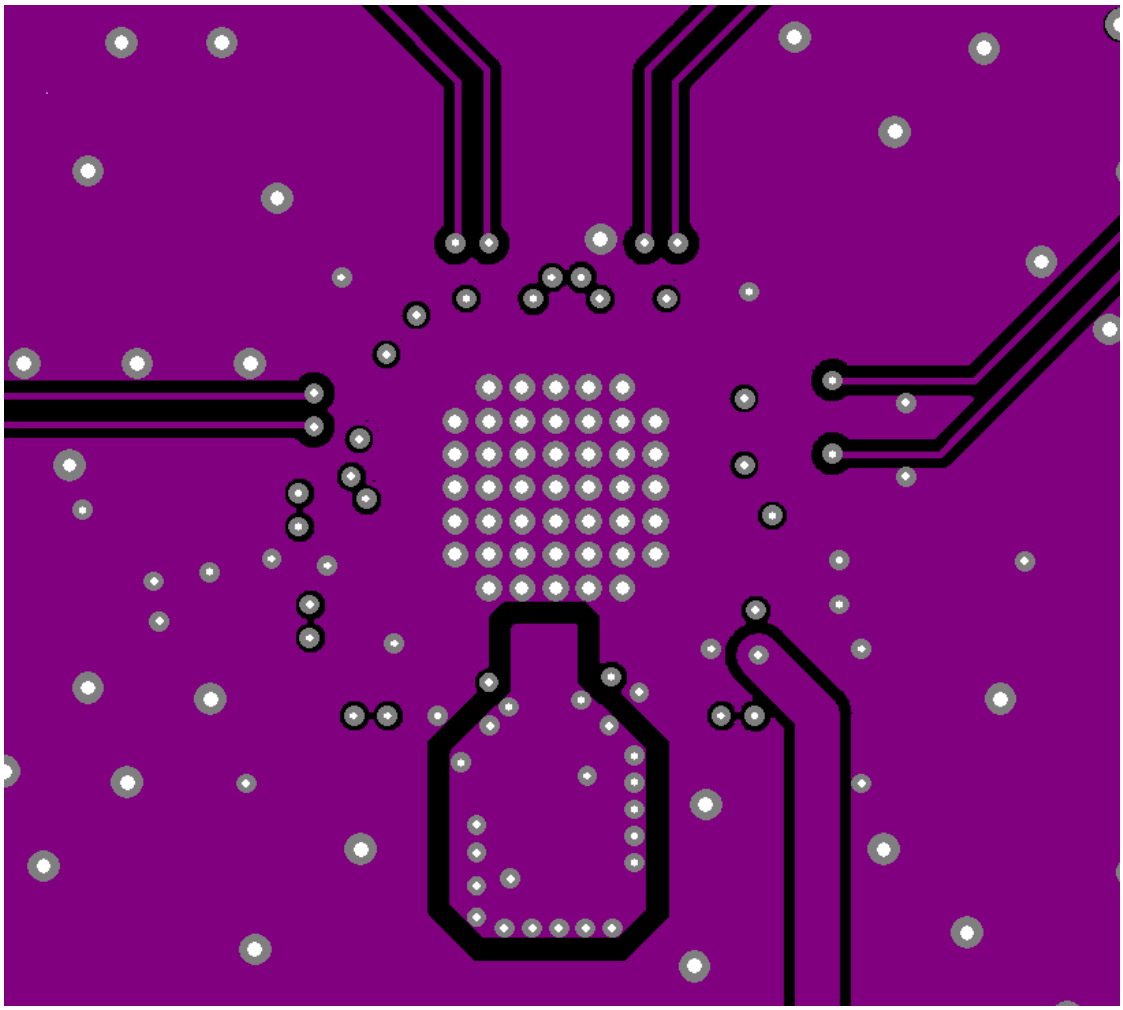


Figure 13.10. Crystal Shield Layer 2

Figure 13.11 Ground Plane (Layer 3) on page 88 is the ground plane and shows a void underneath the crystal shield.

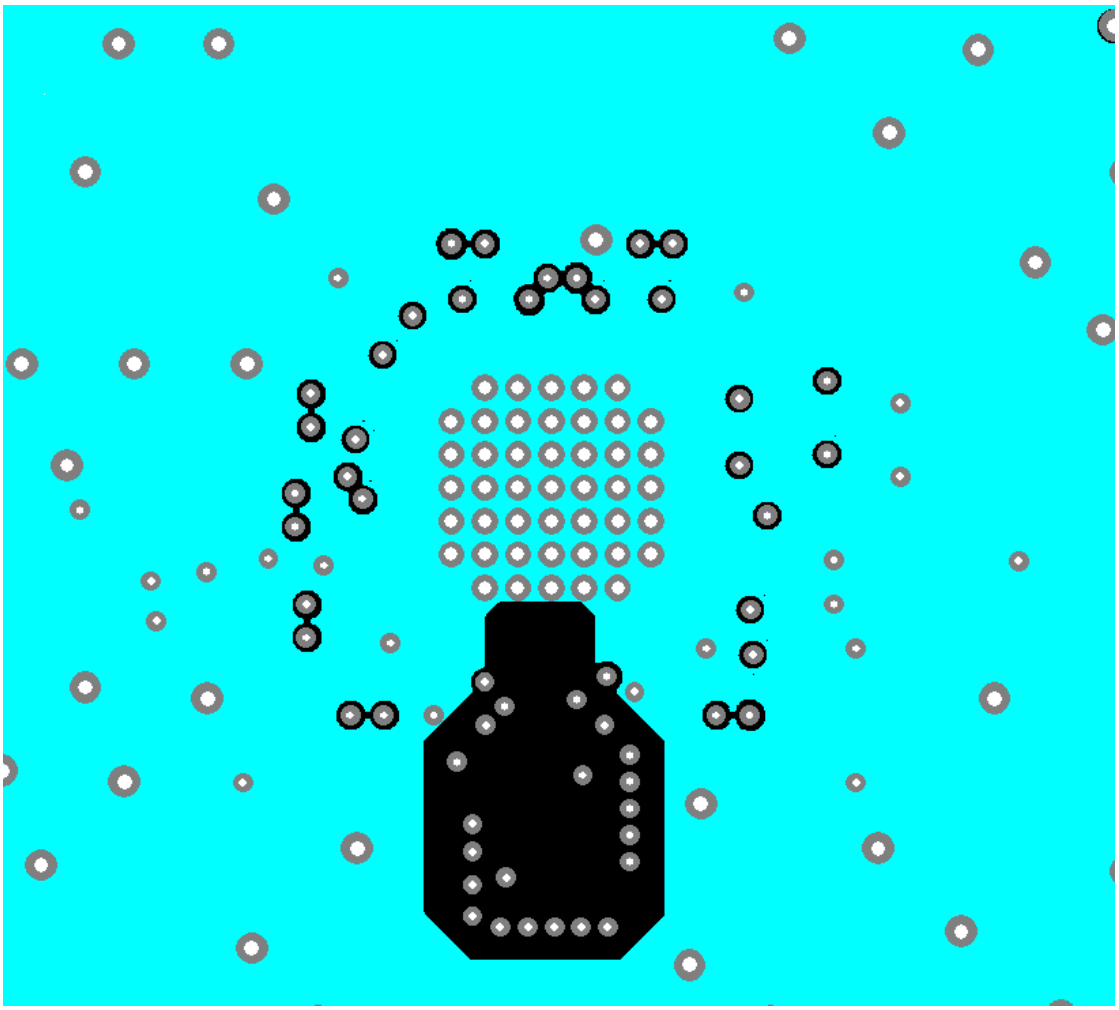


Figure 13.11. Ground Plane (Layer 3)

Figure 13.12 Power Plane and Clock Output Power Supply Traces (Layer 4) on page 89 is a power plane showing the clock output power supply traces. The void underneath the crystal shield is continued.

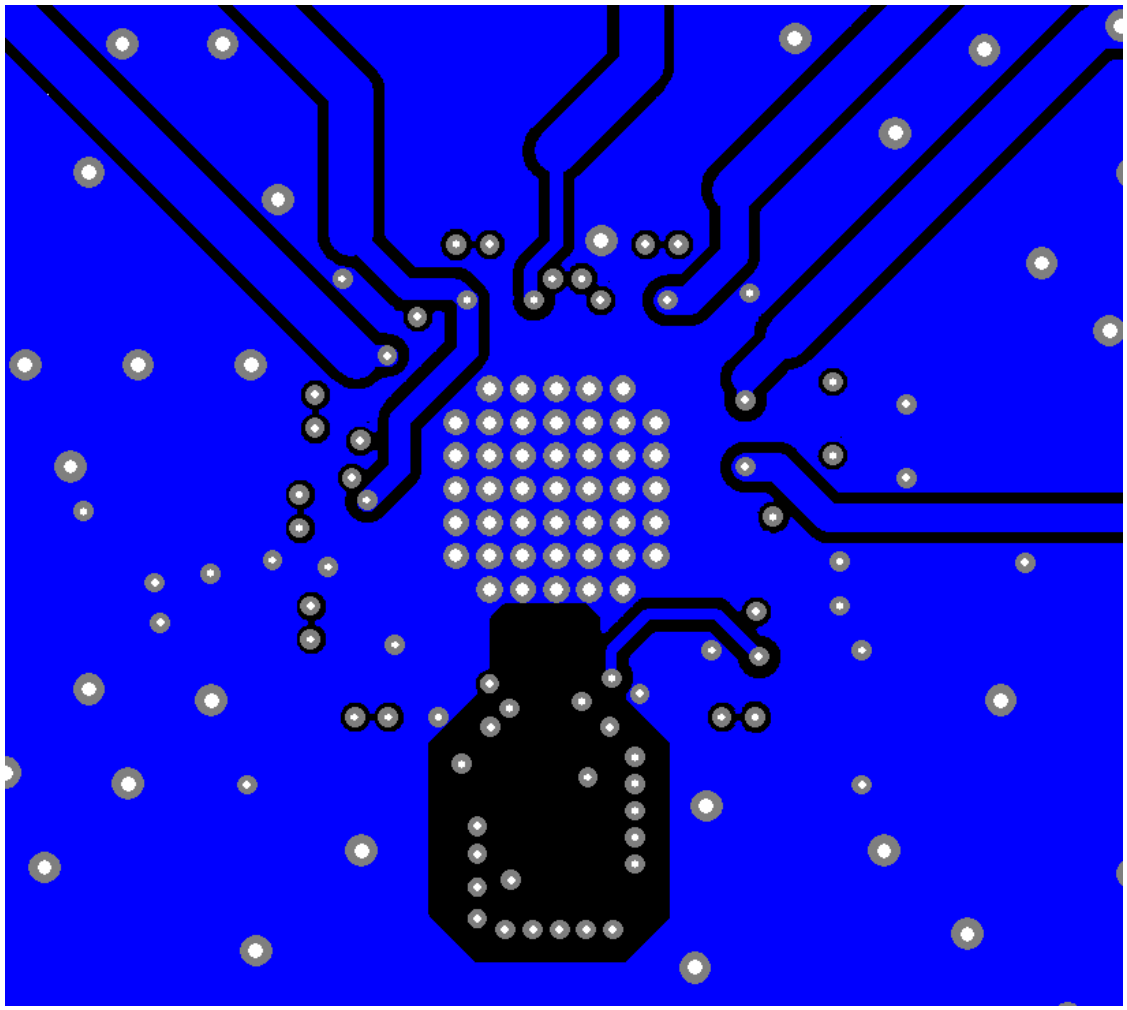


Figure 13.12. Power Plane and Clock Output Power Supply Traces (Layer 4)

Figure 13.13 Clock Input Traces (Layer 5) on page 90 shows layer 5 and the clock input traces. Similar to the clock output traces, they are routed to an inner layer and surrounded by ground to avoid crosstalk.

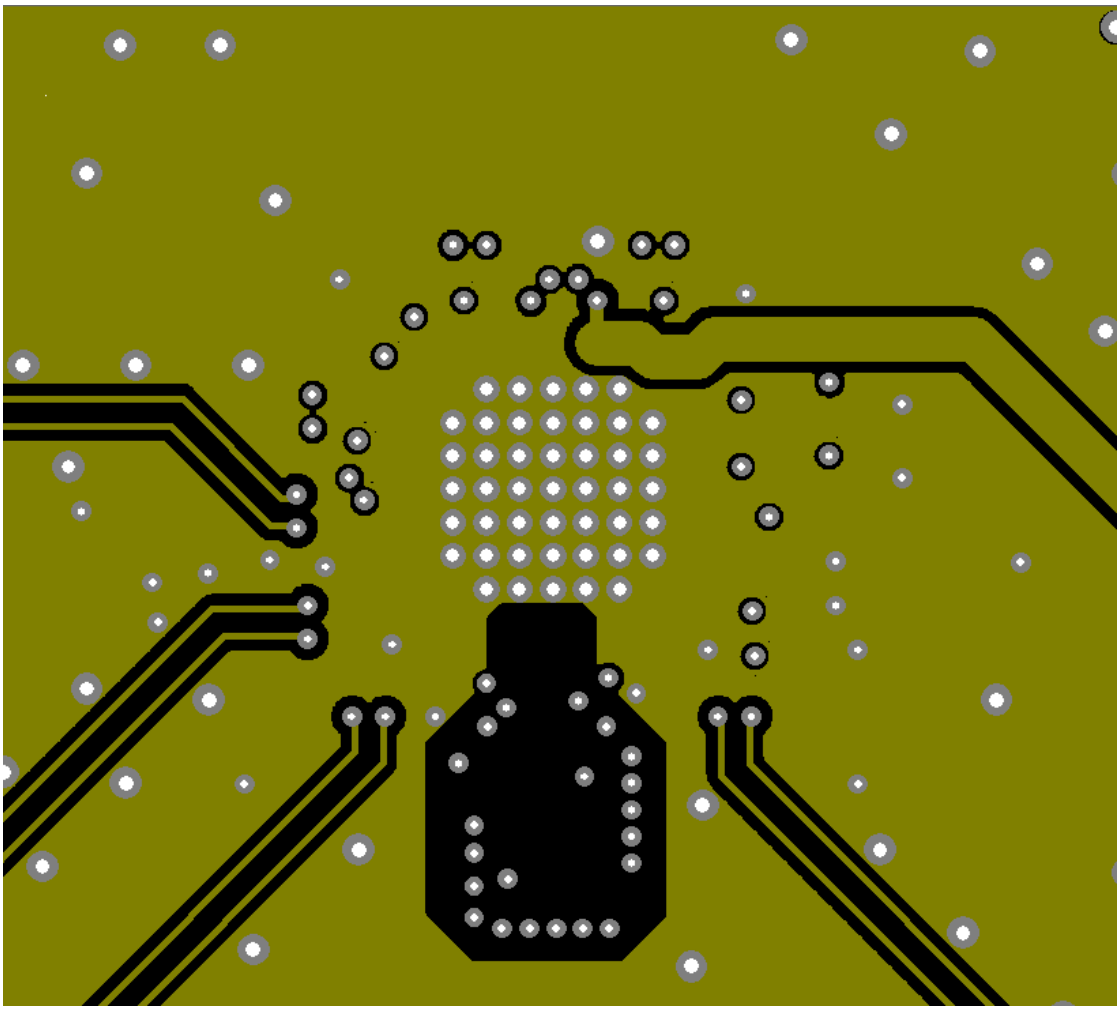


Figure 13.13. Clock Input Traces (Layer 5)

Figure 13.14 Low-Speed CMOS Control and Status Signal Layer 6 (Bottom Layer) on page 91 shows the bottom layer, which continues the void underneath the shield. Layer 6 and layer 1 are mainly used for low speed CMOS control and status signals for which crosstalk is not a significant issue. PCB ground can be placed under the XTAL Ground shield (X1/X2) as long as the PCB ground is at least 0.05 inches below it.

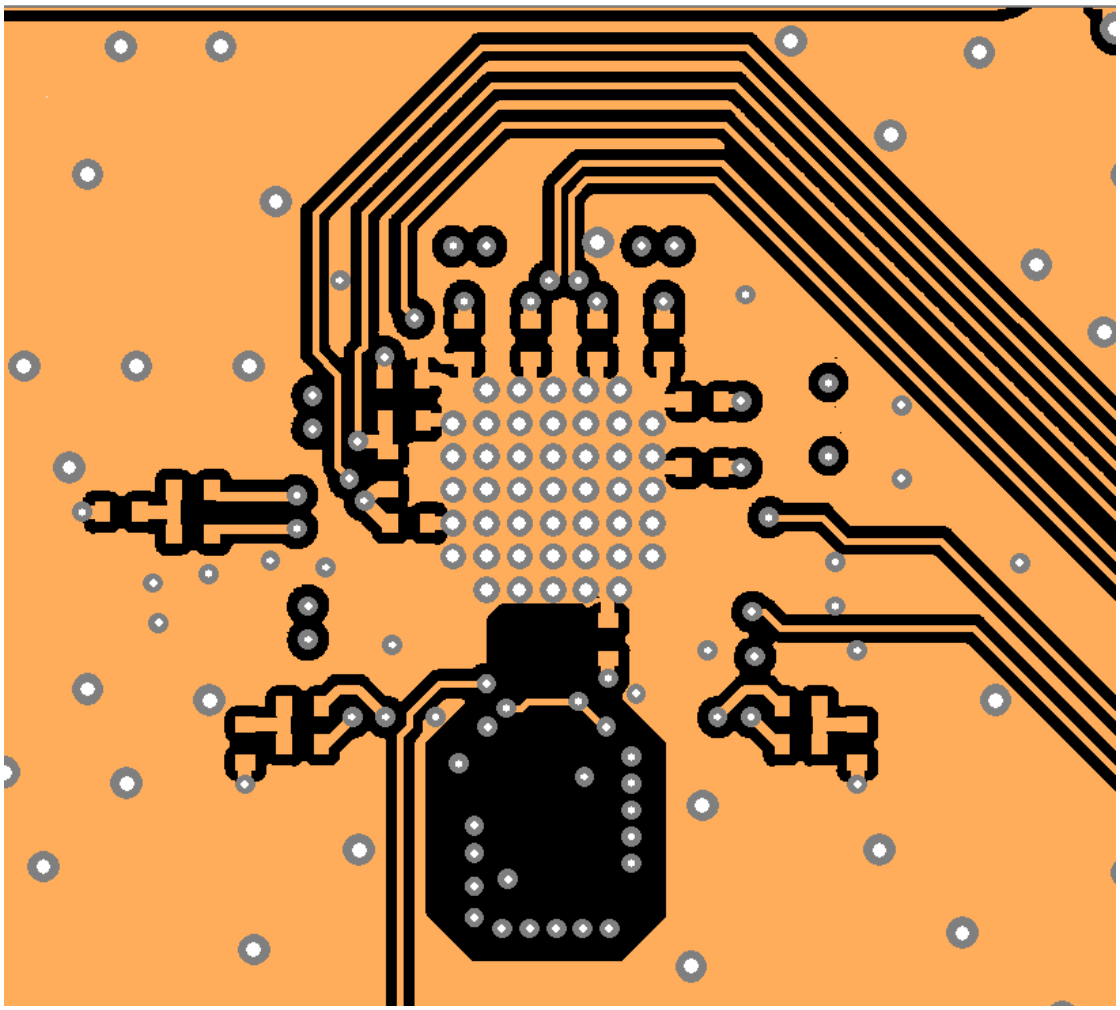


Figure 13.14. Low-Speed CMOS Control and Status Signal Layer 6 (Bottom Layer)

For any high-speed, low-jitter application, the clock signal runs should be impedance-controlled to 100 Ω differential or 50 Ω single-ended. Differential signaling is preferred because of its increased immunity to common-mode noise. All clock I/O runs should be properly terminated.

13.4 44-Pin LGA Si5394/92 Layout Recommendations

The crystal is integrated inside the package so leave XA, XB, X1, and X2 unconnected. An additional benefit of the internal crystal is that is does NOT need a crystal shield or voids on the PCB layers beneath the crystal. It is recommended to minimize traces adjacent to the chip especially if there are clocks or frequently toggling digital signals to avoid coupling of these signals into the device.

14. Power Management

14.1 Power Management Features

Several unused functions can be powered down to minimize power consumption. The registers listed below are used for powering down different features.

Table 14.1. Power-Down Registers

Register Name	Hex Address [Bit Field]			Function
	Si5395	Si5394	Si5392	
PDN	0x001E[0]	0x001E[0]	0x001E[0]	This bit allows the device to be powered down. The serial interface remains powered.
OUT0A_PDN	0x0103[0]	—	—	Powers down all unused clock outputs.
OUT0_PDN	0x0108[0]	0x0112[0]	0x0112[0]	
OUT1_PDN	0x010D[0]	0x0117[0]	0x0117[0]	
OUT2_PDN	0x0112[0]	0x0126[0]	—	
OUT3_PDN	0x0117[0]	0x012B[0]	—	
OUT4_PDN	0x011C[0]	—	—	
OUT5_PDN	0x0121[0]	—	—	
OUT6_PDN	0x0126[0]	—	—	
OUT7_PDN	0x012B[0]	—	—	
OUT8_PDN	0x0130[0]	—	—	
OUT9_PDN	0x0135[0]	—	—	
OUT9A_PDN	0x013A[0]	—	—	
OUT_PDN_ALL	0x0145[0]	0x0145[0]	0x0145[0]	Power down all outputs
XAXB_EXTCLK_EN	0x090E[1]			0 to use a crystal at the XAXB pins, 1 to use an external clock source at the XAXB pins

14.2 Power Supply Recommendations

The power supply filtering generally is important for optimal timing performance. The Si5395/94/92 devices have multiple stages of on-chip regulation to minimize the impact of board level noise on clock jitter. Following conventional power supply filtering and layout techniques will further minimize signal degradation from the power supply.

It is recommended to use a 1 µF 0402 ceramic capacitor on each VDD for optimal performance. It is also suggested to include an optional, single 0603 (resistor/ferrite) bead in series with each supply to enable additional filtering if needed.

14.3 Power Supply Sequencing

Four classes of supply voltages exist on the Si5395/94/92:

1. VDD = 1.8 V (Core digital supply)
2. VDDA = 3.3 V (Analog supply)
3. VDDOx = 1.8/2.5/3.3 V ± 5% (Clock output supply)
4. VDDS = 1.8/3.3V ± 5% (Digital I/O supply)

There is no requirement for power supply sequencing unless the output clocks are required to be phase aligned with each other. In this case, the VDDO of each clock which needs to be aligned must be powered up before VDD and VDDA. VDDS has no effect on output clock alignment.

If output-to-output alignment is required for applications where it is not possible to properly sequence the power supplies, then the output clocks can be aligned by asserting the SOFT_RST 0x001C[0] or Hard Reset 0x001E[1] register bits or driving the RSTB pin. Note that using a hard reset will reload the register with the contents of the NVM and any unsaved changes will be lost.

One may observe that when powering up the VDD = 1.8 V rail first, that the VDDA = 3.3 V rail will initially follow the 1.8 V rail. Likewise, if the VDDA rail is powered down first then it will not drop far below VDD until VDD itself is powered down. This is due to the pad I/O circuits which have large MOSFET switches to select the local supply from either the VDD or VDDA rails. These devices are relatively large and yield a parasitic diode between VDD and VDDA. Please allow for both VDD and VDDA to power-up and power-down before measuring their respective voltages.

14.4 Grounding Vias

The pad on the bottom of the device functions as both the sole electrical ground and primary heat transfer path. Hence it is important to minimize the inductance and maximize the heat transfer from this pad to the internal ground plane of the PCB. Use no fewer than 25 vias from the center pad to a ground plane under the device. In general, more vias will perform better. Having the ground plane near the top layer will also help to minimize the via inductance from the device to ground and maximize the heat transfer away from the device.

15. Register Map

15.1 Base vs. Factory Preprogrammed Devices

The Si5395/94/92 devices can be ordered as “base” or “factory-preprogrammed” (also known as “custom OPN”) versions.

15.2 “Base” Devices (a.k.a. “Blank” Devices)

Example “base” orderable part numbers (OPNs) are of the form “Si5395A-E-GM” or “Si5394B-E-GM”.

Base devices are available for applications where volatile reads and writes are used to program and configure the device for a particular application.

Base devices do not power up in a usable state (all output clocks are disabled).

Base devices are, however, configured by default to use a 48 MHz crystal on the XA/XB reference and a 1.8 V compatible I/O voltage setting for the host I^2C/SPI interface.

Additional programming of a base device is mandatory to achieve a usable configuration.

See the on-line lookup utility at: https://www.silabs.com/products/timing/lookup-customize to access the default configuration plan and register settings for any base OPN.

15.3 “Factory Preprogrammed” (Custom OPN) Devices

Factory preprogammed devices use a “custom OPN”, such as Si5395A-E-xxxxx-GM, where xxxxx is a sequence of characters assigned by Silicon Labs for each customer-specific configuration. These characters are referred to as the “OPN ID”. Customers must initiate custom OPN creation using the ClockBuilder Pro software.

Many customers prefer to order devices which are factory preprogrammed for a particular application that includes specifying the XA/XB reference frequency/type, the clock input frequencies, the clock output frequencies, as well as the other options, such as automatic clock selection, loop BW, etc. The ClockBuilder software is required to select among all of these options and to produce a project file which Silicon Labs uses to preprogram all devices with custom orderable part number (“custom OPN”).

Custom OPN devices contain all of the initialization information in their non-volatile memory (NVM) so that it powers up fully configured and ready to go.

Because preprogrammed device applications are inherently quite different from one another, the default power up values of the register settings can be determined using the custom OPN utility at: https://www.silabs.com/products/timing/lookup-customize.

Custom OPN devices include a device top mark which includes the unique OPN ID. Refer to the device data sheet's Ordering Guide and Top Mark sections for more details.

Both “base” and “factory preprogrammed” devices can have their operating configurations changed at any time using volatile reads and writes to the registers. Both types of devices can also have their current register configuration written to the NVM by executing an NVM bank burn sequence (see Section 4.3 NVM Programming.)

15.4 Register Map Overview and Default Settings Values

The Si5395/94/92 family parts have large register maps that are divided into separate “Pages” of register banks. This allows more register addresses than either the I^2C or SPI serial interface standards 8-bit addressing provide. Each page has a maximum of 256 addresses, however not all addresses are used on every page. Every register has a maximum data size of 8-bits, or 1 byte. Writing the page number to the 8-bit serial interface address of 0x01 on any page (0x0001, 0x0101, 0x0201, etc.) updates the page selection for subsequent register reads and writes. For example, to access the value in register 0x040E, it is first necessary to write the page value 0x04 to serial interface register address 0x01. At this point, the value of serial interface address 0x0E (0x040E) may be read or written. Note that is it not necessary to write the page select register again when accessing other registers on the same page. Similarly, the read-only DEVICE_READY status is available from every page at serial interface address 0xFE (0x00FE, 0x01FE, 0x02FE, etc.).

It is recommended to use dynamic Read-Modify-Write methods when writing to registers which contain multiple settings, such as register 0x0011. To do this, first read the current contents of the register. Next, update only the select bit or bits that are being modified. This may involve using both logical AND and logical OR operations. Finally, write the updated contents back to the register. Writing to pages, registers, or bits not documented below may cause undesired behavior in the device.

Details of the register and settings information are organized hierarchically below. To find the relevant information for your application, first choose the section corresponding to the base part number, Si5395, Si5394, Si5392 for your design. Then, choose the section under that for the page containing the desired register(s).

Default register contents and settings differ for each device part number, or OPN. This information may be found by searching for the Custom OPN for your device using the link below. Both Base/Blank and Custom OPNs are available there. See the previous section on “Base vs. Factory Preprogrammed Devices" for more information on part numbers. The Private Addendum to the datasheet lists the default settings and frequency plan information. You must be logged into the Silicon Labs website to access this information. The Public addendum gives only the general frequency plan information (https://www.silabs.com/products/timing/lookup-customize).

Table 15.1. Register Map Paging Descriptions

Page	Start Address (Hex)	Start Address (Decimal)	Contents
Page 0	0000h	0	Alarms, interrupts, reset, other configuration
Page 1	0100h	256	Clock output configuration
Page 2	0200h	512	P,R dividers, scratch area
Page 3	0300h	768	Output N dividers, N divider Finc/Fdec
Page 4	0400h	1024	ZD mode configuration
Page 5	0500h	1280	M divider, BW, holdover, input switch, FINC/DEC
Page 9	0900h	2304	Control IO configuration
Page A	0A00h	2560	Multisynth Controls
Page B	0B00h	2816	Various
Page C	0C00h	3072	Various

R = Read Only

R/W = Read Write

S = Self Clearing

A self-clearing bit will be cleared by the device once the operation initiated by this bit is complete. Registers with “sticky” flag bits, such as LOS0_FLG, are cleared by writing “0” to the bit that has been automatically set high by the device.

16. Si5395 Register Definitions

16.1 Page 0 Registers Si5395

Table 16.1. 0x0001 Page

Reg Address	Bit Field	Type	Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

On every page, there is a “Page Register” located at address 0x01. When read, it indicates the current page. When written, it changes the page to the value entered. There are page registers at addresses 0x0001, 0x0101, 0x0201, 0x0301, … etc.

Table 16.2. 0x0002–0x0003 Base Part Number

Reg Address	Bit Field	Type	Name	Value	Description
0x0002	7:0	R	PN_BASE	0x95	Four-digit “base” part number, one nibble per digit. Example: Si5395A-A-GM. The base part number (OPN) is 5395, which is stored in this register.
0x0003	15:8	R	PN_BASE	0x53	

Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 16.3. 0x0004 Device Grade

Reg Address	Bit Field	Type	Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed/synthesis mode. 0 = A, 1 = B, 2 = C, 3 = D , 4 =E 9=J, 10=K,11=L,12=M,15=P etc

Table 16.4. 0x0005 Device Revision

Reg Address	Bit Field	Type	Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B, etc. Example Si5395C-A12345-GM, the device revision is “A” and stored as 0.

Table 16.5. 0x0006–0x0008 TOOL_VERSION

Reg Address	Bit Field	Type	Name [1]	Description
0x0006	3:0	R/W	TOOL_VERSION[3:0]	Special
0x0006	7:4	R/W	TOOL_VERSION[7:4]	Revision
0x0007	7:0	R/W	TOOL_VERSION[15:8]	Minor[7:0]
0x0008	0	R/W	TOOL_VERSION[15:8]	Minor[8]

Reg Address	Bit Field	Type	Name [1]	Description
0x0008	4:1	R/W	TOOL_VERSION[16]	Major
0x0008	7:5	R/W	TOOL_VERSION[13:17]	Tool. 0 for ClockBuilder Pro

Note:
1. The software tool version that creates the register values downloaded at power up is represented by TOOL_VERSION.

Table 16.6. 0x0009 Temperature Grade

Reg Address	Bit Field	Type	Name	Description
0x0009	7:0	R/W	TEMP_GRADE	Device temperature grading 0 = Industrial (–40° C to 85° C) ambient conditions

Table 16.7. 0x000A Package ID

Reg Address	Bit Field	Type	Name	Description
0x000A	7:0	R/W	PKG_ID	Package ID 0 = 9x9 mm 64 QFN

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples

Si5395C-A12345-GM.

Applies to a “base” or “blank” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5395C-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5395 but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 16.8. 0x000B I^2C Address

Reg Address	Bit Field	Type	Setting Name	Description
0x000B	6:2	R/W	I2C_ADDR	The upper five bits of the 7-bit I^2C address. The lower two bits are controlled by the A1 and A0 pins. Note: This register is not bank burnable.

Table 16.9. 0x000C Internal Status Bits

Reg Address	Bit Field	Type	Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	3	R	XAXB_ERR	1 if there is a problem locking to the XAXB input signal.
0x000C	5	R	SMBUS_TIMEOUT	1 if there is an SMBus timeout error.

Bit 1 is the LOS status monitor for the XTAL or REFCLK at the XA/XB pins.

Table 16.10. 0x000D Out-of-Frequency (OOF) and Loss-of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Name	Description
0x000D	3:0	R	LOS	1 if the clock input is currently LOS
0x000D	7:4	R	OOF	1 if the clock input is currently OOF

Note that each bit corresponds to the input. The LOS and OOF bits are not sticky.

Input 0 (IN0) corresponds to LOS 0x000D [0], OOF 0x000D [4]

Input 1 (IN1) corresponds to LOS 0x000D [1], OOF 0x000D [5]

Input 2 (IN2) corresponds to LOS 0x000D [2], OOF 0x000D [6]

Input 3 (IN3) corresponds to LOS 0x000D [3], OOF 0x000D [7]

Table 16.11. 0x000E Holdover and LOL Status

Reg Address	Bit Field	Type	Name	Description
0x000E	1	R	LOL	1 if the DSPLL is out of lock
0x000E	5	R	HOLD	1 if the DSPLL is in holdover (or free run)

These status bits indicate if the DSPLL is in holdover and if it is in Loss of Lock. These bits are not sticky.

Table 16.12. 0x000F Calibration Status

Reg Address	Bit Field	Type	Name	Description
0x000F	5	R	CAL_PLL	1 if the DSPLL internal calibration is busy

This status bit indicates if a DSPLL is currently busy with calibration. This bit is not sticky.

Table 16.13. 0x0011 Internal Error Flags

Reg Address	Bit Field	Type	Name	Description
0x0011	0	R/W	SYSINCAL_FLG	Sticky version of SYSINCAL. Write a 0 to this bit to clear.
0x0011	1	R/W	LOSXAXB_FLG	Sticky version of LOSXAXB. Write a 0 to this bit to clear.
0x0011	3	R/W	XAXB_ERR_FLG	Sticky version of XAXB_ERR.Write a 0 to this bit to clear.
0x0011	5	R/W	SMBUS_TIMEOUT_FLG	Sticky version of SMBUS_TIMEOUT. Write a 0 to this bit to clear.

If any of these six bits are high, there is an internal fault. Please contact Silicon Labs. These are sticky flag bits. They are cleared by writing zero to the bit that has been set.

Table 16.14. 0x0012 Sticky OOF and LOS Flags

Reg Address	Bit Field	Type	Name	Description
0x0012	3:0	R/W	LOS_FLG	1 if the clock input is LOS for the given input
0x0012	7:4	R/W	OOF_FLG	1 if the clock input is OOF for the given input

These are the sticky flag versions of register 0x000D. These bits are cleared by writing 0 to the bits that have been set.

Input 0 (IN0) corresponds to LOS_FLG 0x0012 [0], OOF_FLG 0x0012 [4]

Input 1 (IN1) corresponds to LOS_FLG 0x0012 [1], OOF_FLG 0x0012 [5]

Input 2 (IN2) corresponds to LOS_FLG 0x0012 [2], OOF_FLG 0x0012 [6]

Input 3 (IN3) corresponds to LOS_FLG 0x0012 [3], OOF_FLG 0x0012 [7]

Table 16.15. 0x0013 Sticky Holdover and LOL Flags

Reg Address	Bit Field	Type	Name	Description
0x0013	1	R/W	LOL_FLG	1 if the DSPLL was unlocked
0x0013	5	R/W	HOLD_FLG	1 if the DSPLL was in holdover or free run

These are the sticky flag versions of register 0x000E. These bits are cleared by writing 0 to the bits that have been set.

Table 16.16. 0x0014 Sticky PLL In Calibration Flag

Reg Address	Bit Field	Type	Name	Description
0x0014	5	R/W	CAL_FLG_PLL	1 if the internal calibration was busy

This bit is the sticky flag version of 0x000F. This bit is cleared by writing 0 to bit 5.

Table 16.17. 0x0016

Reg Address	Bit Field	Type	Name	Description
0x0016	1	R/W	LOL_ON_HOLD	Set by CBPro.

Table 16.18. 0x0017 Status Flag Masks

Reg Address	Bit Field	Type	Name	Description
0x0017	0	R/W	SYSINCAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt
0x0017	1	R/W	LOSXAXB_INTR_MSK	1 to mask the LOSXAXB_FLG from causing an interrupt
0x0017	5	R/W	SMBUS_TIMEOUT_INTR_MSK	1 to mask SMBUS_TIMEOUT_FLG from the interrupt
0x0017	6	R/W	RESERVED	Factory set to 1 to mask reserved bit from causing an interrupt. Do not clear this bit.
0x0017	7	R/W	RESERVED	Factory set to 1 to mask reserved bit from causing an interrupt. Do not clear this bit.

These are the interrupt mask bits for the fault flags in register 0x0011. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Note: Bit 1 corresponds to XAXB LOS from asserting the interrupt (INTR) pin.

Table 16.19. 0x0018 OOF and LOS Masks

Reg Address	Bit Field	Type	Name	Description
0x0018	3:0	R/W	LOS_INTR_MSK	1 to mask the clock input LOS flag
0x0018	7:4	R/W	OOF_INTR_MSK	1 to mask the clock input OOF flag

These are the interrupt mask bits for the OOF and LOS flags in register 0x0012.

Input 0 (IN0) corresponds to LOS_INTR_MSK 0x0018 [0], OOF_INTR_MSK 0x0018 [4]

Input 1 (IN1) corresponds to LOS_INTR_MSK 0x0018 [1], OOF_INTR_MSK 0x0018 [5]

Input 2 (IN2) corresponds to LOS_INTR_MSK 0x0018 [2], OOF_INTR_MSK 0x0018 [6]

Input 3 (IN3) corresponds to LOS_INTR_MSK 0x0018 [3], OOF_INTR_MSK 0x0018 [7]

Table 16.20. 0x0019 Holdover and LOL Masks

Reg Address	Bit Field	Type	Name	Description
0x0019	1	R/W	LOL_INTR_MSK	1 to mask the clock input LOL flag
0x0019	5	R/W	HOLD_INTR_MSK	1 to mask the holdover flag

These are the interrupt mask bits for the LOL and HOLD flags in register 0x0013. If a mask bit is set the alarm will be blocked from causing an interrupt.

Table 16.21. 0x001A PLL In Calibration Interrupt Mask

Reg Address	Bit Field	Type	Name	Description
0x001A	5	R/W	CAL_INTR_MSK	1 to mask the DSPLL internal calibration busy flag

The interrupt mask for this bit flag bit corresponds to register 0x0014.

Table 16.22. 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Name	Description
0x001C	0	S	SOFT_RST_ALL	1 Initialize and calibrates the entire device 0 No effect
0x001C	2	S	SOFT_RST	1 Initialize outer loop 0 No effect

These bits are of type “S”, which is self-clearing.

Table 16.23. 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Name	Description
0x001D	0	S	FINC	1 a rising edge will cause the selected MultiSynth to increment the output frequency by the Nx_FSTEPW parameter. See registers 0x0339–0x0358
0x001D	1	S	FDEC	1 a rising edge will cause the selected MultiSynth to decrement the output frequency by the Nx_FSTEPW parameter. See registers 0x0339–0x0358

Figure 16.1 FINC, FDEC Logic Diagram on page 101 shows the logic for the FINC, FDEC bits.

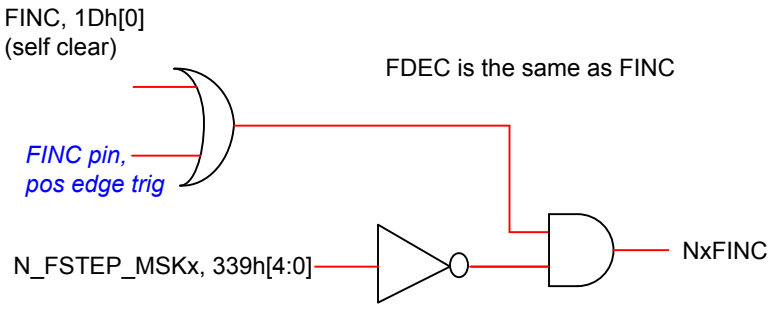


Figure 16.1. FINC, FDEC Logic Diagram

Table 16.24. 0x001E Power Down and Hard Reset

Reg Address	Bit Field	Type	Name	Description
0x001E	0	R/W	PDN	1 to put the device into low-power mode
0x001E	1	R/W	HARD_RST	1 causes hard reset. The same as power up except that the serial port access is not held at reset. 0 No reset
0x001E	2	S	SYNC	1 to reset all output R dividers to the same state.

Table 16.25. 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Name	Description
0x002B	3	R/W	SPI_3WIRE	0 for 4-wire SPI, 1 for 3-wire SPI
0x002B	5	R/W	AUTO_NDIV_UPDATE	Set by CBPro.

Table 16.26. 0x002C LOS Enable

Reg Address	Bit Field	Type	Name	Description
0x002C	3:0	R/W	LOS_EN	1 to enable LOS for a clock input; 0 for disable
0x002C	4	R/W	LOSXAXB_DIS	Enable LOS detection on the XAXB inputs. 0: Enable LOS Detection (default) 1: Disable LOS Detection

Input 0 (IN0): LOS_EN[0]

Input 1 (IN1): LOS_EN[1]

Input 2 (IN2): LOS_EN[2]

Input 3 (IN3): LOS_EN[3]

Table 16.27. 0x002D Loss of Signal Requalification Value

Reg Address	Bit Field	Type	Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0 for 2 msec 1 for 100 msec 2 for 200 msec 3 for one second
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above
0x002D	5:4	R/W	LOS2_VAL_TIME	Clock Input 2, same as above
0x002D	7:6	R/W	LOS3_VAL_TIME	Clock Input 3, same as above

When an input clock is gone (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Table 16.28. 0x002E-0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit Threshold Value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

Table 16.29. 0x0030-0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	16-bit Threshold Value
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Table 16.30. 0x0032-0x0033 LOS2 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x0032	7:0	R/W	LOS2_TRG_THR	16-bit Threshold Value
0x0033	15:8	R/W	LOS2_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 2, given a particular frequency plan.

Table 16.31. 0x0034-0x0035 LOS3 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x0034	7:0	R/W	LOS3_TRG_THR	16-bit Threshold Value
0x0035	15:8	R/W	LOS3_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 3, given a particular frequency plan.

Table 16.32. 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	16-bit Threshold Value
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 0, given a particular frequency plan.

Table 16.33. 0x0038-0x0039 LOS1 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0038	7:0	R/W	LOS1_CLR_THR	16-bit Threshold Value
0x0039	15:8	R/W	LOS1_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 1, given a particular frequency plan.

Table 16.34. 0x003A-0x003B LOS2 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x003A	7:0	R/W	LOS2_CLR_THR	16-bit Threshold Value
0x003B	15:8	R/W	LOS2_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 2, given a particular frequency plan.

Table 16.35. 0x003C-0x003D LOS3 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x003C	7:0	R/W	LOS3_CLR_THR	16-bit Threshold Value
0x003D	15:8	R/W	LOS3_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 3, given a particular frequency plan.

Table 16.36. 0x003E LOS_MIN_PERIOD_EN

Reg Address	Bit Field	Type	Name	Description
0x003E	7:4	R/W	LOS_MIN_PERIOD_EN	Set by CBPro

Table 16.37. 0x003F OOF Enable

Reg Address	Bit Field	Type	Name	Description
0x003F	3:0	R/W	OOF_EN	1 to enable, 0 to disable
0x003F	7:4	R/W	FAST_OOF_EN	1 to enable, 0 to disable

Input 0 corresponds to OOF_EN [0], FAST_OOF_EN [4]

Input 1 corresponds to OOF_EN [1], FAST_OOF_EN [5]

Input 2 corresponds to OOF_EN [2], FAST_OOF_EN [6]

Input 3 corresponds to OOF_EN [3], FAST_OOF_EN [7]

Table 16.38. 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	0 for CLKIN0 1 for CLKIN1 2 for CLKIN2 3 for CLKIN3 4 for XAXB

Table 16.39. 0x0041-0x0045 OOF Divider Select

Reg Address	Bit Field	Type	Name	Description
0x0041	4:0	R/W	OOF0_DIV_SEL	Sets a divider for the OOF circuitry for each input clock 0,1,2,3. The divider value is $2^{OOFx\_DIV\_SEL}$. CBPro sets these dividers.
0x0042	4:0	R/W	OOF1_DIV_SEL	
0x0043	4:0	R/W	OOF2_DIV_SEL	
0x0044	4:0	R/W	OOF3_DIV_SEL	
0x0045	4:0	R/W	OOFXO_DIV_SEL	

Table 16.40. 0x0046-0x0049 Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	OOF Set threshold. Range is up to ±500 ppm in steps of 1/16 ppm.
0x0047	7:0	R/W	OOF1_SET_THR	OOF Set threshold. Range is up to ±500 ppm in steps of 1/16 ppm.
0x0048	7:0	R/W	OOF2_SET_THR	OOF Set threshold. Range is up to ±500 ppm in steps of 1/16 ppm.
0x0049	7:0	R/W	OOF3_SET_THR	OOF Set threshold. Range is up to ±500 ppm in steps of 1/16 ppm.

Table 16.41. 0x004A-0x004D Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	OOF Clear threshold. Range is up to ±500 ppm in steps of 1/16 ppm.
0x004B	7:0	R/W	OOF1_CLR_THR	OOF Clear threshold. Range is up to ±500 ppm in steps of 1/16 ppm.
0x004C	7:0	R/W	OOF2_CLR_THR	OOF Clear threshold. Range is up to ±500 ppm in steps of 1/16 ppm.
0x004D	7:0	R/W	OOF3_CLR_THR	OOF Clear threshold. Range is up to ±500 ppm in steps of 1/16 ppm.

Table 16.42. 0x004E-0x04F OOF Detection Windows

Reg Address	Bit Field	Type	Setting Name	Description
0x004E	2:0	R/W	OOF0_DETWIN_SEL	Values calculated by CBPro
0x004E	6:4	R/W	OOF1_DETWIN_SEL	
0x004F	2:0	R/W	OOF2_DETWIN_SEL	
0x004F	6:4	R/W	OOF3_DETWIN_SEL	

Table 16.43. 0x0050 OOF_ON_LOS

Reg Address	Bit Field	Type	Setting Name	Description
0x0050	3:0	R/W	OOF_ON_LOS	Values set by CBPro

Table 16.44. 0x0051-0x0054 Fast OFF Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x0051	3:0	R/W	FAST_OOF0_SET_THR	(1+ value) x 1000 ppm
0x0052	3:0	R/W	FAST_OOF1_SET_THR	(1+ value) x 1000 ppm
0x0053	3:0	R/W	FAST_OOF2_SET_THR	(1+ value) x 1000 ppm
0x0054	3:0	R/W	FAST_OOF3_SET_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm set threshold for IN3, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

Table 16.45. 0x0055-0x0058 Fast OFF Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0055	3:0	R/W	FAST_OOF0_CLR_THR	(1+ value) x 1000 ppm
0x0056	3:0	R/W	FAST_OOF1_CLR_THR	(1+ value) x 1000 ppm
0x0057	3:0	R/W	FAST_OOF2_CLR_THR	(1+ value) x 1000 ppm
0x0058	3:0	R/W	FAST_OOF3_CLR_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm clear threshold for IN3, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

OOF needs a frequency reference. ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Table 16.46. 0x0059 Fast OOF Detection Window

Reg Address	Bit Field	Type	Name	Description
0x0059	1:0	R/W	FAST_OOF0_DETWIN_SEL	Values calculated by CBPro
0x0059	3:2	R/W	FAST_OOF1_DETWIN_SEL	
0x0059	5:4	R/W	FAST_OOF2_DETWIN_SEL	
0x0059	7:6	R/W	FAST_OOF3_DETWIN_SEL	

Table 16.47. 0x005A-0x005D OOF0 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x005A	7:0	R/W	OOF0_RATIO_REF	Values calculated by CBPro
0x005B	15:8	R/W	OOF0_RATIO_REF	
0x005C	23:16	R/W	OOF0_RATIO_REF	
0x005D	25:24	R/W	OOF0_RATIO_REF	

Table 16.48. 0x005E-0x0061 OOF1 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x005E	7:0	R/W	OOF1_RATIO_REF	Values calculated by CBPro
0x005F	15:8	R/W	OOF1_RATIO_REF	
0x0060	23:16	R/W	OOF1_RATIO_REF	
0x0061	25:24	R/W	OOF1_RATIO_REF	

Table 16.49. 0x0062-0x0065 OOF2 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x0062	7:0	R/W	OOF2_RATIO_REF	Values calculated by CBPro
0x0063	15:8	R/W	OOF2_RATIO_REF	
0x0064	23:16	R/W	OOF2_RATIO_REF	
0x0065	25:24	R/W	OOF2_RATIO_REF	

Table 16.50. 0x0066-0x0069 OOF3 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x0066	7:0	R/W	OOF3_RATIO_REF	Values calculated by CBPro
0x0067	15:8	R/W	OOF3_RATIO_REF	
0x0068	23:16	R/W	OOF3_RATIO_REF	
0x0069	25:24	R/W	OOF3_RATIO_REF	

Table 16.51. 0x0092 Fast LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x0092	1	R/W	LOL_FST_EN	Enables fast detection of LOL. A large input frequency error will quickly assert LOL when this is enabled.

Table 16.52. 0x0093 Fast LOL Detection Window

Reg Address	Bit Field	Type	Name	Description
0x0093	7:4	R/W	LOL_FST_DETWIN_SEL	Values calculated by CBPro

Table 16.53. 0x0095 Fast LOL Detection Value

Reg Address	Bit Field	Type	Name	Description
0x0095	3:2	R/W	LOL_FST_VALWIN_SEL	Values calculated by CBPro

Table 16.54. 0x0096 Fast LOL Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x0096	7:4	R/W	LOL_FST_SET_THR_SEL	Values calculated by CBPro

Table 16.55. 0x0098 Fast LOL Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0098	7:4	R/W	LOL_FST_CLR_THR_SEL	Values calculated by CBPro

Table 16.56. 0x009A LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x009A	1	R/W	LOL_SLOW_EN_PLL	1 to enable LOL; 0 to disable LOL.

ClockBuilder Pro provides the LOL register values for a particular frequency plan.

Table 16.57. 0x009B Slow LOL Detection Window

Reg Address	Bit Field	Type	Name	Description
0x009B	7:4	R/W	LOL_SLW_DETWIN_SEL	Values calculated by CBPro

Table 16.58. 0x009D Slow LOL Detection Value

Reg Address	Bit Field	Type	Setting Name	Description
0x009D	3:2	R/W	LOL_SLW_VALWIN_SEL	Values calculated by CBPro

Table 16.59. 0x009E LOL Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x009E	7:4	R/W	LOL_SLW_SET_THR	Configures the loss of lock set thresholds. Selectable as 0.1, 0.3, 1, 3, 10, 30, 100, 300, 1000, 3000, 10000. Values are in ppm.

The following are the thresholds for the value that is placed in the top four bits of register 0x009E.

0 = 0.1 ppm

1 = 0.3 ppm

2 = 1 ppm

3 = 3 ppm

4 = 10 ppm

5 = 30 ppm

6 = 100 ppm

7 = 300 ppm

8 = 1000 ppm

9 = 3000 ppm

10 = 10000 ppm

Table 16.60. 0x00A0 LOL Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x00A0	7:4	R/W	LOL_SLW_CLR_THR	Configures the loss of lock set thresholds. Selectable as 0.1, 0.3, 1, 3, 10, 30, 100, 300, 1000, 3000, 10000. Values are in ppm.

The following are the thresholds for the value that is placed in the top four bits of register 0x00A0. ClockBuilder Pro™ sets these values.

0 = 0.1 ppm

1 = 0.3 ppm

2 = 1 ppm

3 = 3 ppm

4 = 10 ppm

5 = 30 ppm

6 = 100 ppm

7 = 300 ppm

8 = 1000 ppm

9 = 3000 ppm

10 = 10000 ppm

Table 16.61. 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Name	Description
0x00A2	1	R/W	LOL_TIMER_EN	0 to disable 1 to enable

Table 16.62. 0x00A9-0x00AC LOL_CLR_DELAY_DIV256

Reg Address	Bit Field	Type	Name	Description
0x00A9	7:0	R/W	LOL_CLR_DELAY_DIV256	Set by CBPro.
0x00AA	15:8	R/W	LOL_CLR_DELAY_DIV256	Set by CBPro.
0x00AB	23:16	R/W	LOL_CLR_DELAY_DIV256	Set by CBPro.
0x00AC	28:24	R/W	LOL_CLR_DELAY_DIV256	Set by CBPro.

Table 16.63. 0x00E2

Reg Address	Bit Field	Type	Name	Description
0x00E2	7:0	R	ACTIVE_NVM_BANK	Read-only field indicating number of user bank writes carried out so far. Value Description 0 zero 3 one 15 two 63 three

Table 16.64. 0x00E3

Reg Address	Bit Field	Type	Setting Name	Description
0x00E3	7:0	R/W	NVM_WRITE	Write 0xC7 to initiate an NVM bank burn.

Table 16.65. 0x00E4

Reg Address	Bit Field	Type	Setting Name	Description
0x00E4	0	S	NVM_READ_BANK	When set, this bit will read the NVM down into the volatile memory.

Table 16.66. 0x00E5 Fastlock Extend Enable

Reg Address	Bit Field	Type	Name	Description
0x00E5	5	R/W	FASTLOCK_EXTEND_EN	Extend Fastlock bandwidth period past LOL Clear 0: Do not extend Fastlock period 1: Extend Fastlock period (default)

Table 16.67. 0x00EA-0x00ED FASTLOCK EXTEND

Reg Address	Bit Field	Type	Name	Description
0x00EA	7:0	R/W	FASTLOCK_EXTEND	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL.
0x00EB	15:8	R/W	FASTLOCK_EXTEND	
0x00EC	23:16	R/W	FASTLOCK_EXTEND	
0x00ED	28:24	R/W	FASTLOCK_EXTEND	

Table 16.68. 0x00F6

Reg Address	Bit Field	Type	Name	Description
0x00F6	0	R	REG_0XF7_INTR	Set by CBPro.

Reg Address	Bit Field	Type	Name	Description
0x00F6	1	R	REG_0XF8_INTR	Set by CBPro.
0x00F6	2	R	REG_0XF9_INTR	Set by CBPro.

Table 16.69. 0x00F7

Reg Address	Bit Field	Type	Name	Description
0x00F7	0	R	SYSINCAL_INTR	Set by CBPro.
0x00F7	1	R	LOSXAXB_INTR	Set by CBPro.
0x00F7	2	R	LOSREF_INTR	Set by CBPro.
0x00F7	4	R	LOSVCO_INTR	Set by CBPro.
0x00F7	5	R	SMBUS_TIME_OUT_INTR	Set by CBPro.

Table 16.70. 0x00F8

Reg Address	Bit Field	Type	Name	Description
0x00F8	3:0	R	LOS_INTR	Set by CBPro.
0x00F8	7:4	R	OOF_INTR	Set by CBPro.

Table 16.71. 0x00F9

Reg Address	Bit Field	Type	Name	Description
0x00F9	1	R	LOL_INTR	Set by CBPro.
0x00F9	5	R	HOLD_INTR	Set by CBPro.

Table 16.72. 0x00FE Device Ready

Reg Address	Bit Field	Type	Name	Description
0x00FE	7:0	R	DEVICE_READY	Ready Only byte to indicate device is ready. When read data is 0x0F one can safely read/write registers. This register is repeated on every page therefore a page write is not ever required to read the DEVICE_READY status.

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Table 16.73. 0x0102 Global OE Gating for all Clock Output Drivers

Reg Address	Bit Field	Type	Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	1 Pass through the output enables, 0 disables all output drivers

Table 16.74. Register 0x0103 OUT0A Output Enable and R0A Divider Configuration

Reg Address	Bit Field	Type	Name	Description
0x0103	0	R/W	OUT0A_PDN	Powerdown output driver. 0: Normal Operation (default) 1: Powerdown output driver When powered down, outputs pins will be high impedance with a light pull down effect.
0x0103	1	R/W	OUT0A_OE	Enable/Disable individual output. 0: Disable output (default) 1: Enable output
0x0103	2	R/W	OUT0A_RDIV_FORCE	Force R0A output divider divide-by-2. 0: R0A_REG sets divide value (default) 1: Divide value forced to divide-by-2

Setting R0A_REG=0 will not set the divide value to divide-by-2 automatically. OUT0A_RDIV_FORCE must be set to a value of 1 to force R0A to divide-by-2. Note that the R0A_REG value will be ignored while OUT0A_RDIV_FORCE=1. See R0A_REG registers, 0x0247-0x0249, for more information.

Table 16.75. Register 0x0104 OUT0A Output Format and Configuration

Reg Address	Bit Field	Type	Name	Description
0x0104	2:0	R/W	OUT0A_FORMAT	Select output format. 0: Reserved 1: Differential Normal mode 2: Differential Low-Power mode 3: Reserved 4: LVCMOS single ended 5–7: Reserved

Reg Address	Bit Field	Type	Name	Description
0x0104	3	R/W	OUT0A_SYNC_EN	Synchronous Enable/ Disable selection. 0: Asynchronous Enable/ Disable (default) 1: Synchronous Enable/ Disable (Glitchless)
0x0104	5:4	R/W	OUT0A_DIS_STATE	Determines the logic state of the output driver when disabled: 0: Disable logic Low 1: Disable logic High 2-3: Reserved
0x0104	7:6	R/W	OUT0A_CMOS_DRV	LVCMOS output impedance selection. See 6.3.5 LVCMOS Output Impedance and Drive Strength Selectionfor valid selections.

Table 16.76. Register 0x0105 Output OUT0A Differential Amplitude and Common Mode

Reg Address	Bit Field	Type	Name	Description
0x0105	3:0	R/W	OUT0A_CM	OUT0A Common Mode Voltage selection. Only applies when OUT0A_FORMAT=1 or 2.
0x0105	6:4	R/W	OUT0A_AMPL	OUT0A Differential Amplitude setting. Only applies when OUT0A_FORMAT=1 or 2.

ClockBuilder Pro is used to select the correct settings for this register. See 6.3.9 Setting the Differential Output Driver to Non-Standard Amplitudes for details of the settings.

Table 16.77. Register 0x0106 Output OUT0A Source, VDD Select, and LVCMOS Inversion

Reg Address	Bit Field	Type	Name	Description
0x0106	2:0	R/W	OUT0A_MUX_SEL	OUT0A output source divider select. 0: N0 is the source for OUT0A 1: N1 is the source for OUT0A 2: N2 is the source for OUT0A 3: N3 is the source for OUT0A 4: N4 is the source for OUT0A 5-7: Reserved
0x0106	3	R/W	OUT0A_VDD_SEL_EN	Output Driver VDD Select Enable. Set to 1 for normal operation.

Reg Address	Bit Field	Type	Name	Description
0x0106	5:4	R/W	OUT0A_VDD_SEL	Output Driver VDD Select 0: 1.8 V 1: 2.5 V 2, 3: 3.3 V
0x0106	7:6	R/W	OUT0A_INV	OUT0A output LVCMOS inversion. Only applies when OUT0A_FORMAT= 4. See 6.3.7 LVCMOS Output Polarity for more information.

Each output can be independently configured to use one of the N0-N4 divider outputs as its source. Nx_NUM and Nx_DEN for each N-divider are set in registers 0x0302-0x0337 for N0 to N4. Five different frequencies can be set in the N-dividers (N0-N4) and each of the 12 outputs can be configured to use any of the five different frequencies.

All 12 output drivers are identical in terms of control. The single set of descriptions above for OUT0A also applies to OUT0-OUT9A:

Table 16.78. Output Registers Following the Same Definitions as OUT0A

Register Address	Description	(Same as) Address
0x0108	OUT0 Powerdown, Output Enable, and R0 Divide-by-2	0x0103
0x0109	OUT0 Signal Format and Configuration	0x0104
0x010A	OUT0 Differential Amplitude and Common Mode	0x0105
0x010B	OUT0 Source Selection and LVCMOS Inversion	0x0106
0x010D	OUT1 Powerdown, Output Enable, and R1 Divide-by-2	0x0103
0x010E	OUT1 Signal Format and Configuration	0x0104
0x010F	OUT1 Differential Amplitude and Common Mode	0x0105
0x0110	OUT1 Source Selection and LVCMOS Inversion	0x0106
0x0112	OUT2 Powerdown, Output Enable, and R2 Divide-by-2	0x0103
0x0113	OUT2 Signal Format and Configuration	0x0104
0x0114	OUT2 Differential Amplitude and Common Mode	0x0105
0x0115	OUT2 Source Selection and LVCMOS Inversion	0x0106
0x0117	OUT3 Powerdown, Output Enable, and R3 Divide-by-2	0x0103
0x0118	OUT3 Signal Format and Configuration	0x0104
0x0119	OUT3 Differential Amplitude and Common Mode	0x0105

Register Address	Description	(Same as) Address
0x011A	OUT3 Source Selection and LVCMOS Inversion	0x0106
0x011C	OUT4 Powerdown, Output Enable, and R4 Divide-by-2	0x0103
0x011D	OUT4 Signal Format and Configuration	0x0104
0x011E	OUT4 Differential Amplitude and Common Mode	0x0105
0x011F	OUT4 Source Selection and LVCMOS Inversion	0x0106
0x0121	OUT5 Powerdown, Output Enable, and R5 Divide-by-2	0x0103
0x0122	OUT5 Signal Format and Configuration	0x0104
0x0123	OUT5 Differential Amplitude and Common Mode	0x0105
0x0124	OUT5 Source Selection and LVCMOS Inversion	0x0106
0x0126	OUT6 Powerdown, Output Enable, and R6 Divide-by-2	0x0103
0x0127	OUT6 Signal Format and Configuration	0x0104
0x0128	OUT6 Differential Amplitude and Common Mode	0x0105
0x0129	OUT6 Source Selection and LVCMOS Inversion	0x0106
0x012B	OUT7 Powerdown, Output Enable, and R7 Divide-by-2	0x0103
0x012C	OUT7 Signal Format and Configuration	0x0104
0x012D	OUT7 Differential Amplitude and Common Mode	0x0105
0x012E	OUT7 Source Selection and LVCMOS Inversion	0x0106
0x0130	OUT8 Powerdown, Output Enable, and R8 Divide-by-2	0x0103
0x0131	OUT8 Signal Format and Configuration	0x0104
0x0132	OUT8 Differential Amplitude and Common Mode	0x0105
0x0133	OUT8 Source Selection and LVCMOS Inversion	0x0106
0x0135	OUT9 Powerdown, Output Enable, and R9 Divide-by-2	0x0103
0x0136	OUT9 Signal Format and Configuration	0x0104

Register Address	Description	(Same as) Address
0x0137	OUT9 Differential Amplitude and Common Mode	0x0105
0x0138	OUT9 Source Selection and LVCMOS Inversion	0x0106
0x013A	OUT9A Powerdown, Output Enable, and R9A Divide-by-2	0x0103
0x013B	OUT9A Signal Format and Configu-ration	0x0104
0x013C	OUT9A Differential Amplitude and Common Mode	0x0105
0x013D	OUT9A Source Selection and LVCMOS Inversion	0x0106

Table 16.79. 0x013F-0x0140

Reg Address	Bit Field	Type	Setting Name	Description
0x013F	7:0	R/W	OUTX_ALWAYS_ON	This setting is managed by CBPro during zero delay mode.
0x0140	11:8	R/W	OUTX_ALWAYS_ON	

Table 16.80. 0x0141 Output Disable Mask for LOS XAXB

Reg Address	Bit Field	Type	Setting Name	Description
0x0141	1	R/W	OUT_DIS_MSK	Set by CBPro.
0x0141	5	R/W	OUT_DIS_LOL_MSK	Set by CBPro.
0x0141	6	R/W	OUT_DIS_LOSXAXB_MSK	Determines if outputs are disabled during an LOSXAXB condition. 0: All outputs disabled on LOSXAXB 1: All outputs remain enabled during LOSXAXB condition
0x0141	7	R/W	OUT_DIS_MSK_LOS_PFD	Set by CBPro.

Table 16.81. 0x0142 Output Disable Loss of Lock PLL

Reg Address	Bit Field	Type	Setting Name	Description
0x0142	1	R/W	OUT_DIS_MSK_LOL	0: LOL will disable all connected out-puts 1: LOL does not disable any outputs
0x0142	5	R/W	OUT_DIS_MSK_HOLD	Set by CBPro.

Table 16.82. 0x0145 Power Down All

Reg Address	Bit Field	Type	Name	Description
0x0145	0	R/W	OUT_PDN_ALL	0- no effect 1- all drivers powered down

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Table 16.83. 0x0206 Pre-Scale Reference Divide Ratio

Reg Address	Bit Field	Type	Name	Description
0x0206	1:0	R/W	PXAXB	Sets the prescale divider for the input clock on XAXB.

0 = pre-scale value 1

1 = pre-scale value 2

2 = pre-scale value 4

3 = pre-scale value 8

This can only be used with external clock sources, not crystals.

Table 16.84. 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Name	Description
0x0208	7:0	R/W	P0_NUM	48-bit Integer Number
0x0209	15:8	R/W	P0_NUM	
0x020A	23:16	R/W	P0_NUM	
0x020B	31:24	R/W	P0_NUM	
0x020C	39:32	R/W	P0_NUM	
0x020D	47:40	R/W	P0_NUM	

This set of registers configures the P-dividers which are located at the four input clocks seen in Section 3. DSPLL and MultiSynth. ClockBuilder Pro calculates the correct values for the P-dividers.

Table 16.85. 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Name	Description
0x020E	7:0	R/W	P0_DEN	32-bit Integer Number
0x020F	15:8	R/W	P0_DEN	
0x0210	23:16	R/W	P0_DEN	
0x0211	31:24	R/W	P0_DEN	

The P1, P2 and P3 divider numerator and denominator follow the same format as P0 described above. ClockBuilder Pro calculates the correct values for the P-dividers.

Table 16.86. Registers that Follow the P0_NUM and P0_DEN Above

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1 Divider Denominator	32-bit Integer Number	0x020E-0x0211
0x021C-0x0221	P2 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0222-0x0225	P2 Divider Denominator	32-bit Integer Number	0x020E-0x0211
0x0226-0x022B	P3 Divider Numerator	48-bit Integer Number	0x0208-0x020D

Register Address	Description	Size	Same as Address
0x022C-0x022F	P3 Divider Denominator	32-bit Integer Number	0x020E-0x0211

This set of registers configure the P-dividers which are located at the four input clocks seen in Section 3. DSPLL and MultiSynth. ClockBuilder Pro calculates the correct values for the P-dividers. The Px_Update bit (register 0x0230) for the appropriate channel must be updated for the new P value to take affect.

Table 16.87. 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Name	Description
0x0230	0	S	P0_UPDATE	0 - No update for P-divider value 1 - Update P-divider value
0x0230	1	S	P1_UPDATE	
0x0230	2	S	P2_UPDATE	
0x0230	3	S	P3_UPDATE	

The Px_Update bit must be asserted to update the P-Divider. The update bits are provided so that all of the divider bits can be changed at the same time. First, write all of the new values to the divider, then set the update bit.

Table 16.88. 0x0231 P0 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0231	3:0	R/W	P0_FRACN_MODE	P0 (IN0) input divider fractional mode. Must be set to 0xB for proper operation.
0x0231	4	R/W	P0_FRAC_EN	P0 (IN0) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 16.89. 0x0232 P1 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0232	3:0	R/W	P1_FRACN_MODE	P1 (IN1) input divider fractional mode. Must be set to 0xB for proper operation.
0x0232	4	R/W	P1_FRAC_EN	P1 (IN1) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 16.90. 0x0233 P2 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0233	3:0	R/W	P2_FRACN_MODE	P2 (IN2) input divider fractional mode. Must be set to 0xB for proper operation.
0x0233	4	R/W	P2_FRAC_EN	P2 (IN2) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 16.91. 0x0234 P3 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0234	3:0	R/W	P3_FRACN_MODE	P3 (IN3) input divider fractional mode. Must be set to 0xB for proper operation.
0x0234	4	R/W	P3_FRAC_EN	P3 (IN3) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 16.92. 0x0235-0x023A MXAXB Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0235	7:0	R/W	MXAXB_NUM	44-bit Integer Number
0x0236	15:8	R/W	MXAXB_NUM	
0x0237	23:16	R/W	MXAXB_NUM	
0x0238	31:24	R/W	MXAXB_NUM	
0x0239	39:32	R/W	MXAXB_NUM	
0x023A	43:40	R/W	MXAXB_NUM	

Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in Section 4.2 Dynamic PLL Changes are followed.

Table 16.93. 0x023B-0x023E MXAXB Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x023B	7:0	R/W	MXAXB_DEN	32-bit Integer Number
0x023C	15:8	R/W	MXAXB_DEN	
0x023D	23:16	R/W	MXAXB_DEN	
0x023E	31:24	R/W	MXAXB_DEN	

The M-divider numerator and denominator are set by ClockBuilder Pro for a given frequency plan. Note that changing this register during operation may cause indefinite loss of lock unless the guidelines inSection 4.2 Dynamic PLL Changes are followed.

Table 16.94. 0x023F MXAXB Update

Reg Address	Bit Field	Type	Setting Name	Description
0x023F	0	S	MXAXB_UPDATE	Set to 1 to update the MXAXB_NUM and MXAXB_DEN values. A SOFT_RST may also be used to update these values.

Table 16.95. Register 0x0247-0x0249 R0 Divider

Reg Address	Bit Field	Type	Name	Description
0x0247	7:0	R/W	R0A_REG	24-bit integer final R0A divider selection. R Divisor = (R0A_REG+1) x 2 However, note that setting R0A_REG = 0 will not set the output to divide-by-2. See notes below.
0x0248	15:8			
0x0249	23:16			

The final output R dividers are even dividers beginning with divide-by-2. While all other values follow the formula in the bit description above, divide-by-2 requires an extra bit to be set. For divide-by-2, set OUT0_RDIV_FORCE=1. See the description for register bit 0x0103[2] in this register map.

The R0-R9A dividers follow the same format as the R0A divider description above.

Table 16.96. Registers that Follow the R0A_REG

Register Address	Description	Size	Same as Address
0x024A-0x024C	R0_REG	24-bit Integer Number	0x0247-0x0249
0x024D-0x024F	R1_REG	24-bit Integer Number	0x0247-0x0249
0x0250-0x0252	R2_REG	24-bit Integer Number	0x0247-0x0249
0x0253-0x0255	R3_REG	24-bit Integer Number	0x0247-0x0249
0x0256-0x0258	R4_REG	24-bit Integer Number	0x0247-0x0249
0x0259-0x025B	R5_REG	24-bit Integer Number	0x0247-0x0249
0x025C-0x025E	R6_REG	24-bit Integer Number	0x0247-0x0249
0x025F-0x0261	R7_REG	24-bit Integer Number	0x0247-0x0249
0x0262-0x0264	R8_REG	24-bit Integer Number	0x0247-0x0249
0x0265-0x0267	R9_REG	24-bit Integer Number	0x0247-0x0249
0x0268-0x026A	R9A_REG	24-bit Integer Number	0x0247-0x0249

Table 16.97. 0x026B–0x0272 User Scratch Pad

Reg Address	Bit Field	Type	Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by CBPro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, “ULT.1A” with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6:0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Table 16.98. 0x0278–0x027C OPN Identifier

Reg Address	Bit Field	Type	Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: 5395C-A12345-GM, 12345 is the OPN unique identifier, which sets: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5395C-A12345-GM.

Applies to a “custom” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5395C-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5395 but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 16.99. 0x027D

Reg Address	Bit Field	Type	Setting Name	Description
0x027D	7:0	R/W	OPN_REVISION	

Table 16.100. 0x027E

Reg Address	Bit Field	Type	Setting Name	Description
0x027E	7:0	R/W	BASELINE_ID	

Table 16.101. 0x028A-0x028D OOFx_TRG_THR_EXT

Reg Address	Bit Field	Type	Name	Description
0x028A	4:0	R/W	OOF0_TRG_THR_EXT	Set by CBPro.
0x028B	4:0	R/W	OOF1_TRG_THR_EXT	Set by CBPro.
0x028C	4:0	R/W	OOF2_TRG_THR_EXT	Set by CBPro.
0x028D	4:0	R/W	OOF3_TRG_THR_EXT	Set by CBPro.

Table 16.102. 0x028E-0x0291 OOFx_CLR_THR_EXT

Reg Address	Bit Field	Type	Name	Description
0x028E	4:0	R/W	OOF0_TRG_THR_EXT	Set by CBPro.
0x028F	4:0	R/W	OOF1_TRG_THR_EXT	Set by CBPro.
0x0290	4:0	R/W	OOF2_TRG_THR_EXT	Set by CBPro.
0x0291	4:0	R/W	OOF3_TRG_THR_EXT	Set by CBPro.

Table 16.103. 0x0292 OOF_STOP_ON_LOS

Reg Address	Bit Field	Type	Name	Description
0x0292	3:0	R/W	OOF_STOP_ON_LOS	Set by CBPro

Table 16.104. 0x0293 OOF_CLEAR_ON_LOS

Reg Address	Bit Field	Type	Name	Description
0x0293	3:0	R/W	OOF_CLEAR_ON_LOS	Set by CBPro

Table 16.105. 0x0294 Fastlock Extend Scale

Reg Address	Bit Field	Type	Name	Description
0x0294	7:4	R/W	FASTLOCK_EXTEND_SCL	Scales LOLB_INT_TIMER_DIV256. Set by CBPro

Table 16.106. 0x0296

Reg Address	Bit Field	Type	Name	Description
0x0296	1	R/W	LOL_SLW_VALWIN_SELX	Set by CBPro.

Table 16.107. 0x0297 Fastlock Delay on Input Switch Enable

Reg Address	Bit Field	Type	Name	Description
0x0297	1	R/W	FASTLOCK_DLY_ONSW_EN	Set by CBPro.

Table 16.108. 0x0299 Fastlock Delay on LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x0299	1	R/W	FASTLOCK_DLY_ONLOL_EN	Set by CBPro.

Table 16.109. 0x029D-0x029F Fastlock Delay on LOL

Reg Address	Bit Field	Type	Name	Description
0x029D	7:0	R/W	FASTLOCK_DLY_ONLOL	Set by CBPro.
0x029E	15:8	R/W	FASTLOCK_DLY_ONLOL	Set by CBPro.
0x029F	19:16	R/W	FASTLOCK_DLY_ONLOL	Set by CBPro.

Table 16.110. 0x02A9-0x02AB Fastlock Delay on Input Switch

Reg Address	Bit Field	Type	Name	Description
0x02A9	7:0	R/W	FASTLOCK_DLY_ONSW	20-bit value. Set by CBPro.
0x02AA	15:8	R/W	FASTLOCK_DLY_ONSW	
0x02AB	19:16	R/W	FASTLOCK_DLY_ONSW	

Table 16.111. 0x02B7 LOL Delay from LOS

Reg Address	Bit Field	Type	Name	Description
0x02B7	3:2	R/W	LOL_NOSIG_TIME	Set by CBPro.

Table 16.112. 0x02B8

Reg Address	Bit Field	Type	Name	Description
0x02B8	1	R/W	LOL_LOS_REFCLK	Set by CBPro.

Table 16.113. 0x02BC LOS_CMOS_MIN_PER_EN

Reg Address	Bit Field	Type	Name	Description
0x02BC	7:6	R/W	LOS_CMOS_MIN_PER_EN	Set by CBPro.

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Table 16.114. 0x0302-0x0307 N0 Numerator

Reg Address	Bit Field	Type	Name	Description
0x0302	7:0	R/W	N0_NUM	48-bit Integer Number
0x0303	15:8	R/W	N0_NUM	
0x0304	23:16	R/W	N0_NUM	
0x0305	31:24	R/W	N0_NUM	
0x0306	39:32	R/W	N0_NUM	
0x0307	43:40	R/W	N0_NUM	

The N dividers are interpolative dividers that are used as output dividers that feed into the R dividers. ClockBuilder Pro calculates the correct values for the N-dividers.

Table 16.115. 0x0308–0x030C N0 Denominator

Reg Address	Bit Field	Type	Name	Description
0x0308	7:0	R/W	N0_DEN	32-bit Integer Number
0x0309	15:8	R/W	N0_DEN	
0x030A	23:16	R/W	N0_DEN	
0x030B	31:24	R/W	N0_DEN	
0x030C	0	S	N0_UPDATE	Set this bit to update the N0 divider.

This bit is provided so that all of the N0 divider bits can be changed at the same time. First, write all of the new values to the divider; then, set the update bit.

Table 16.116. Registers that Follow the N0_NUM and N0_DEN Definitions

Register Address	Description	Size	Same as Address
0x030D-0x0312	N1 Numerator	44-bit Integer Number	0x0302-0x0307
0x0313-0x0316	N1 Denominator	32-bit Integer Number	0x0308-0x030B
0x0317	N1_UPDATE	one bit	0x030C
0x0318-0x031D	N2 Numerator	44-bit Integer Number	0x0302-0x0307
0x031E-0x0321	N2 Denominator	32-bit Integer Number	0x0308-0x030B
0x0322	N2_UPDATE	one bit	0x030C
0x0323-0x0328	N3 Numerator	44-bit Integer Number	0x0302-0x0307
0x0329-0x032C	N3 Denominator	32-bit Integer Number	0x0308-0x030B
0x032D	N3_UPDATE	one bit	0x030C
0x032E-0x0333	N4 Numerator	44-bit Integer Number	0x0302-0x0307
0x0334-0x0337	N4 Denominator	32-bit Integer Number	0x0308-0x030B

Table 16.117. 0x0338 N4 and Global N Divider Update

Reg Address	Bit Field	Type	Name	Description
0x0338	1	S	N_UPDATE_ALL	Set this bit to update all five N dividers.
0x0338	0	S	N4_UPDATE	Set this bit to update N4 divider.

This bit is provided so that all of the divider bits can be changed at the same time. First, write all of the new values to the divider, then set the update bit.

Note: If the intent is to write to the N_UPDATE_ALL to have all dividers update at the same time, then make sure only bit 1 N_UPDATE_ALL bit gets set.

Table 16.118. 0x0339 FINC/FDEC Masks

Reg Address	Bit Field	Type	Name	Description
0x0339	4:0	R/W	N_FSTEP_MSK	0 to enable FINC/FDEC updates 1 to disable FINC/FDEC updates

Bit 0 corresponds to MultiSynth N0 N_FSTEP_MSK 0x0339[0]

Bit 1 corresponds to MultiSynth N1 N_FSTEP_MSK 0x0339[1]

Bit 2 corresponds to MultiSynth N2 N_FSTEP_MSK 0x0339[2]

Bit 3 corresponds to MultiSynth N3 N_FSTEP_MSK 0x0339[3]

Bit 4 corresponds to MultiSynth N4 N_FSTEP_MSK 0x0339[4]

There is one mask bit for each of the five N dividers. Figure 16.2 Logic Diagram of the FINC/FDEC Masks on page 124 shows the logic diagram of the FINC/FDEC masks.

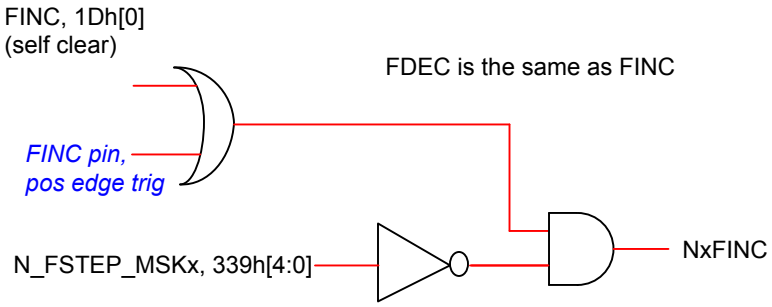

Figure 16.2. Logic Diagram of the FINC/FDEC Masks

Table 16.119. 0x033B-0x0340 N0 Frequency Step Word

Reg Address	Bit Field	Type	Name	Description
0x033B	7:0	R/W	N0_FSTEPW	44-bit Integer Number
0x033C	15:8	R/W	N0_FSTEPW	
0x033D	23:16	R/W	N0_FSTEPW	
0x033E	31:24	R/W	N0_ FSTEPW	
0x033F	39:32	R/W	N0_ FSTEPW	
0x0340	43:40	R/W	N0_ FSTEPW	

This is a 44-bit integer value which is directly added or subtracted from the N-divider when FINC or FDEC is set to a 1. ClockBuilder Pro calculates the correct values for the N0 Frequency Step Word. Each N divider has the ability to add or subtract up to a 44-bit value.

Table 16.120. Registers that Follow the N0_FSTEPW Definitions

Register Address	Description	Size	Same as Address
0x0341-0x0346	N1 Frequency Step Word	44-bit Integer Number	0x033B-0x0340
0x0347-0x034C	N2 Frequency Step Word	44-bit Integer Number	0x033B-0x0340
0x034D-0x0352	N3 Frequency Step Word	44-bit Integer Number	0x033B-0x0340
0x0353-0x0358	N4 Frequency Step Word	44-bit Integer Number	0x033B-0x0340

Table 16.121. 0x0359–0x35A N0 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x0359	7:0	R/W	N0_DELAY[7:0]	Lower byte of N0_DELAY[15:0]
0x035A	15:8	R/W	N0_DELAY[15:8]	Upper byte of N0_DELAY[15:0]

Nx_DELAY[15:0] is a 2s complement number that sets the output delay of MultiSynthx.

The delay in seconds is Nx_DELAY/(256 x Fvco) where Fvco is the VCO frequency in Hz. The maximum positive and negative delay is $\pm(2^{15}-1)/(256 \times Fvco)$. ClockBuilder Pro calculates the correct value for this register. Changing any of the Nx_DELAY values requires a SOFT_RST, a HARD_RST, or a power up sequence.

Table 16.122. 0x035B–0x035C Divider N1 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x035B	7:0	R/W	N1_DELAY[7:0]	Lower byte of N1_DELAY[15:0]
0x035C	15:8	R/W	N1_DELAY[15:8]	Upper byte of N1_DELAY[15:0]

N1_DELAY behaves in the same manner as N0_DELAY

Table 16.123. 0x035D–0x035E Divider N2 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x035D	7:0	R/W	N2_DELAY[7:0]	Lower byte of N2_DELAY[15:0]
0x035E	15:8	R/W	N2_DELAY[15:8]	Upper byte of N2_DELAY[15:0]

N2_DELAY behaves in the same manner as N0_DELAY

Table 16.124. 0x035F–0x0360 Divider N3 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x035F	7:0	R/W	N3_DELAY[7:0]	Lower byte of N3_DELAY[15:0]
0x0360	15:8	R/W	N3_DELAY[15:8]	Upper byte of N3_DELAY[15:0]

N3_DELAY behaves in the same manner as N0_DELAY

Table 16.125. 0x0361–0x0362 Divider N4 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x0361	7:0	R/W	N4_DELAY[7:0]	Lower byte of N4_DELAY[15:0]
0x0362	15:8	R/W	N4_DELAY[15:8]	Upper byte of N4_DELAY[15:0]

N4_DELAY behaves in the same manner as N0_DELAY.

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Table 16.126. 0x0487 Zero Delay Mode Setup

Reg Address	Bit Field	Type	Name	Description
0x0487	0	R/W	ZDM_EN	0 to disable ZD mode 1 to enable ZD mode
0x0487	2:1	R/W	ZDM_IN_SEL	Clock input select when in ZD mode. 0 for IN0, 1 for IN1,2 for IN2, 3 Reserved Note: In ZD mode the feedback clock comes into IN3
0x0487	4	R/W	ZDM_AUTOSW_EN	Set by CBPro.

Note: When ZDM_EN (0x0487, bit 0) and IN_SEL_REGCTRL are both high, IN_SEL does not do anything and the clock selection is register controlled using ZDM_IN_SEL at address 0x0487. When IN_SEL_REGCTRL is low, IN_SEL does not do anything and the clock selection is pin controlled.

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Table 16.127. 0x0507 Active Input

Reg Address	Bit Field	Type	Name	Description
0x0507	7:6	R	IN_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

Table 16.128. 0x0508–0x050D Loop Bandwidth

Reg Address	Bit Field	Type	Name	Description
0x0508	5:0	R/W	BW0_PLL	PLL bandwidth parameter
0x0509	5:0	R/W	BW1_PLL	PLL bandwidth parameter
0x050A	5:0	R/W	BW2_PLL	PLL bandwidth parameter
0x050B	5:0	R/W	BW3_PLL	PLL bandwidth parameter
0x050C	5:0	R/W	BW4_PLL	PLL bandwidth parameter
0x050D	5:0	R/W	BW5_PLL	PLL bandwidth parameter

This group of registers determine the loop bandwidth for the DSPLL. It is selectable as 0.1 Hz, 1 Hz, 4 Hz, 10 Hz, 40 Hz, 100 Hz, 400 Hz, 1 kHz, and 4 kHz. The loop BW values are calculated by ClockBuilder Pro and are written into these registers. The BW_UPDATE_PLL bit (reg 0x0514[0]) must be set to cause the BWx_PLL parameters to take effect.

Table 16.129. 0x050E-0x0514 Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Name	Description
0x050E	5:0	R/W	FAST_BW0_PLL	PLL fast bandwidth parameter
0x050F	5:0	R/W	FAST_BW1_PLL	PLL fast bandwidth parameter
0x0510	5:0	R/W	FAST_BW2_PLL	PLL fast bandwidth parameter
0x0511	5:0	R/W	FAST_BW3_PLL	PLL fast bandwidth parameter
0x0512	5:0	R/W	FAST_BW4_PLL	PLL fast bandwidth parameter
0x0513	5:0	R/W	FAST_BW5_PLL	PLL fast bandwidth parameter
0x0514	0	S	BW_UPDATE_PLL	Must be set to 1 to update the BWx_PLL and FAST_BWx_PLL parameters

The fast lock loop BW values are calculated by ClockBuilder Pro and used when fast lock is enabled.

Table 16.130. 0x0515-0x051B M Divider Numerator, 56-bits

Reg Address	Bit Field	Type	Name	Description
0x0515	7:0	R/W	M_NUM	56-bit Number
0x0516	15:8	R/W	M_NUM	
0x0517	23:16	R/W	M_NUM	
0x0518	31:24	R/W	M_NUM	
0x0519	39:32	R/W	M_NUM	
0x051A	47:40	R/W	M_NUM	
0x051B	55:48	R/W	M_NUM	

Table 16.131. 0x051C-0x051F M Divider Denominator, 32-bits

Reg Address	Bit Field	Type	Name	Description
0x051C	7:0	R/W	M_DEN	32-bit Number
0x051E	15:8	R/W	M_DEN	
0x051E	23:16	R/W	M_DEN	
0x051F	31:24	R/W	M_DEN	

The loop M divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers. Note that there is a /5 prescaler before the M divider (e.g., if the M_NUM/M_DEN divide ratio is 100, the effective feedback divide ratio will be 500).

Table 16.132. 0x0520 M Divider Update Bit

Reg Address	Bit Field	Type	Name	Description
0x0520	0	S	M_UPDATE	Set this bit to update the M divider.

Table 16.133. 0x0521 DSPLL M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0521	3:0	R/W	M_FRAC_MODE	M feedback divider fractional mode. Must be set to 0xB for proper operation.
0x0521	4	R/W	M_FRAC_EN	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0521	5	R/W	Reserved	Must be set to 1

Table 16.134. 0x052A Input Clock Select

Reg Address	Bit Field	Type	Name	Description
0x052A	0	R/W	IN_SEL_REGCTRL	0 for pin controlled clock selection 1 for register controlled clock selection

Reg Address	Bit Field	Type	Name	Description
0x052A	2:1	R/W	IN_SEL	0 for IN0, 1 for IN1, 2 for IN2, 3 for IN3 (or FB_IN)

Input clock selection for manual register based and pin controlled clock selection. Note: when ZDM_EN (0x0487, bit 0) and IN_SEL_REGCTRL are both high, IN_SEL does not do anything.

Table 16.135. 0x052B Fast Lock Control

Reg Address	Bit Field	Type	Name	Description
0x052B	0	R/W	FASTLOCK_AUTO_EN	Applies only when FASTLOCK_MAN = 0 (see below): 0 to disable auto fast lock when the DSPLL is out of lock. 1 to enable auto fast lock.
0x052B	1	R/W	FASTLOCK_MAN	0 for normal operation (see above) 1 to force fast lock

When in fast lock, the fast lock loop BW can be automatically used.

Table 16.136. 0x052C Holdover Exit Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052C	0	R/W	HOLD_EN	Holdover enable 0: Holdover Disabled 1: Holdover Enabled (default)
0x052C	3	R/W	HOLD_RAMP_BYP	HOLD_RAMP_BYP
0x052C	4	R/W	HOLDEXIT_BW_SEL1	Holdover Exit Bandwidth select. Selects the exit bandwidth from Holdover when ramped exit is disabled (HOLD_RAMP_BYP = 1). 0: Exit Holdover using Holdover Exit or Fastlock bandwidths (default). See HOLDEXIT_BW_SEL0 (0x059B[6]) for additional information. 1: Exit Holdover using the Normal loop bandwidth
0x052C	7:5	R/W	RAMP_STEP_INTERVAL	Time Interval of the frequency ramp steps when ramping between inputs or when exiting holdover. Calculated by CBPro based on selection.

Table 16.137. 0x052D

Reg Address	Bit Field	Type	Name	Description
0x052D	1	R/W	HOLD_RAMPBYP_NOHIST	Set by CBPro.

Table 16.138. 0x052E Holdover History Average Length

Reg Address	Bit Field	Type	Name	Description
0x052E	4:0	R/W	HOLD_HIST_LEN	5-bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency.

time (s) = $((2^{LEN}) - 1) \times 268$ ns

Table 16.139. 0x052F Holdover History Delay

Reg Address	Bit Field	Type	Name	Description
0x052F	4:0	R/W	HOLD_HIST_DELAY	5-bit value

time(s) = $(2^{DELAY}) \times 268$ ns

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past, above the averaging window. The amount that the average window is delayed is the holdover history delay.

Table 16.140. 0x0531

Reg Address	Bit Field	Type	Setting Name	Description
0x0531	4:0	R/W	HOLD_REF_COUNT_FRC	5-bit value

Table 16.141. 0x0532–0x0534

Reg Address	Bit Field	Type	Setting Name	Description
0x0532	7:0	R/W	HOLD_15M_CYC_COUNT	Value calculated by CBPro
0x0533	15:8	R/W	HOLD_15M_CYC_COUNT	
0x0534	23:16	R/W	HOLD_15M_CYC_COUNT	

Table 16.142. 0x0535 Force Holdover

Reg Address	Bit Field	Type	Name	Description
0x0535	0	R/W	FORCE_HOLD	0 for normal operation 1 for force holdover

Table 16.143. 0x0536 Input Clock Switching Control

Reg Address	Bit Field	Type	Name	Description
0x0536	1:0	R/W	CLK_SWTCH_MODE	0 = manual 1 = automatic/non-revertive 2 = automatic/revertive 3 = reserved

Reg Address	Bit Field	Type	Name	Description
0x0536	2	R/W	HSW_EN	0 glitchless switching mode (phase buildout turned off) 1 hitless switching mode (phase buildout turned on) [1]

Note:
1. Hitless switching and zero delay mode are incompatible.

Table 16.144. 0x0537 Input Alarm Masks

Reg Address	Bit Field	Type	Name	Description
0x0537	3:0	R/W	IN_LOS_MSK	For each clock input LOS alarm: 0 to use LOS in the clock selection logic 1 to mask LOS from the clock selection logic
0x0537	7:4	R/W	IN_OOF_MSK	For each clock input OOF alarm: 0 to use OOF in the clock selection logic 1 to mask OOF from the clock selection logic

This register is for the input clock switch alarm masks. For each of the four clock inputs, the OOF and/or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

Table 16.145. 0x0538 Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Name	Description
0x0538	2:0	R/W	IN0_PRIORITY	The priority for clock input 0 is: 0 no priority 1 for priority 1 2 for priority 2 3 for priority 3 4 for priority 4 5 to 7 are reserved
0x0538	6:4	R/W	IN1_PRIORITY	The priority for clock input 1 is: 0 no priority 1 for priority 1 2 for priority 2 3 for priority 3 4 for priority 4 5 to 7 are reserved

This register is used to assign a priority to an input clock for automatic clock input switching. The available clock with the lowest priority level will be selected. When input clocks are assigned the same priority, they will use the following default priority list: 0, 1, 2, 3.

Table 16.146. 0x0539 Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Name	Description
0x0539	2:0	R/W	IN2_PRIORITY	The priority for clock input 2 is: 0 no priority 1 for priority 1 2 for priority 2 3 for priority 3 4 for priority 4 5 to 7 are reserved
0x0539	6:4	R/W	IN3_PRIORITY	The priority for clock input 3 is: 0 no priority 1 for priority 1 2 for priority 2 3 for priority 3 4 for priority 4 5 to 7 are reserved

This register is used to assign a priority to an input clock for automatic clock input switching. The available clock with the lowest priority level will be selected. When input clocks are assigned the same priority, they will use the following default priority list: 0, 1, 2, 3.

Table 16.147. 0x053A Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x053A	1:0	R/W	HSW_MODE	1: Default setting, do not modify 0, 2, 3: Reserved
0x053A	3:2	R/W	HSW_PHMEAS_CTRL	0: Default setting, do not modify 1, 2, 3: Reserved

Table 16.148. 0x053B–0x053C Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Name	Description
0x053B	7:0	R/W	HSW_PHMEAS_THR	10-bit value. Set by CBPro.
0x053C	9:8	R/W	HSW_PHMEAS_THR	

Table 16.149. 0x053D

Reg Address	Bit Field	Type	Name	Description
0x053D	4:0	R/W	HSW_COARSE_PM_LEN	Set by CBPro.

Table 16.150. 0x053E

Reg Address	Bit Field	Type	Name	Description
0x053E	4:0	R/W	HSW_COARSE_PM_DLY	Set by CBPro.

Table 16.151. 0x053F

Reg Address	Bit Field	Type	Name	Description
0x053F	1	R/O	HOLD_HIST_VALID	1 = there is enough historical frequency data collected for valid holdover.
0x053F	2	R/O	FASTLOCK_STATUS	1 = PLL is in Fast Lock operation

Table 16.152. 0x0540 Reserved

Reg Address	Bit Field	Type	Name	Description
0x0540	7:0	R/W	RESERVED	This register is used when making certain changes to the device. See Section 4.2 Dynamic PLL Changes for more information.

Table 16.153. 0x0588 Hitless Switching Length

Reg Address	Bit Field	Type	Setting Name	Description
0x0588	3:0	R/W	HSW_FINE_PM_LEN	Set by CBPro.

Table 16.154. 0x0589-0x058A PFD Enable Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x0589	7:0	R/W	PFD_EN_DELAY	Set by CBPro.
0x058A	12:8	R/W	PFD_EN_DELAY	

Table 16.155. 0x058B–0x058D

Reg Address	Bit Field	Type	Setting Name	Description
0x058B	7:0	R/W	HSW_MEAS_SETTLE	Set by CBPro.
0x058C	15:8	R/W	HSW_MEAS_SETTLE	Set by CBPro.
0x058D	19:16	R/W	HSW_MEAS_SETTLE	Set by CBPro.

Table 16.156. 0x059B Holdover Exit

Reg Address	Bit Field	Type	Setting Name	Description
0x059B	1	R/W	INIT_LP_CLOSE_HO	Set by CBPro.
0x059B	4	R/W	HOLD_PRESERVE_HIST	Set by CBPro.
0x059B	5	R/W	HOLD_FRZ_WITH_INTONLY	

Reg Address	Bit Field	Type	Setting Name	Description
0x059B	6	R/W	HOLDEXIT_BW_SEL0	Set by CBPro. See HOLDEXIT_BW_SEL1
0x059B	7	R/W	HOLDEXIT_STD_BO	Set by CBPro.

Table 16.157. 0x059C

Reg Address	Bit Field	Type	Setting Name	Description
0x059C	7	R/W	HOLD_RAMPBP_NOHIST	Set by CBPro

Table 16.158. 0x059C

Reg Address	Bit Field	Type	Setting Name	Description
0x059C	6	R/W	HOLDEXIT_ST_BO	Set by CBPro

Table 16.159. 0x059D Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x059D	5:0	R/W	HOLDEXIT_BW0	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 16.160. 0x059E Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x059E	5:0	R/W	HOLDEXIT_BW1	Set by CBPro to set the PLL bandwidth when exiting holdover; works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1.

Table 16.161. 0x059F Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x059F	5:0	R/W	HOLDEXIT_BW2	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 16.162. 0x05A0 Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x05A0	5:0	R/W	HOLDEXIT_BW3	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 16.163. 0x05A1 Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x05A1	5:0	R/W	HOLDEXIT_BW4	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 16.164. 0x059A2 Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x05A2	5:0	R/W	HOLDEXIT_BW5	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 16.165. 0x05A4

Reg Address	Bit Field	Type	Setting Name	Description
0x05A4	7:0	R/W	HSW_LIMIT	Set by CBPro

Table 16.166. 0x05A5

Reg Address	Bit Field	Type	Setting Name	Description
0x05A5	0	R/W	HSW_LIMIT_ACTION	Set by CBPro

Table 16.167. 0x05A6 Hitless Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x05A6	2:0	R/W	RAMP_STEP_SIZE	Size of the frequency ramp steps when ramping between inputs or when exiting holdover. Calculated by CBPro based on selection.
0x05A6	3	R/W	RAMP_SWITCH_EN	Ramp Switching Enable 0: Disable Ramp Switching 1: Enable Ramp Switching (default)

Table 16.168. 0x05AC

Reg Address	Bit Field	Type	Setting Name	Description
0x05AC	0	R/W	OUT_MAX_LIMIT_EN	Set by CBPro
0x05AC	3	R/W	HOLD_SETTLE_DET_EN	Set by CBPro

Table 16.169. 0x05AD–0x05AE

Reg Address	Bit Field	Type	Setting Name	Description
0x05AD	7:0	R/W	OUT_MAX_LIMIT_LMT	Set by CBPro
0x05AE	15:8	R/W	OUT_MAX_LIMIT_LMT	Set by CBPro

Table 16.170. 0x05B1–0x05B2

Reg Address	Bit Field	Type	Setting Name	Description
0x05B1	7:0	R/W	HOLD_SETTLE_TARGET	Set by CBPro
0x05B2	15:8	R/W	HOLD_SETTLE_TARGET	Set by CBPro

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Table 16.171. 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	0 to use a crystal at the XAXB pins 1 to use an external clock source at the XAXB pins

Table 16.172. 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Name	Description
0x0943	0	R/W	IO_VDD_SEL	0 for 1.8 V external connections 1 for 3.3 V external connections

The IO_VDD_SEL configuration bit selects the option of operating the serial interface, and other control/status IO which are not controlled by VDDS via either the VDD or VDDA pins. These pins are always 3.3 V tolerant even when the device's VDD pin is supplied from a 1.8 V source. When the I^2C or SPI host is operating at 3.3 V and the Si5395/94/92 at VDD = 1.8 V, the host must write the IO_VDD_SEL configuration bit to the VDDA option. This will ensure that both the host and the serial interface are operating at the optimum voltage thresholds. The pins that are controlled by the IO_VDD_SEL bit are I2C_SEL, IN_SEL, RSTb, OEb, A1, SCLK, A0/CSb, FINC, FDEC, SDA/SDIO, LOLb, INTRb, and SDO.

Table 16.173. 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Name	Description
0x0949	3:0	R/W	IN_EN	0: Disable and Powerdown Input Buffer 1: Enable Input Buffer for IN3–IN0.
0x0949	7:4	R/W	IN_PULSED_CMOS_EN	0: Standard Input Format 1: Pulsed CMOS Input Format for IN3–IN0. See Section 5. Clock Inputs for more information.

When a clock input is disabled, it is powered down.

Input 0 corresponds to IN_SEL 0x0949 [0], IN_PULSED_CMOS_EN 0x0949 [4]

Input 1 corresponds to IN_SEL 0x0949 [1], IN_PULSED_CMOS_EN 0x0949 [5]

Input 2 corresponds to IN_SEL 0x0949 [2], IN_PULSED_CMOS_EN 0x0949 [6]

Input 3 corresponds to IN_SEL 0x0949 [3], IN_PULSED_CMOS_EN 0x0949 [7]

Table 16.174. 0x094A Input Clock Enable to DSPLL

Reg Address	Bit Field	Type	Setting Name	Description
0x094A	3:0	R/W	INX_TO_PFD_EN	Value calculated in CBPro

Table 16.175. 0x094E–0x094F Input Clock Buffer Hysteresis

Reg Address	Bit Field	Type	Setting Name	Description
0x094E	7:0	R/W	REFCLK_HYS_SEL	Value calculated in CBPro
0x094F	3:0	R/W	REFCLK_HYS_SEL	

Table 16.176. 0x094F CMOS High Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x094F	7:4	R/W	IN_CMOS_USE1P8	0 = selects the Pulsed CMOS input buffer mode 1 = selects the LVCMOS input buffer mode

Table 16.177. 0x095E MXAXB Fractional Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x095E	0	R/W	MXAXB_INTE-GER	Set by CBPro.

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Table 16.178. 0x0A02 Enable N-divider 0.5x

Reg Address	Bit Field	Type	Setting Name	Description
0x0A02	4:0	R/W	N_ADD_0P5	Value calculated in CBPro.

Table 16.179. 0x0A03 Output Multisynth Clock to Output Driver

Reg Address	Bit Field	Type	Name	Description
0x0A03	4:0	R/W	N_CLK_TO_OUTX_EN	Routes Multisynth outputs to output driver muxes.

Table 16.180. 0x0A04 Output Multisynth Integer Divide Mode

Reg Address	Bit Field	Type	Name	Description
0x0A04	4:0	R/W	N_PIBYP	Output Multisynth integer divide mode. Bit 0 for ID0, Bit 1 for ID1, etc. 0: Nx divider is fractional. 1: Nx divider is integer.

A soft reset reg 0x001C [0] should be asserted after changing any of these bits. If it is expected that any of the N dividers will be changing from integer to fractional, it is recommended that the corresponding bits be initialized to 0 so that when the change from integer to fractional occurs there will be no need for a soft reset. For this reason DCO (digitally controlled oscillator) and FOTF (frequency on the fly) applications should have zeros for these bits. See DCO Applications with Jitter Attenuators .

Table 16.181. 0x0A05 Output Multisynth Divider Power Down

Reg Address	Bit Field	Type	Name	Description
0x0A05	4:0	R/W	N_PDNB	Powers down the N dividers. Set to 0 to power down unused N dividers. Must set to 1 for all active N dividers. See also related registers 0x0A03 and 0x0B4A.

Table 16.182. Nx_HIGH_FREQ

Reg Address	Bit Field	Type	Name	Description
0x0A14	3	R/W	N0_HIGH_FREQ	Set by CBPro.
0x0A1A	3	R/W	N1_HIGH_FREQ	Set by CBPro.
0x0A20	3	R/W	N2_HIGH_FREQ	Set by CBPro.
0x0A26	3	R/W	N3_HIGH_FREQ	Set by CBPro.
0x0A2C	3	R/W	N4_HIGH_FREQ	Set by CBPro.

Table 16.183. 0x0A38 N0 Dynamic Phase Adjust Step Size

Reg Address	Bit Field	Type	Name	Description
0x0A38	7:0	R/W	N0_PHASE_STEP	N0 step size from 1 to 255 in units of Tvco, the VCO period.

N0_PHASE_STEP and N0_PHASE_COUNT are used to produce a phase change anywhere from 0 degrees to 360 degrees with a resolution of the VCO period. N0_PHASE_STEP can be invoked multiple times by using N0_PHASE_COUNT. The phase change is initiated by writing to either N0_PHASE_INC or N0_PHASE_DEC (at addr 0x0A3B). The resulting phase change will be:

N0_PHASE_STEP * N0_PHASE_COUNT * Tvco, for Tvco = 1 / Fvco

Table 16.184. 0x0A39 N0 Dynamic Phase Adjust Step Size Count

Reg Address	Bit Field	Type	Name	Description
0x0A39	7:0	R/W	N0_PHASE_COUNT	Lower byte of number of N0 step size changes.
0x0A3A	15:8	R/W	N0_PHASE_COUNT	Upper byte of number of N0 step size changes.

Table 16.185. 0x0A3B N0 Dynamic Phase Adjust Command

Reg Address	Bit Field	Type	Name	Description
0x0A3B	0	R/W	N0_PHASE_INC	Writing a 1 initiates a phase increment.
0x0A3B	1	R/W	N0_PHASE_DEC	Writing a 1 initiates a phase decrement.

Once set, these register bits will self clear as soon as the entire phase adjust sequence has completed.

N1 dynamic phase adjust works the same as N0 dynamic phase adjust (0xA38).

Table 16.186. 0x0A3C N1 Dynamic Phase Adjust Step Size

Reg Address	Bit Field	Type	Name	Description
0x0A3C	7:0	R/W	N1_PHASE_STEP	N1 step size from 1 to 255 in units of Tvco, the VCO period.

Table 16.187. 0x0A3D N1 Dynamic Phase Adjust Step Size Count

Reg Address	Bit Field	Type	Name	Description
0x0A3D	7:0	R/W	N1_PHASE_COUNT	Lower byte of number of N1 step size changes.
0x0A3E	15:8	R/W	N1_PHASE_COUNT	Upper byte of number of N1 step size changes.

Table 16.188. 0x0A3F N1 Dynamic Phase Adjust Command

Reg Address	Bit Field	Type	Name	Description
0x0A3F	0	R/W	N1_PHASE_INC	Writing a 1 initiates a phase increment.
0x0A3F	1	R/W	N1_PHASE_DEC	Writing a 1 initiates a phase decrement.

N2 dynamic phase adjust works the same as N0 dynamic phase adjust (0xA38).

Table 16.189. 0x0A40 N2 Dynamic Phase Adjust Step Size

Reg Address	Bit Field	Type	Name	Description
0x0A40	7:0	R/W	N2_PHASE_STEP	N2 step size from 1 to 255 in units of Tvco, the VCO period.

Table 16.190. 0x0A41 N2 Dynamic Phase Adjust Step Size Count

Reg Address	Bit Field	Type	Name	Description
0x0A41	7:0	R/W	N2_PHASE_COUNT	Lower byte of number of N2 step size changes.
0x0A42	15:8	R/W	N2_PHASE_COUNT	Upper byte of number of N2 step size changes.

Table 16.191. 0x0A3 N2 Dynamic Phase Adjust Command

Reg Address	Bit Field	Type	Name	Description
0x0A43	0	R/W	N2_PHASE_INC	Writing a 1 initiates a phase increment.
0x0A43	1	R/W	N2_PHASE_DEC	Writing a 1 initiates a phase decrement.

N3 dynamic phase adjust works the same as N0 dynamic phase adjust (0xA38).

Table 16.192. 0x0A44 N3 Dynamic Phase Adjust Step Size

Reg Address	Bit Field	Type	Name	Description
0x0A44	7:0	R/W	N3_PHASE_STEP	N3 step size from 1 to 255 in units of Tvco, the VCO period.

Table 16.193. 0x0A45 N3 Dynamic Phase Adjust Step Size Count

Reg Address	Bit Field	Type	Name	Description
0x0A45	7:0	R/W	N3_PHASE_COUNT	Lower byte of number of N3 step size changes.
0x0A46	15:8	R/W	N3_PHASE_COUNT	Upper byte of number of N3 step size changes.

Table 16.194. 0x0A47 N3 Dynamic Phase Adjust Command

Reg Address	Bit Field	Type	Name	Description
0x0A47	0	R/W	N3_PHASE_INC	Writing a 1 initiates a phase increment.
0x0A47	1	R/W	N3_PHASE_DEC	Writing a 1 initiates a phase decrement.

N4 dynamic phase adjust works the same as N0 dynamic phase adjust (0xA38).

Table 16.195. 0x0A48 N4 Dynamic Phase Adjust Step Size

Reg Address	Bit Field	Type	Name	Description
0x0A48	7:0	R/W	N4_PHASE_STEP	N4 step size from 1 to 255 in units of Tvco, the VCO period.

Table 16.196. 0x0A49 N4 Dynamic Phase Adjust Step Size Count

Reg Address	Bit Field	Type	Name	Description
0x0A49	7:0	R/W	N4_PHASE_COUNT	Lower byte of number of N4 step size changes.
0x0A4A	15:8	R/W	N4_PHASE_COUNT	Upper byte of number of N4 step size changes.

Table 16.197. 0x0AB N4 Dynamic Phase Adjust Command

Reg Address	Bit Field	Type	Name	Description
0x0A4B	0	R/W	N4_PHASE_INC	Writing a 1 initiates a phase increment.
0x0A4B	1	R/W	N4_PHASE_DEC	Writing a 1 initiates a phase decrement.

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Table 16.198. 0x0B24

Reg Address	Bit Field	Type	Name	Description
0x0B24	7:0	R/W	RESERVED	Reserved. This register is used when making certain changes to the device. See Section 4.2 Dynamic PLL Changes for more information.

Table 16.199. 0x0B25

Reg Address	Bit Field	Type	Name	Description
0x0B25	7:0	R/W	RESERVED	Reserved. This register is used when making certain changes to the device. See Section 4.2 Dynamic PLL Changes for more information.

Table 16.200. 0x0B44 Output Multisynth Clock to Output Driver

Reg Address	Bit Field	Type	Name	Description
0x0B44	3:0	R/W	PDIV_FRACN_CLK_DIS	Disable digital clocks to input P (IN0–3) fractional dividers.
0x0B44	5	R/W	FRACN_CLK_DIS_PLL	Disable digital clock to M fractional divider.

Table 16.201. 0x0B46

Reg Address	Bit Field	Type	Name	Description
0x0B46	3:0	R/W	LOS_CLK_DIS	Set to 0 for normal operation.

Table 16.202. 0x0B47

Reg Address	Bit Field	Type	Name	Description
0x0B47	4:0	R/W	OOF_CLK_DIS	Set to 0 for normal operation.

Table 16.203. 0x0B48 OOF Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B48	4:0	R/W	OOF_DIV_CLK_DIS	Set to 0 for normal operation. Digital OOF divider clock user disable. Bits 3:0 are for IN3,2,1,0, Bit 4 is for OOF for the XAXB input.

Table 16.204. 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	4:0	R/W	N_CLK_DIS	Disable digital clocks to N dividers. Must be set to 0 to use each N divider. See also related registers 0x0A03 and 0x0A05.

Table 16.205. 0x0B57-0x0B58 VCO Calcode

Reg Address	Bit Field	Type	Name	Description
0x0B57	7:0	R/W	VCO_RESET_CALCODE	12-bit value. Controls the VCO frequency when a reset occurs.
0x0B58	11:8	R/W	VCO_RESET_CALCODE	

16.10 Page C Registers Si5395

Table 16.206. 0x0C02

Reg Address	Bit Field	Type	Name	Description
0x0C02	2:0	R/W	VAL_DIV_CTL0	Set by CBPro
0x0C02	4	R/W	VAL_DIV_CTL1	Set by CBPro

Table 16.207. 0x0C03

Reg Address	Bit Field	Type	Name	Description
0x0C03	3:0	R/W	IN_CLK_VAL_PWR_UP_DIS	Set by CBPro

Table 16.208. 0x0C07

Reg Address	Bit Field	Type	Name	Description
0x0C07	0	R/W	IN_CLK_VAL_EN	Set by CBPro

Table 16.209. 0x0C08

Reg Address	Bit Field	Type	Name	Description
0x0C08	7:0	R/W	IN_CLK_VAL_TIME	Set by CBPro

17. Si5394 Register Definitions

17.1 Page 0 Registers Si5394

Table 17.1. 0x0001 Page

Reg Address	Bit Field	Type	Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

There is the “Page Register” which is located at address 0x01 on every page. When read, it will indicate the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, … etc.

Table 17.2. 0x0002–0x0003 Base Part Number

Reg Address	Bit Field	Type	Name	Value	Description
0x0002	7:0	R	PN_BASE	0x94	Four-digit “base” part number, one nibble per digit Example: Si5394A-A-GM. The base part number (OPN) is 5394, which is stored in this register
0x0003	15:8	R	PN_BASE	0x53	

Table 17.3. 0x0004 Device Grade

Reg Address	Bit Field	Type	Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed/ synthesis mode 0 = A, 1 = B, 2 = C, 3 = D , 4 =E 9=J, 10=K,11=L,12=M,15=P etc

Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 17.4. 0x0005 Device Revision

Reg Address	Bit Field	Type	Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B, etc. Example Si5394C-A12345-GM, the device revision is “A” and stored as 0

Table 17.5. 0x0006–0x0008 TOOL_VERSION

Reg Address	Bit Field	Type	Name	Description
0x0006	3:0	R/W	TOOL_VERSION[3:0]	Special
0x0006	7:4	R/W	TOOL_VERSION[7:4]	Revision
0x0007	7:0	R/W	TOOL_VERSION[15:8]	Minor[7:0]
0x0008	0	R/W	TOOL_VERSION[15:8]	Minor[8]
0x0008	4:1	R/W	TOOL_VERSION[16]	Major
0x0008	7:5	R/W	TOOL_VERSION[13:17]	Tool. 0 for ClockBuilder Pro

The software tool version that created the register values that are downloaded at power up is represented by TOOL_VERSION.

Table 17.6. 0x0009 Temperature Grade

Reg Address	Bit Field	Type	Name	Description
0x0009	7:0	R/W	TEMP_GRADE	Device temperature grading 0 = Industrial (–40° C to 85° C) ambient conditions

Table 17.7. 0x000A Package ID

Reg Address	Bit Field	Type	Name	Description
0x000A	7:0	R/W	PKG_ID	Package ID 1 = 7x7 mm 44-QFN

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5394C-A12345-GM.

Applies to a “base” or “blank” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5394C-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5394 but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 17.8. 0x000B I^2C Address

Reg Address	Bit Field	Type	Setting Name	Description
0x000B	6:2	R/W	I2C_ADDR	The upper 5 bits of the 7 bit I^2C address. The lower 2 bits are controlled by the A1 and A0 pins. Note: This register is not bank burnable.

Table 17.9. 0x000C Internal Status Bits

Reg Address	Bit Field	Type	Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	3	R	XAXB_ERR	1 if there is a problem locking to the XAXB input signal.
0x000C	5	R	SMBUS_TIMEOUT	1 if there is an SMBus timeout error.

Bit 1 is the LOS status monitor for the XTAL or REFCLK at the XA/XB pins.

Table 17.10. 0x000D Out-of-Frequency (OOF) and Loss-of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Name	Description
0x000D	3:0	R	LOS	1 if the clock input is currently LOS

Reg Address	Bit Field	Type	Name	Description
0x000D	7:4	R	OOF	1 if the clock input is currently OOF

Note that each bit corresponds to the input. The LOS and OOF bits are not sticky.

Input 0 (IN0) corresponds to LOS 0x000D [0], OOF 0x000D [4]

Input 1 (IN1) corresponds to LOS 0x000D [1], OOF 0x000D [5]

Input 2 (IN2) corresponds to LOS 0x000D [2], OOF 0x000D [6]

Input 3 (IN3) corresponds to LOS 0x000D [3], OOF 0x000D [7]

Table 17.11. 0x000E Holdover and LOL Status

Reg Address	Bit Field	Type	Name	Description
0x000E	1	R	LOL	1 if the DSPLL is out of lock
0x000E	5	R	HOLD	1 if the DSPLL is in holdover (or free run)

These status bits indicate if the DSPLL is in holdover and if it is in Loss of Lock. These bits are not sticky.

Table 17.12. 0x000F Calibration Status

Reg Address	Bit Field	Type	Name	Description
0x000F	5	R	CAL_PLL	1 if the DSPLL internal calibration is busy

This status bit indicates if a DSPLL is currently busy with calibration. This bit is not sticky.

Table 17.13. 0x0011 Internal Error Flags

Reg Address	Bit Field	Type	Name	Description
0x0011	0	R/W	SYSINCAL_FLG	Sticky version of SYSINCAL. Write a 0 to this bit to clear.
0x0011	1	R/W	LOSXAXB_FLG	Sticky version of LOSXAXB. Write a 0 to this bit to clear.
0x0011	3	R/W	XAXB_ERR_FLG	Sticky version of XAXB_ERR.Write a 0 to this bit to clear.
0x0011	5	R/W	SMBUS_TIMEOUT_FLG	Sticky version of SMBUS_TIMEOUT. Write a 0 to this bit to clear.

These are sticky flag bits. They are cleared by writing zero to the bit that has been set.

Table 17.14. 0x0012 Sticky OOF and LOS Flags

Reg Address	Bit Field	Type	Name	Description
0x0012	3:0	R/W	LOS_FLG	1 if the clock input is LOS for the given input
0x0012	7:4	R/W	OOF_FLG	1 if the clock input is OOF for the given input

These are the sticky flag versions of register 0x000D. These bits are cleared by writing 0 to the bits that have been set.

Input 0 (IN0) corresponds to LOS_FLG 0x0012 [0], OOF_FLG 0x0012 [4]

Input 1 (IN1) corresponds to LOS_FLG 0x0012 [1], OOF_FLG 0x0012 [5]

Input 2 (IN2) corresponds to LOS_FLG 0x0012 [2], OOF_FLG 0x0012 [6]

Input 3 (IN3) corresponds to LOS_FLG 0x0012 [3], OOF_FLG 0x0012 [7]

Table 17.15. 0x0013 Sticky Holdover and LOL Flags

Reg Address	Bit Field	Type	Name	Description
0x0013	1	R/W	LOL_FLG	1 if the DSPLL was unlocked
0x0013	5	R/W	HOLD_FLG	1 if the DSPLL was in holdover or free run

These are the sticky flag versions of register 0x000E. These bits are cleared by writing 0 to the bits that have been set.

Table 17.16. 0x0014 Sticky PLL Calibration Flag

Reg Address	Bit Field	Type	Name	Description
0x0014	5	R/W	CAL_FLG_PLL	1 if the internal calibration is busy

This bit is the sticky flag version of 0x000F. This bit is cleared by writing 0 to bit 5.

Table 17.17. 0x0016

Reg Address	Bit Field	Type	Name	Description
0x0016	1	R/W	LOL_ON_HOLD	Set by CBPro.

Table 17.18. 0x0017 Status Flag Masks

Reg Address	Bit Field	Type	Name	Description
0x0017	0	R/W	SYSINCAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt
0x0017	1	R/W	LOSXAXB_INTR_MSK	1 to mask the LOSXAXB_FLG from causing an interrupt
0x0017	5	R/W	SMBUS_TMOUT_INTR_MSK	1 to mask SMBUS_TIMEOUT_FLG from the interrupt
0x0017	6	R/W	RESERVED	Factory set to 1 to mask reserved bit from causing an interrupt. Do not clear this bit.
0x0017	7	R/W	RESERVED	Factory set to 1 to mask reserved bit from causing an interrupt. Do not clear this bit.

These are the interrupt mask bits for the fault flags in register 0x0011. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Note: Bit 1 corresponds to XAXB LOS from asserting the interrupt (INTR) pin.

Table 17.19. 0x0018 OOF and LOS Masks

Reg Address	Bit Field	Type	Name	Description
0x0018	3:0	R/W	LOS_INTR_MSK	1 to mask the clock input LOS flag
0x0018	7:4	R/W	OOF_INTR_MSK	1 to mask the clock input OOF flag

These are the interrupt mask bits for the OOF and LOS flags in register 0x0012.

Input 0 (IN0) corresponds to LOS_INTR_MSK 0x0018 [0], OOF_INTR_MSK 0x0018 [4]

Input 1 (IN1) corresponds to LOS_INTR_MSK 0x0018 [1], OOF_INTR_MSK 0x0018 [5]

Input 2 (IN2) corresponds to LOS_INTR_MSK 0x0018 [2], OOF_INTR_MSK 0x0018 [6]

Input 3 (IN3) corresponds to LOS_INTR_MSK 0x0018 [3], OOF_INTR_MSK 0x0018 [7]

Table 17.20. 0x0019 Holdover and LOL Masks

Reg Address	Bit Field	Type	Name	Description
0x0019	1	R/W	LOL_INTR_MSK	1 to mask the clock input LOL flag
0x0019	5	R/W	HOLD_INTR_MSK	1 to mask the holdover flag

These are the interrupt mask bits for the LOL and HOLD flags in register 0x0013. If a mask bit is set the alarm will be blocked from causing an interrupt.

Table 17.21. 0x001A PLL Calibration Interrupt Mask

Reg Address	Bit Field	Type	Name	Description
0x001A	5	R/W	CAL_INTR_MSK	1 to mask the DSPLL internal calibration busy flag

The interrupt mask for this bit flag bit corresponds to register 0x0014.

the error flags in register 0x0017. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Table 17.22. 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Name	Description
0x001C	0	S	SOFT_RST_ALL	1 Initialize and calibrates the entire device 0 No effect
0x001C	2	S	SOFT_RST	1 Initialize outer loop 0 No effect

These bits are of type “S”, which is self-clearing.

Table 17.23. 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Name	Description
0x001D	0	S	FINC	1 a rising edge will cause the selected MultiSynth to increment the output frequency by the Nx_FSTEPW parameter. See registers 0x0339-0x0353
0x001D	1	S	FDEC	1 a rising edge will cause the selected MultiSynth to decrement the output frequency by the Nx_FSTEPW parameter. See registers 0x0339-0x0353

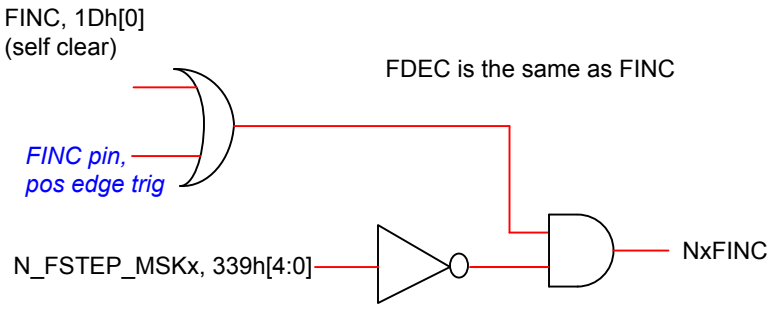

Figure 17.1. Logic Diagram of the FINC/FDEC Masks

Table 17.24. 0x001E Power Down and Hard Reset

Reg Address	Bit Field	Type	Name	Description
0x001E	0	R/W	PDN	1 to put the device into low power mode
0x001E	1	R/W	HARD_RST	1 causes hard reset. The same as power up except that the serial port access is not held at reset. 0 No reset
0x001E	2	S	SYNC	1 to reset all output R dividers to the same state.

Table 17.25. 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Name	Description
0x002B	3	R/W	SPI_3WIRE	0 for 4-wire SPI, 1 for 3-wire SPI
0x002B	5	R/W	AUTO_NDIV_UPDATE	Set by CBPro.

Table 17.26. 0x002C LOS Enable

Reg Address	Bit Field	Type	Name	Description
0x002C	3:0	R/W	LOS_EN	1 to enable LOS for a clock input; 0 for disable
0x002C	4	R/W	LOSXAXB_DIS	Enable LOS detection on the XAXB inputs. 0: Enable LOS Detection (default) 1: Disable LOS Detection

Input 0 (IN0): LOS_EN[0]

Input 1 (IN1): LOS_EN[1]

Input 2 (IN2): LOS_EN[2]

Input 3 (IN3): LOS_EN[3]

Table 17.27. 0x002D Loss of Signal Requalification Value

Reg Address	Bit Field	Type	Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0 for 2 msec 1 for 100 msec 2 for 200 msec 3 for one second
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above
0x002D	5:4	R/W	LOS2_VAL_TIME	Clock Input 2, same as above
0x002D	7:6	R/W	LOS3_VAL_TIME	Clock Input 3, same as above

When an input clock disappears (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Table 17.28. 0x002E-0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit Threshold Value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

Table 17.29. 0x0030-0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	16-bit Threshold Value
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Table 17.30. 0x0032-0x0033 LOS2 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x0032	7:0	R/W	LOS2_TRG_THR	16-bit Threshold Value
0x0033	15:8	R/W	LOS2_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 2, given a particular frequency plan.

Table 17.31. 0x0034-0x0035 LOS3 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x0034	7:0	R/W	LOS3_TRG_THR	16-bit Threshold Value
0x0035	15:8	R/W	LOS3_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 3, given a particular frequency plan.

Table 17.32. 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	16-bit Threshold Value
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 0, given a particular frequency plan.

Table 17.33. 0x0038-0x0039 LOS1 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0038	7:0	R/W	LOS1_CLR_THR	16-bit Threshold Value
0x0039	15:8	R/W	LOS1_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 1, given a particular frequency plan.

Table 17.34. 0x003A-0x003B LOS2 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x003A	7:0	R/W	LOS2_CLR_THR	16-bit Threshold Value
0x003B	15:8	R/W	LOS2_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 2, given a particular frequency plan.

Table 17.35. 0x003C-0x003D LOS3 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x003C	7:0	R/W	LOS3_CLR_THR	16-bit Threshold Value
0x003D	15:8	R/W	LOS3_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 3, given a particular frequency plan.

Table 17.36. 0x003E LOS_MIN_PERIOD_EN

Reg Address	Bit Field	Type	Name	Description
0x003E	7:4	R/W	LOS_MIN_PERIOD_EN	Set by CBPro

Table 17.37. 0x003F OOF Enable

Reg Address	Bit Field	Type	Name	Description
0x003F	3:0	R/W	OOF_EN	1 to enable, 0 to disable
0x003F	7:4	R/W	FAST_OOF_EN	1 to enable, 0 to disable

Input 0 corresponds to OOF_EN [0], FAST_OOF_EN [4]

Input 1 corresponds to OOF_EN [1], FAST_OOF_EN [5]

Input 2 corresponds to OOF_EN [2], FAST_OOF_EN [6]

Input 3 corresponds to OOF_EN [3], FAST_OOF_EN [7]

Table 17.38. 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	0 for CLKIN0 1 for CLKIN1 2 for CLKIN2 3 for CLKIN3 4 for XAXB

Table 17.39. 0x0041–0x0045 OOF Divider Select

Reg Address	Bit Field	Type	Name	Description
0x0041	4:0	R/W	OOF0_DIV_SEL	Sets a divider for the OOF circuitry for each input clock 0,1,2,3. The divider value is $2^{OOFx\_DIV\_SEL}$. CBPro sets these dividers.
0x0042	4:0	R/W	OOF1_DIV_SEL	
0x0043	4:0	R/W	OOF2_DIV_SEL	
0x0044	4:0	R/W	OOF3_DIV_SEL	
0x0045	4:0	R/W	OOFXO_DIV_SEL	

Table 17.40. 0x0046–0x0049 Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	OOF Set threshold. Range is up to ±500 ppm in steps of 1/16 ppm
0x0047	7:0	R/W	OOF1_SET_THR	OOF Set threshold. Range is up to ±500 ppm in steps of 1/16 ppm
0x0048	7:0	R/W	OOF2_SET_THR	OOF Set threshold. Range is up to ±500 ppm in steps of 1/16 ppm
0x0049	7:0	R/W	OOF3_SET_THR	OOF Set threshold. Range is up to ±500 ppm in steps of 1/16 ppm

Table 17.41. 0x004A-0x004D Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	OOF Clear threshold. Range is up to ±500 ppm in steps of 1/16 ppm
0x004B	7:0	R/W	OOF1_CLR_THR	OOF Clear threshold. Range is up to ±500 ppm in steps of 1/16 ppm
0x004C	7:0	R/W	OOF2_CLR_THR	OOF Clear threshold. Range is up to ±500 ppm in steps of 1/16 ppm
0x004D	7:0	R/W	OOF3_CLR_THR	OOF Clear threshold. Range is up to ±500 ppm in steps of 1/16 ppm

Table 17.42. 0x004E-0x04F OOF Detection Windows

Reg Address	Bit Field	Type	Setting Name	Description
0x004E	2:0	R/W	OOF0_DET-WIN_SEL	Values calculated by CBPro
0x004E	6:4	R/W	OOF1_DET-WIN_SEL	Values calculated by CBPro
0x004F	2:0	R/W	OOF2_DET-WIN_SEL	Values calculated by CBPro
0x004F	6:4	R/W	OOF3_DET-WIN_SEL	Values calculated by CBPro

Table 17.43. 0x0050

Reg Address	Bit Field	Type	Setting Name	Description
0x0050	3:0	R/W	OOF_ON_LOS	Set by CBPro

Table 17.44. 0x0051-0x0054 Fast Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x0051	3:0	R/W	FAST_OOF0_SET_THR	(1+ value) x 1000 ppm
0x0052	3:0	R/W	FAST_OOF1_SET_THR	(1+ value) x 1000 ppm
0x0053	3:0	R/W	FAST_OOF2_SET_THR	(1+ value) x 1000 ppm
0x0054	3:0	R/W	FAST_OOF3_SET_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm set threshold for IN3, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

Table 17.45. 0x0055-0x0058 Fast Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0055	3:0	R/W	FAST_OOF0_CLR_THR	(1+ value) x 1000 ppm
0x0056	3:0	R/W	FAST_OOF1_CLR_THR	(1+ value) x 1000 ppm
0x0057	3:0	R/W	FAST_OOF2_CLR_THR	(1+ value) x 1000 ppm
0x0058	3:0	R/W	FAST_OOF3_CLR_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm clear threshold for IN3, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value)*1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

OOF needs a frequency reference. ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Table 17.46. 0x0059 Fast OOF Detection Window

Reg Address	Bit Field	Type	Name	Description
0x0059	1:0	R/W	FAST_OOF0_DETWIN_SEL	Values calculated by CBPro
0x0059	3:2	R/W	FAST_OOF1_DETWIN_SEL	Values calculated by CBPro
0x0059	5:4	R/W	FAST_OOF2_DETWIN_SEL	Values calculated by CBPro
0x0059	7:6	R/W	FAST_OOF3_DETWIN_SEL	Values calculated by CBPro

Table 17.47. 0x005A-0x005D OOF0 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x005A	7:0	R/W	OOF0_RATIO_REF	Values calculated by CBPro
0x005B	15:8	R/W	OOF0_RATIO_REF	
0x005C	23:16	R/W	OOF0_RATIO_REF	
0x005D	25:24	R/W	OOF0_RATIO_REF	

Table 17.48. 0x005E-0x0061 OOF1 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x005E	7:0	R/W	OOF1_RATIO_REF	Values calculated by CBPro
0x005F	15:8	R/W	OOF1_RATIO_REF	
0x0060	23:16	R/W	OOF1_RATIO_REF	
0x0061	25:24	R/W	OOF1_RATIO_REF	

Table 17.49. 0x0062-0x0065 OOF2 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x0062	7:0	R/W	OOF2_RATIO_REF	Values calculated by CBPro
0x0063	15:8	R/W	OOF2_RATIO_REF	
0x0064	23:16	R/W	OOF2_RATIO_REF	
0x0065	25:24	R/W	OOF2_RATIO_REF	

Table 17.50. 0x0066-0x0069 OOF3 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x0066	7:0	R/W	OOF3_RATIO_REF	Values calculated by CBPro
0x0067	15:8	R/W	OOF3_RATIO_REF	
0x0068	23:16	R/W	OOF3_RATIO_REF	
0x0069	25:24	R/W	OOF3_RATIO_REF	

Table 17.51. 0x0092 Fast LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x0092	1	R/W	LOL_FST_EN	Enables fast detection of LOL. A large input frequency error will quickly assert LOL when this is enabled.

Table 17.52. 0x0093 Fast LOL Detection Window

Reg Address	Bit Field	Type	Name	Description
0x0093	7:4	R/W	LOL_FST_DETWIN_SEL	Values calculated by CBPro

Table 17.53. 0x0095 Fast LOL Detection Value

Reg Address	Bit Field	Type	Name	Description
0x0095	3:2	R/W	LOL_FST_VALWIN_SEL	Values calculated by CBPro

Table 17.54. 0x0096 Fast LOL Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x0096	7:4	R/W	LOL_FST_SET_THR_SEL	Values calculated by CBPro

Table 17.55. 0x0098 Fast LOL Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0098	7:4	R/W	LOL_FST_CLR_THR_SEL	Values calculated by CBPro

Table 17.56. 0x009A LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x009A	1	R/W	LOL_SLOW_EN_PLL	1 to enable LOL; 0 to disable LOL.

ClockBuilder Pro provides the LOL register values for a particular frequency plan.

Table 17.57. 0x009B Slow LOL Detection Window

Reg Address	Bit Field	Type	Name	Description
0x009B	7:4	R/W	LOL_SLW_DETWIN_SEL	Values calculated by CBPro

Table 17.58. 0x009D Slow LOL Detection Value

Reg Address	Bit Field	Type	Setting Name	Description
0x009D	3:2	R/W	LOL_SLW_VALWIN_SEL	Values calculated by CBPro

Table 17.59. 0x009E LOL Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x009E	7:4	R/W	LOL_SLW_SET_THR	Configures the loss of lock set thresholds. Selectable as 0.1, 0.3, 1, 3, 10, 30, 100, 300, 1000, 3000, 10000. Values are in ppm.

The following are the thresholds for the value that is placed in the top four bits of register 0x009E.

0 = 0.1 ppm

1 = 0.3 ppm

2 = 1 ppm

3 = 3 ppm

4 = 10 ppm

5 = 30 ppm

6 = 100 ppm

7 = 300 ppm

8 = 1000 ppm

9 = 3000 ppm

10 = 10000 ppm

Table 17.60. 0x00A0 LOL Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x00A0	7:4	R/W	LOL_SLW_CLR_THR	Configures the loss of lock set thresholds. Selectable as 0.1, 0.3, 1, 3, 10, 30, 100, 300, 1000, 3000, 10000. Values are in ppm.

The following are the thresholds for the value that is placed in the top four bits of register 0x00A0. ClockBuilder Pro sets these values.

0 = 0.1 ppm

1 = 0.3 ppm

2 = 1 ppm

3 = 3 ppm

4 = 10 ppm

5 = 30 ppm

6 = 100 ppm

7 = 300 ppm

8 = 1000 ppm

9 = 3000 ppm

10 = 10000 ppm

Table 17.61. 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Name	Description
0x00A2	1	R/W	LOL_TIMER_EN	0 to disable 1 to enable

Table 17.62. 0x00A9-0x00AC LOL_CLR_DELAY_DIV256

Reg Address	Bit Field	Type	Name	Description
0x00A9	7:0	R/W	LOL_CLR_DELAY_DIV256	Set by CBPro.
0x00AA	15:8	R/W	LOL_CLR_DELAY_DIV256	Set by CBPro.
0x00AB	23:16	R/W	LOL_CLR_DELAY_DIV256	Set by CBPro.
0x00AC	28:24	R/W	LOL_CLR_DELAY_DIV256	Set by CBPro.

Table 17.63. 0x00E2

Reg Address	Bit Field	Type	Name	Description
0x00E2	7:0	R	ACTIVE_NVM_BANK	Read-only field indicating number of user bank writes caried out so far. Value Description 0 zero 3 one 15 two 63 three

Table 17.64. 0x00E3

Reg Address	Bit Field	Type	Setting Name	Description
0x00E3	7:0	R/W	NVM_WRITE	Write 0xC7 to initiate an NVM bank burn.

Table 17.65. 0x00E4

Reg Address	Bit Field	Type	Setting Name	Description
0x00E4	0	S	NVM_READ_BANK	When set, this bit will read the NVM down into the volatile memory.

Table 17.66. 0x00E5 Fastlock Extend Enable

Reg Address	Bit Field	Type	Name	Description
0x00E5	5	R/W	FASTLOCK_EXTEND_EN	Extend Fastlock bandwidth period past LOL Clear 0: Do not extend Fastlock period 1: Extend Fastlock period (default)

Table 17.67. 0x00EA-0x00ED LOL Detection Value

Reg Address	Bit Field	Type	Name	Description
0x00EA	7:0	R/W	FASTLOCK_EXTEND	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL.
0x00EB	15:8	R/W	FASTLOCK_EXTEND	
0x00EC	23:16	R/W	FASTLOCK_EXTEND	
0x00ED	28:24	R/W	FASTLOCK_EXTEND	

Table 17.68. 0x00F6

Reg Address	Bit Field	Type	Name	Description
0x00F6	0	R	REG_0XF7_INTR	Set by CBPro.

Reg Address	Bit Field	Type	Name	Description
0x00F6	1	R	REG_0XF8_INTR	Set by CBPro.
0x00F6	2	R	REG_0XF9_INTR	Set by CBPro.

Table 17.69. 0x00F7

Reg Address	Bit Field	Type	Name	Description
0x00F7	0	R	SYSINCAL_INTR	Set by CBPro.
0x00F7	1	R	LOSXAXB_INTR	Set by CBPro.
0x00F7	2	R	LOSREF_INTR	Set by CBPro.
0x00F7	4	R	LOSVCO_INTR	Set by CBPro.
0x00F7	5	R	SMBUS_TIME_OUT_INTR	Set by CBPro.

Table 17.70. 0x00F8

Reg Address	Bit Field	Type	Name	Description
0x00F8	3:0	R	LOS_INTR	Set by CBPro.
0x00F8	7:4	R	OOF_INTR	Set by CBPro.

Table 17.71. 0x00F9

Reg Address	Bit Field	Type	Name	Description
0x00F9	1	R	LOL_INTR	Set by CBPro.
0x00F9	5	R	HOLD_INTR	Set by CBPro.

Table 17.72. 0x00FE Device Ready

Reg Address	Bit Field	Type	Name	Description
0x00FE	7:0	R	DEVICE_READY	Ready Only byte to indicate device is ready. When read data is 0x0F one can safely read/write registers. This register is repeated on every page therefore a page write is not ever required to read the DEVICE_READY status.

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Table 17.73. 0x0102 Global OE Gating for all Clock Output Drivers

Reg Address	Bit Field	Type	Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	1 Pass through the output enables, 0 disables all output drivers.

Table 17.74. 0x0112 Clock Output Driver 0 and R-Divider 0 Configuration

Reg Address	Bit Field	Type	Name	Description
0x0112	0	R/W	OUT0_PDN	Output driver 0: 0 to power up the regulator, 1 to power down the regulator. Clock outputs will be weakly pulled-low.
0x0112	1	R/W	OUT0_OE	Output driver 0: 0 to disable the output, 1 to enable the output
0x0112	2	R/W	OUT0_RDIV_FORCE2	0 R0 divider value is set by R0_REG 1 R0 divider value is forced into divide by 2

Table 17.75. 0x0113 Output 0 Format

Reg Address	Bit Field	Type	Name	Description
0x0113	2:0	R/W	OUT0_FORMAT	0 Reserved 1 swing mode (normal swing) differential 2 swing mode (high swing) differential 3 Reserved 4 LVCMOS single ended 5 LVCMOS (+ pin only) 6 LVCMOS (– pin only) 7 Reserved
0x0113	3	R/W	OUT0_SYNC_EN	0 disable 1 enable
0x0113	5:4	R/W	OUT0_DIS_STATE	Determines the state of an output driver when disabled, selectable as 00 Disable low 01 Disable high 10 Reserved 11 Reserved
0x0113	7:6	R/W	OUT0_CMOS_DRV	LVCMOS output impedance. Selectable as CMOS1,CMOS2, CMOS3.

See Section 6.2 Performance Guidelines for Outputs .

Table 17.76. 0x0114 Output 0 Swing and Amplitude

Reg Address	Bit Field	Type	Name	Description
0x0114	3:0	R/W	OUT0_CM	Output common mode voltage adjustment Programmable swing mode with normal swing configuration: Step size = 100 mV Range = 0.9 V to 2.3 V if VDDO = 3.3 V Range = 0.6 V to 1.5V if VDDO = 2.5 V Range=0.5 V to 0.9 V if VDDO = 1.8 V Programmable swing mode with high0 swing configuration: Step size = 100 mV Range = 0.9 V to 2.3 V if VDDO = 3.3 V Range = 0.6 V to 1.5 V if VDDO = 2.5 V Range = 0.5 V to 0.9 V if VDDO = 1.8 V LVCMOS mode: Not supported/No effect
0x0114	6:4	R/W	OUT0_AMPL	Output swing adjustment Programmable swing mode with normal swing configuration: Step size = 100 mV Range = 100 mVpp-se to 800 mVpp-se Programmable swing mode with high swing configuration: Step size = 200 mV Range = 200 mVpp-se to 1600 mVpp-se LVCMOS mode: Not supported/No effect

See the settings and values from Section 6.3.8 Output Driver Settings for LVPECL, LVDS, HCSL, and CML for details of the settings. ClockBuilder Pro is used to select the correct settings for this register.

Table 17.77. 0x0115 R-Divider 0 Mux Selection

Reg Address	Bit Field	Type	Name	Description
0x0115	2:0	R/W	OUT0_MUX_SEL	Output driver 0 input mux select.This selects the source of the multisynth. 0: MS0 1: MS1 2: MS2 3: MS3 4: MS4 5: Reserved 6: Reserved 7: Reserved
0x0115	3	R/W	OUT0_VDD_SEL_EN	1 = Enable OUT0_VDD_SEL
0x0115	5:4	R/W	OUT0_VDD_SEL	Must be set to the VDD0 voltage. 0: 3.3 V 1: 1.8 V 2: 2.5 V 3: Reserved
0x0115	7:6	R/W	OUT0_INV	CLK and CLK not inverted CLK inverted CLK and CLK inverted CLK inverted

Each output can be configured to use Multisynth N0-N3 divider. The frequency for each N-divider is set in registers 0x0302-0x032C for N0 to N3. Four different frequencies can be set in the N-dividers (N0–N3) and each of the 4 outputs can be configured to any of the 4 different frequencies.

The four output drivers are all identical. The single set of descriptions above for output driver 0 applies to the other 3 output drivers.

Table 17.78. Registers that Follow the Same Definitions Above

Register Address	Description	(Same as) Address
0x0117	Clock Output Driver 1 Config	0x0112
0x0118	Clock Output Driver 1 Format, Sync	0x0113
0x0119	Clock Output Driver 1 Ampl, CM	0x0114
0x011A	OUT1_MUX_SEL, OUT1_VDD_SEL_EN, OUT1_VDD_SEL, OUT1_INV	0x0115
0x0126	Clock Output Driver 2 Config	0x0112
0x0127	Clock Output Driver 2 Format, Sync	0x0113
0x0128	Clock Output Driver 2 Ampl, CM	0x0114
0x0129	OUT2_MUX_SEL, OUT2_VDD_SEL_EN, OUT2_VDD_SEL, OUT2_INV	0x0115

Register Address	Description	(Same as) Address
0x012B	Clock Output Driver 3 Config	0x0112
0x012C	Clock Output Driver 3 Format, Sync	0x0113
0x012D	Clock Output Driver 3 Ampl, CM	0x0114
0x012E	OUT3_MUX_SEL, OUT3_VDD_SEL_EN, OUT3_VDD_SEL, OUT3_INV	0x0115

Table 17.79. 0x013F–0x0140

Reg Address	Bit Field	Type	Setting Name	Description
0x013F	7:0	R/W	OUTX_ALWAYS_ON	This setting is managed by CBPro during zero delay mode.
0x0140	11:8	R/W	OUTX_ALWAYS_ON	

Table 17.80. 0x0141 Output Disable Mask for LOS XAXB

Reg Address	Bit Field	Type	Setting Name	Description
0x0141	1	R/W	OUT_DIS_MSK	Set by CBPro.
0x0141	5	R/W	OUT_DIS_LOL_MSK	Set by CBPro.
0x0141	6	R/W	OUT_DIS_LOSXAXB_MSK	Determines if outputs are disabled during an LOSXAXB condition. 0: All outputs disabled on LOSXAXB 1: All outputs remain enabled during LOSXAXB condition
0x0141	7	R/W	OUT_DIS_MSK_LOS_PFD	Set by CBPro.

Table 17.81. 0x0142 Output Disable Loss of Lock PLL

Reg Address	Bit Field	Type	Setting Name	Description
0x0142	1	R/W	OUT_DIS_MSK_LOL	0: LOL will disable all connected outputs 1: LOL does not disable any outputs
0x0142	5	R/W	OUT_DIS_MSK_HOLD	Set by CBPro.

Table 17.82. 0x0145 Power Down All

Reg Address	Bit Field	Type	Name	Description
0x0145	0	R/W	OUT_PDN_ALL	0- no effect 1- all drivers powered down

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Table 17.83. 0x0206 Prescale Reference Divide Ratio

Reg Address	Bit Field	Type	Name	Description
0x0206	1:0	R/W	PXAXB	Sets the divider for the input on XAXB

0 = pre-scale value 1

1 = pre-scale value 2

2 = pre-scale value 4

3 = pre-scale value 8

This can only be used with external clock sources, not crystals.

Table 17.84. 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Name	Description
0x0208	7:0	R/W	P0_NUM	48-bit Integer Number
0x0209	15:8	R/W	P0_NUM	
0x020A	23:16	R/W	P0_NUM	
0x020B	31:24	R/W	P0_NUM	
0x020C	39:32	R/W	P0_NUM	
0x020D	47:40	R/W	P0_NUM	

This set of registers configure the P-dividers which are located at the four input clocks seen in Section . ClockBuilder Pro calculates the correct values for the P-dividers.

Table 17.85. 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Name	Description
0x020E	7:0	R/W	P0_DEN	32-bit Integer Number
0x020F	15:8	R/W	P0_DEN	
0x0210	23:16	R/W	P0_DEN	
0x0211	31:24	R/W	P0_DEN	

The P1, P2 and P3 divider numerator and denominator follow the same format as P0 described above. ClockBuilder Pro calculates the correct values for the P-dividers.

Table 17.86. Registers that Follow the P0_NUM and P0_DEN

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1 Divider Denominator	32-bit Integer Number	0x020E-0x0211
0x021C-0x0221	P2 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0222-0x0225	P2 Divider Denominator	32-bit Integer Number	0x020E-0x0211
0x0226-0x022B	P3 Divider Numerator	48-bit Integer Number	0x0208-0x020D

Register Address	Description	Size	Same as Address
0x022C-0x022F	P3 Divider Denominator	32-bit Integer Number	0x020E-0x0211

This set of registers configure the P-dividers which are located at the four input clocks seen in Section . ClockBuilder Pro calculates the correct values for the P-dividers.

Table 17.87. 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Name	Description
0x0230	0	S, R/W	P0_UPDATE	0 - No update for P-divider value 1 - Update P-divider value
0x0230	1	S, R/W	P1_UPDATE	
0x0230	2	S, R/W	P2_UPDATE	
0x0230	3	S, R/W	P3_UPDATE	

The Px_Update bit must be asserted to update the P-Divider. The update bits are provided so that all of the divider bits can be changed at the same time. First, write all of the new values to the divider, then set the update bit.

Table 17.88. 0x0231 P0 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0231	3:0	R/W	P0_FRACN_MODE	P0 (IN0) input divider fractional mode. Must be set to 0xB for proper operation.
0x0231	4	R/W	P0_FRAC_EN	P0 (IN0) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 17.89. 0x0232 P1 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0232	3:0	R/W	P1_FRACN_MODE	P1 (IN1) input divider fractional mode. Must be set to 0xB for proper operation.
0x0232	4	R/W	P1_FRAC_EN	P1 (IN1) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 17.90. 0x0233 P2 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0233	3:0	R/W	P2_FRACN_MODE	P2 (IN2) input divider fractional mode. Must be set to 0xB for proper operation.
0x0233	4	R/W	P2_FRAC_EN	P2 (IN2) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 17.91. 0x0234 P3 Fractional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0234	3:0	R/W	P3_FRACN_MODE	P3 (IN3) input divider fractional mode. Must be set to 0xB for proper operation.
0x0234	4	R/W	P3_FRAC_EN	P3 (IN3) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 17.92. 0x0235-0x023A MXAXB Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0235	7:0	R/W	MXAXB_NUM	44-bit Integer Number
0x0236	15:8	R/W	MXAXB_NUM	
0x0237	23:16	R/W	MXAXB_NUM	
0x0238	31:24	R/W	MXAXB_NUM	
0x0239	39:32	R/W	MXAXB_NUM	
0x023A	43:40	R/W	MXAXB_NUM	

Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in 4.2 Dynamic PLL Changes are followed.

Table 17.93. 0x023B-0x023E MXAXB Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x023B	7:0	R/W	MXAXB_DEN	32-bit Integer Number
0x023C	15:8	R/W	MXAXB_DEN	
0x023D	23:16	R/W	MXAXB_DEN	
0x023E	31:24	R/W	MXAXB_DEN	

The M-divider numerator and denominator are set by ClockBuilder Pro for a given frequency plan. Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in 4.2 Dynamic PLL Changes are followed.

Table 17.94. 0x023F MXAXB Update

Reg Address	Bit Field	Type	Setting Name	Description
0x023F	0	S	MXAXB_UPDATE	Set to 1 to update the MXAXB_NUM and MXAXB_DEN values. A SOFT_RST may also be used to update these values.

Table 17.95. 0x0250-0x0252 R0 Divider

Reg Address	Bit Field	Type	Name	Description
0x0250	7:0	R/W	R0_REG	A 24 bit integer divide value divide value = (R0_REG+1) x 2 To set R0 = 2, set OUT0_RDIV_FORCE2 = 1 and then the R0_REG value is irrelevant.
0x0251	15:8	R/W	R0_REG	
0x0252	23:16	R/W	R0_REG	

The R dividers are at the output clocks and are purely integer division. The R1–R3 dividers follow the same format as the R0 divider described above.

Table 17.96. Registers that Follow the R0_REG

Register Address	Description	Size	Same as Address
0x0253–0x0255	R1_REG	24-bit Integer Number	0x0250–0x052
0x025C–0x025E	R2_REG	24-bit Integer Number	0x0250–0x0252
0x025F–0x0261	R3_REG	24-bit Integer Number	0x0250–0x0252

Table 17.97. 0x026B-0x0272 User Scratch Pad

Reg Address	Bit Field	Type	Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by CBPro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, “ULT.1A” with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6:0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Table 17.98. 0x0278-0x027C OPN Identifier

Reg Address	Bit Field	Type	Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: 5394C-A12345-GM, 12345 is the OPN unique identifier, which sets: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5394C-A12345-GM.

Applies to a “custom” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5394C-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5394 but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 17.99. 0x027D

Reg Address	Bit Field	Type	Setting Name	Description
0x027D	7:0	R/W	OPN_REVISION	

Table 17.100. 0x027E

Reg Address	Bit Field	Type	Setting Name	Description
0x027E	7:0	R/W	BASELINE_ID	

Table 17.101. OOFx_TRG_THR_EXT

Reg Address	Bit Field	Type	Setting Name	Description
0x028A	4:0	R/W	OOF0_TRG_THR_EXT	Set by CBPro.
0x028B	4:0	R/W	OOF1_TRG_THR_EXT	Set by CBPro.
0x028C	4:0	R/W	OOF2_TRG_THR_EXT	Set by CBPro.
0x028D	4:0	R/W	OOF3_TRG_THR_EXT	Set by CBPro.

Table 17.102. OOFx_CLR_THR_EXT

Reg Address	Bit Field	Type	Setting Name	Description
0x028E	4:0	R/W	OOF0_CLR_THR_EXT	Set by CBPro.
0x028F	4:0	R/W	OOF1_CLR_THR_EXT	Set by CBPro.
0x0290	4:0	R/W	OOF2_CLR_THR_EXT	Set by CBPro.
0x0291	4:0	R/W	OOF3_CLR_THR_EXT	Set by CBPro.

Table 17.103. 0x0292 OOF_STOP_ON_LOS

Reg Address	Bit Field	Type	Name	Description
0x0292	3:0	R/W	OOF_STOP_ON_LOS	Set by CBPro

Table 17.104. 0x0293 OOF_CLEAR_ON_LOS

Reg Address	Bit Field	Type	Name	Description
0x0293	3:0	R/W	OOF_CLEAR_ON_LOS	Set by CBPro

Table 17.105. 0x0294 Fastlock Extend Scale

Reg Address	Bit Field	Type	Name	Description
0x0294	7:4	R/W	FASTLOCK_EXTEND_SCL	Scales LOLB_INT_TIM-ER_DIV256

Table 17.106. 0x0296 Fastlock Delay on Input Switch Enable

Reg Address	Bit Field	Type	Name	Description
0x0296	1	R/W	LOL_SLW_VALWIN_SELX	Set by CBPro.

Table 17.107. 0x0297 Fastlock Delay on Input Switch Enable

Reg Address	Bit Field	Type	Name	Description
0x0297	1	R/W	FASTLOCK_DLY_ONSW_EN	Set by CBPro.

Table 17.108. 0x0299 Fastlock Delay on LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x0299	1	R/W	FASTLOCK_DLY_ONLOL_EN	Set by CBPro.

Table 17.109. 0x029D-0x029F Fastlock Delay on LOL

Reg Address	Bit Field	Type	Name	Description
0x029D	7:0	R/W	FASTLOCK_DLY_ONLOL	Set by CBPro.
0x029E	15:8	R/W	FASTLOCK_DLY_ONLOL	
0x029F	19:16:	R/W	FASTLOCK_DLY_ONLOL	

Table 17.110. 0x02A9 Fastlock Delay on Input Switch

Reg Address	Bit Field	Type	Name	Description
0x02A9	7:0	R/W	FASTLOCK_DLY_ONSW	20-bit value. Set by CBPro.
0x02AA	15:8	R/W	FASTLOCK_DLY_ONSW	
0x02AB	19:16	R/W	FASTLOCK_DLY_ONSW	

Table 17.111. 0x02B7 LOL Delay from LOS

Reg Address	Bit Field	Type	Name	Description
0x02B7	3:2	R/W	LOL_NOSIG_TIME	Set by CBPro.

Table 17.112. 0x02B8

Reg Address	Bit Field	Type	Name	Description
0x02B8	1	R	LOL_LOS_REFCLK	Set by CBPro.

Table 17.113. 0x02BC LOS_CMOS_MIN_PER_EN

Reg Address	Bit Field	Type	Name	Description
0x02BC	7:6	R/W	LOS_CMOS_MIN_PER_EN	Set by CBPro.

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Table 17.114. 0x0302–0x0307 N0 Numerator

Reg Address	Bit Field	Type	Name	Description
0x0302	7:0	R/W	N0_NUM	44-bit Integer Number
0x0303	15:8	R/W	N0_NUM	The N0 value is N0_NUM/N0_DEN
0x0304	23:16	R/W	N0_NUM	
0x0305	31:24	R/W	N0_NUM	
0x0306	39:32	R/W	N0_NUM	
0x0307	43:40	R/W	N0_NUM	

The N dividers are interpolative dividers that are used as output dividers that feed into the R dividers. ClockBuilder Pro calculates the correct values for the N-dividers.

Table 17.115. 0x0308–0x030C N0 Denominator

Reg Address	Bit Field	Type	Name	Description
0x0308	7:0	R/W	N0_DEN	32-bit Integer Number
0x0309	15:8	R/W	N0_DEN	The N0 value is N0_NUM/N0_DEN
0x030A	23:16	R/W	N0_DEN	
0x030B	31:24	R/W	N0_DEN	
0x030C	0	S	N0_UPDATE	Set this bit to update the N0 divider.

This bit is provided so that all of the N0 divider bits can be changed at the same time. First, write all of the new values to the divider; then, set the update bit.

Table 17.116. Registers that Follow the N0_NUM and N0_DEN Definitions

Register Address	Description	Size	Same as Address
0x030D-0x0312	N1 Numerator	44-bit Integer Number	0x0302-0x0307
0x0313-0x0316	N1 Denominator	32-bit Integer Number	0x0308-0x030B
0x0317	N1_UPDATE	one bit	0x030C
0x0318-0x031D	N2 Numerator	44-bit Integer Number	0x0302-0x0307
0x031E-0x0321	N2 Denominator	32-bit Integer Number	0x0308-0x030B
0x0322	N2_UPDATE	one bit	0x030C
0x0323-0x0328	N3 Numerator	44-bit Integer Number	0x0302-0x0307
0x0329-0x032C	N3 Denominator	32-bit Integer Number	0x0308-0x030B
0x032D	N3_UPDATE	one bit	0x030C

Table 17.117. 0x0338 Global N Divider Update

Reg Address	Bit Field	Type	Name	Description
0x0338	1	S	N_UPDATE_ALL	Set this bit to update all four N dividers.

This bit is provided so that all of the divider bits can be changed at the same time. First, write all of the new values to the divider, then set the update bit.

Note: If the intent is to write to the N_UPDATE_ALL to have all dividers update at the same time then make sure only N_UPDATE_ALL bit gets set.

Table 17.118. 0x0339 FINC/FDEC Masks

Reg Address	Bit Field	Type	Name	Description
0x0339	4:0	R/W	N_FSTEP_MSK	0 to enable FINC/FDEC updates 1 to disable FINC/FDEC updates

Bit 0 corresponds to MultiSynth N0 N_FSTEP_MSK 0x0339[0]

Bit 1 corresponds to MultiSynth N1 N_FSTEP_MSK 0x0339[1]

Bit 2 corresponds to MultiSynth N2 N_FSTEP_MSK 0x0339[2]

Bit 3 corresponds to MultiSynth N3 N_FSTEP_MSK 0x0339[3]

Bit 4 is reserved.

Table 17.119. 0x033B–0x0340 N0 Frequency Step Word

Reg Address	Bit Field	Type	Name	Description
0x033B	7:0	R/W	N0_FSTEPW	44-bit Integer Number
0x033C	15:8	R/W	N0_FSTEPW	
0x033D	23:16	R/W	N0_FSTEPW	
0x033E	31:24	R/W	N0_ FSTEPW	
0x033F	39:32	R/W	N0_ FSTEPW	
0x0340	43:40	R/W	N0_ FSTEPW	

This is a 44-bit integer value which is directly added or subtracted from the N-divider. When FINC or FDEC is set to a 1, ClockBuilder Pro calculates the correct values for the N0 Frequency Step Word. Each N divider has the ability to add or subtract up to a 44-bit value.

Table 17.120. Registers that Follow the N0_FSTEPW Definition

Register Address	Description	Size	Same as Address
0x0341-0x0346	N1 Frequency Step Word	44-bit Integer Number	0x033B-0x0340
0x0347-0x034C	N2 Frequency Step Word	44-bit Integer Number	0x033B-0x0340
0x034D-0x0352	N3 Frequency Step Word	44-bit Integer Number	0x033B-0x0340

Table 17.121. 0x0359–0x35A N0 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x0359	7:0	R/W	N0_DELAY[7:0]	Lower byte of N0_DELAY[15:0]
0x035A	7:0	R/W	N0_DELAY[15:8]	Upper byte of N0_DELAY[15:0]

Nx_DELAY[15:0] is a 2s complement number that sets the output delay of MultiSynthx.

The delay in seconds is Nx_DELAY/(256 x Fvco) where Fvco is the VCO frequency in Hz. The maximum positive and negative delay is ±(2^{15}–1)/(256 x Fvco). ClockBuilder Pro calculates the correct value for this register. Changing any of the Nx_DELAY values requires a SOFT_RST, a HARD_RST, or a power up sequence.

Table 17.122. 0x035B-0x035C Divider N1 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x35B	7:0	R/W	N1_DELAY[7:0]	Lower byte of N1_DELAY[15:0]
0x35C	7:0	R/W	N1_DELAY[15:8]	Upper byte of N1_DELAY[15:0]

Table 17.123. 0x035D-0x035E Divider N2 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x35D	7:0	R/W	N2_DELAY[7:0]	Lower byte of N2_DELAY[15:0]
0x35E	7:0	R/W	N2_DELAY[15:8]	Upper byte of N2_DELAY[15:0]

Table 17.124. 0x035F-0x0360 Divider N3 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x35F	7:0	R/W	N3_DELAY[7:0]	Lower byte of N3_DELAY[15:0]
0x360	7:0	R/W	N3_DELAY[15:8]	Upper byte of N3_DELAY[15:0]

Nx_DELAY[15:0] is a 2s complement number that sets the output delay of MultiSynthx.

The delay in seconds is Nx_DELAY/(256 x Fvco) where Fvco is the VCO frequency in Hz. The maximum positive and negative delay is ±(2^{15} – 1)/(256 x Fvco). ClockBuilder Pro calculates the correct value for this register.

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Table 17.125. 0x0487 Zero Delay Mode Setup

Reg Address	Bit Field	Type	Name	Description
0x0487	0	R/W	ZDM_EN	0 to disable ZD mode 1 to enable ZD mode
0x0487	2:1	R/W	ZDM_IN_SEL	Clock input select when in ZD mode. 0 for IN0, 1 for IN1,2 for IN2, 3 reserved Note: In ZD mode the feedback clock comes into IN3
0x0487	4	R/W	ZDM_AUTOSW_EN	Set by CBPro.

This register is used for enabling the zero delay mode (ZDM) and selecting the source. The phase difference between the output, which is connected to the selected input below will be nulled to zero. When in zero delay mode, the DSPLL cannot have either hitless or automatic switching. In addition, the frequency of the clock selected by ZDM_IN_SEL must either be the same or have a simple integer relationship to the clock at the FB_IN pins. Pin controlled clock selection is available in ZD mode (see register 0x052A).

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Table 17.126. 0x0507 Active Input

Reg Address	Bit Field	Type	Name	Description
0x0507	7:6	R	IN_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

Table 17.127. 0x0508–0x050D Loop Bandwidth

Reg Address	Bit Field	Type	Name	Description
0x0508	5:0	R/W	BW0_PLL	PLL bandwidth parameter
0x0509	5:0	R/W	BW1_PLL	PLL bandwidth parameter
0x050A	5:0	R/W	BW2_PLL	PLL bandwidth parameter
0x050B	5:0	R/W	BW3_PLL	PLL bandwidth parameter
0x050C	5:0	R/W	BW4_PLL	PLL bandwidth parameter
0x050D	5:0	R/W	BW5_PLL	PLL bandwidth parameter

This group of registers determine the loop bandwidth for the DSPLL. It is selectable as 0.1 Hz, 1 Hz, 4 Hz, 10 Hz, 40 Hz, 100 Hz, 400 Hz, 1 kHz, and 4 kHz. The loop BW values are calculated by ClockBuilder Pro and are written into these registers. The BW_UPDATE_PLL bit (reg 0x0514[0]) must be set to cause the BWx_PLL parameters to take effect.

Table 17.128. 0x050E–0x0514 Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Name	Description
0x050E	5:0	R/W	FAST-LOCK_BW0_PLL	PLL fast bandwidth parameter
0x050F	5:0	R/W	FAST-LOCK_BW1_PLL	PLL fast bandwidth parameter
0x0510	5:0	R/W	FAST-LOCK_BW2_PLL	PLL fast bandwidth parameter
0x0511	5:0	R/W	FAST-LOCK_BW3_PLL	PLL fast bandwidth parameter
0x0512	5:0	R/W	FAST-LOCK_BW4_PLL	PLL fast bandwidth parameter
0x0513	5:0	R/W	FAST-LOCK_BW5_PLL	PLL fast bandwidth parameter
0x0514	0	S	BW_UPDATE_PLL	Must be set to 1 to update the BWx_PLL and FAST_BWx_PLL parameters

The fast lock loop BW values are calculated by ClockBuilder Pro and used when fast lock is enabled.

Table 17.129. 0x0515–0x051B M Divider Numerator, 56-bits

Reg Address	Bit Field	Type	Name	Description
0x0515	7:0	R/W	M_NUM	56-bit Number
0x0516	15:8	R/W	M_NUM	
0x0517	23:16	R/W	M_NUM	
0x0518	31:24	R/W	M_NUM	
0x0519	39:32	R/W	M_NUM	
0x051A	47:40	R/W	M_NUM	
0x051B	55:48	R/W	M_NUM	

Table 17.130. 0x051C–0x051F M Divider Denominator, 32-bits

Reg Address	Bit Field	Type	Name	Description
0x051C	7:0	R/W	M_DEN	32-bit Number
0x051E	15:8	R/W	M_DEN	
0x051E	23:16	R/W	M_DEN	
0x051F	31:24	R/W	M_DEN	

The loop M divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 17.131. 0x0520 M Divider Update Bit

Reg Address	Bit Field	Type	Name	Description
0x0520	0	S	M_UPDATE	Set this bit to update the M divider.

Table 17.132. 0x0521 DSPLL M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0521	3:0	R/W	M_FRAC_MODE	M feedback divider fractional mode. Must be set to 0xB for proper operation.
0x0521	4	R/W	M_FRAC_EN	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0521	5	R/W	Reserved	Must be set to 1

Table 17.133. 0x052A Input Clock Select

Reg Address	Bit Field	Type	Name	Description
0x052A	0	R/W	IN_SEL_REGCTRL	0 for pin controlled clock selection 1 for register controlled clock selection

Reg Address	Bit Field	Type	Name	Description
0x052A	2:1	R/W	IN_SEL	0 for IN0, 1 for IN1, 2 for IN2, 3 for IN3 (or FB_IN)

Input clock selection for manual register based and pin controlled clock selection. Note: when ZDM_EN (0x0487, bit 0) and IN_SEL_REGCTRL are both high, IN_SEL does not do anything.

Table 17.134. 0x052B Fast Lock Control

Reg Address	Bit Field	Type	Name	Description
0x052B	0	R/W	FASTLOCK_AUTO_EN	Applies only when FASTLOCK_MAN = 0 (see below): 0 to disable auto fast lock when the DSPLL is out of lock 1 to enable auto fast lock
0x052B	1	R/W	FASTLOCK_MAN	0 for normal operation (see above) 1 to force fast lock

When in fast lock, the fast lock loop BW can be automatically used.

Table 17.135. 0x052C Holdover Exit Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052C	0	R/W	HOLD_EN	Holdover enable 0: Holdover Disabled 1: Holdover Enabled (default)
0x052C	3	R/W	HOLD_RAMP_BYP	HOLD_RAMP_BYP
0x052C	4	R/W	HOLDEXIT_BW_SEL1	Holdover Exit Bandwidth select. Selects the exit bandwidth from Holdover when ramped exit is disabled (HOLD_RAMP_BYP = 1). 0: Exit Holdover using Holdover Exit or Fastlock bandwidths (default). See HOLDEXIT_BW_SEL0 (0x059B[6]) for additional information. 1: Exit Holdover using the Normal loop bandwidth
0x052C	7:5	R/W	RAMP_STEP_INTERVAL	Time Interval of the frequency ramp steps when ramping between inputs or when exiting holdover. Calculated by CBPro based on selection.

Table 17.136. 0x052D

Reg Address	Bit Field	Type	Name	Description
0x052D	1	R/W	HOLD_RAMPBYP_NOHIST	Set by CBPro.

Table 17.137. 0x052E Holdover History Average Length

Reg Address	Bit Field	Type	Name	Description
0x052E	4:0	R/W	HOLD_HIST_LEN	5-bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency.

time (s) = $((2^{LEN}) - 1) \times 268$ ns

Table 17.138. 0x052F Holdover History Delay

Reg Address	Bit Field	Type	Name	Description
0x052F	4:0	R/W	HOLD_HIST_DELAY	5-bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past, above the averaging window. The amount that the average window is delayed is the holdover history delay.

time(s) = $(2^{DELAY}) \times 268$ ns

Table 17.139. 0x0531

Reg Address	Bit Field	Type	Setting Name	Description
0x0531	4:0	R/W	HOLD_REF_COUNT_FRC	5- bit value

Table 17.140. 0x0532–0x0534

Reg Address	Bit Field	Type	Setting Name	Description
0x0532	7:0	R/W	HOLD_15M_CYC_COUNT	Value calculated by CBPro
0x0533	15:8	R/W	HOLD_15M_CYC_COUNT	
0x0534	23:16	R/W	HOLD_15M_CYC_COUNT	

Table 17.141. 0x0535 Force Holdover

Reg Address	Bit Field	Type	Name	Description
0x0535	0	R/W	FORCE_HOLD	0 for normal operation 1 for force holdover

Table 17.142. 0x0536 Input Clock Switching Control

Reg Address	Bit Field	Type	Name	Description
0x0536	1:0	R/W	CLK_SWTCH_MODE	0 = manual 1 = automatic/non-revertive 2 = automatic/revertive 3 = reserved

Reg Address	Bit Field	Type	Name	Description
0x0536	2	R/W	HSW_EN	0 glitchless switching mode (phase buildout turned off) 1 hitless switching mode (phase buildout turned on) Note that hitless switching is not available in zero delay mode.

Table 17.143. 0x0537 Input Alarm Masks

Reg Address	Bit Field	Type	Name	Description
0x0537	3:0	R/W	IN_LOS_MSK	For each clock input LOS alarm: 0 to use LOS in the clock selection logic 1 to mask LOS from the clock selection logic
0x0537	7:4	R/W	IN_OOF_MSK	For each clock input OOF alarm: 0 to use OOF in the clock selection logic 1 to mask OOF from the clock selection logic

This register is for the input clock switch alarm masks. For each of the four clock inputs, the OOF and/or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

Table 17.144. 0x0538 Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Name	Description
0x0538	2:0	R/W	IN0_PRIORITY	The priority for clock input 0 is: 0 No Priority 1 for priority 1 2 for priority 2 3 for priority 3 4 for priority 4 5 to 7 are reserved
0x0538	6:4	R/W	IN1_PRIORITY	The priority for clock input 1 is: 0 No Priority 1 for priority 1 2 for priority 2 3 for priority 3 4 for priority 4 5 to 7 are reserved

This register is used to assign a priority to an input clock for automatic clock input switching. The available clock with the lowest priority level will be selected. When input clocks are assigned the same priority, they will use the following default priority list: 0, 1, 2, 3.

Table 17.145. 0x0539 Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Name	Description
0x0539	2:0	R/W	IN2_PRIORITY	The priority for clock input 2 is: 0 No Priority 1 for priority 1 2 for priority 2 3 for priority 3 4 for priority 4 5 to 7 are reserved
0x0539	6:4	R/W	IN3_PRIORITY	The priority for clock input 3 is: 0 No Priority 1 for priority 1 2 for priority 2 3 for priority 3 4 for priority 4 5 to 7 are reserved

This register is used to assign a priority to an input clock for automatic clock input switching. The available clock with the lowest priority level will be selected. When input clocks are assigned the same priority, they will use the following priority list: 0, 1, 2, 3.

Table 17.146. 0x053A Hitless Switching Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x053A	1:0	R/W	HSW_MODE	1: Default setting, do not modify 0, 2, 3: Reserved
0x053A	3:2	R/W	HSW_PHMEAS_CTRL	0: Default setting, do not modify 1, 2, 3: Reserved

Table 17.147. 0x053B–0x053C Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Name	Description
0x053B	7:0	R/W	HSW_PHMEAS_THR	10-bit value. Set by CBPro.
0x053C	9:8	R/W	HSW_PHMEAS_THR	

Table 17.148. 0x053D

Reg Address	Bit Field	Type	Name	Description
0x053D	4:0	R/W	HSW_COARSE_PM_LEN	Set by CBPro.

Table 17.149. 0x053E

Reg Address	Bit Field	Type	Name	Description
0x053E	4:0	R/W	HSW_COARSE_PM_DLY	Set by CBPro.

Table 17.150. 0x053F

Reg Address	Bit Field	Type	Name	Description
0x053F	1	R	HOLD_HIST_VALID	1 = there is enough historical frequency data collected for valid holdover.
0x053F	2	R	FASTLOCK_STATUS	1 = PLL is in Fast Lock operation

Table 17.151. 0x0540 Reserved

Reg Address	Bit Field	Type	Name	Description
0x0540	7:0	R/W	RESERVED	This register is used when making certain changes to the device. See Section 4.2 Dynamic PLL Changes for more information.

This register is used when making certain changes to the device. See Section 4.2 Dynamic PLL Changes for more information.

Table 17.152. 0x0588 Hitless Switching Length

Reg Address	Bit Field	Type	Setting Name	Description
0x0588	3:0	R/W	HSW_FINE_PM_LEN	Set by CBPro.

Table 17.153. 0x0589–0x058A PFD Enable Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x0589	7:0	R/W	PFD_EN_DELAY	Set by CBPro.
0x058A	12:8	R/W	PFD_EN_DELAY	

Table 17.154. 0x058B–0x058D

Reg Address	Bit Field	Type	Setting Name	Description
0x058B	7:0	R/W	HSW_MEAS_SETTLE	Set by CBPro.
0x058C	15:8	R/W	HSW_MEAS_SETTLE	Set by CBPro.
0x058D	19:16	R/W	HSW_MEAS_SETTLE	Set by CBPro.

Table 17.155. 0x059B Holdover Exit

Reg Address	Bit Field	Type	Setting Name	Description
0x059B	1	R/W	INIT_LP_CLOSE_HO	Set by CBPro.
0x059B	4	R/W	HOLD_PRESERVE_HIST	Set by CBPro
0x059B	5	R/W	HOLD_FRZ_WITH_INTONLY	Set by CBPro

Reg Address	Bit Field	Type	Setting Name	Description
0x059B	6	R/W	HOLDEXIT_BW_SEL0	Set by CBPro See HOLDEXIT_BW_SEL1
0x059B	7	R/W	HOLDEXIT_STD_BO	Set by CBPro.

Table 17.156. 0x059C

Reg Address	Bit Field	Type	Setting Name	Description
0x059C	7	R/W	HOLD_RAMPBP_NOHIST	Set by CBPro

Table 17.157. 0x059C

Reg Address	Bit Field	Type	Setting Name	Description
0x059C	6	R/W	HOLDEXIT_ST_BO	Set by CBPro

Table 17.158. 0x059D Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x059D	5:0	R/W	HOLDEXIT_BW0	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 17.159. 0x059E Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x059E	5:0	R/W	HOLDEXIT_BW1	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 17.160. 0x059F Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x059F	5:0	R/W	HOLDEXIT_BW2	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 17.161. 0x05A0 Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x05A0	5:0	R/W	HOLDEXIT_BW3	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 17.162. 0x05A1 Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x05A1	5:0	R/W	HOLDEXIT_BW4	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 17.163. 0x059A2 Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x05A2	5:0	R/W	HOLDEXIT_BW5	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 17.164. 0x05A4

Reg Address	Bit Field	Type	Setting Name	Description
0x05A4	7:0	R/W	HSW_LIMIT	Set by CBPro

Table 17.165. 0x05A5

Reg Address	Bit Field	Type	Setting Name	Description
0x05A5	0	R/W	HSW_LIMIT_ACTION	Set by CBPro

Table 17.166. 0x05A6 Hitless Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x05A6	2:0	R/W	RAMP_STEP_SIZE	Size of the frequency ramp steps when ramping between inputs or when exiting holdover. Calculated by CBPro based on selection.
0x05A6	3	R/W	RAMP_SWITCH_EN	Ramp Switching Enable 0: Disable Ramp Switching 1: Enable Ramp Switching (default)

Table 17.167. 0x05AC

Reg Address	Bit Field	Type	Setting Name	Description
0x05AC	0	R/W	OUT_MAX_LIMIT_EN	Set by CBPro

Table 17.168. 0x05AC

Reg Address	Bit Field	Type	Setting Name	Description
0x05AC	3	R/W	HOLD_SETTLE_DET_EN	Set by CBPro

Table 17.169. 0x05AD–0x05AE

Reg Address	Bit Field	Type	Setting Name	Description
0x05AD	7:0	R/W	OUT_MAX_LIMIT_LMT	Set by CBPro
0x05AE	15:8	R/W	OUT_MAX_LIMIT_LMT	Set by CBPro

Table 17.170. 0x05B1–0x05B2

Reg Address	Bit Field	Type	Setting Name	Description
0x05B1	7:0	R/W	HOLD_SETTLE_TARGET	Set by CBPro
0x05B2	15:8	R/W	HOLD_SETTLE_TARGET	Set by CBPro

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Table 17.171. 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	0 to use a crystal at the XAXB pins 1 to use an external clock source at the XAXB pins

Table 17.172. 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Name	Description
0x0943	0	R/W	IO_VDD_SEL	0 for 1.8 V external connections 1 for 3.3 V external connections

The IO_VDD_SEL configuration bit selects the option of operating the serial interface, and other control/status IO which are not controlled by VDDS via either the VDD or VDDA pins. These pins are always 3.3 V tolerant even when the device's VDD pin is supplied from a 1.8 V source. When the I^2C or SPI host is operating at 3.3 V and the Si5395/94/92 at VDD = 1.8 V, the host must write the IO_VDD_SEL configuration bit to the VDDA option. This will ensure that both the host and the serial interface are operating at the optimum voltage thresholds. The pins that are controlled by the IO_VDD_SEL bit are I2C_SEL, IN_SEL, RSTb, OEb, A1, SCLK, A0/CSb, SDA/SDIO, INTRb, SDO.

Table 17.173. 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Name	Description
0x0949	3:0	R/W	IN_EN	0: Disable and Powerdown Input Buffer. 1: Enable Input Buffer for IN3–IN0.
0x0949	7:4	R/W	IN_PULSED_CMOS_EN	0: Standard Input Format. 1: Pulsed CMOS Input Format for IN3–IN0. See Section 5. Clock Inputs for more information.

When a clock input is disabled, it is powered down.

Input 0 corresponds to IN_SEL 0x0949 [0], IN_PULSED_CMOS_EN 0x0949 [4]

Input 1 corresponds to IN_SEL 0x0949 [1], IN_PULSED_CMOS_EN 0x0949 [5]

Input 2 corresponds to IN_SEL 0x0949 [2], IN_PULSED_CMOS_EN 0x0949 [6]

Input 3 corresponds to IN_SEL 0x0949 [3], IN_PULSED_CMOS_EN 0x0949 [7]

Table 17.174. 0x094A Input Clock Enable to DSPLL

Reg Address	Bit Field	Type	Setting Name	Description
0x094A	3:0	R/W	INX_TO_PFD_EN	Value calculated in CBPro

Table 17.175. 0x094E–0x094F Input Clock Buffer Hysteresis

Reg Address	Bit Field	Type	Setting Name	Description
0x094E	7:0	R/W	REFCLK_HYS_SEL	Value calculated in CBPro
0x094F	3:0	R/W	REFCLK_HYS_SEL	Value calculated in CBPro

Table 17.176. 0x094F CMOS High Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x094F	7:4	R/W	IN_CMOS_USE1P8	0 = selects the Pulsed CMOS input buffer mode 1 = selects the LVCMOS input buffer mode

Table 17.177. 0x095E MXAXB Fractional Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x095E	0	R/W	MXAXB_INTE-GER	Set by CBPro.

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Table 17.178. 0x0A02 Output Multisynth Integer Divide Mode

Reg Address	Bit Field	Type	Name	Description
0x0A02	4:0	R/W	N_ADD_0P5	Value calculated in CBPro

Table 17.179. 0x0A03 Output Multisynth Clock to Output Driver

Reg Address	Bit Field	Type	Name	Description
0x0A03	4:0	R/W	N_CLK_TO_OUTX_EN	Routes Multisynth outputs to output driver muxes.

Table 17.180. 0x0A04 Output Multisynth Integer Divide Mode

Reg Address	Bit Field	Type	Name	Description
0x0A04	4:0	R/W	N_PIBYP	Output Multisynth integer divide mode. Bit 0 for ID0, Bit 1 for ID1, etc. 0: Nx divider is fractional. 1: Nx divider is integer.

A soft reset reg 0x001C [0] should be asserted after changing any of these bits. If it is expected that any of the N dividers will be changing from integer to fractional, it is recommended that the corresponding bits be initialized to 0 so that when the change from integer to fractional occurs there will be no need for a soft reset. For this reason, the DCO (digitally controlled oscillator) and FOTF (frequency on the fly) applications should have zeros for these bits. See AN858: DCO Applications with Jitter Attenuators for more information.

Table 17.181. 0x0A05 Output Multisynth Divider Power Down

Reg Address	Bit Field	Type	Name	Description
0x0A05	4:0	R/W	N_PDNB	Powers down the N dividers. Set to 0 to power down unused N dividers. Must set to 1 for all active N dividers. See also related registers 0x0A03 and 0x0B4A.

Table 17.182. Nx_HIGH_FREQ

Reg Address	Bit Field	Type	Name	Description
0x0A14	3	R/W	N0_HIGH_FREQ	Set by CBPro.
0x0A1A	3	R/W	N1_HIGH_FREQ	Set by CBPro.
0x0A20	3	R/W	N2_HIGH_FREQ	Set by CBPro.
0x0A26	3	R/W	N3_HIGH_FREQ	Set by CBPro.

Table 17.183. 0x0A38 N0 Dynamic Phase Adjust Step Size

Reg Address	Bit Field	Type	Name	Description
0x0A38	7:0	R/W	N0_PHASE_STEP	N0 step size from 1 to 255 in units of Tvco, the VCO period.

N0_PHASE_STEP and N0_PHASE_COUNT are used to produce a phase change anywhere from 0 degrees to 360 degrees with a resolution of the VCO period. N0_PHASE_STEP can be invoked multiple times by using N0_PHASE_COUNT. The phase change is initiated by writing to either N0_PHASE_INC or N0_PHASE_DEC (at addr 0x0A3B). The resulting phase change will be:

N0_PHASE_STEP * N0_PHASE_COUNT * Tvco, for Tvco = 1 / Fvco

Table 17.184. 0x0A39 N0 Dynamic Phase Adjust Step Size Count

Reg Address	Bit Field	Type	Name	Description
0x0A39	7:0	R/W	N0_PHASE_COUNT	Lower byte of number of N0 step size changes.
0x0A3A	15:8	R/W	N0_PHASE_COUNT	Upper byte of number of N0 step size changes.

Table 17.185. 0x0A3B N0 Dynamic Phase Adjust Command

Reg Address	Bit Field	Type	Name	Description
0x0A3B	0	R/W	N0_PHASE_INC	Writing a 1 initiates a phase increment.
0x0A3B	1	R/W	N0_PHASE_DEC	Writing a 1 initiates a phase decrement.

Once set, these register bits will self clear as soon as the entire phase adjust sequence has completed.

N1 dynamic phase adjust works the same as N0 dynamic phase adjust (0xA38).

Table 17.186. 0x0A3C N1 Dynamic Phase Adjust Step Size

Reg Address	Bit Field	Type	Name	Description
0x0A3C	7:0	R/W	N1_PHASE_STEP	N1 step size from 1 to 255 in units of Tvco, the VCO period.

Table 17.187. 0x0A3D N1 Dynamic Phase Adjust Step Size Count

Reg Address	Bit Field	Type	Name	Description
0x0A3D	7:0	R/W	N1_PHASE_COUNT	Lower byte of number of N1 step size changes.
0x0A3E	15:8	R/W	N1_PHASE_COUNT	Upper byte of number of N1 step size changes.

Table 17.188. 0x0A3F N1 Dynamic Phase Adjust Command

Reg Address	Bit Field	Type	Name	Description
0x0A3F	0	R/W	N1_PHASE_INC	Writing a 1 initiates a phase increment.
0x0A3F	1	R/W	N1_PHASE_DEC	Writing a 1 initiates a phase decrement.

N2 dynamic phase adjust works the same as N0 dynamic phase adjust (0xA38).

Table 17.189. 0x0A40 N2 Dynamic Phase Adjust Step Size

Reg Address	Bit Field	Type	Name	Description
0x0A40	7:0	R/W	N2_PHASE_STEP	N2 step size from 1 to 255 in units of Tvco, the VCO period.

Table 17.190. 0x0A41 N2 Dynamic Phase Adjust Step Size Count

Reg Address	Bit Field	Type	Name	Description
0x0A41	7:0	R/W	N2_PHASE_COUNT	Lower byte of number of N2 step size changes.
0x0A42	15:8	R/W	N2_PHASE_COUNT	Upper byte of number of N2 step size changes.

Table 17.191. 0x0A3 N2 Dynamic Phase Adjust Command

Reg Address	Bit Field	Type	Name	Description
0x0A43	0	R/W	N2_PHASE_INC	Writing a 1 initiates a phase increment.
0x0A43	1	R/W	N2_PHASE_DEC	Writing a 1 initiates a phase decrement.

N3 dynamic phase adjust works the same as N0 dynamic phase adjust (0xA38).

Table 17.192. 0x0A44 N3 Dynamic Phase Adjust Step Size

Reg Address	Bit Field	Type	Name	Description
0x0A44	7:0	R/W	N3_PHASE_STEP	N3 step size from 1 to 255 in units of Tvco, the VCO period.

Table 17.193. 0x0A45 N3 Dynamic Phase Adjust Step Size Count

Reg Address	Bit Field	Type	Name	Description
0x0A45	7:0	R/W	N3_PHASE_COUNT	Lower byte of number of N3 step size changes.
0x0A46	15:8	R/W	N3_PHASE_COUNT	Upper byte of number of N3 step size changes.

Table 17.194. 0x0A47 N3 Dynamic Phase Adjust Command

Reg Address	Bit Field	Type	Name	Description
0x0A47	0	R/W	N3_PHASE_INC	Writing a 1 initiates a phase increment.
0x0A47	1	R/W	N3_PHASE_DEC	Writing a 1 initiates a phase decrement.

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Table 17.195. 0x0B24

Reg Address	Bit Field	Type	Name	Description
0x0B24	7:0	R/W	RERSERVED	Reserved This register is used when making certain changes to the device. See Section 4.2 Dynamic PLL Changes for more information.

Table 17.196. 0x0B25

Reg Address	Bit Field	Type	Name	Description
0x0B25	7:0	R/W	RERSERVED	Reserved This register is used when making certain changes to the device. See Section 4.2 Dynamic PLL Changes for more information.

Table 17.197. 0x0B44 Output Multisynth Clock to Output Driver

Reg Address	Bit Field	Type	Name	Description
0x0B44	3:0	R/W	PDIV_FRACN_CLK_DIS	Disable digital clocks to input P (IN0–3) fractional dividers.
0x0B44	5	R/W	FRACN_CLK_DIS_PLL	Disable digital clock to M fractional divider.

Table 17.198. 0x0B46

Reg Address	Bit Field	Type	Name	Description
0x0B46	3:0	R/W	LOS_CLK_DIS	Set to 0 for normal operation.

Table 17.199. 0x0B47

Reg Address	Bit Field	Type	Name	Description
0x0B47	4:0	R/W	OOF_CLK_DIS	Set to 0 for normal operation.

Table 17.200. 0x0B48 OOF Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B48	4:0	R/W	OOF_DIV_CLK_DIS	Set to 0 for normal operation Digital OOF divider clock user disable. Bits 3:0 are for IN3,2,1,0, Bit 4 is for OOF for the XAXB input.

Table 17.201. 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	4:0	R/W	N_CLK_DIS	Disable digital clocks to N dividers. Must be set to 0 to use each N divider. See also related registers 0x0A03 and 0x0A05.

Table 17.202. 0x0B57-0x0B58 VCO Calcode

Reg Address	Bit Field	Type	Name	Description
0x0B57	7:0	R/W	VCO_RESET_CALCODE	12-bit value. Controls the VCO frequency when a reset occurs.
0x0B58	11:8	R/W	VCO_RESET_CALCODE	

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Table 17.203. 0x0C02

Reg Address	Bit Field	Type	Name	Description
0x0C02	2:0	R/W	VAL_DIV_CTL0	Set by CBPro

Table 17.204. 0x0C02

Reg Address	Bit Field	Type	Name	Description
0x0C02	4	R/W	VAL_DIV_CTL1	Set by CBPro

Table 17.205. 0x0C03

Reg Address	Bit Field	Type	Name	Description
0x0C03	3:0	R/W	IN_CLK_VAL_PWR_UP_DIS	Set by CBPro

Table 17.206. 0x0C07

Reg Address	Bit Field	Type	Name	Description
0x0C07	0	R/W	IN_CLK_VAL_EN	Set by CBPro

Table 17.207. 0x0C08

Reg Address	Bit Field	Type	Name	Description
0x0C08	7:0	R/W	IN_CLK_VAL_TIME	Set by CBPro

18. Si5392 Register Definitions

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Table 18.1. 0x0001 Page

Reg Address	Bit Field	Type	Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

There is the “Page Register” which i s located at address 0x01 on every page. When read, it will indicate the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, … etc.

Table 18.2. 0x0002–0x0003 Base Part Number

Reg Address	Bit Field	Type	Name	Value	Description
0x0002	7:0	R	PN_BASE	0x92	Four-digit “base” part number, one nibble per digit Example: Si5392A-A-GM. The base part number (OPN) is 5392, which is stored in this register.
0x0003	15:8	R	PN_BASE	0x53	

Table 18.3. 0x0004 Device Grade

Reg Address	Bit Field	Type	Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed/ synthesis mode 0 = A, 1 = B, 2 = C, 3 = D , 4 =E 9=J, 10=K,11=L,12=M,15=P etc

Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 18.4. 0x0005 Device Revision

Reg Address	Bit Field	Type	Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B, etc. Example Si5392C-A12345-GM, the device revision is “A” and stored as 0.

Table 18.5. 0x0006–0x0008 TOOL_VERSION

Reg Address	Bit Field	Type	Name	Description
0x0006	3:0	R/W	TOOL_VERSION[3:0]	Special
0x0006	7:4	R/W	TOOL_VERSION[7:4]	Revision
0x0007	7:0	R/W	TOOL_VERSION[15:8]	Minor[7:0]
0x0008	0	R/W	TOOL_VERSION[15:8]	Minor[8]
0x0008	4:1	R/W	TOOL_VERSION[16]	Major
0x0008	7:5	R/W	TOOL_VERSION[13:17]	Tool. 0 for ClockBuilder Pro

The software tool version that created the register values that are downloaded at power up is represented by TOOL_VERSION.

Table 18.6. 0x0009 Temperature Grade

Reg Address	Bit Field	Type	Name	Description
0x0009	7:0	R/W	TEMP_GRADE	Device temperature grading 0 = Industrial (–40° C to 85° C) ambient conditions

Table 18.7. 0x000A Package ID

Reg Address	Bit Field	Type	Name	Description
0x000A	7:0	R/W	PKG_ID	Package ID 1 = 7 x 7 mm 44-QFN

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5392-A12345-GM.

Applies to a “base” or “blank” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5392C-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5392 but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 18.8. 0x000B I^2C Address

Reg Address	Bit Field	Type	Setting Name	Description
0x000B	6:2	R/W	I2C_ADDR	The upper 5 bits of the 7 bit I^2C address. The lower 2 bits are controlled by the A1 and A0 pins. Note: This register is not bank burnable.

Table 18.9. 0x000C Internal Status Bits

Reg Address	Bit Field	Type	Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	3	R	XAXB_ERR	1 if there is a problem locking to the XAXB input signal.
0x000C	5	R	SMBUS_TIMEOUT	1 if there is an SMBus timeout error.

Bit 1 is the LOS status monitor for the XTAL or REFCLK at the XA/XB pins.

Table 18.10. 0x000D Out-of-Frequency (OOF) and Loss-of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Name	Description
0x000D	3:0	R	LOS	1 if the clock input is currently LOS

Reg Address	Bit Field	Type	Name	Description
0x000D	7:4	R	OOF	1 if the clock input is currently OOF

Note that each bit corresponds to the input. The LOS and OOF bits are not sticky.

Input 0 (IN0) corresponds to LOS 0x000D [0], OOF 0x000D [4]

Input 1 (IN1) corresponds to LOS 0x000D [1], OOF 0x000D [5]

Input 2 (IN2) corresponds to LOS 0x000D [2], OOF 0x000D [6]

Input 3 (IN3) corresponds to LOS 0x000D [3], OOF 0x000D [7]

Table 18.11. 0x000E Holdover and LOL Status

Reg Address	Bit Field	Type	Name	Description
0x000E	1	R	LOL	1 if the DSPLL is out of lock
0x000E	5	R	HOLD	1 if the DSPLL is in holdover (or free run)

These status bits indicate if the DSPLL is in holdover and if it is in Loss of Lock. These bits are not sticky.

Table 18.12. 0x000F Calibration Status

Reg Address	Bit Field	Type	Name	Description
0x000F	5	R	CAL_PLL	1 if the DSPLL internal calibration is busy

This status bit indicates if a DSPLL is currently busy with calibration. This bit is not sticky.

Table 18.13. 0x0011 Internal Error Flags

Reg Address	Bit Field	Type	Name	Description
0x0011	0	R/W	SYSINCAL_FLG	Sticky version of SYSINCAL. Write a 0 to this bit to clear.
0x0011	1	R/W	LOSXAXB_FLG	Sticky version of LOSXAXB. Write a 0 to this bit to clear.
0x0011	3	R/W	XAXB_ERR_FLG	Sticky version of XAXB_ERR.Write a 0 to this bit to clear.
0x0011	5	R/W	SMBUS_TIMEOUT_FLG	Sticky version of SMBUS_TIMEOUT. Write a 0 to this bit to clear.

If any of these six bits are high, there is an internal fault. Please contact Silicon Labs. These are sticky flag bits. They are cleared by writing zero to the bit that has been set.

Table 18.14. 0x0012 Sticky OOF and LOS Flags

Reg Address	Bit Field	Type	Name	Description
0x0012	3:0	R/W	LOS_FLG	1 if the clock input is LOS for the given input
0x0012	7:4	R/W	OOF_FLG	1 if the clock input is OOF for the given input

These are the sticky flag versions of register 0x000D. These bits are cleared by writing 0 to the bits that have been set.

Input 0 (IN0) corresponds to LOS_FLG 0x0012 [0], OOF_FLG 0x0012 [4]

Input 1 (IN1) corresponds to LOS_FLG 0x0012 [1], OOF_FLG 0x0012 [5]

Input 2 (IN2) corresponds to LOS_FLG 0x0012 [2], OOF_FLG 0x0012 [6]

Input 3 (IN3) corresponds to LOS_FLG 0x0012 [3], OOF_FLG 0x0012 [7]

Table 18.15. 0x0013 Sticky Holdover and LOL Flags

Reg Address	Bit Field	Type	Name	Description
0x0013	1	R/W	LOL_FLG	1 if the DSPLL was unlocked
0x0013	5	R/W	HOLD_FLG	1 if the DSPLL was in holdover or free run

These are the sticky flag versions of register 0x000E. These bits are cleared by writing 0 to the bits that have been set.

Table 18.16. 0x0014 Sticky INCAL Flag

Reg Address	Bit Field	Type	Name	Description
0x0014	5	R/W	CAL_FLG_PLL	1 if the internal calibration was busy

This bit is the sticky flag version of 0x000F. This bit is cleared by writing 0 to bit 5.

Table 18.17. 0x0016 LOL_ON_HOLD

Reg Address	Bit Field	Type	Name	Description
0x0016	1	R/W	LOL_ON_HOLD	Set by CBPro.

Table 18.18. 0x0017 Status Flag Masks

Reg Address	Bit Field	Type	Name	Description
0x0017	0	R/W	SYSINCAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt
0x0017	1	R/W	LOSXAXB_INTR_MSK	1 to mask the LOSXAXB_FLG from causing an interrupt
0x0017	5	R/W	SMB_TMOUT_INTR_MSK	1 to mask SMBUS_TIMEOUT_FLG from the interrupt
0x0017	6	R/W	RESERVED	Factory set to 1 to mask reserved bit from causing an interrupt. Do not clear this bit.
0x0017	7	R/W	RESERVED	Factory set to 1 to mask reserved bit from causing an interrupt. Do not clear this bit.

These are the interrupt mask bits for the fault flags in register 0x0011. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Note: Bit 1 corresponds to XAXB LOS from asserting the interrupt (INTR) pin.

Table 18.19. 0x0018 OOF and LOS Masks

Reg Address	Bit Field	Type	Name	Description
0x0018	3:0	R/W	LOS_INTR_MSK	1 to mask the clock input LOS flag
0x0018	7:4	R/W	OOF_INTR_MSK	1 to mask the clock input OOF flag

These are the interrupt mask bits for the OOF and LOS flags in register 0x0012.

Input 0 (IN0) corresponds to LOS_INTR_MSK 0x0018 [0], OOF_INTR_MSK 0x0018 [4]

Input 1 (IN1) corresponds to LOS_INTR_MSK 0x0018 [1], OOF_INTR_MSK 0x0018 [5]

Input 2 (IN2) corresponds to LOS_INTR_MSK 0x0018 [2], OOF_INTR_MSK 0x0018 [6]

Input 3 (IN3) corresponds to LOS_INTR_MSK 0x0018 [3], OOF_INTR_MSK 0x0018 [7]

Table 18.20. 0x0019 Holdover and LOL Masks

Reg Address	Bit Field	Type	Name	Description
0x0019	1	R/W	LOL_INTR_MSK	1 to mask the clock input LOL flag
0x0019	5	R/W	HOLD_INTR_MSK	1 to mask the holdover flag

These are the interrupt mask bits for the LOL and HOLD flags in register 0x0013. If a mask bit is set the alarm will be blocked from causing an interrupt.

Table 18.21. 0x001A

Reg Address	Bit Field	Type	Name	Description
0x001A	5	R/W	CAL_PLL_INTR_MSK	1 to mask the DSPLL internal calibration busy flag

The interrupt mask for this bit flag bit corresponds to register 0x0014.

Table 18.22. 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Name	Description
0x001C	0	S	SOFT_RST_ALL	1 Initialize and calibrates the entire device 0 No effect
0x001C	2	S	SOFT_RST	1 Initialize outer loop 0 No effect

These bits are of type “S”, which is self-clearing.

Table 18.23. 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Name	Description
0x001D	0	S	FINC	1 a rising edge will cause the selected MultiSynth to increment the output frequency by the Nx_FSTEPW parameter. See registers 0x0339-0x0353 0 No effect
0x001D	1	S	FDEC	1 a rising edge will cause the selected MultiSynth to decrement the output frequency by the Nx_FSTEPW parameter. See registers 0x0339-0x03530 No effect

Figure 18.1 FINC, FDEC Logic Diagram on page 196 shows the logic for the FINC, FDEC bits.

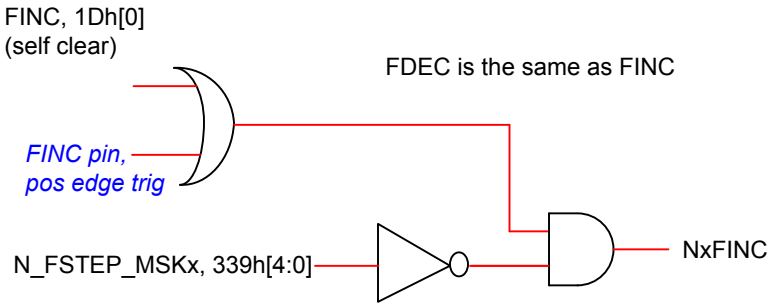

Figure 18.1. FINC, FDEC Logic Diagram

Table 18.24. 0x001E Power Down and Hard Reset

Reg Address	Bit Field	Type	Name	Description
0x001E	0	R/W	PDN	1 to put the device into low power mode
0x001E	1	R/W	HARD_RST	1 causes hard reset. The same as power up except that the serial port access is not held at reset. 0 No reset
0x001E	2	S	SYNC	1 to reset all output R dividers to the same state.

Table 18.25. 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Name	Description
0x002B	3	R/W	SPI_3WIRE	0 for 4-wire SPI, 1 for 3-wire SPI
0x002B	5	R/W	AUTO_NDIV_UPDATE	

Table 18.26. 0x002C LOS Enable

Reg Address	Bit Field	Type	Name	Description
0x002C	3:0	R/W	LOS_EN	1 to enable LOS for a clock input; 0 for disable
0x002C	4	R/W	LOSXAXB_DIS	Enable LOS detection on the XAXB inputs. 0: Enable LOS Detection (default) 1: Disable LOS Detection

Input 0 (IN0): LOS_EN[0]

Input 1 (IN1): LOS_EN[1]

Input 2 (IN2): LOS_EN[2]

Input 3 (IN3): LOS_EN[3]

Table 18.27. 0x002D Loss of Signal Requalification Value

Reg Address	Bit Field	Type	Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0 for 2 msec 1 for 100 msec 2 for 200 msec 3 for one second
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above
0x002D	5:4	R/W	LOS2_VAL_TIME	Clock Input 2, same as above
0x002D	7:6	R/W	LOS3_VAL_TIME	Clock Input 3, same as above

When an input clock disappears (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Table 18.28. 0x002E–0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit Threshold Value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

Table 18.29. 0x0030–0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	16-bit Threshold Value
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Table 18.30. 0x0032–0x0033 LOS2 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x0032	7:0	R/W	LOS2_TRG_THR	16-bit Threshold Value
0x0033	15:8	R/W	LOS2_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 2, given a particular frequency plan.

Table 18.31. 0x0034–0x0035 LOS3 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x0034	7:0	R/W	LOS3_TRG_THR	16-bit Threshold Value
0x0035	15:8	R/W	LOS3_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 3, given a particular frequency plan.

Table 18.32. 0x0036–0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	16-bit Threshold Value
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 0, given a particular frequency plan.

Table 18.33. 0x0038–0x0039 LOS1 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0038	7:0	R/W	LOS1_CLR_THR	16-bit Threshold Value
0x0039	15:8	R/W	LOS1_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 1, given a particular frequency plan.

Table 18.34. 0x003A–0x003B LOS2 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x003A	7:0	R/W	LOS2_CLR_THR	16-bit Threshold Value
0x003B	15:8	R/W	LOS2_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 2, given a particular frequency plan.

Table 18.35. 0x003C–0x003D LOS3 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x003C	7:0	R/W	LOS3_CLR_THR	16-bit Threshold Value
0x003D	15:8	R/W	LOS3_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 3, given a particular frequency plan.

Table 18.36. 0x003E LOS_MIN_PERIOD_EN

Reg Address	Bit Field	Type	Name	Description
0x003E	7:4	R/W	LOS_MIN_PERIOD_EN	Set by CBPro

Table 18.37. 0x003F OOF Enable

Reg Address	Bit Field	Type	Name	Description
0x003F	3:0	R/W	OOF_EN	1 to enable, 0 to disable
0x003F	7:4	R/W	FAST_OOF_EN	1 to enable, 0 to disable

Input 0 corresponds to OOF_EN [0], FAST_OOF_EN [4]

Input 1 corresponds to OOF_EN [1], FAST_OOF_EN [5]

Input 2 corresponds to OOF_EN [2], FAST_OOF_EN [6]

Input 3 corresponds to OOF_EN [3], FAST_OOF_EN [7]

Table 18.38. 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	0 for CLKIN0 1 for CLKIN1 2 for CLKIN2 3 for CLKIN3 4 for XAXB

Table 18.39. 0x0041–0x0045 OOF Divider Select

Reg Address	Bit Field	Type	Name	Description
0x0041	4:0	R/W	OOF0_DIV_SEL	Sets a divider for the OOF circuitry for each input clock 0,1,2,3. The divider value is $2^{OOFx\_DIV\_SEL}$. CBPro sets these dividers.
0x0042	4:0	R/W	OOF1_DIV_SEL	
0x0043	4:0	R/W	OOF2_DIV_SEL	
0x0044	4:0	R/W	OOF3_DIV_SEL	
0x0045	4:0	R/W	OOF-XO_DIV_SEL	

Table 18.40. 0x0046–0x0049 Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	OOF Set threshold. Range is up to ±500 ppm in steps of 1/16 ppm.
0x0047	7:0	R/W	OOF1_SET_THR	OOF Set threshold. Range is up to ±500 ppm in steps of 1/16 ppm.
0x0048	7:0	R/W	OOF2_SET_THR	OOF Set threshold. Range is up to ±500 ppm in steps of 1/16 ppm.
0x0049	7:0	R/W	OOF3_SET_THR	OOF Set threshold. Range is up to ±500 ppm in steps of 1/16 ppm.

Table 18.41. 0x004A–0x004D Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	OOF Clear threshold. Range is up to ±500 ppm in steps of 1/16 ppm.
0x004B	7:0	R/W	OOF1_CLR_THR	OOF Clear threshold. Range is up to ±500 ppm in steps of 1/16 ppm.
0x004C	7:0	R/W	OOF2_CLR_THR	OOF Clear threshold. Range is up to ±500 ppm in steps of 1/16 ppm.
0x004D	7:0	R/W	OOF3_CLR_THR	OOF Clear threshold. Range is up to ±500 ppm in steps of 1/16 ppm.

Table 18.42. 0x004E–0x04F OOF Detection Windows

Reg Address	Bit Field	Type	Setting Name	Description
0x004E	2:0	R/W	OOF0_DETWIN_SEL	Values calculated by CBPro
0x004E	6:4	R/W	OOF1_DETWIN_SEL	
0x004F	2:0	R/W	OOF2_DETWIN_SEL	
0x004F	6:4	R/W	OOF3_DETWIN_SEL	

Table 18.43. 0x0050

Reg Address	Bit Field	Type	Setting Name	Description
0x0050	3:0	R/W	OOF_ON_LOS	Set by CBPro

Table 18.44. 0x0051–0x0054 Fast Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x0051	3:0	R/W	FAST_OOF0_SET_THR	(1+ value) x 1000 ppm
0x0052	3:0	R/W	FAST_OOF1_SET_THR	(1+ value) x 1000 ppm
0x0053	3:0	R/W	FAST_OOF2_SET_THR	(1+ value) x 1000 ppm
0x0054	3:0	R/W	FAST_OOF3_SET_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm set threshold for IN3, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

Table 18.45. 0x0055–0x0058 Fast Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0055	3:0	R/W	FAST_OOF0_CLR_THR	(1+ value) x 1000 ppm
0x0056	3:0	R/W	FAST_OOF1_CLR_THR	(1+ value) x 1000 ppm
0x0057	3:0	R/W	FAST_OOF2_CLR_THR	(1+ value) x 1000 ppm
0x0058	3:0	R/W	FAST_OOF3_CLR_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm clear threshold for IN3, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

OOF needs a frequency reference. ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Table 18.46. 0x0059 Fast OOF Detection Window

Reg Address	Bit Field	Type	Name	Description
0x0059	1:0	R/W	FAST_OOF0_DETWIN_SEL	Values calculated by CBPro
0x0059	3:2	R/W	FAST_OOF1_DETWIN_SEL	
0x0059	5:4	R/W	FAST_OOF2_DETWIN_SEL	
0x0059	7:6	R/W	FAST_OOF3_DETWIN_SEL	

Table 18.47. 0x005A–0x005D OOF0 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x005A	7:0	R/W	OOF0_RATIO_REF	Values calculated by CBPro
0x005B	15:8	R/W	OOF0_RATIO_REF	
0x005C	23:16	R/W	OOF0_RATIO_REF	
0x005D	25:24	R/W	OOF0_RATIO_REF	

Table 18.48. 0x005E–0x0061 OOF1 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x005E	7:0	R/W	OOF1_RATIO_REF	Values calculated by CBPro
0x005F	15:8	R/W	OOF1_RATIO_REF	
0x0060	23:16	R/W	OOF1_RATIO_REF	
0x0061	25:24	R/W	OOF1_RATIO_REF	

Table 18.49. 0x0062–0x0065 OOF2 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x0062	7:0	R/W	OOF2_RATIO_REF	Values calculated by CBPro
0x0063	15:8	R/W	OOF2_RATIO_REF	
0x0064	23:16	R/W	OOF2_RATIO_REF	
0x0065	25:24	R/W	OOF2_RATIO_REF	

Table 18.50. 0x0066–0x0069 OOF3 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x0066	7:0	R/W	OOF3_RATIO_REF	Values calculated by CBPro
0x0067	15:8	R/W	OOF3_RATIO_REF	
0x0068	23:16	R/W	OOF3_RATIO_REF	
0x0069	25:24	R/W	OOF3_RATIO_REF	

Table 18.51. 0x0092 Fast LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x0092	1	R/W	LOL_FST_EN	Enables fast detection of LOL. A large input frequency error will quickly assert LOL when this is enabled.

Table 18.52. 0x0093 Fast LOL Detection Window

Reg Address	Bit Field	Type	Name	Description
0x0093	7:4	R/W	LOL_FST_DETWIN_SEL	Values calculated by CBPro

Table 18.53. 0x0095 Fast LOL Detection Value

Reg Address	Bit Field	Type	Name	Description
0x0095	3:2	R/W	LOL_FST_VALWIN_SEL	Values calculated by CBPro

Table 18.54. 0x0096 Fast LOL Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x0096	7:4	R/W	LOL_FST_SET_THR_SEL	Values calculated by CBPro

Table 18.55. 0x0098 Fast LOL Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0098	7:4	R/W	LOL_FST_CLR_THR_SEL	Values calculated by CBPro

Table 18.56. 0x009A LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x009A	1	R/W	LOL_SLOW_EN_PLL	1 to enable LOL; 0 to disable LOL.

ClockBuilder Pro provides the LOL register values for a particular frequency plan.

Table 18.57. 0x009B Slow LOL Detection Window

Reg Address	Bit Field	Type	Name	Description
0x009B	7:4	R/W	LOL_SLW_DETWIN_SEL	Values calculated by CBPro

Table 18.58. 0x009D Slow LOL Detection Value

Reg Address	Bit Field	Type	Setting Name	Description
0x009D	3:2	R/W	LOL_SLW_VALWIN_SEL	Values calculated by CBPro

Table 18.59. 0x009E LOL Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x009E	7:4	R/W	LOL_SLW_SET_THR	Configures the loss of lock set thresholds. Selectable as 0.1, 0.3, 1, 3, 10, 30, 100, 300, 1000, 3000, 10000. Values are in ppm.

The following are the thresholds for the value that is placed in the top four bits of register 0x009E.

0 = 0.1 ppm

1 = 0.3 ppm

2 = 1 ppm

3 = 3 ppm

4 = 10 ppm

5 = 30 ppm

6 = 100 ppm

7 = 300 ppm

8 = 1000 ppm

9 = 3000 ppm

10 = 10000 ppm

Table 18.60. 0x00A0 LOL Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x00A0	7:4	R/W	LOL_SLW_CLR_THR	Configures the loss of lock set thresholds. Selectable as 0.1, 0.3, 1, 3, 10, 30, 100, 300, 1000, 3000, 10000. Values are in ppm.

The following are the thresholds for the value that is placed in the top four bits of register 0x00A0. ClockBuilder Pro sets these values.

0 = 0.1 ppm

1 = 0.3 ppm

2 = 1 ppm

3 = 3 ppm

4 = 10 ppm

5 = 30 ppm

6 = 100 ppm

7 = 300 ppm

8 = 1000 ppm

9 = 3000 ppm

10 = 10000 ppm

Table 18.61. 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Name	Description
0x00A2	1	R/W	LOL_TIMER_EN	0 to disable 1 to enable

Table 18.62. 0x00A9-0x00AC LOL_CLR_DELAY_DIV256

Reg Address	Bit Field	Type	Name	Description
0x00A9	7:0	R/W	LOL_CLR_DELAY_DIV256	Set by CBPro.
0x00AA	15:8	R/W	LOL_CLR_DELAY_DIV256	Set by CBPro.
0x00AB	23:16	R/W	LOL_CLR_DELAY_DIV256	Set by CBPro.
0x00A9	28:24	R/W	LOL_CLR_DELAY_DIV256	Set by CBPro.

Table 18.63. 0x00E2

Reg Address	Bit Field	Type	Name	Description
0x00E2	7:0	R	ACTIVE_NVM_BANK	Read-only field indicating number of user bank writes carried out so far. Value Description 0 zero 3 one 15 two 63 three

Table 18.64. 0x00E3

Reg Address	Bit Field	Type	Setting Name	Description
0x00E3	7:0	R/W	NVM_WRITE	Write 0xC7 to initiate an NVM bank burn.

Table 18.65. 0x00E4

Reg Address	Bit Field	Type	Setting Name	Description
0x00E4	0	S	NVM_READ_BANK	When set, this bit will read the NVM down into the volatile memory.

Table 18.66. 0x00E5 Fastlock Extend Enable

Reg Address	Bit Field	Type	Name	Description
0x00E5	5	R/W	FASTLOCK_EXTEND_EN	Extend Fastlock bandwidth period past LOL Clear 0: Do not extend Fastlock period 1: Extend Fastlock period (default)

Table 18.67. 0x00EA–0x00ED LOL Detection Value

Reg Address	Bit Field	Type	Name	Description
0x00EA	7:0	R/W	FASTLOCK_EXTEND	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL.
0x00EB	15:8	R/W	FASTLOCK_EXTEND	
0x00EC	23:16	R/W	FASTLOCK_EXTEND	
0x00ED	28:24	R/W	FASTLOCK_EXTEND	

Table 18.68. 0x00F6

Reg Address	Bit Field	Type	Name	Description
0x00F6	0	R	REG_0XF7_INTR	Set by CBPro.

Reg Address	Bit Field	Type	Name	Description
0x00F6	1	R	REG_0XF8_INTR	Set by CBPro.
0x00F6	2	R	REG_0XF9_INTR	Set by CBPro.

Table 18.69. 0x00F7

Reg Address	Bit Field	Type	Name	Description
0x00F7	0	R	SYSINCAL_INTR	Set by CBPro.
0x00F7	1	R	LOSXAXB_INTR	Set by CBPro.
0x00F7	2	R	LOSREF_INTR	Set by CBPro.
0x00F7	4	R	LOSVCO_INTR	Set by CBPro.
0x00F7	5	R	SMBUS_TIME_OUT_INTR	Set by CBPro.

Table 18.70. 0x00F8

Reg Address	Bit Field	Type	Name	Description
0x00F8	3:0	R	LOS_INTR	Set by CBPro.

Table 18.71. 0x00F9

Reg Address	Bit Field	Type	Name	Description
0x00F9	1	R	LOL_INTR	Set by CBPro.
0x00F9	5	R	HOLD_INTR	Set by CBPro.

Table 18.72. 0x00FE Device Ready

Reg Address	Bit Field	Type	Name	Description
0x00FE	7:0	R	DEVICE_READY	Ready Only byte to indicate device is ready. When read data is 0x0F one can safely read/write registers. This register is repeated on every page therefore a page write is not ever required to read the DEVICE_READY status.

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Table 18.73. 0x0102 Global OE Gating for all Clock Output Drivers

Reg Address	Bit Field	Type	Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	1 Pass through the output enables, 0 disables all output drivers

Table 18.74. 0x0112 Clock Output Driver 0 and R-Divider 0 Configuration

Reg Address	Bit Field	Type	Name	Description
0x0112	0	R/W	OUT0_PDN	Output driver 0: 0 to power up the regulator, 1 to power down the regulator. Clock outputs will be weakly pulled-low.
0x0112	1	R/W	OUT0_OE	Output driver 0: 0 to disable the output, 1 to enable the output
0x0112	2	R/W	OUT0_RDIV_FORCE2	0 R0 divider value is set by R0_REG 1 R0 divider value is forced into divide by 2

Table 18.75. 0x0113 Output 0 Format

Reg Address	Bit Field	Type	Name	Description
0x0113	2:0	R/W	OUT0_FORMAT	0 Reserved 1 swing mode (normal swing) differential 2 swing mode (high swing) differential 3 Reserved 4 LVCMOS single ended 5 LVCMOS (+ pin only) 6 LVCMOS (– pin only) 7 Reserved
0x0113	3	R/W	OUT0_SYNC_EN	0 disable 1 enable Enable/disable synchronized (glitchless) operation. When enabled, the power down and output enables are synchronized to the output clock.
0x0113	5:4	R/W	OUT0_DIS_STATE	Determines the state of an output driver when disabled, selectable as 00 Disable low 01 Disable high 10 Reserved 11 Reserved
0x0113	7:6	R/W	OUT0_CMOS_DRV	LVCMOS output impedance. Selectable as CMOS1,CMOS2, CMOS3.

See Section 6.2 Performance Guidelines for Outputs

Table 18.76. 0x0114 Output 0 Swing and Amplitude

Reg Address	Bit Field	Type	Name	Description
0x0114	3:0	R/W	OUT0_CM	Output common mode voltage adjustment Programmable swing mode with normal swing configuration: Step size = 100 mV Range = 0.9 V to 2.3 V if VDDO = 3.3 V Range = 0.6 V to 1.5V if VDDO=2.5 V Range = 0.5 V to 0.9V if VDDO=1.8 V Programmable swing mode with high0 swing configuration: Step size = 100 mV Range = 0.9 V to 2.3 V if VDDO = 3.3 V Range = 0.6 V to 1.5 V if VDDO = 2.5 V Range = 0.5 V to 0.9 V if VDDO = 1.8 V LVCMOS mode: Not supported/No effect
0x0114	6:4	R/W	OUT0_AMPL	Output swing adjustment Programmable swing mode with normal swing configuration: Step size = 100 mV Range = 100 mVpp-se to 800 mVpp-se Programmable swing mode with high swing configuration: Step size = 200 mV Range = 200 mVpp-se to 1600 mVpp-se LVCMOS mode: Not supported/No effect

See the settings and values from Section 6.3.8 Output Driver Settings for LVPECL, LVDS, HCSL, and CML for details of the settings. ClockBuilder Pro is used to select the correct settings for this register.

Table 18.77. 0x0115 R-Divider 0 Mux Selection

Reg Address	Bit Field	Type	Name	Description
0x0115	1:0	R/W	OUT0_MUX_SEL	Output driver 0 input mux select.This selects the source of the multisynth. 0: N0 1: N1 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
0x0115	3	R/W	OUT0_VDD_SEL_EN	1 = Enable OUT0_VDD_SEL
0x0115	5:4	R/W	OUT0_VDD_SEL	Must be set to the VDD0 voltage. 0: 3.3 V 1: 1.8 V 2: 2.5 V 3: Reserved
0x0115	7:6	R/W	OUT0_INV	CLK and CLK not inverted CLK inverted CLK and CLK inverted CLK inverted

Each output can be configured to use Multisynth N0–N1 divider. The frequency for each N-divider is set in registers 0x0302–0x0316 for N0 to N1. Two different frequencies can be set in the N-dividers (N0–N1) and each of the 2 outputs can be configured to any of the 2 different frequencies.

The two output drivers are all identical. The single set of descriptions above for output driver 0 applies to the other output driver.

Table 18.78. Registers that Follow the Same Definition as Above

Register Address	Description	(Same as) Address
0x0117	Clock Output Driver 1 Config	0x0112
0x0118	Clock Output Driver 1 Format, Sync	0x0113
0x0119	Clock Output Driver 1 Ampl, CM	0x0114
0x011A	OUT1_MUX_SEL, OUT1_VDD_SEL_EN, OUT1_VDD_SEL, OUT1_INV	0x0115

Table 18.79. 0x013F–0x0140

Reg Address	Bit Field	Type	Setting Name	Description
0x013F	7:0	R/W	OUTX_ALWAYS_ON	This setting is managed by CBPro during zero delay mode.
0x0140	11:8	R/W	OUTX_ALWAYS_ON	

Table 18.80. 0x0141 Output Disable Mask for LOS XAXB

Reg Address	Bit Field	Type	Setting Name	Description
0x0141	1	R/W	OUT_DIS_MSK	
0x0141	5	R/W	OUT_DIS_LOL_MSK	
0x0141	6	R/W	OUT_DIS_LOSXAXB_MSK	Determines if outputs are disabled during an LOSXAXB condition. 0: All outputs disabled on LOSXAXB 1: All outputs remain enabled during LOSXAXB condition
0x0141	7	R/W	OUT_DIS_MSK_LOS_PFD	

Table 18.81. 0x0142 Output Disable Loss of Lock PLL

Reg Address	Bit Field	Type	Setting Name	Description
0x0142	1	R/W	OUT_DIS_MSK_LOL	0: LOL will disable all connected outputs 1: LOL does not disable any outputs
0x0142	5	R/W	OUT_DIS_MSK_HOLD	

Table 18.82. 0x0145 Power Down All

Reg Address	Bit Field	Type	Name	Description
0x0145	0	R/W	OUT_PDN_ALL	0- no effect 1- all drivers powered down

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Table 18.83. 0x0206 Pre-scale Reference Divide Ratio

Reg Address	Bit Field	Type	Name	Description
0x0206	1:0	R/W	PXAXB	Sets the prescale divider for the input clock on XAXB.

This can only be used with an external clock source, not with crystals.

0 = pre-scale value 1

1 = pre-scale value 2

2 = pre-scale value 4

3 = pre-scale value 8

Table 18.84. 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Name	Description
0x0208	7:0	R/W	P0_NUM	48-bit Integer Number
0x0209	15:8	R/W	P0_NUM	
0x020A	23:16	R/W	P0_NUM	
0x020B	31:24	R/W	P0_NUM	
0x020C	39:32	R/W	P0_NUM	
0x020D	47:40	R/W	P0_NUM	

This set of registers configure the P-dividers which are located at the four input clocks seen in Section . ClockBuilder Pro calculates the correct values for the P-dividers.

Table 18.85. 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Name	Description
0x020E	7:0	R/W	P0_DEN	32-bit Integer Number
0x020F	15:8	R/W	P0_DEN	
0x0210	23:16	R/W	P0_DEN	
0x0211	31:24	R/W	P0_DEN	

The P1-P3 divider numerator and denominator follow the same format as P0 described above. ClockBuilder Pro calculates the correct values for the P-dividers.

Table 18.86. Registers that Follow the P0_NUM and P0_DEN Definitions

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1 Divider Denominator	32-bit Integer Number	0x020E-0x0211
0x021C-0x0221	P2 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0222-0x0225	P2 Divider Denominator	32-bit Integer Number	0x020E-0x0211
0x0226-0x022B	P3 Divider Numerator	48-bit Integer Number	0x0208-0x020D

Register Address	Description	Size	Same as Address
0x022C-0x022F	P3 Divider Denominator	32-bit Integer Number	0x020E-0x0211

This set of registers configure the P-dividers which are located at the four input clocks seen in Section . ClockBuilder Pro calculates the correct values for the P-dividers.

Table 18.87. 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Setting Name	Description
0x0230	0	S	P0_UPDATE	0: No update for P-divider value 1: Update P-divider value
0x0230	1	S	P1_UPDATE	
0x0230	2	S	P2_UPDATE	
0x0230	3	S	P3_UPDATE	

Note that these controls are not needed when following the guidelines in Section 4.2 Dynamic PLL Changes. Specifically, they are not needed when using the global soft reset “SOFT_RST_ALL”.

Table 18.88. 0x0231 P0 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0231	3:0	R/W	P0_FRACN_MODE	P0 (IN0) input divider fractional mode. Must be set to 0xB for proper operation.
0x0231	4	R/W	P0_FRAC_EN	P0 (IN0) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 18.89. 0x0232 P1 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0232	3:0	R/W	P1_FRACN_MODE	P1 (IN1) input divider fractional mode. Must be set to 0xB for proper operation.
0x0232	4	R/W	P1_FRAC_EN	P1 (IN1) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 18.90. 0x0233 P2 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0233	3:0	R/W	P2_FRACN_MODE	P2 (IN2) input divider fractional mode. Must be set to 0xB for proper operation.
0x0233	4	R/W	P2_FRAC_EN	P2 (IN2) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 18.91. 0x0234 P3 Factional Division Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0234	3:0	R/W	P3_FRACN_MODE	P3 (IN3) input divider fractional mode. Must be set to 0xB for proper operation.
0x0234	4	R/W	P3_FRAC_EN	P3 (IN3) input divider fractional enable 0: Integer-only division. 1: Fractional (or Integer) division.

Table 18.92. 0x0235-0x023A MXAXB Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0235	7:0	R/W	MXAXB_NUM	44-bit Integer Number
0x0236	15:8	R/W	MXAXB_NUM	
0x0237	23:16	R/W	MXAXB_NUM	
0x0238	31:24	R/W	MXAXB_NUM	
0x0239	39:32	R/W	MXAXB_NUM	
0x023A	43:40	R/W	MXAXB_NUM	

Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in 4.2 Dynamic PLL Changes are followed.

Table 18.93. 0x023B-0x023E MXAXB Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x023B	7:0	R/W	MXAXB_DEN	32-bit Integer Number
0x023C	15:8	R/W	MXAXB_DEN	
0x023D	23:16	R/W	MXAXB_DEN	
0x023E	31:24	R/W	MXAXB_DEN	

The M-divider numerator and denominator are set by ClockBuilder Pro for a given frequency plan. Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in 4.2 Dynamic PLL Changes are followed.

Table 18.94. 0x023F MXAXB Update

Reg Address	Bit Field	Type	Setting Name	Description
0x023F	0	S	MXAXB_UPDATE	Set to 1 to update the MXAXB_NUM and MXAXB_DEN values. A SOFT_RST may also be used to update these values.

Table 18.95. 0x0250-0x0252 R0 Divider

Reg Address	Bit Field	Type	Name	Description
0x0250	7:0	R/W	R0_REG	A 24 bit integer divider. Divide value = (R0_REG+1) x 2 To set R0 = 2, set OUT0_RDIV_FORCE2 = 1, and then the R0_REG value is irrelevant.
0x0251	15:8	R/W	R0_REG	
0x0252	23:16	R/W	R0_REG	

The R dividers are at the output clocks and are purely integer division. The R1divider follow the same format as the R0 divider described above.

Table 18.96. Registers that Follow the R0_REG

Register Address	Description	Size	Same as Address
0x0253–0x0255	R1_REG	24-bit Integer Number	0x0250–0x0252

Table 18.97. 0x026B-0x0272 User Scratch Pad

Reg Address	Bit Field	Type	Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by CBPro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, “ULT.1A” with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6:0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Table 18.98. 0x0278-0x027C OPN Identifier

Reg Address	Bit Field	Type	Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: 5392C-A12345-GM, 12345 is the OPN unique identifier, which sets: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5392C-A12345-GM.

Applies to a “custom” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5392C-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5392 but exclude any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Table 18.99. 0x027D

Reg Address	Bit Field	Type	Setting Name	Description
0x027D	7:0	R/W	OPN_REVISION	

Table 18.100. 0x027E

Reg Address	Bit Field	Type	Setting Name	Description
0x027E	7:0	R/W	BASELINE_ID	

Table 18.101. OOFx_TRG_THR_EXT

Reg Address	Bit Field	Type	Name	Description
0x028A	4:0	R/W	OOF0_TRG_THR_EXT	Set by CBPro.
0x028B	4:0	R/W	OOF1_TRG_THR_EXT	Set by CBPro
0x028C	4:0	R/W	OOF2_TRG_THR_EXT	Set by CBPro
0x028D	4:0	R/W	OOF3_TRG_THR_EXT	Set by CBPro

Table 18.102. OOFx_CLR_THR_EXT

Reg Address	Bit Field	Type	Name	Description
0x028E	4:0	R/W	OOF0_CLR_THR_EXT	Set by CBPro.
0x028F	4:0	R/W	OOF1_CLR_THR_EXT	Set by CBPro
0x0290	4:0	R/W	OOF2_CLR_THR_EXT	Set by CBPro
0x0291	4:0	R/W	OOF3_CLR_THR_EXT	Set by CBPro

Table 18.103. 0x0292 OOF_STOP_ON_LOS

Reg Address	Bit Field	Type	Name	Description
0x0292	3:0	R/W	OOF_STOP_ON_LOS	Set by CBPro

Table 18.104. 0x0293 OOF_CLEAR_ON_LOS

Reg Address	Bit Field	Type	Name	Description
0x0293	3:0	R/W	OOF_CLEAR_ON_LOS	Set by CBPro

Table 18.105. 0x0294 Fastlock Extend Scale

Reg Address	Bit Field	Type	Name	Description
0x0294	7:4	R/W	FASTLOCK_EXTEND_SCL	Scales LOLB_INT_TIM-ER_DIV256

Table 18.106. 0x0296 Fastlock Delay on Input Switch

Reg Address	Bit Field	Type	Name	Description
0x0296	1	R/W	LOL_SLW_VALWIN_SELX	Set by CBPro

Table 18.107. 0x0297 Fastlock Delay on Input Switch Enable

Reg Address	Bit Field	Type	Name	Description
0x0297	1	R/W	FASTLOCK_DLY_ONSW_EN	Set by CBPro.

Table 18.108. 0x0299 Fastlock Delay on LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x0299	1	R/W	FASTLOCK_DLY_ONLOL_EN	Set by CBPro.

Table 18.109. 0x029D Fastlock Delay on LOL

Reg Address	Bit Field	Type	Name	Description
0x029D	1	R/W	FASTLOCK_DLY_ONLOL	Set by CBPro.

Table 18.110. 0x02A9 Fastlock Delay on Input Switch

Reg Address	Bit Field	Type	Name	Description
0x02A9	7:0	R/W	FASTLOCK_DLY_ONSW	20-bit value. Set by CBPro.
0x02AA	15:8	R/W	FASTLOCK_DLY_ONSW	
0x02AB	19:16	R/W	FASTLOCK_DLY_ONSW	

Table 18.111. 0x02B7 LOL Delay from LOS

Reg Address	Bit Field	Type	Name	Description
0x02B7	3:2	R/W	LOL_NOSIG_TIME	Set by CBPro.

Table 18.112. 0x02BC LOS_CMOS_MIN_PER_EN

Reg Address	Bit Field	Type	Name	Description
0x02BC	7:6	R/W	LOS_CMOS_MIN_PER_EN	Set by CBPro.

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Table 18.113. 0x0302–0x0307 N0 Numerator

Reg Address	Bit Field	Type	Name	Description
0x0302	7:0	R/W	N0_NUM	44-bit Integer Number
0x0303	15:8	R/W	N0_NUM	44-bit Integer Number
0x0304	23:16	R/W	N0_NUM	44-bit Integer Number
0x0305	31:24	R/W	N0_NUM	44-bit Integer Number
0x0306	39:32	R/W	N0_NUM	44-bit Integer Number
0x0307	43:40	R/W	N0_NUM	44-bit Integer Number

The N dividers are interpolative dividers that are used as output dividers that feed into the R dividers. ClockBuilder Pro calculates the correct values for the N-dividers.

Table 18.114. 0x0308–0x030C N0 Denominator

Reg Address	Bit Field	Type	Name	Description
0x0308	7:0	R/W	N0_DEN	32-bit Integer Number
0x0309	15:8	R/W	N0_DEN	32-bit Integer Number
0x030A	23:16	R/W	N0_DEN	32-bit Integer Number
0x030B	31:24	R/W	N0_DEN	32-bit Integer Number
0x030C	0	S	N0_UPDATE	Set this bit to update the N0 divider.

This bit is provided so that all of the N0 divider bits can be changed at the same time. First, write all of the new values to the divider, then set the update bit.

Table 18.115. Register that Follows the N0_NUM and N0_DEN Definitions

Register Address	Description	Size	Same as Address
0x030D–0x0312	N1 Numerator	44-bit Integer Number	0x0302–0x0307
0x0313–0x0316	N1 Denominator	32-bit Integer Number	0x0308–0x030B

Table 18.116. 0x0317

Reg Address	Bit Field	Type	Name	Description
0x0317	0	S	N1_UPDATE	Set this bit to update the N1 divider

This bit is provided so that all of the N1 divider bits can be changed at the same time. First, write all of the new values to the divider, then set the update bit.

Table 18.117. 0x0338 Global N Divider Update

Reg Address	Bit Field	Type	Name	Description
0x0338	1	S	N_UPDATE_ALL	Set this bit to update both N dividers

This bit is provided so that both of the N dividers can be changed at the same time. First, write all of the new values to the divider, then set the update bit.

Note: If the intent is to write to the N_UPDATE_ALL to have all dividers update at the same time, then make sure only N_UPDATE_ALL bit gets set.

Table 18.118. 0x0339 FINC/FDEC Masks

Reg Address	Bit Field	Type	Name	Description
0x0339	1:0	R/W	N_FSTEP_MSK	0 to enable FINC/FDEC updates 1 to disable FINC/FDEC updates

Bit 0 corresponds to MultiSynth N0 N_FSTEP_MSK 0x0339[0]

Bit 1 corresponds to MultiSynth N1 N_FSTEP_MSK 0x0339[1]

Table 18.119. 0x033B–0x0340 N0 Frequency Step Word

Reg Address	Bit Field	Type	Name	Description
0x033B	7:0	R/W	N0_FSTEPW	44-bit Integer Number
0x033C	15:8	R/W	N0_FSTEPW	
0x033D	23:16	R/W	N0_FSTEPW	
0x033E	31:24	R/W	N0_ FSTEPW	
0x033F	39:32	R/W	N0_ FSTEPW	
0x0340	43:40	R/W	N0_ FSTEPW	

This is a 44-bit integer value which is directly added or subtracted from the N-divider. ClockBuilder Pro calculates the correct values for the N0 Frequency Step Word. Each N divider has the ability to add or subtract up to a 44-bit value. Changing any of the Nx_DELAY values requires a SOFT_RST, a HARD_RST, or a power up sequence.

Table 18.120. Registers that Follow the N0_FSTEPW Definition

Register Address	Description	Size	Same as Address
0x0341-0x0346	N1 Frequency Step Word	44-bit Integer Number	0x033B-0x0340

Table 18.121. 0x0359–0x035A N0 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x0359	7:0	R/W	N0_DELAY[7:0]	8-bit Integer delay portion
0x035A	7:0	R/W	N0_DELAY[7:0]	Upper byte of N0_DELAY[15:0]

Nx_DELAY[15:0] is a 2s complement number that sets the output delay of MultiSynthx.

The delay in seconds is Nx_DELAY/(256 x Fvco) where Fvco is the VCO frequency in Hz. The maximum positive and negative delay is $\pm(2^{15} - 1)/(256 \times Fvco)$. ClockBuilder Pro calculates the correct value for this register. Changing any of the Nx_DELAY values requires a SOFT_RST, a HARD_RST, or a power up sequence.

Table 18.122. Registers that Follow the N0_DELAY Definition

Register Address	Description	Size	Same as Address
0x035B	N1 Delay Integer	8-bit Integer Number	0x0359
0x035C	N1 Delay Fractional	8-bit Integer Number	0x035A

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Table 18.123. 0x0487 Zero Delay Mode Setup

Reg Address	Bit Field	Type	Name	Description
0x0487	0	R/W	ZDM_EN	0 to disable ZD mode 1 to enable ZD mode
0x0487	2:1	R/W	ZDM_IN_SEL	Clock input select when in ZD mode. 0 for IN0, 1 for IN1,2 for IN2, 3 reserved Note: In ZD mode the feedback clock comes into IN3
0x0487	4	R/W	ZDM_AUTOSW_EN	Set by CBPro.

This register is used for enabling the zero delay mode (ZDM) and selecting the source. The phase difference between the output, which is connected to the selected input below will be nulled to zero. When in zero delay mode, the DSPLL cannot have either hitless or automatic switching. In addition, the frequency of the clock selected by ZDM_IN_SEL must either be the same or have a simple integer relationship to the clock at the FB_IN pins. Pin controlled clock selection is available in ZD mode (see register 0x052A).

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Table 18.124. 0x0507 Active Input

Reg Address	Bit Field	Type	Name	Description
0x0507	7:6	R	IN_ACTV	PLL bandwidth parameter 0: IN0 1: IN1 2: IN2 3: IN3

Table 18.125. 0x0508-0x050D Loop Bandwidth

Reg Address	Bit Field	Type	Name	Description
0x0508	5:0	R/W	BW0_PLL	PLL bandwidth parameter
0x0509	5:0	R/W	BW1_PLL	PLL bandwidth parameter
0x050A	5:0	R/W	BW2_PLL	PLL bandwidth parameter
0x050B	5:0	R/W	BW3_PLL	PLL bandwidth parameter
0x050C	5:0	R/W	BW4_PLL	PLL bandwidth parameter
0x050D	5:0	R/W	BW5_PLL	PLL bandwidth parameter

This group of registers determine the loop bandwidth for the DSPLL. It is selectable as 0.1 Hz, 1 Hz, 4 Hz, 10 Hz, 40 Hz, 100 Hz, 400 Hz, 1 kHz, and 4 kHz. The loop BW values are calculated by ClockBuilder Pro and are written into these registers. The BW_UPDATE_PLL bit (reg 0x0514[0]) must be set to cause the BWx_PLL parameters to take effect.

Table 18.126. 0x050E-0x0514 Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Name	Description
0x050E	5:0	R/W	FAST_BW0_PLL	PLL fast bandwidth parameter
0x050F	5:0	R/W	FAST_BW1_PLL	PLL fast bandwidth parameter
0x0510	5:0	R/W	FASTL_BW2_PLL	PLL fast bandwidth parameter
0x0511	5:0	R/W	FAST_BW3_PLL	PLL fast bandwidth parameter
0x0512	5:0	R/W	FAST_BW4_PLL	PLL fast bandwidth parameter
0x0513	5:0	R/W	FAST_BW5_PLL	PLL fast bandwidth parameter
0x0514	0	S	BW_UPDATE_PLL	Must be set to 1 to update the BWx_PLL and FAST_BWx_PLL parameters

The fast lock loop BW values are calculated by ClockBuilder Pro and used when fast lock is enabled.

Table 18.127. 0x0515-0x051B M Divider Numerator, 56-bits

Reg Address	Bit Field	Type	Name	Description
0x0515	7:0	R/W	M_NUM	56-bit Number
0x0516	15:8	R/W	M_NUM	
0x0517	23:16	R/W	M_NUM	
0x0518	31:24	R/W	M_NUM	
0x0519	39:32	R/W	M_NUM	
0x051A	47:40	R/W	M_NUM	
0x051B	55:48	R/W	M_NUM	

Table 18.128. 0x051C-0x051F M Divider Denominator, 32-bits

Reg Address	Bit Field	Type	Name	Description
0x051C	7:0	R/W	M_DEN	32-bit Number
0x051E	15:8	R/W	M_DEN	
0x051E	23:16	R/W	M_DEN	
0x051F	31:24	R/W	M_DEN	

The loop M divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 18.129. 0x0520 M Divider Update Bit

Reg Address	Bit Field	Type	Name	Description
0x0520	0	S	M_UPDATE	Set this bit to update the M divider.

Table 18.130. 0x0521 DSPLL M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0521	3:0	R/W	M_FRAC_MODE	M feedback divider fractional mode. Must be set to 0xB for proper operation.
0x0521	4	R/W	M_FRAC_EN	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0521	5	R/W	Reserved	Must be set to 1

Table 18.131. 0x052A Input Clock Select

Reg Address	Bit Field	Type	Name	Description
0x052A	0	R/W	IN_SEL_REGCTRL	0 for pin controlled clock selection 1 for register controlled clock selection

Reg Address	Bit Field	Type	Name	Description
0x052A	2:1	R/W	IN_SEL	0 for IN0, 1 for IN1, 2 for IN2, 3 for IN3 (or FB_IN)

Input clock selection for manual register based and pin controlled clock selection. Note: when ZDM_EN (0x0487, bit 0) and IN_SEL_REGCTRL are both high, IN_SEL does not do anything.

Table 18.132. 0x052B Fast Lock Control

Reg Address	Bit Field	Type	Name	Description
0x052B	0	R/W	FASTLOCK_AUTO_EN	Applies only when FASTLOCK_MAN = 0 (see below): 0 to disable auto fast lock when the DSPLL is out of lock 1 to enable auto fast lock
0x052B	1	R/W	FASTLOCK_MAN	0 for normal operation (see above) 1 to force fast lock

When in fast lock, the fast lock loop BW can be automatically used.

Table 18.133. 0x052C Holdover Exit Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052C	0	R/W	HOLD_EN	Holdover enable 0: Holdover Disabled 1: Holdover Enabled (default)
0x052C	3	R/W	HOLD_RAMP_BYP	HOLD_RAMP_BYP
0x052C	4	R/W	HOLDEXIT_BW_SEL1	Holdover Exit Bandwidth select. Selects the exit bandwidth from Holdover when ramped exit is disabled (HOLD_RAMP_BYP = 1). 0: Exit Holdover using Holdover Exit or Fastlock bandwidths (default). See HOLDEXIT_BW_SEL0 (0x059B[6]) for additional information. 1: Exit Holdover using the Normal loop bandwidth
0x052C	7:5	R/W	RAMP_STEP_INTERVAL	Time Interval of the frequency ramp steps when ramping between inputs or when exiting holdover. Calculated by CBPro based on selection.

Table 18.134. 0x052E Holdover History Average Length

Reg Address	Bit Field	Type	Name	Description
0x052E	4:0	R/W	HOLD_HIST_LEN	5-bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency.

time (s) = $((2^{LEN}) - 1)$ x 268 ns

Table 18.135. 0x052F Holdover History Delay

Reg Address	Bit Field	Type	Name	Description
0x052F	4:0	R/W	HOLD_HIST_DELAY	

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past, above the averaging window. The amount that the average window is delayed is the holdover history delay.

time(s) = (2^{DELAY}) x 268 ns

Table 18.136. 0x0531

Reg Address	Bit Field	Type	Setting Name	Description
0x0531	4:0	R/W	HOLD_REF_COUNT_FRC	5- bit value

Table 18.137. 0x0532–0x0534

Reg Address	Bit Field	Type	Setting Name	Description
0x0532	7:0	R/W	HOLD_15M_CYC_COUNT	Value calculated by CBPro
0x0533	15:8	R/W	HOLD_15M_CYC_COUNT	
0x0534	23:16	R/W	HOLD_15M_CYC_COUNT	

Table 18.138. 0x0535 Force Holdover

Reg Address	Bit Field	Type	Name	Description
0x0535	0	R/W	FORCE_HOLD	0 for normal operation 1 for force holdover

Table 18.139. 0x0536 Input Clock Switching Control

Reg Address	Bit Field	Type	Name	Description
0x0536	1:0	R/W	CLK_SWTCH_MODE	0 = manual 1 = automatic/non-revertive 2 = automatic/revertive 3 = Reserved
0x0536	2	R/W	HSW_EN	0 glitchless switching mode (phase buildout turned off) 1 hitless switching mode (phase buildout turned on) Note that hitless switching is not available in zero delay mode.

Table 18.140. 0x0537 Input Alarm Masks

Reg Address	Bit Field	Type	Name	Description
0x0537	3:0	R/W	IN_LOS_MSK	For each clock input LOS alarm: 0 to use LOS in the clock selection logic 1 to mask LOS from the clock selection logic
0x0537	7:4	R/W	IN_OOF_MSK	For each clock input OOF alarm: 0 to use OOF in the clock selection logic 1 to mask OOF from the clock selection logic This bit is forced to 1 if precision and fast OOF are disabled on input in CBPro.

This register is for the input clock switch alarm masks. For each of the four clock inputs, the OOF and/or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

Table 18.141. 0x0538 Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Name	Description
0x0538	2:0	R/W	IN0_PRIORITY	The priority for clock input 0 is: 0 No priority 1 for priority 1 2 for priority 2 3 for priority 3 4 for priority 4 5 to 7 are reserved
0x0538	6:4	R/W	IN1_PRIORITY	The priority for clock input 1 is: 0 No priority 1 for priority 1 2 for priority 2 3 for priority 3 4 for priority 4 5 to 7 are reserved

This register is used to assign a priority to an input clock for automatic clock input switching. The available clock with the lowest priority level will be selected. When input clocks are assigned the same priority, they will use the following default priority list: 0, 1, 2, 3.

Table 18.142. 0x0539 Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Name	Description
0x0539	2:0	R/W	IN2_PRIORITY	The priority for clock input 2 is: 0 No priority 1 for priority 1 2 for priority 2 3 for priority 3 4 for priority 4 5 to 7 are reserved
0x0539	6:4	R/W	IN3_PRIORITY	The priority for clock input 3 is: 0 No priority 1 for priority 1 2 for priority 2 3 for priority 3 4 for priority 4 5 to 7 are reserved

This register is used to assign a priority to an input clock for automatic clock input switching. The available clock with the lowest priority level will be selected. When input clocks are assigned the same priority, they will use the following default priority list: 0, 1, 2, 3.

Table 18.143. 0x053A Hitless Switching Mode

Reg Address	Bit Field	Type	Name	Description
0x053A	1:0	R/W	HSW_MODE	1: Default setting, do not modify 0, 2, 3: Reserved
0x053A	3:2	R/W	HSW_PHMEAS_CTRL	0: Default setting, do not modify 1, 2, 3: Reserved

Table 18.144. 0x053B-0x053C Hitless Switching Phase Threshold

Reg Address	Bit Field	Type	Name	Description
0x053B	7:0	R/W	HSW_PHMEAS_THR	10-bit value. Set by CBPro.
0x053C	9:8	R/W	HSW_PHMEAS_THR	

Table 18.145. 0x053D

Reg Address	Bit Field	Type	Name	Description
0x053D	4:0	R/W	HSW_COARSE_PM_LEN	Set by CBPro.

Table 18.146. 0x053E

Reg Address	Bit Field	Type	Name	Description
0x053E	4:0	R/W	HSW_COARSE_PM_DLY	Set by CBPro.

Table 18.147. 0x053F

Reg Address	Bit Field	Type	Name	Description
0x053F	1	R/O	HOLD_HIST_VALID	1 = there is enough historical frequency data collected for valid holdover.
0x053F	2	R/O	FASTLOCK_STATUS	1 = PLL is in Fast Lock operation

Table 18.148. 0x0540 Reserved

Reg Address	Bit Field	Type	Name	Description
0x0540	7:0	R/W	RESERVED	This register is used when making certain changes to the device. See Section 4.2 Dynamic PLL Changes for more information.

This register is used when making certain changes to the device. See Section 4.2 Dynamic PLL Changes for more information.

Table 18.149. 0x0588 Hitless Switching Length

Reg Address	Bit Field	Type	Setting Name	Description
0x0588	3:0	R/W	HSW_FINE_PM_LEN	Set by CBPro.

Table 18.150. 0x0589-0x058A PFD Enable Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x0589	7:0	R/W	PFD_EN_DELAY	Set by CBPro.
0x058A	12:8	R/W	PFD_EN_DELAY	

Table 18.151. 0x058B–0x058D

Reg Address	Bit Field	Type	Setting Name	Description
0x058B	7:0	R/W	HSW_MEAS_SETTLE	Set by CBPro.
0x058C	15:8	R/W	HSW_MEAS_SETTLE	Set by CBPro.
0x058D	19:16	R/W	HSW_MEAS_SETTLE	Set by CBPro.

Table 18.152. 0x059B Holdover Exit

Reg Address	Bit Field	Type	Setting Name	Description
0x059B	1	R/W	INIT_LP_CLOSE_HO	Set by CBPro.
0x059B	4	R/W	HOLD_PRESERVE_HIST	
0x059B	5	R/W	HOLD_FRZ_WITH_INTONLY	

Reg Address	Bit Field	Type	Setting Name	Description
0x059B	6	R/W	HOLDEXIT_BW_SEL0	Set by CBPro. See HOLDEXIT_BW_SEL1
0x059B	7	R/W	HOLDEXIT_STD_BO	Set by CBPro.

Table 18.153. 0x059C

Reg Address	Bit Field	Type	Setting Name	Description
0x059C	7	R/W	HOLD_RAMPBP_NOHIST	Set by CBPro

Table 18.154. 0x059C

Reg Address	Bit Field	Type	Setting Name	Description
0x059C	6	R/W	HOLDEXIT_ST_BO	Set by CBPro

Table 18.155. 0x059D Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x059D	5:0	R/W	HOLDEXIT_BW0	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 18.156. 0x059E Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x059E	5:0	R/W	HOLDEXIT_BW1	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 18.157. 0x059F Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x059F	5:0	R/W	HOLDEXIT_BW2	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 18.158. 0x05A0 Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x05A0	5:0	R/W	HOLDEXIT_BW3	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 18.159. 0x05A1 Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x05A1	5:0	R/W	HOLDEXIT_BW4	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 18.160. 0x059A2 Holdover Exit BW

Reg Address	Bit Field	Type	Setting Name	Description
0x05A2	5:0	R/W	HOLDEXIT_BW5	Set by CBPro to set the PLL bandwidth when exiting holdover, works with HOLDEXIT_BW_SEL0 and HOLD_BW_SEL1

Table 18.161. 0x05A4

Reg Address	Bit Field	Type	Setting Name	Description
0x05A4	7:0	R/W	HSW_LIMIT	Set by CBPro

Table 18.162. 0x05A5

Reg Address	Bit Field	Type	Setting Name	Description
0x05A5	0	R/W	HSW_LIMIT_ACTION	Set by CBPro

Table 18.163. 0x05A6 Hitless Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x05A6	2:0	R/W	RAMP_STEP_SIZE	Size of the frequency ramp steps when ramping between inputs or when exiting holdover. Calculated by CBPro based on selection.
0x05A6	3	R/W	RAMP_SWITCH_EN	Ramp Switching Enable 0: Disable Ramp Switching 1: Enable Ramp Switching (default)

Table 18.164. 0x05AC

Reg Address	Bit Field	Type	Setting Name	Description
0x05AC	0	R/W	OUT_MAX_LIMIT_EN	Set by CBPro

Table 18.165. 0x05AC

Reg Address	Bit Field	Type	Setting Name	Description
0x05AC	3	R/W	HOLD_SETTLE_DET_EN	Set by CBPro

Table 18.166. 0x05AD–0x05AE

Reg Address	Bit Field	Type	Setting Name	Description
0x05AD	7:0	R/W	OUT_MAX_LIMIT_LMT	Set by CBPro
0x05AE	15:8	R/W	OUT_MAX_LIMIT_LMT	Set by CBPro

Table 18.167. 0x05B1–0x05B2

Reg Address	Bit Field	Type	Setting Name	Description
0x05B1	7:0	R/W	HOLD_SETTLE_TARGET	Set by CBPro
0x05B2	15:8	R/W	HOLD_SETTLE_TARGET	Set by CBPro

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Table 18.168. 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	0 to use a crystal at the XAXB pins 1 to use an external clock source at the XAXB pins

Table 18.169. 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Name	Description
0x0943	0	R/W	IO_VDD_SEL	0 for 1.8 V external connections 1 for 3.3 V external connections

The IO_VDD_SEL configuration bit selects the option of operating the serial interface, and other control/status IO which are not controlled by VDDS via either the VDD or VDDA pins. These pins are always 3.3 V tolerant even when the device's VDD pin is supplied from a 1.8 V source. When the I^2C or SPI host is operating at 3.3 V and the Si5395/94/92 at VDD = 1.8 V, the host must write the IO_VDD_SEL configuration bit to the VDDA option. This will ensure that both the host and the serial interface are operating at the optimum voltage thresholds. The pins that are controlled by the IO_VDD_SEL bit are I2C_SEL, IN_SEL, RSTb, OEb, A1, SCLK, A0/CSb, SDA/SDIO, INTRb, and SDO.

Table 18.170. 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Name	Description
0x0949	3:0	R/W	IN_EN	0: Disable and Powerdown Input Buffer. 1: Enable Input Buffer for IN3–IN0.
0x0949	7:4	R/W	IN_PULSED_CMOS_EN	0: Standard Input Format. 1: Pulsed CMOS Input Format for IN3–IN0. See Section 5. Clock Inputs for more information.

When a clock input is disabled, it is powered down.

Input 0 corresponds to IN_SEL 0x0949 [0], IN_PULSED_CMOS_EN 0x0949 [4]

Input 1 corresponds to IN_SEL 0x0949 [1], IN_PULSED_CMOS_EN 0x0949 [5]

Input 2 corresponds to IN_SEL 0x0949 [2], IN_PULSED_CMOS_EN 0x0949 [6]

Input 3 corresponds to IN_SEL 0x0949 [3], IN_PULSED_CMOS_EN 0x0949 [7]

Table 18.171. 0x094A Input Clock Enable to DSPLL

Reg Address	Bit Field	Type	Setting Name	Description
0x094A	3:0	R/W	INX_TO_PFD_EN	Value calculated in CBPro

Table 18.172. 0x094E–0x094F Input Clock Buffer Hysteresis

Reg Address	Bit Field	Type	Setting Name	Description
0x094E	7:0	R/W	REFCLK_HYS_SEL	Value calculated in CBPro
0x094F	3:0	R/W	REFCLK_HYS_SEL	

Table 18.173. 0x094F CMOS High Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x094F	7:4	R/W	IN_CMOS_USE1P8	0 = selects the Pulsed CMOS input buffer mode 1 = selects the LVCMOS input buffer mode

Table 18.174. 0x095E MXAXB Fractional Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x095E	0	R/W	MXAXB_INTE-GER	Set by CBPro

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Table 18.175. 0x0A02 Output Multisynth Integer Divide Mode

Reg Address	Bit Field	Type	Name	Description
0x0A02	4:0	R/W	N_ADD_0P5	Value calculated in CBPro

Table 18.176. 0x0A03 Output Multisynth Clock to Output Driver

Reg Address	Bit Field	Type	Name	Description
0x0A03	4:0	R/W	N_CLK_TO_OUTX_EN	Routes Multisynth outputs to output driver muxes.

Table 18.177. 0x0A04 Output Multisynth Integer Divide Mode

Reg Address	Bit Field	Type	Name	Description
0x0A04	4:0	R/W	N_PIBYP	Output Multisynth integer divide mode. Bit 0 for ID0, Bit 1 for ID1, etc. 0: Nx divider is fractional. 1: Nx divider is integer.

A soft reset reg 0x001C [0] should be asserted after changing any of these bits. If it is expected that any of the N dividers will be changing from integer to fractional, it is recommended that the corresponding bits be initialized to 0 so that when the change from integer to fractional occurs there will be no need for a soft reset. For this reason, digitally controlled oscillator (DCO) and frequency on the fly (FOTF) applications should have zeros for these bits. See AN858: DCO Applications with Jitter Attenuators for more information.

Table 18.178. 0x0A05 Output Multisynth Divider Power Down

Reg Address	Bit Field	Type	Name	Description
0x0A05	4:0	R/W	N_PDNB	Powers down the N dividers. Set to 0 to power down unused N dividers. Must set to 1 for all active N dividers. See also related registers 0x0A03 and 0x0B4A.

Table 18.179. Nx_HIGH_FREQ

Reg Address	Bit Field	Type	Name	Description
0x0A14	3	R/W	N0_HIGH_FREQ	Set by CBPro.
0x0A1A	3	R/W	N1_HIGH_FREQ	Set by CBPro.

Table 18.180. 0x0A38 N0 Dynamic Phase Adjust Step Size

Reg Address	Bit Field	Type	Name	Description
0x0A38	7:0	R/W	N0_PHASE_STEP	N0 step size from 1 to 255 in units of Tvco, the VCO period.

N0_PHASE_STEP and N0_PHASE_COUNT are used to produce a phase change anywhere from 0 degrees to 360 degrees with a resolution of the VCO period. N0_PHASE_STEP can be invoked multiple times by using N0_PHASE_COUNT. The phase change is initiated by writing to either N0_PHASE_INC or N0_PHASE_DEC (at addr 0x0A3B). The resulting phase change will be:

N0_PHASE_STEP * N0_PHASE_COUNT * Tvco, for Tvco = 1 / Fvco

Table 18.181. 0x0A39 N0 Dynamic Phase Adjust Step Size Count

Reg Address	Bit Field	Type	Name	Description
0x0A39	7:0	R/W	N0_PHASE_COUNT	Lower byte of number of N0 step size changes.
0x0A3A	15:8	R/W	N0_PHASE_COUNT	Upper byte of number of N0 step size changes.

Table 18.182. 0x0A3B N0 Dynamic Phase Adjust Command

Reg Address	Bit Field	Type	Name	Description
0x0A3B	0	R/W	N0_PHASE_INC	Writing a 1 initiates a phase increment.
0x0A3B	1	R/W	N0_PHASE_DEC	Writing a 1 initiates a phase decrement.

Once set, these register bits will self clear as soon as the entire phase adjust sequence has completed.

N1 dynamic phase adjust works the same as N0 dynamic phase adjust (0xA38).

Table 18.183. 0x0A3C N1 Dynamic Phase Adjust Step Size

Reg Address	Bit Field	Type	Name	Description
0x0A3C	7:0	R/W	N1_PHASE_STEP	N1 step size from 1 to 255 in units of Tvco, the VCO period.

Table 18.184. 0x0A3D N1 Dynamic Phase Adjust Step Size Count

Reg Address	Bit Field	Type	Name	Description
0x0A3D	7:0	R/W	N1_PHASE_COUNT	Lower byte of number of N1 step size changes.
0x0A3E	15:8	R/W	N1_PHASE_COUNT	Upper byte of number of N1 step size changes.

Table 18.185. 0x0A3F N1 Dynamic Phase Adjust Command

Reg Address	Bit Field	Type	Name	Description
0x0A3F	0	R/W	N1_PHASE_INC	Writing a 1 initiates a phase increment.
0x0A3F	1	R/W	N1_PHASE_DEC	Writing a 1 initiates a phase decrement.

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Table 18.186. 0x0B24

Reg Address	Bit Field	Type	Name	Description
0x0B24	3:0	R/W	RESERVED	Reserved. This register is used when making certain changes to the device. See Section 4.2 Dynamic PLL Changes for more information.

Table 18.187. 0x0B25

Reg Address	Bit Field	Type	Name	Description
0x0B25	3:0	R/W	RESERVED	Reserved. This register is used when making certain changes to the device. See Section 4.2 Dynamic PLL Changes for more information.

Table 18.188. 0x0B44 Output Multisynth Clock to Output Driver

Reg Address	Bit Field	Type	Name	Description
0x0B44	3:0	R/W	PDIV_FRACN_CLK_DIS	Disable digital clocks to input P (IN0–3) fractional dividers.
0x0B44	5	R/W	FRACN_CLK_DIS_PLL	Disable digital clock to M fractional divider.

Table 18.189. 0x0B46

Reg Address	Bit Field	Type	Name	Description
0x0B46	3:0	R/W	LOS_CLK_DIS	Set to 0 for normal operation.

Table 18.190. 0x0B47

Reg Address	Bit Field	Type	Name	Description
0x0B47	4:0	R/W	OOF_CLK_DIS	Set to 0 for normal operation.

Table 18.191. 0x0B48 OOF Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B48	4:0	R/W	OOF_DIV_CLK_DIS	Set to 0 for normal operation Digital OOF divider clock user disable. Bits 3:0 are for IN3,2,1,0, Bit 4 is for OOF for the XAXB input

Table 18.192. 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	4:0	R/W	N_CLK_DIS	Disable digital clocks to N dividers. Must be set to 0 to use each N divider. See also related registers 0x0A03 and 0x0A05.

Table 18.193. 0x0B57-0x0B58 VCO Calcode

Reg Address	Bit Field	Type	Name	Description
0x0B57	7:0	R/W	VCO_RESET_CALCODE	12-bit value. Controls the VCO frequency when a reset occurs.
0x0B58	11:8	R/W	VCO_RESET_CALCODE	

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Table 18.194. 0x0C02

Reg Address	Bit Field	Type	Name	Description
0x0C02	2:0	R/W	VAL_DIV_CTL0	Set by CBPro

Table 18.195. 0x0C02

Reg Address	Bit Field	Type	Name	Description
0x0C02	4	R/W	VAL_DIV_CTL1	Set by CBPro

Table 18.196. 0x0C03

Reg Address	Bit Field	Type	Name	Description
0x0C03	3:0	R/W	IN_CLK_VAL_PWR_UP_DIS	Set by CBPro

Table 18.197. 0x0C07

Reg Address	Bit Field	Type	Name	Description
0x0C07	0	R/W	IN_CLK_VAL_EN	Set by CBPro

Table 18.198. 0x0C08

Reg Address	Bit Field	Type	Name	Description
0x0C08	7:0	R/W	IN_CLK_VAL_TIME	Set by CBPro

19. Revision History

Revision 1.2

January 2020

- Fixed Error in Register 0x0004 Device Grade. The internal reference grades had a numerical error.
- Added Section 5.2.3 Use Case Scenario: Using More Than Two Inputs.

Revision 1.1

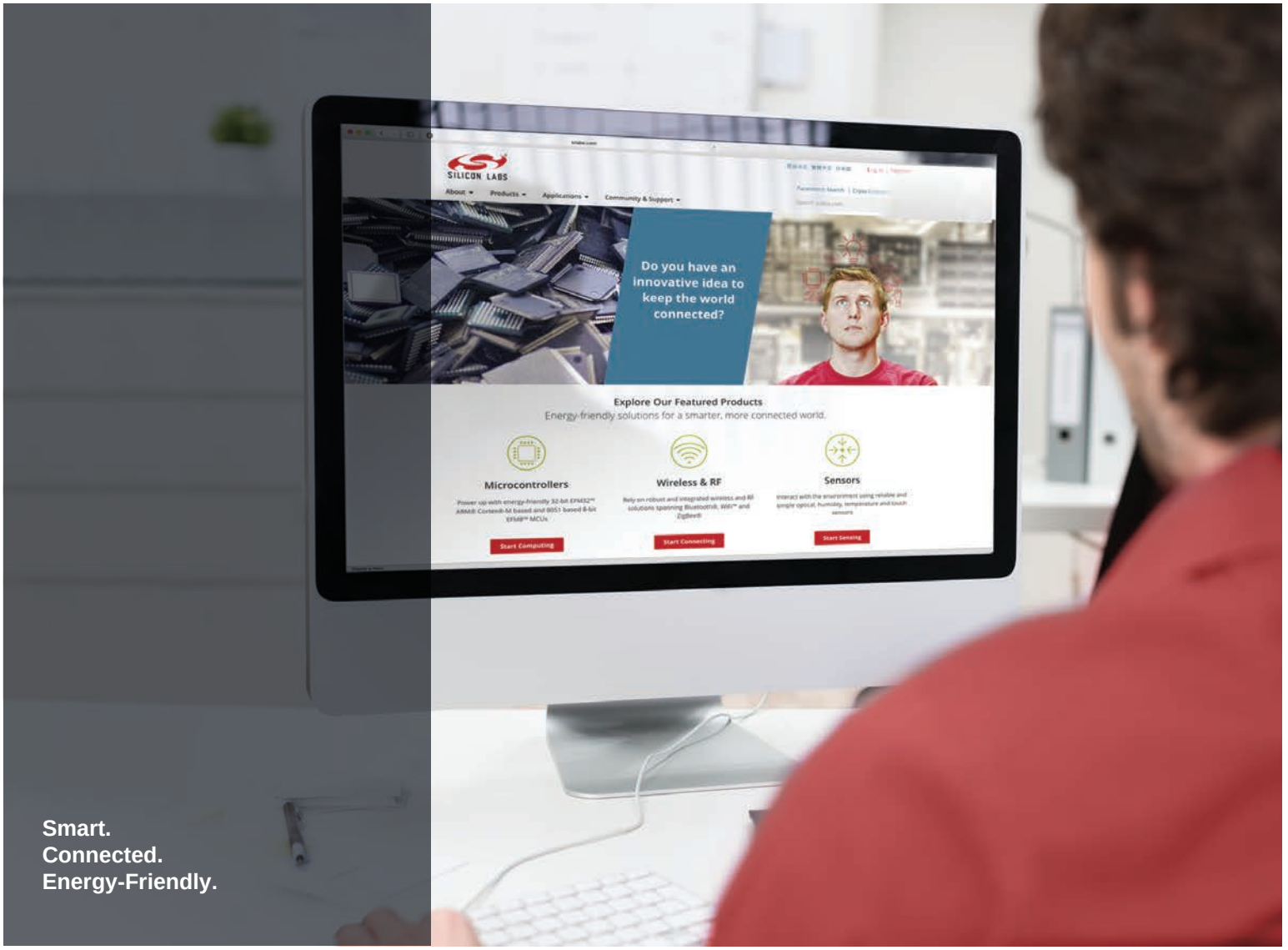
June 2019

- Update CMOS input buffer section
- Updated Grade P/E Rules
- Added information for internal reference devices

Revision 0.1

June 2018

- Intitial Release



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