

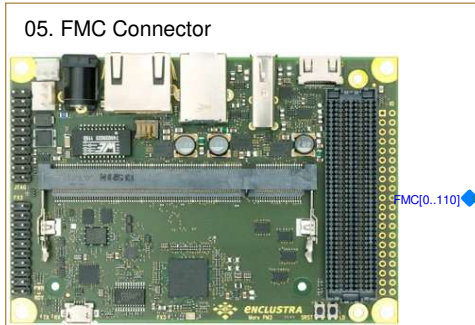
VCCIO (2.5V or 3.3V) is set on the Enclustra PM3 board using a DIP switch.
The GIB requires 2.5V!

D

C

B

A



05. FMC Connector

Utilities

06. Utilities

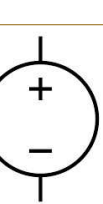
GPS Interface

01. GPS Interface



Clock Generation

02. Clock Generation



Power

04. Power

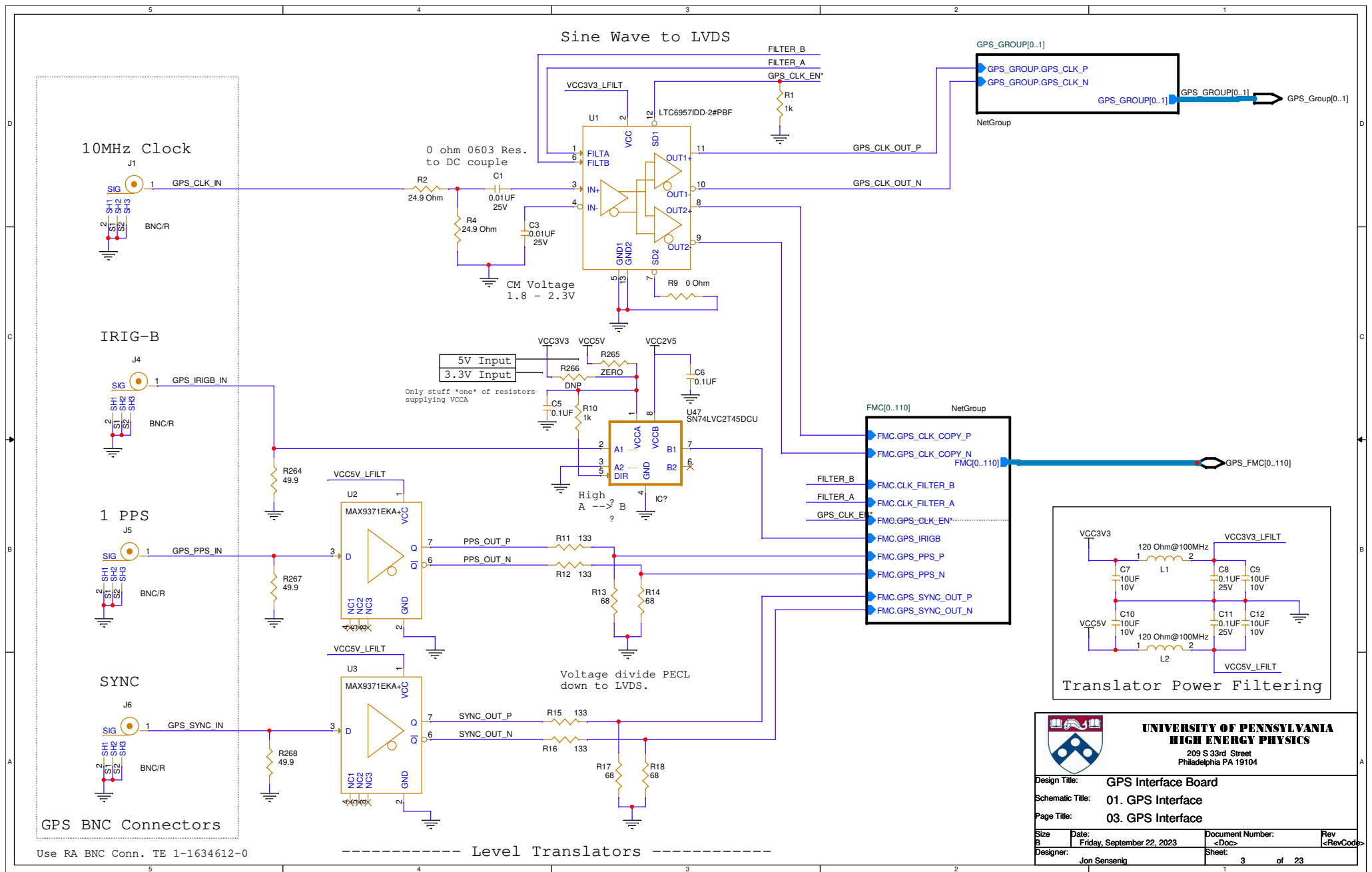
SFP Interface

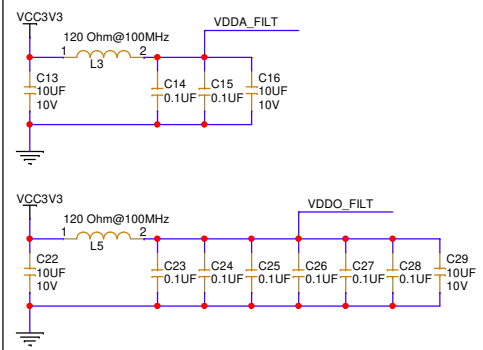
03. SFP Interface



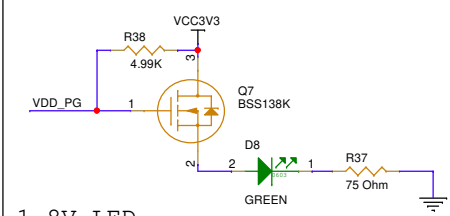
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Design Title: GPS Interface Board			
Schematic Title: 00. GIB Top			
Page Title: 02. Top Level			
Size B	Date: Thursday, August 29, 2024	Document Number:	Rev
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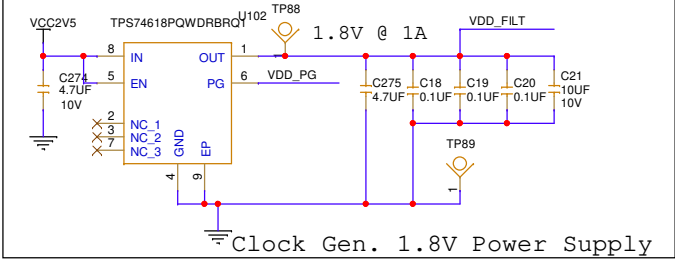




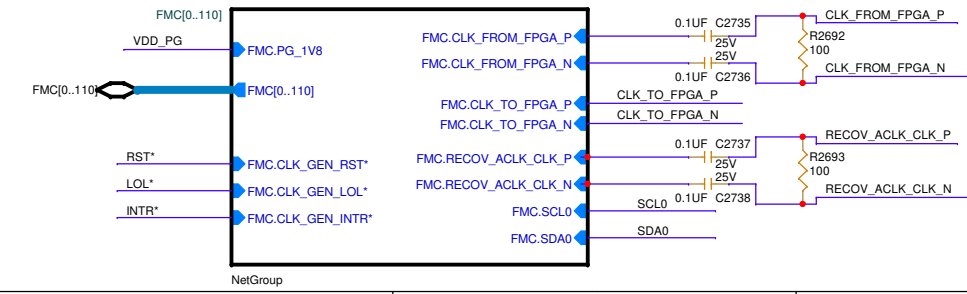
Clock Gen. Power Filtering



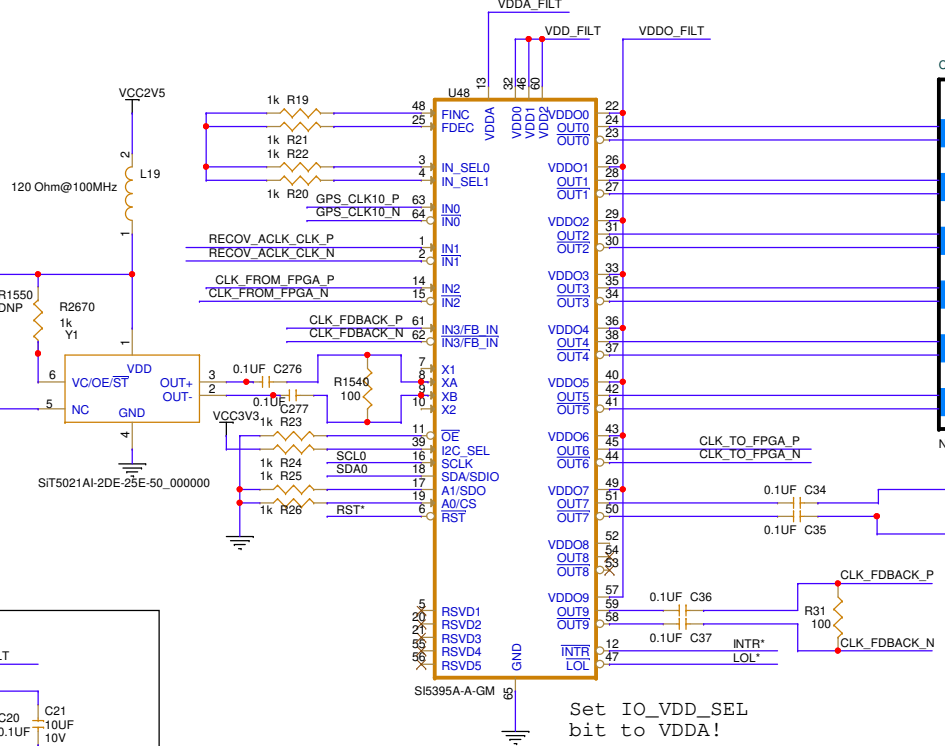
1.8V LED



Clock Gen. 1.8V Power Supply

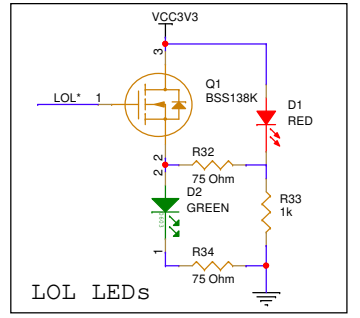
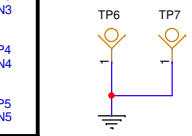
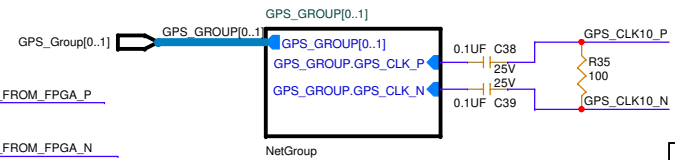


Clock Generator (312.5 MHz)




Set IO_VDD_SEL bit to VDDA!

I2C Address = 0x68

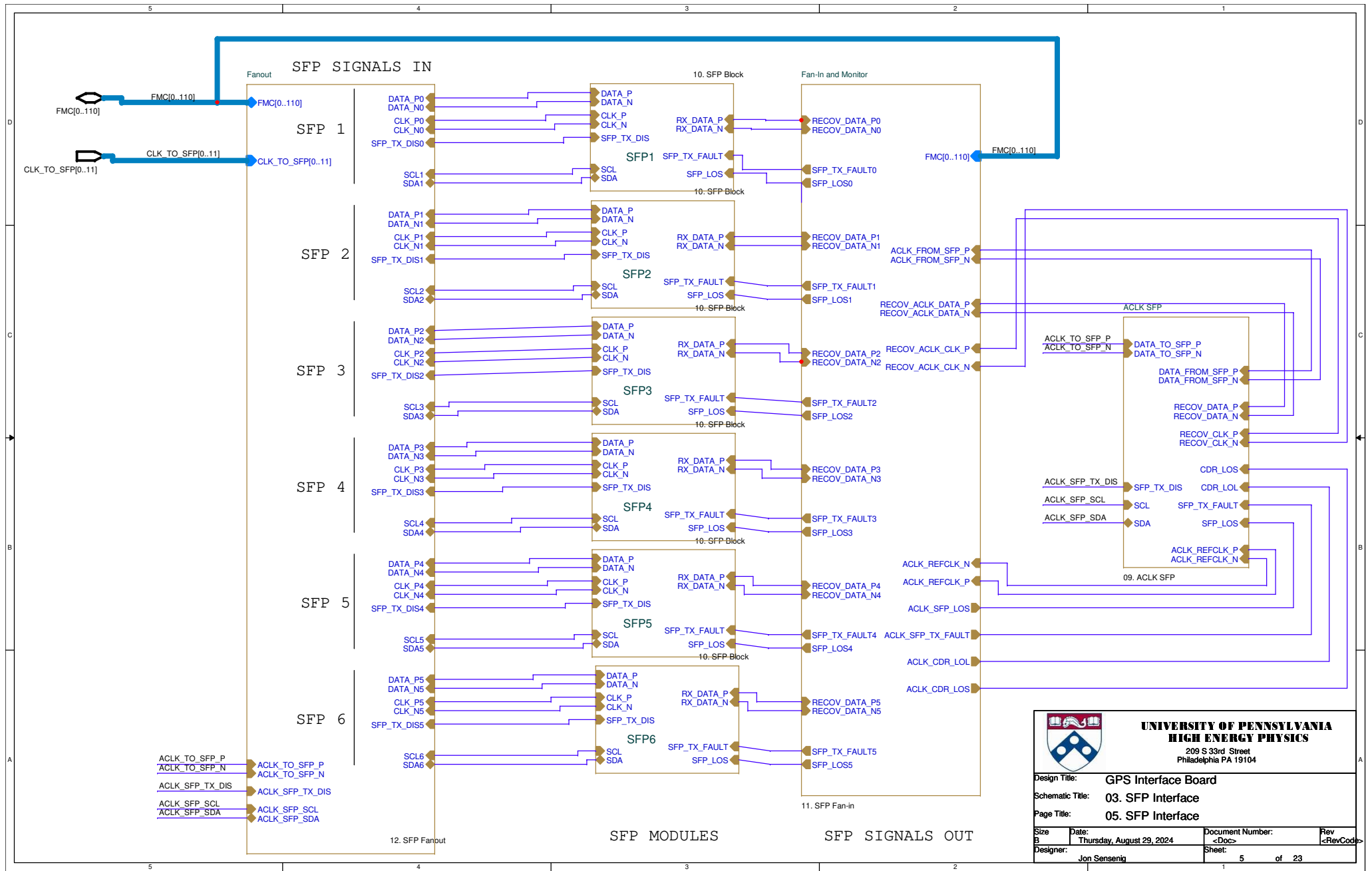


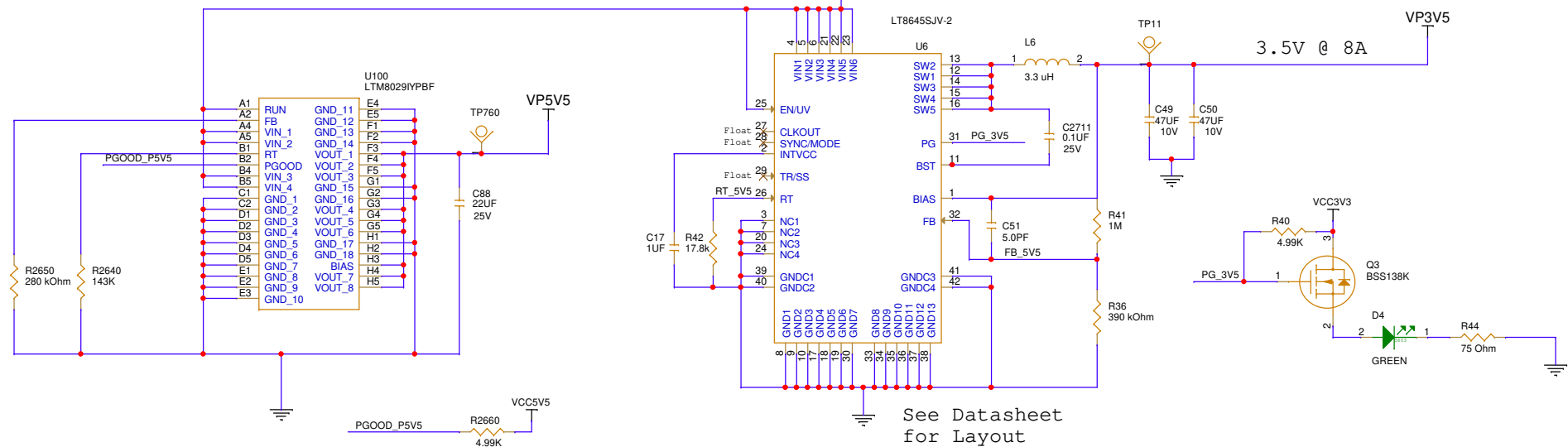
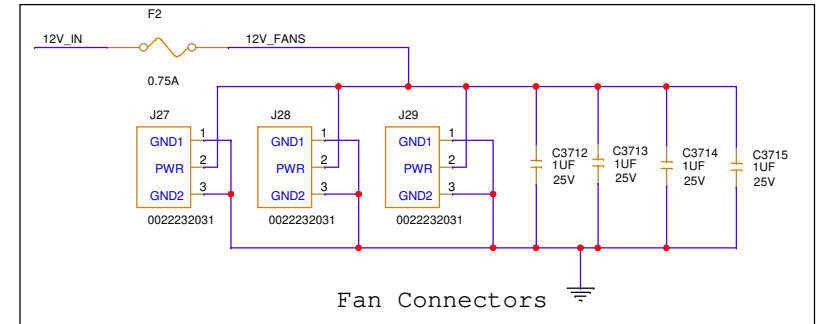
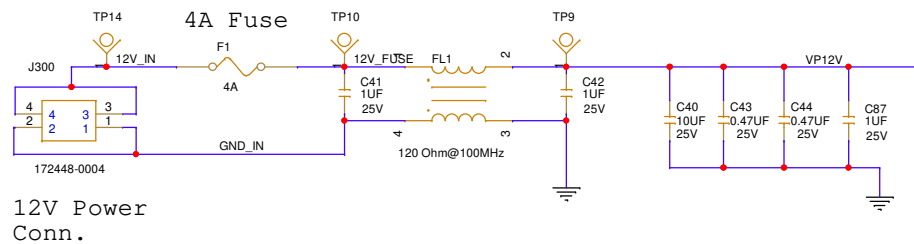
LOL LEDs



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Schematic Title: 02. Clock Generation			
Page Title: 04. Clock Generation			
Size: B	Date: Friday, September 22, 2023	Document Number: <Doc>	Rev: <RevCode>
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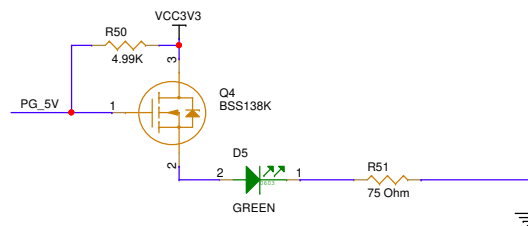
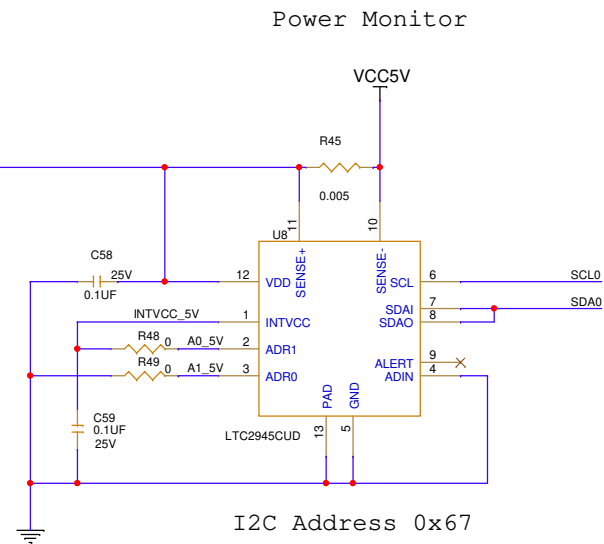
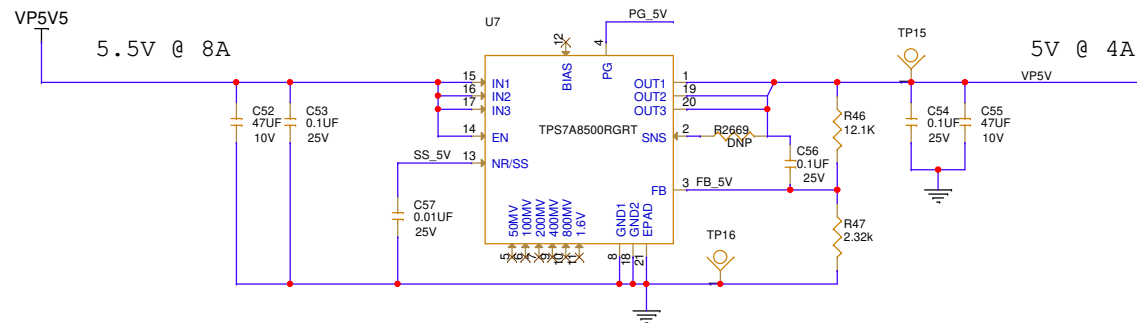





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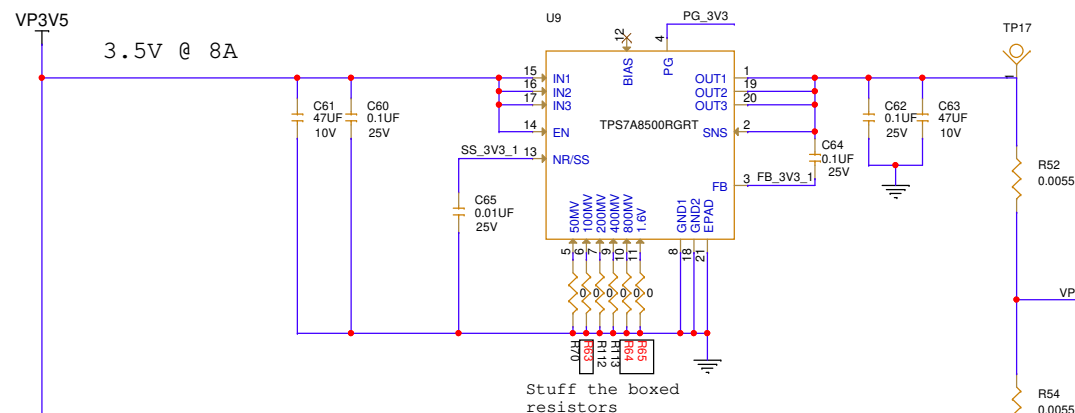
Design Title: **GPS Interface Board**
Schematic Title: **04. Power**
Page Title: **06. Power 12V Main**

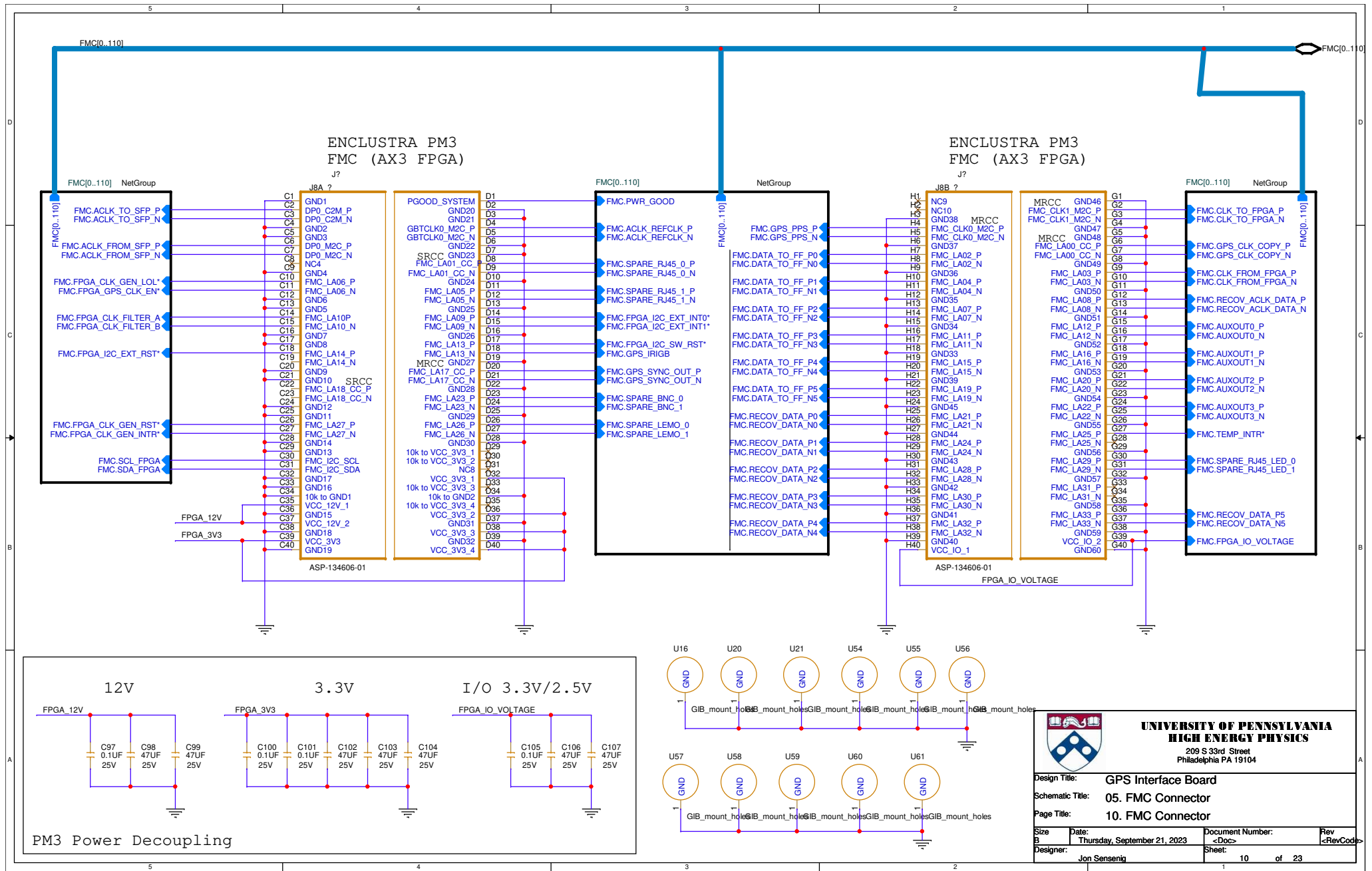
Size: **B** Date: **Thursday, September 21, 2023** Document Number: **<Doc>** Rev: **<RevCode>**
Designer: **Jon Sensenig** Sheet: **6** of **23**

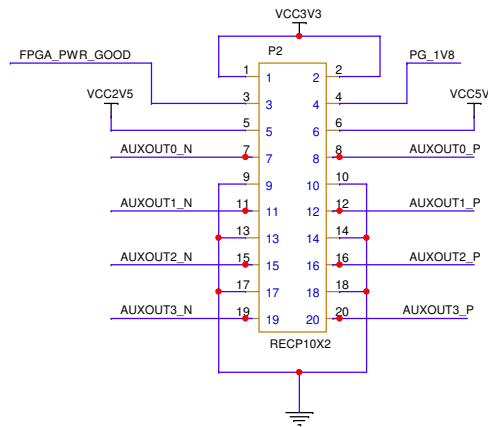


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Design Title:	GPS Interface Board		
Schematic Title:	04. Power		
Page Title:	07. Power VCC5V		
Size B	Date: Thursday, September 21, 2023	Document Number: <Doc>	Rev <RevCode>
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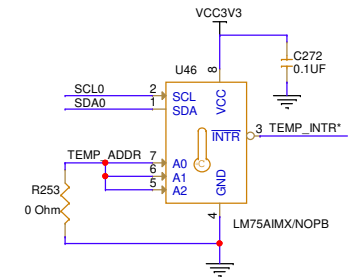
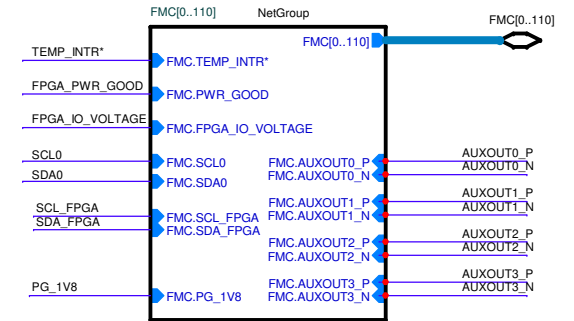
SCL0 << SCL0
SDA0 << SDA0







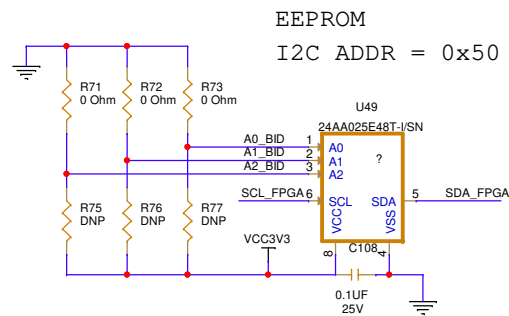
Connections to front panel LEDs / Auxilliary I/O



I2C ADDR = 0x48

Temp. Monitor

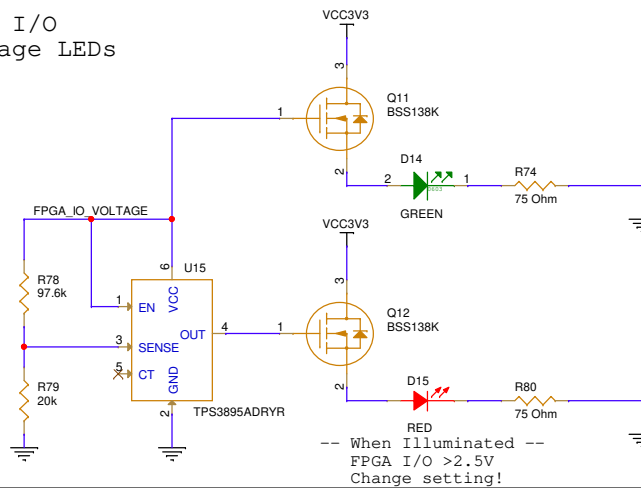
Note: Temperature measured from component's die.




EEPROM
I2C ADDR = 0x50

Board ID

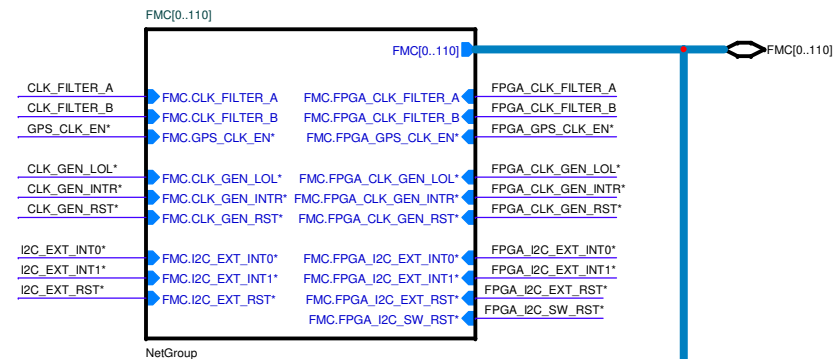
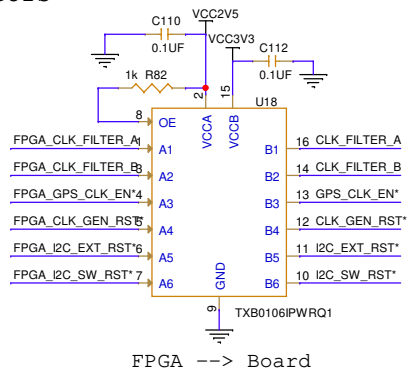
FPGA I/O
Voltage LEDs



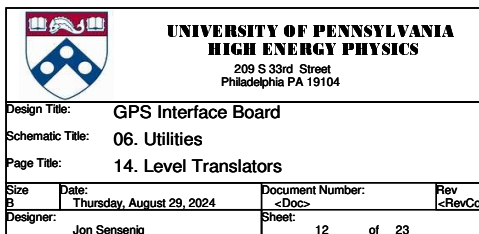
-- When Illuminated --
FPGA I/O >2.5V
Change setting!

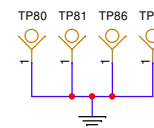
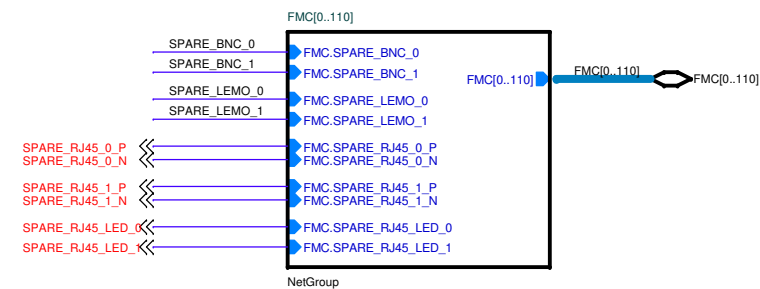
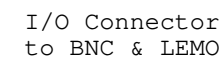
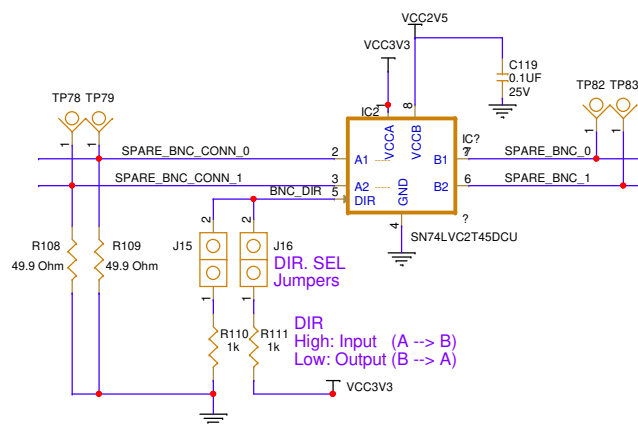
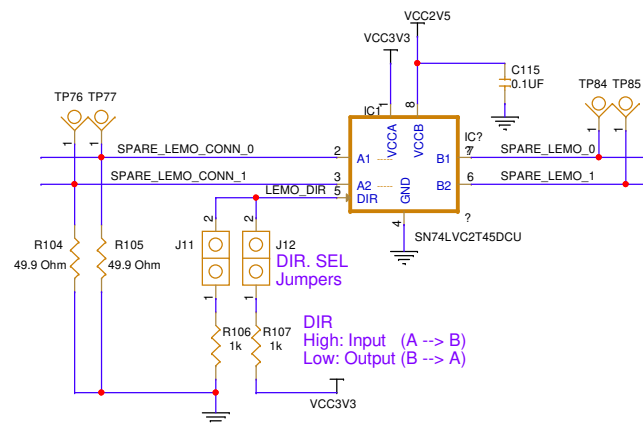
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Design Title:	GPS Interface Board		
Schematic Title:	06. Utilities		
Page Title:	13. Utilities		
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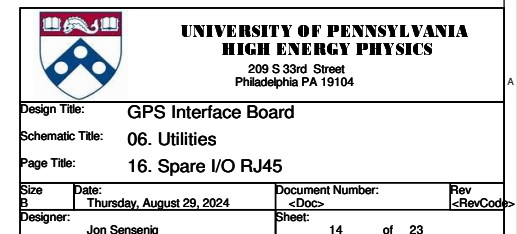
Board --> FPGA

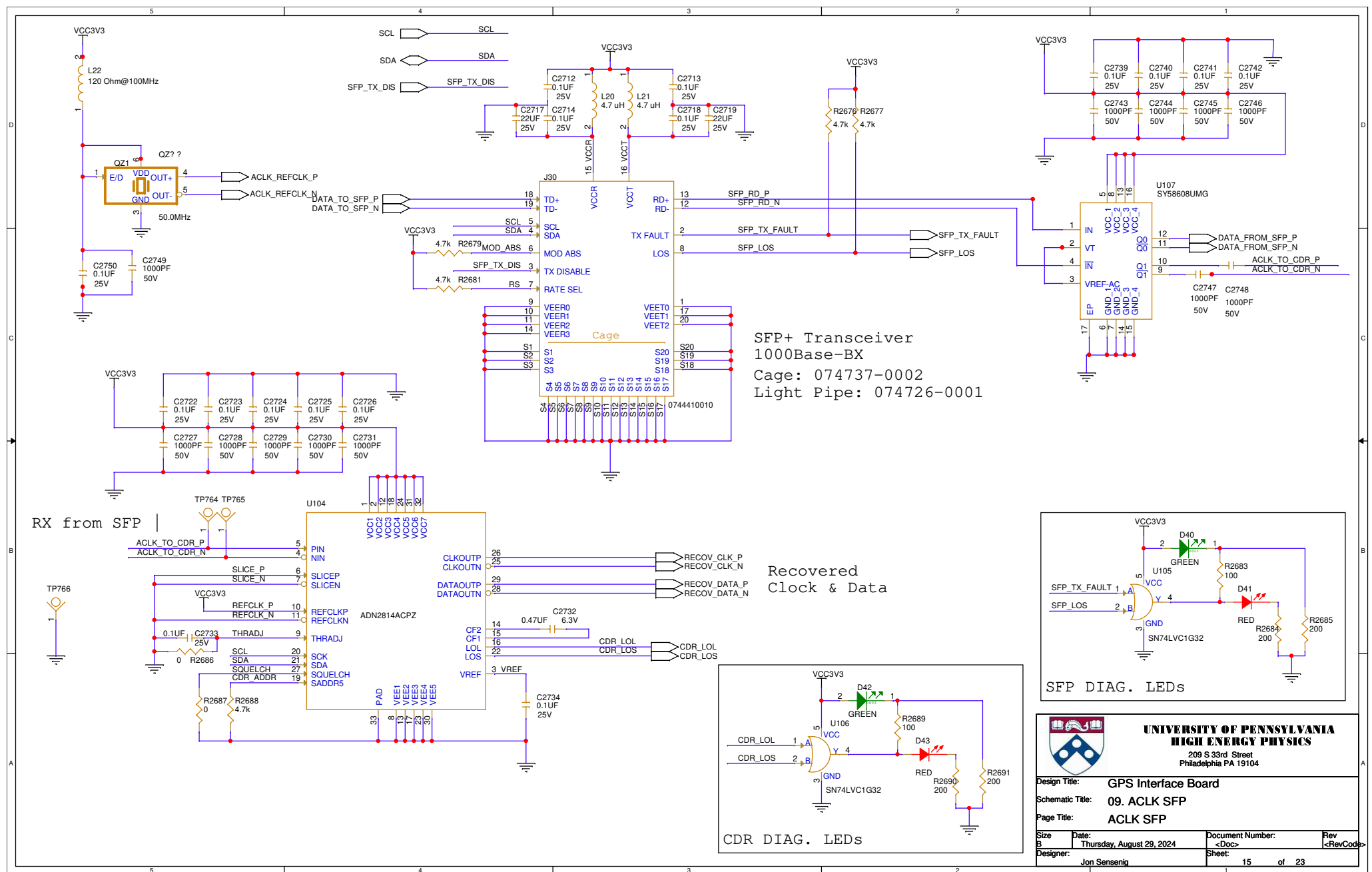


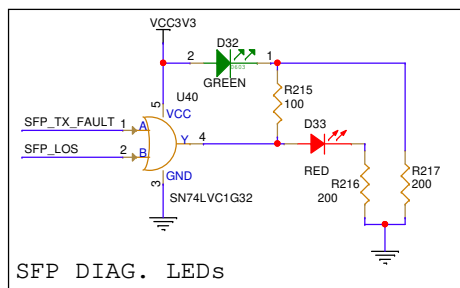
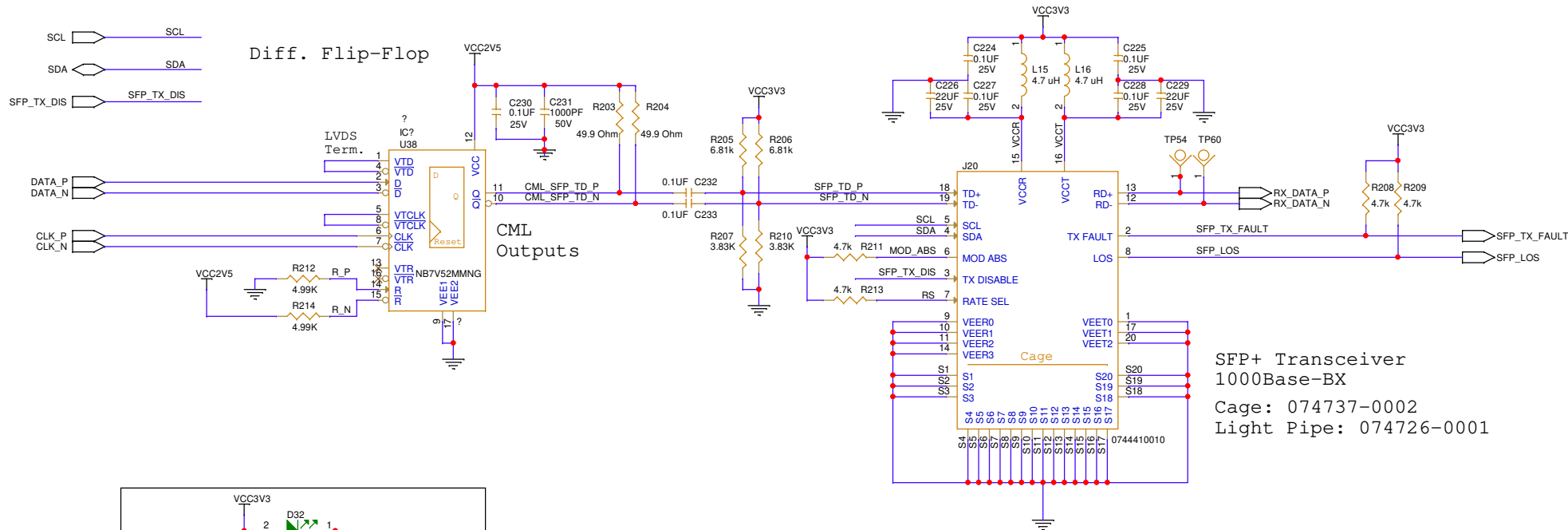
The diagram illustrates the PCB layout for an I2C switch circuit. The I2C switch IC (U19, TCA9548APWR) is connected to an I2C master (SCL_FPGA, SDA_FPGA) and multiple I2C slaves (FMC_SCL0 to FMC_SDA7). The switch is controlled by an I2C SW_RST* signal. The layout shows various components like resistors (R83-R103), capacitors (C113), and test points (TP23, TP38-TP45, TP80-TP89, TP93-TP96).












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Schematic Title:	10. SFP Block		
Page Title:	SFP		
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