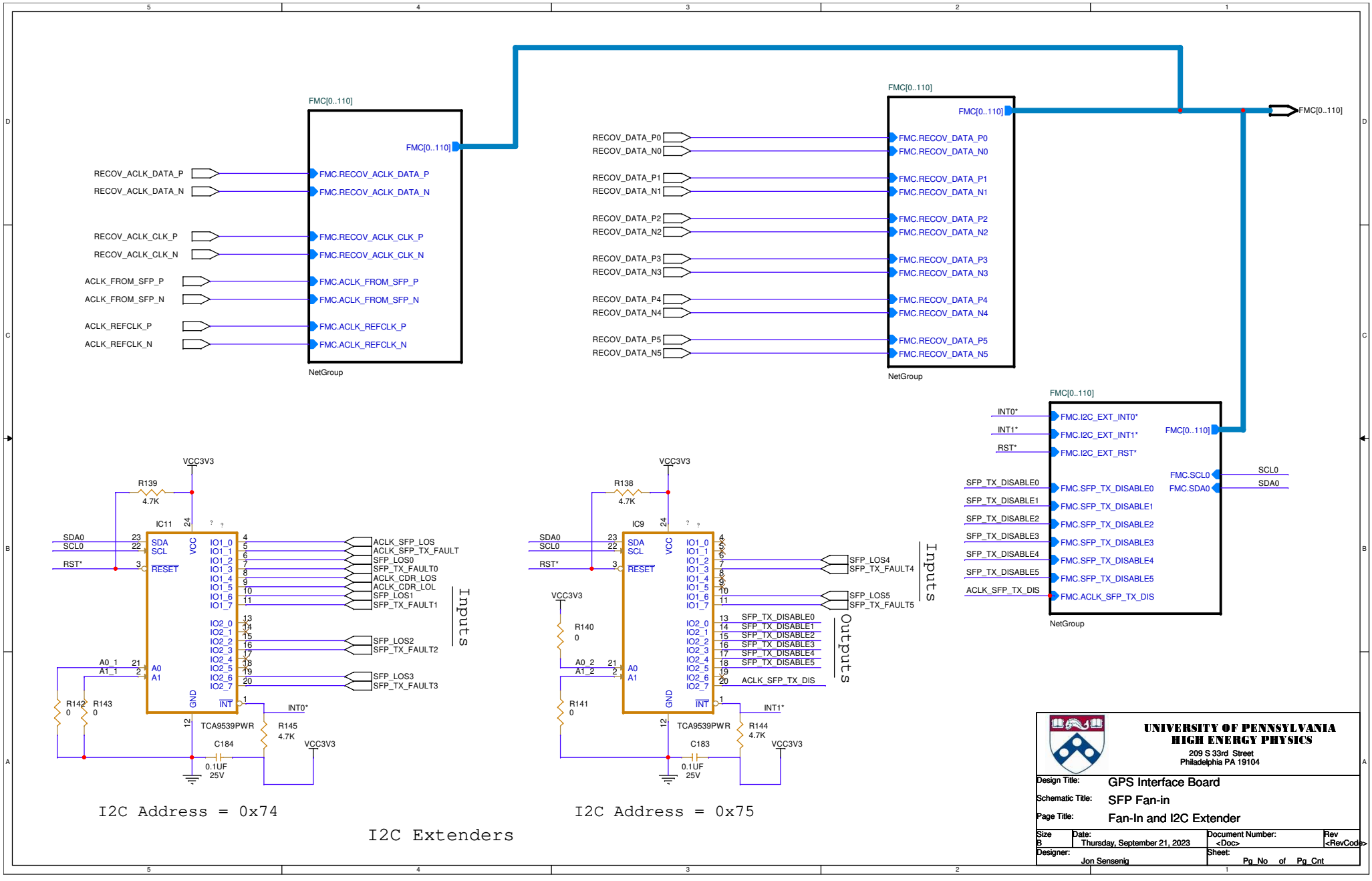
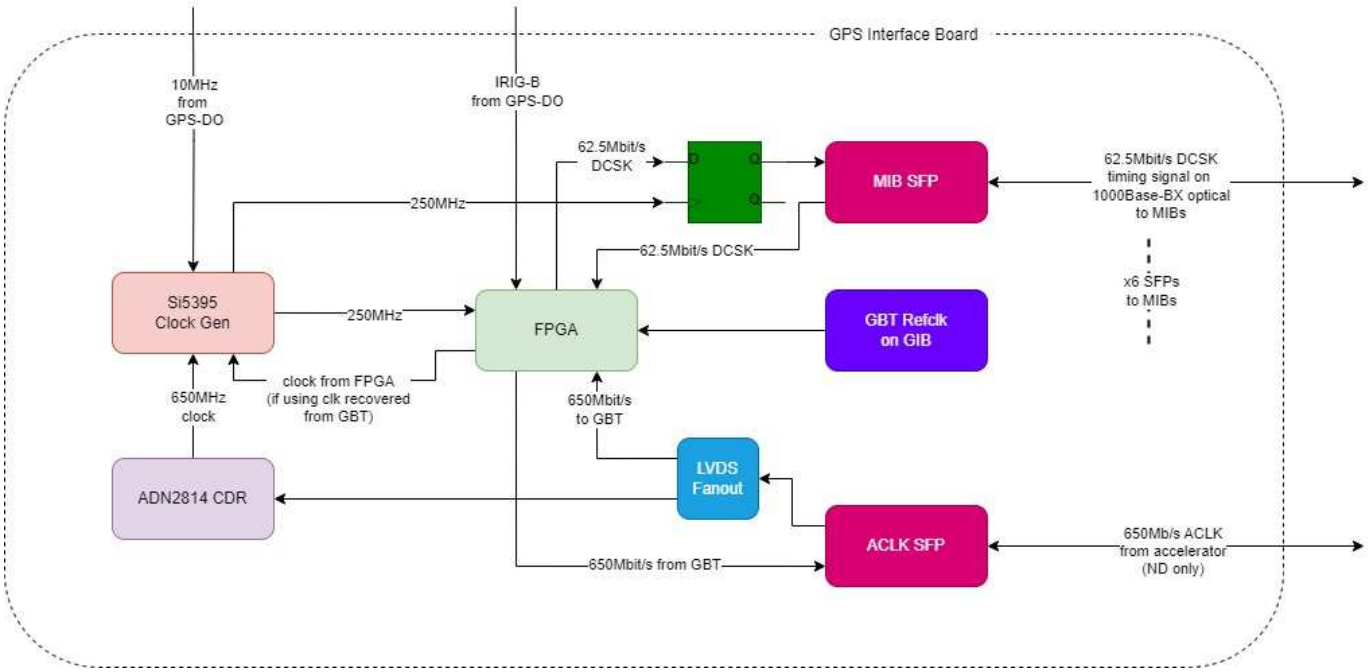

FMC[0..110]
RECOV_ACLK_DATA_P
RECOV_ACLK_DATA_N
RECOV_ACLK_CLK_P
RECOV_ACLK_CLK_N
ACLK_FROM_SFP_P
ACLK_FROM_SFP_N
ACLK_REFCLK_P
ACLK_REFCLK_N
FMC.RECOV_ACLK_DATA_P
FMC.RECOV_ACLK_DATA_N
FMC.RECOV_ACLK_CLK_P
FMC.RECOV_ACLK_CLK_N
FMC.ACLK_FROM_SFP_P
FMC.ACLK_FROM_SFP_N
FMC.ACLK_REFCLK_P
FMC.ACLK_REFCLK_N
NetGroup
RECOV_DATA_P0
RECOV_DATA_N0
RECOV_DATA_P1
RECOV_DATA_N1
RECOV_DATA_P2
RECOV_DATA_N2
RECOV_DATA_P3
RECOV_DATA_N3
RECOV_DATA_P4
RECOV_DATA_N4
RECOV_DATA_P5
RECOV_DATA_N5
FMC.RECOV_DATA_P0
FMC.RECOV_DATA_N0
FMC.RECOV_DATA_P1
FMC.RECOV_DATA_N1
FMC.RECOV_DATA_P2
FMC.RECOV_DATA_N2
FMC.RECOV_DATA_P3
FMC.RECOV_DATA_N3
FMC.RECOV_DATA_P4
FMC.RECOV_DATA_N4
FMC.RECOV_DATA_P5
FMC.RECOV_DATA_N5
INT0*
INT1*
RST*
FMC.I2C_EXT_INT0*
FMC.I2C_EXT_INT1*
FMC.I2C_EXT_RST*
FMC.SCL0
FMC.SDA0
SCL0
SDA0
SFP_TX_DISABLE0
SFP_TX_DISABLE1
SFP_TX_DISABLE2
SFP_TX_DISABLE3
SFP_TX_DISABLE4
SFP_TX_DISABLE5
ACLK_SFP_TX_DIS
FMC.SFP_TX_DISABLE0
FMC.SFP_TX_DISABLE1
FMC.SFP_TX_DISABLE2
FMC.SFP_TX_DISABLE3
FMC.SFP_TX_DISABLE4
FMC.SFP_TX_DISABLE5
FMC.ACLK_SFP_TX_DIS
VCC3V3
R139
4.7K
IC11
TCA9539PWR
SDA0
SCL0
RST*
A0_1
A1_1
R142
R143
0
C184
0.1UF
25V
R145
4.7K
INT0*
ACLK_SFP_LOS
ACLK_SFP_TX_FAULT
SFP_LOS0
SFP_TX_FAULT0
ACLK_CDR_LOS
ACLK_CDR_LOL
SFP_LOS1
SFP_TX_FAULT1
SFP_LOS2
SFP_TX_FAULT2
SFP_LOS3
SFP_TX_FAULT3
Inputs
R138
IC9
A0_2
A1_2
R140
R141
C183
R144
INT1*
SFP_LOS4
SFP_TX_FAULT4
SFP_LOS5
SFP_TX_FAULT5
SFP_TX_DISABLE0
SFP_TX_DISABLE1
SFP_TX_DISABLE2
SFP_TX_DISABLE3
SFP_TX_DISABLE4
SFP_TX_DISABLE5
ACLK_SFP_TX_DIS
Outputs
I2C Address = 0x74
I2C Address = 0x75
I2C Extenders
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104
Design Title: GPS Interface Board
Schematic Title: SFP Fan-in
Page Title: Fan-In and I2C Extender
Size B
Date: Thursday, September 21, 2023
Document Number: <Doc>
Rev <RevCode>
Designer: Jon Sensenig
Sheet: Pg_No of Pg_Cnt



Part	I2C Address
ACLK SFP	0x50
ACLK CDR	0x40
SFP 1	0x50
SFP 2	
SFP 3	
SFP 4	
SFP 5	
SFP 6	

Part	I2C Address
Board ID EEPROM	0x50
SI5395 Clock Gen.	0x68
I2C Extender 1	0x74
I2C Extender 2	0x75
VCC5V Power Monitor	0x67
VCC3V3 Power Monitor	0x6A
VCC2V5 Power Monitor	0x69
I2C Switch	0x70
Temperature Monitor	0x48

Power Estimate			Max Current (mA)				
Part	Description	Occurence	VCC5V	VCC3V3	VCC2V5	VCC1V8	12V Main PWR
LTC6957-2	Sine Wave to LVDS	1		72			
MAX9371	Low Jitter 5V TTL to LVDS	2	16				
SN74avc2t45	5V <--> 3.3V	1	100	100			
SN74avc2t45	3.3V <--> 2.5V	5		100	100		
SI5395	Clock Generator	1		302		300	
LTC2945	Power Monitor	4	1.2				
24AA025E48T	Board ID EEPROM	1		3			
LEDs		13		20			
NB7V52M	Diff. Flip-Flop	6			90		
ADN2814	CDR	6		145			
SFP		6		280			
SN74lvc1g32	OR Gate	12		100			
PCA9539	I2C Extender	2		160			
TCA9548A	I2C Switch	1			100		
LM75A	Temp Monitor	1		20			
NC7SZ08	AND Gate	1		50			
SN65LVDM176	LVDS Transceiver	2		15			
TXB0104(6)	Level Translator	2		100	100		
	Totals	Current (A)	0.14	5.41	1.14	0.30	
		Power (W)	0.68	17.84	3.76	0.54	22.83
	Max Power Supply	Current (A)	2	8			4
		Power (W)	11	28			48

UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104

Design Title:	GPS Interface Board
Schematic Title:	GIB Top
Page Title:	01. Address Table

Size	Date:	Document Number:	Rev
B	Thursday, August 29, 2024	<Doc>	<RevCode>
Designer: Jon Sensenig		Sheet: 1 of 23	

VCCIO (2.5V or 3.3V) is set on the Enclustra PM3 board using a DIP switch.
The GIB requires 2.5V!

Power

04. Power

FMC[0..110]

FMC[0..110]

GPS Interface

01. GPS Interface

GPS_FMC[0..110]

GPS_Group[0..1]

GPS_GROUP[0..1]

Clock Generation

02. Clock Generation

GPS_Group[0..1]

CLK_TO_SFP[0..11]

CLK_TO_SFP[0..11]

FMC[0..110]

FMC[0..110]

05. FMC Connector

FMC[0..110]

FMC[0..110]

PM3_FMC

SFP Interface

03. SFP Interface

CLK_TO_SFP[0..11]

FMC[0..110]

FMC[0..110]

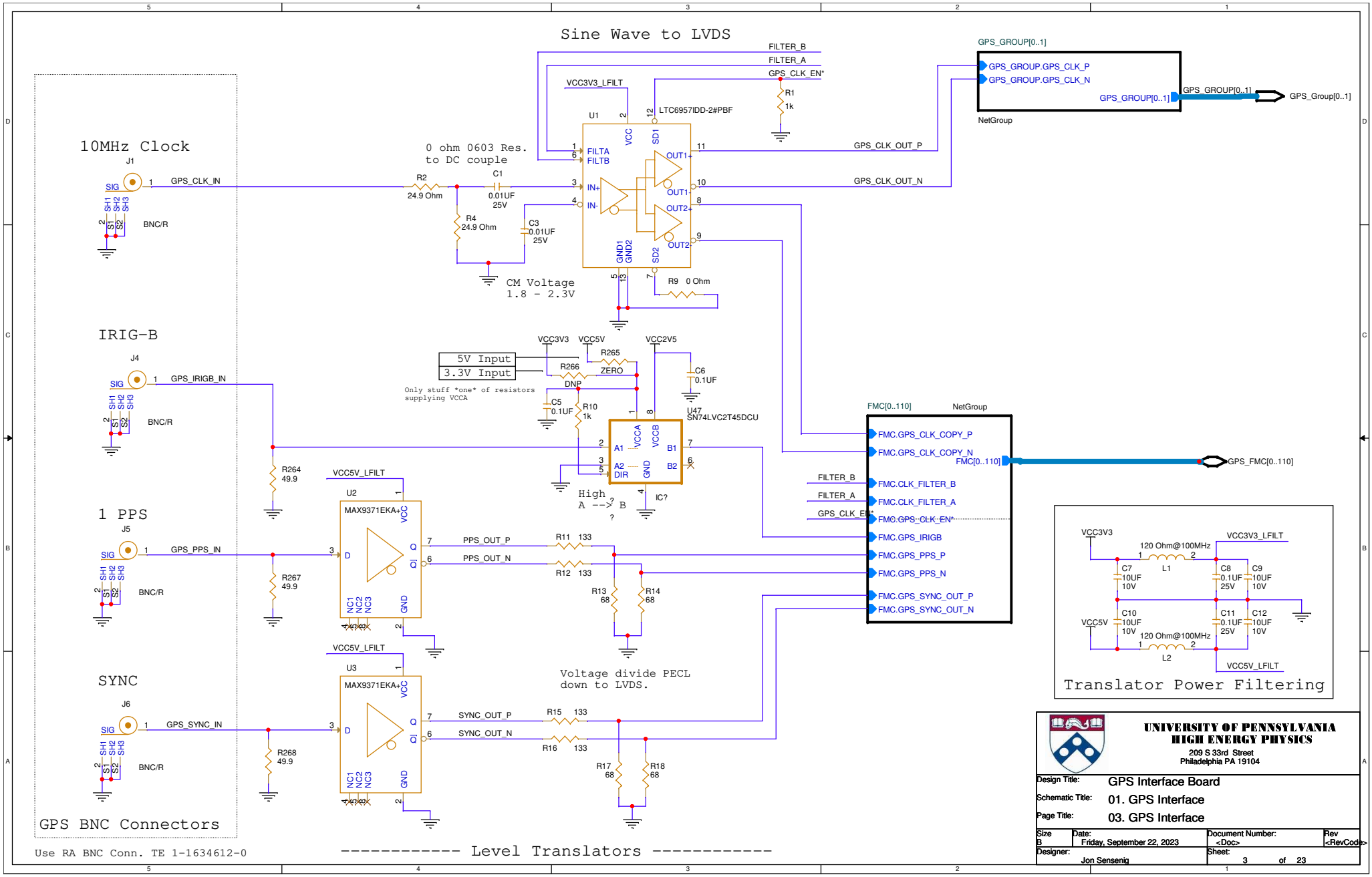
Utilities

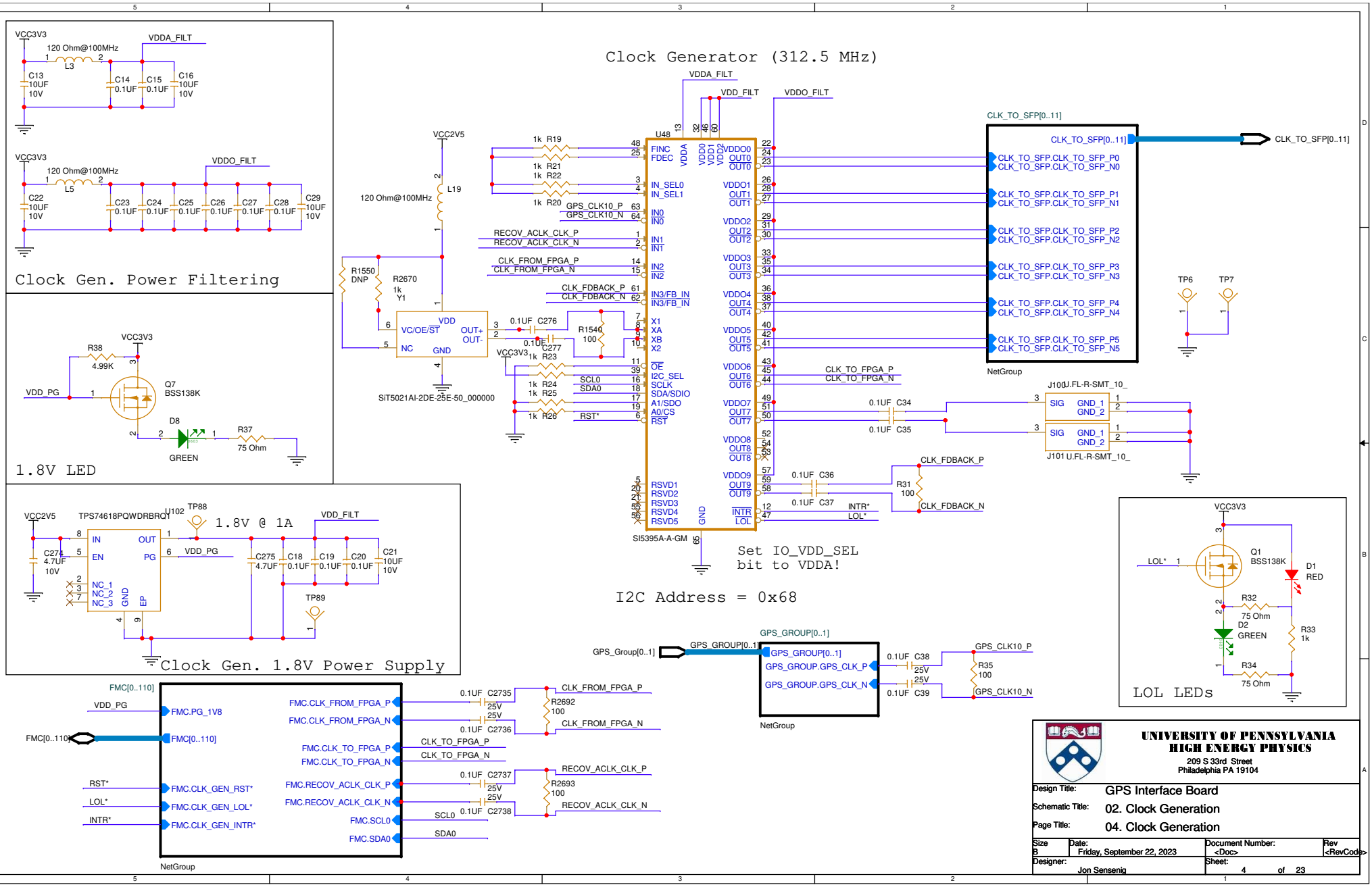
06. Utilities

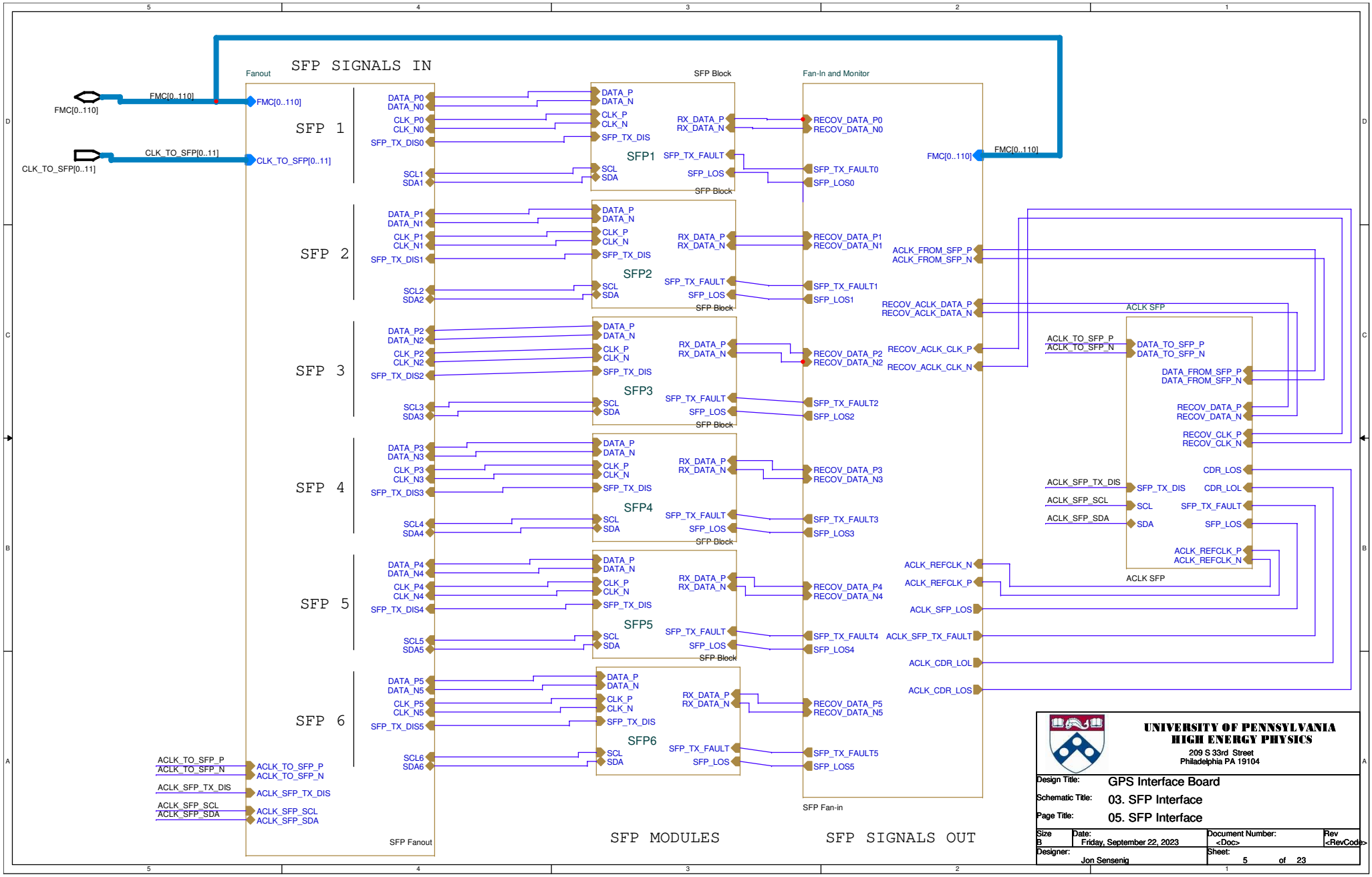
FMC[0..110]

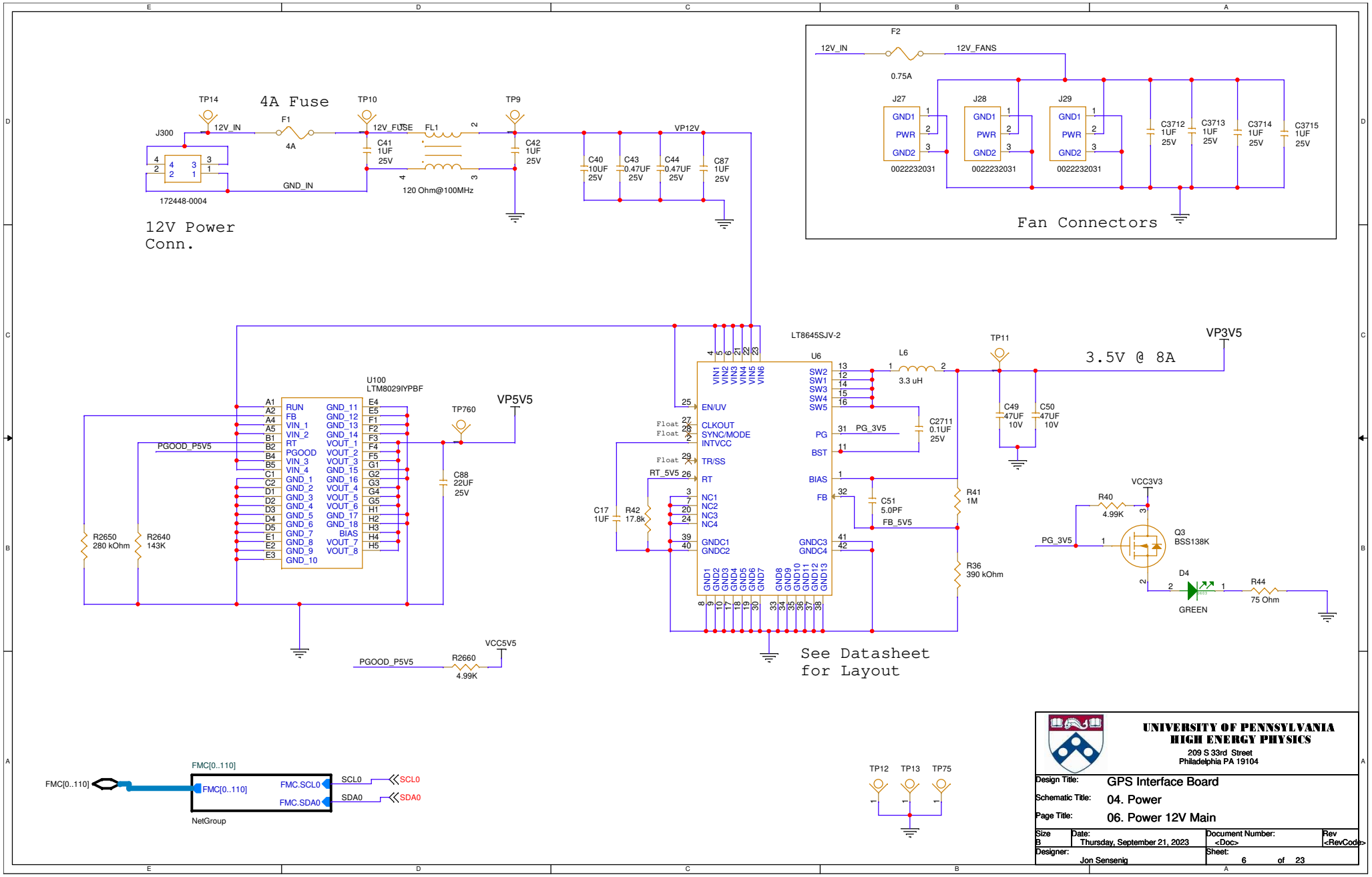
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104

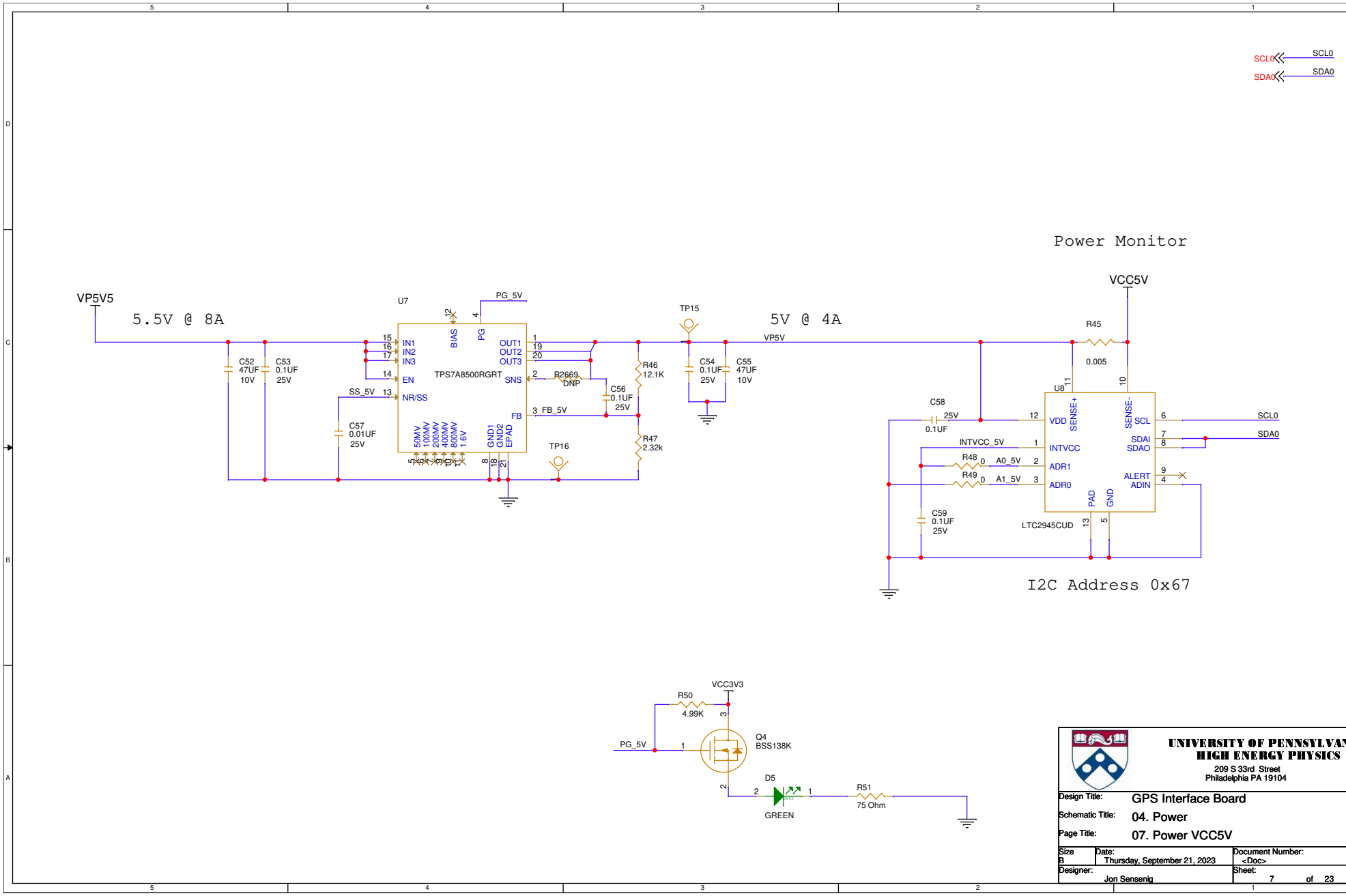
Design Title:	GPS Interface Board
Schematic Title:	GIB Top
Page Title:	02. Top Level
Size: B	Date: Thursday, September 21, 2023
Document Number:	Rev
Designer: Jon Sensenig	Sheet: 2 of 23

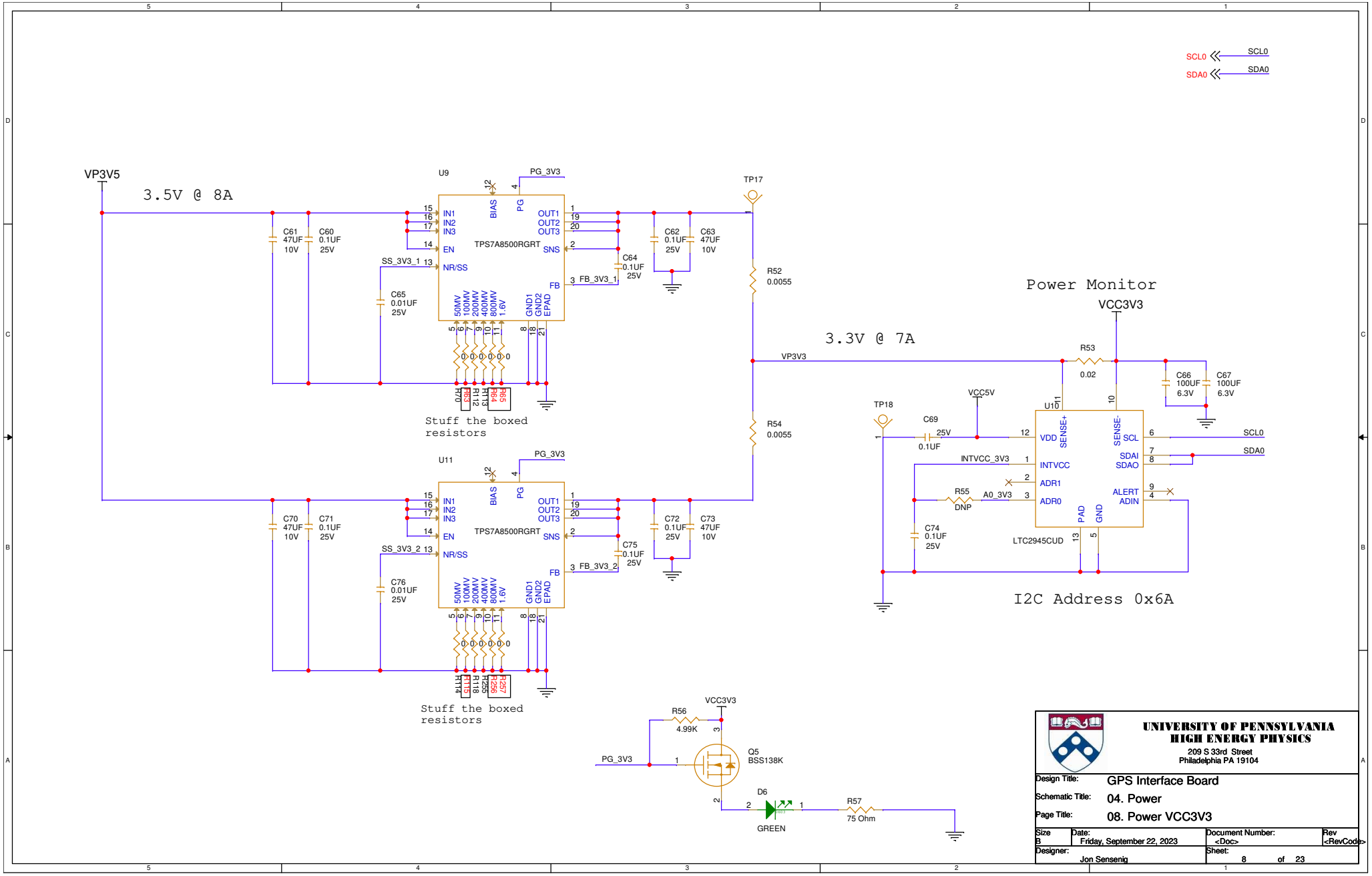

Sine Wave to LVDS
10MHz Clock
J1
SIG
GPS_CLK_IN
BNC/R
0 ohm 0603 Res.
to DC couple
R2
24.9 Ohm
C1
0.01UF
25V
R4
24.9 Ohm
C3
0.01UF
25V
CM Voltage
1.8 - 2.3V
U1
LTC6957IDD-2#PBF
FILTA
FILTB
VCC
SD1
IN+
IN-
OUT1+
OUT1-
OUT2+
OUT2-
GND1
GND2
SD2
FILTER_B
FILTER_A
GPS_CLK_EN*
VCC3V3_LFILT
R1
1k
GPS_CLK_OUT_P
GPS_CLK_OUT_N
R9 0 Ohm
GPS_GROUP[0..1]
GPS_GROUP.GPS_CLK_P
GPS_GROUP.GPS_CLK_N
NetGroup
GPS_Group[0..1]
IRIG-B
J4
GPS_IRIGB_IN
5V Input
3.3V Input
Only stuff *one* of resistors
supplying VCCA
VCC3V3
VCC5V
VCC2V5
R265
ZERO
R266
DNP
C6
0.1UF
C5
0.1UF
R10
1k
U47
SN74LVC2T45DCU
VCCA
VCCB
A1
A2
DIR
GND
B1
B2
IC?
High
A --> B
?
R264
49.9
VCC5V_LFILT
U2
MAX9371EKA+
1 PPS
J5
GPS_PPS_IN
R267
49.9
PPS_OUT_P
PPS_OUT_N
R11 133
R12 133
R13
68
R14
68
SYNC
J6
GPS_SYNC_IN
R268
49.9
U3
SYNC_OUT_P
SYNC_OUT_N
R15 133
R16 133
R17
68
R18
68
Voltage divide PECL
down to LVDS.
FMC[0..110]
NetGroup
FMC.GPS_CLK_COPY_P
FMC.GPS_CLK_COPY_N
FMC[0..110]
GPS_FMC[0..110]
FMC.CLK_FILTER_B
FMC.CLK_FILTER_A
FMC.GPS_CLK_EN*
FMC.GPS_IRIGB
FMC.GPS_PPS_P
FMC.GPS_PPS_N
FMC.GPS_SYNC_OUT_P
FMC.GPS_SYNC_OUT_N
VCC3V3
VCC3V3_LFILT
120 Ohm@100MHz
C7
10UF
10V
L1
C8
0.1UF
25V
C9
10UF
10V
C10
10UF
10V
C11
0.1UF
25V
C12
10UF
10V
L2
VCC5V
VCC5V_LFILT
Translator Power Filtering
GPS BNC Connectors
Use RA BNC Conn. TE 1-1634612-0
---------- Level Translators ----------
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104
Design Title: GPS Interface Board
Schematic Title: 01. GPS Interface
Page Title: 03. GPS Interface
Size B
Date: Friday, September 22, 2023
Document Number: <Doc>
Rev <RevCode>
Designer: Jon Sensenig
Sheet: 3 of 23

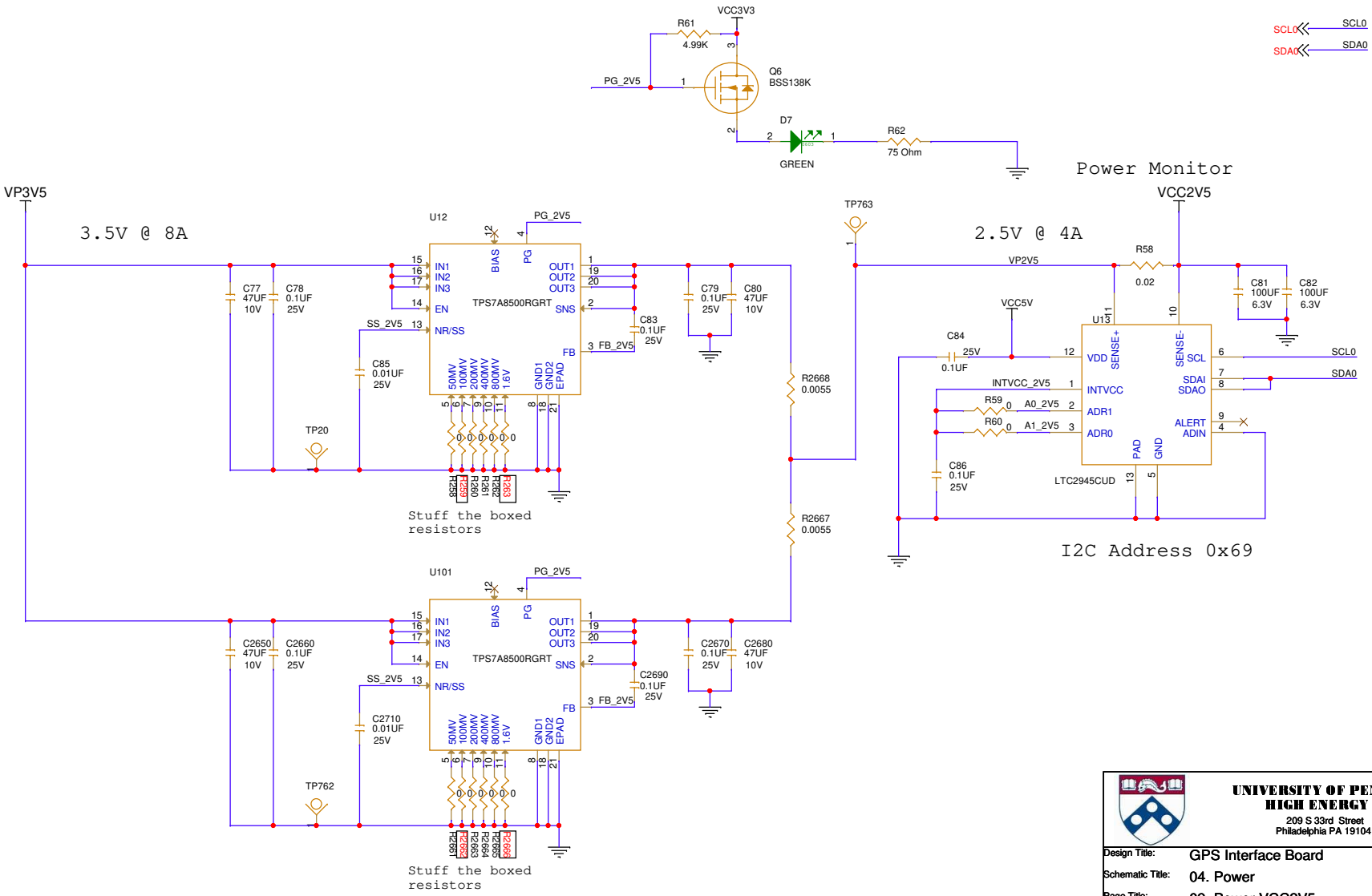

Clock Generator (312.5 MHz)
Clock Gen. Power Filtering
1.8V LED
Clock Gen. 1.8V Power Supply
Set IO_VDD_SEL bit to VDDA!
I2C Address = 0x68
LOL LEDs
NetGroup
SiT5021AI-2DE-25E-50_000000
SI5395A-A-GM
TPS74618PQWDRBRQ1
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104
Design Title: GPS Interface Board
Schematic Title: 02. Clock Generation
Page Title: 04. Clock Generation
Size: B
Date: Friday, September 22, 2023
Document Number: <Doc>
Rev: <RevCode>
Designer: Jon Sensenig
Sheet: 4 of 23

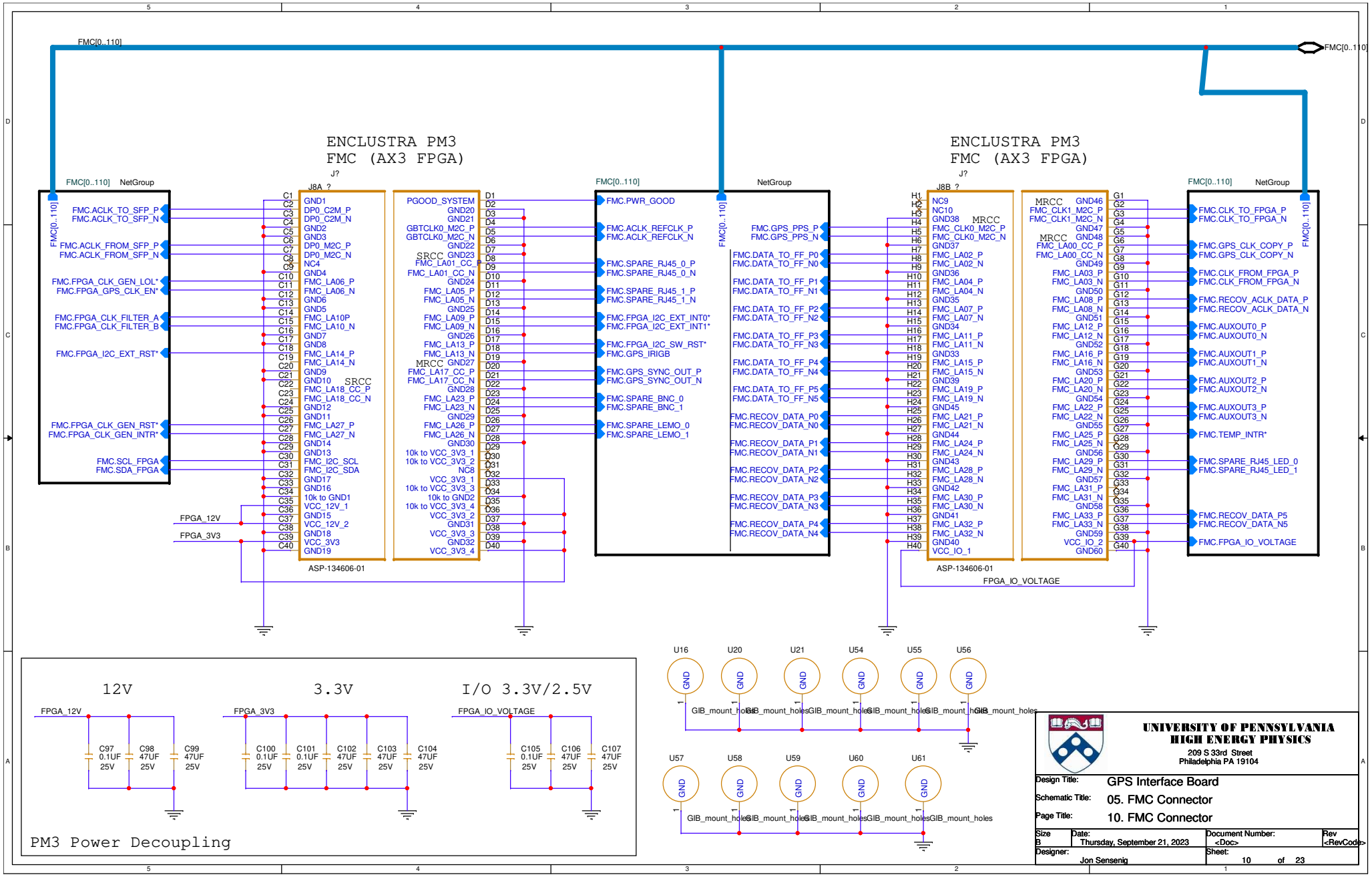

SFP SIGNALS IN
Fanout
SFP Block
Fan-In and Monitor
FMC[0..110]
CLK_TO_SFP[0..11]
SFP 1
SFP 2
SFP 3
SFP 4
SFP 5
SFP 6
SFP1
SFP2
SFP3
SFP4
SFP5
SFP6
SFP Fanout
SFP Fan-in
SFP MODULES
SFP SIGNALS OUT
ACLK SFP
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104
Design Title: GPS Interface Board
Schematic Title: 03. SFP Interface
Page Title: 05. SFP Interface
Size B
Date: Friday, September 22, 2023
Document Number: <Doc>
Rev <RevCode>
Designer: Jon Sensenig
Sheet: 5 of 23

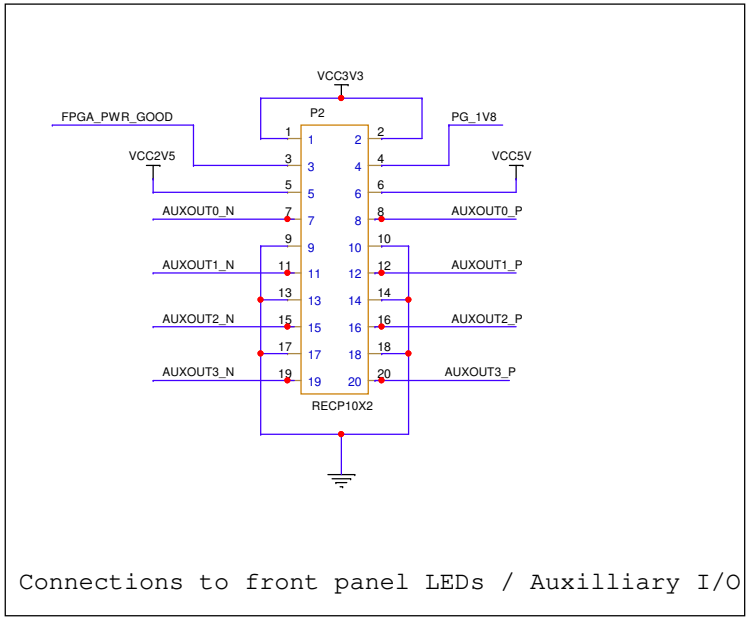

4A Fuse
TP14
12V_IN
F1
4A
TP10
12V_FUSE
FL1
TP9
J300
172448-0004
GND_IN
C41
1UF
25V
120 Ohm@100MHz
C42
1UF
25V
VP12V
C40
10UF
25V
C43
0.47UF
25V
C44
0.47UF
25V
C87
1UF
25V
12V Power
Conn.
F2
12V_IN
0.75A
12V_FANS
J27
J28
J29
GND1
PWR
GND2
0022232031
C3712
1UF
25V
C3713
1UF
25V
C3714
1UF
25V
C3715
1UF
25V
Fan Connectors
U100
LTM8029IYPBF
RUN
FB
VIN_1
VIN_2
RT
PGOOD
VIN_3
VIN_4
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
GND_12
GND_13
GND_14
GND_15
GND_16
GND_17
GND_18
BIAS
VOUT_1
VOUT_2
VOUT_3
VOUT_4
VOUT_5
VOUT_6
VOUT_7
VOUT_8
PGOOD_P5V5
R2650
280 kOhm
R2640
143K
TP760
VP5V5
C88
22UF
25V
PGOOD_P5V5
R2660
4.99K
VCC5V5
LT8645SJV-2
U6
VIN1
VIN2
VIN3
VIN4
VIN5
VIN6
EN/UV
CLKOUT
SYNC/MODE
INTVCC
TR/SS
RT
NC1
NC2
NC3
NC4
GNDC1
GNDC2
SW2
SW1
SW3
SW4
SW5
PG
BST
BIAS
FB
GNDC3
GNDC4
L6
3.3 uH
TP11
VP3V5
3.5V @ 8A
C49
47UF
10V
C50
47UF
10V
C2711
0.1UF
25V
PG_3V5
C51
5.0PF
FB_5V5
R41
1M
R36
390 kOhm
C17
1UF
R42
17.8k
RT_5V5
See Datasheet
for Layout
VCC3V3
R40
4.99K
Q3
BSS138K
D4
GREEN
R44
75 Ohm
FMC[0..110]
FMC.SCL0
FMC.SDA0
SCL0
SDA0
NetGroup
TP12
TP13
TP75
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104
Design Title: GPS Interface Board
Schematic Title: 04. Power
Page Title: 06. Power 12V Main
Size B
Date: Thursday, September 21, 2023
Document Number: <Doc>
Rev <RevCode>
Designer: Jon Sensenig
Sheet: 6 of 23

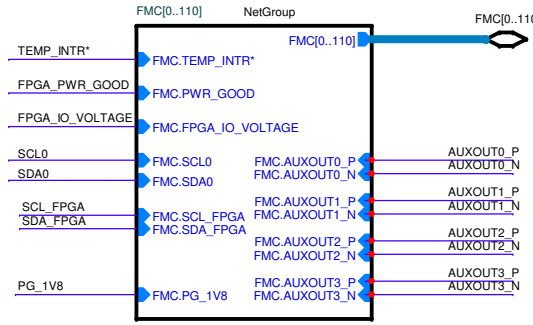

SCL0
SDA0
Power Monitor
VP5V5
5.5V @ 8A
U7
PG_5V
TPS7A8500RGRT
IN1
IN2
IN3
EN
NR/SS
BIAS
PG
OUT1
OUT2
OUT3
SNS
FB
GND1
GND2
EPAD
C52 47UF 10V
C53 0.1UF 25V
C57 0.01UF 25V
SS_5V
R2669 DNP
C56 0.1UF 25V
FB_5V
R46 12.1K
R47 2.32k
TP15
TP16
5V @ 4A
VP5V
C54 0.1UF 25V
C55 47UF 10V
VCC5V
R45
0.005
U8
LTC2945CUD
VDD
SENSE+
SENSE-
INTVCC
ADR1
ADR0
SCL
SDAI
SDAO
ALERT
ADIN
PAD
GND
C58 0.1UF 25V
C59 0.1UF 25V
INTVCC_5V
R48 0 A0_5V
R49 0 A1_5V
I2C Address 0x67
VCC3V3
R50 4.99K
Q4 BSS138K
D5
GREEN
R51 75 Ohm
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104
Design Title: GPS Interface Board
Schematic Title: 04. Power
Page Title: 07. Power VCC5V
Size B
Date: Thursday, September 21, 2023
Document Number: <Doc>
Rev <RevCode>
Designer: Jon Sensenig
Sheet: 7 of 23

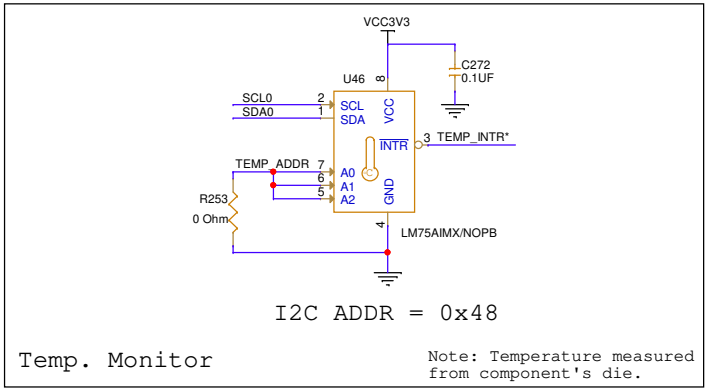

SCL0
SDA0
SCL0
SDA0
VP3V5
3.5V @ 8A
U9
PG_3V3
TPS7A8500RGRT
C61 47UF 10V
C60 0.1UF 25V
C62 0.1UF 25V
C63 47UF 10V
C64 0.1UF 25V
C65 0.01UF 25V
SS_3V3_1
FB_3V3_1
R70
R112
R113
R64
R65
Stuff the boxed resistors
TP17
R52 0.0055
R54 0.0055
3.3V @ 7A
VP3V3
U11
TPS7A8500RGRT
C70 47UF 10V
C71 0.1UF 25V
C72 0.1UF 25V
C73 47UF 10V
C75 0.1UF 25V
C76 0.01UF 25V
SS_3V3_2
FB_3V3_2
R114
R115
R116
R255
R256
R257
Stuff the boxed resistors
Power Monitor
VCC3V3
R53 0.02
C66 100UF 6.3V
C67 100UF 6.3V
TP18
C69 0.1UF 25V
VCC5V
U10
LTC2945CUD
INTVCC_3V3
R55 DNP
A0_3V3
C74 0.1UF 25V
I2C Address 0x6A
R56 4.99K
VCC3V3
PG_3V3
Q5 BSS138K
D6
GREEN
R57 75 Ohm
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104
Design Title: GPS Interface Board
Schematic Title: 04. Power
Page Title: 08. Power VCC3V3
Size B
Date: Friday, September 22, 2023
Document Number: <Doc>
Rev <RevCode>
Designer: Jon Sensenig
Sheet: 8 of 23

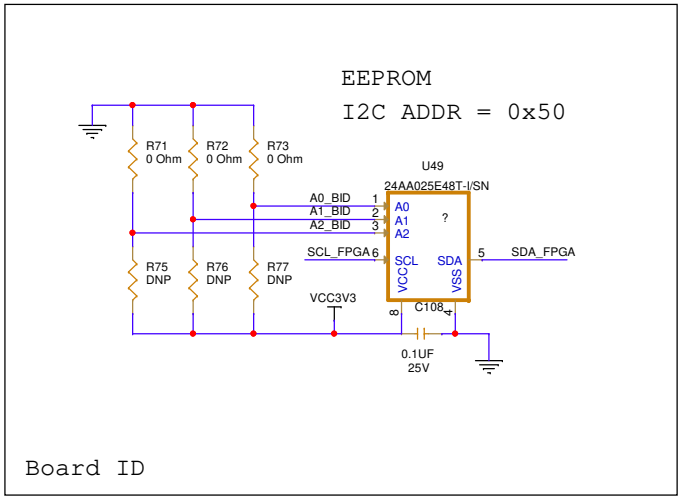

VCC3V3
R61
4.99K
PG_2V5
Q6
BSS138K
D7
GREEN
R62
75 Ohm
SCL0
SDA0
Power Monitor
VP3V5
3.5V @ 8A
U12
TPS7A8500RGRT
TP20
C77
47UF
10V
C78
0.1UF
25V
C85
0.01UF
25V
C79
0.1UF
25V
C80
47UF
10V
C83
0.1UF
25V
SS_2V5
FB_2V5
R2668
0.0055
R2667
0.0055
Stuff the boxed resistors
U101
TPS7A8500RGRT
TP762
C2650
47UF
10V
C2660
0.1UF
25V
C2710
0.01UF
25V
C2670
0.1UF
25V
C2680
47UF
10V
C2690
0.1UF
25V
Stuff the boxed resistors
TP763
VCC2V5
2.5V @ 4A
VP2V5
R58
0.02
C81
100UF
6.3V
C82
100UF
6.3V
VCC5V
C84
0.1UF
25V
U11
LTC2945CUD
INTVCC_2V5
R59
A0_2V5
R60
A1_2V5
C86
0.1UF
25V
I2C Address 0x69
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104
Design Title: GPS Interface Board
Schematic Title: 04. Power
Page Title: 09. Power VCC2V5
Size B
Date: Thursday, September 21, 2023
Document Number: <Doc>
Rev <RevCode>
Designer: Jon Sensenig
Sheet: 9 of 23

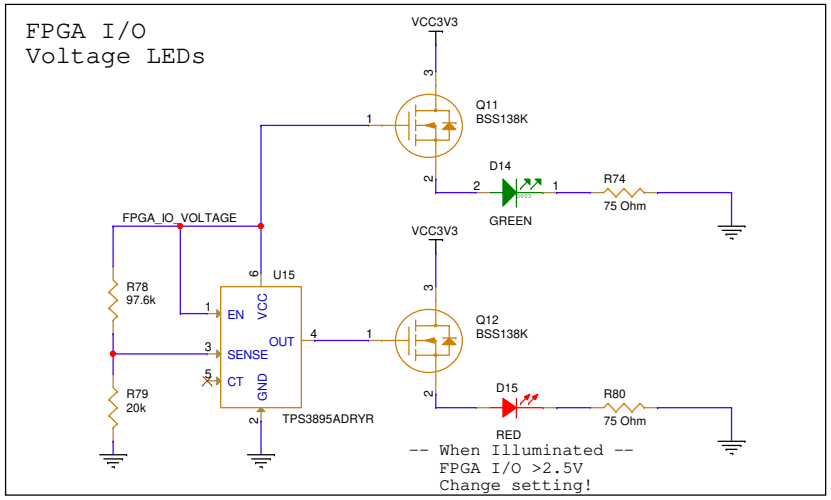

FMC[0..110]
ENCLUSTRA PM3
FMC (AX3 FPGA)
J8A ?
J8B ?
NetGroup
ASP-134606-01
FPGA_12V
FPGA_3V3
FPGA_IO_VOLTAGE
12V
3.3V
I/O 3.3V/2.5V
PM3 Power Decoupling
GIB_mount_holes
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104
Design Title: GPS Interface Board
Schematic Title: 05. FMC Connector
Page Title: 10. FMC Connector
Size B
Date: Thursday, September 21, 2023
Document Number: <Doc>
Rev <RevCode>
Designer: Jon Sensenig
Sheet: 10 of 23

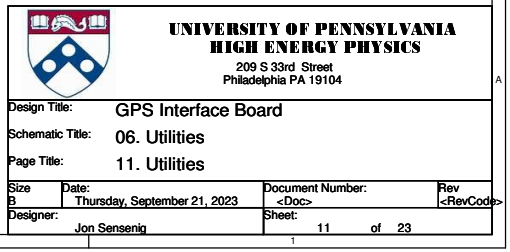

VCC3V3
P2
FPGA_PWR_GOOD
PG_1V8
VCC2V5
VCC5V
AUXOUT0_N
AUXOUT0_P
AUXOUT1_N
AUXOUT1_P
AUXOUT2_N
AUXOUT2_P
AUXOUT3_N
AUXOUT3_P
RECP10X2
Connections to front panel LEDs / Auxilliary I/O


FMC[0..110]
NetGroup
FMC[0..110]
FMC[0..110]
TEMP_INTR*
FMC.TEMP_INTR*
FPGA_PWR_GOOD
FMC.PWR_GOOD
FPGA_IO_VOLTAGE
FMC.FPGA_IO_VOLTAGE
SCL0
SDA0
FMC.SCL0
FMC.SDA0
SCL_FPGA
SDA_FPGA
FMC.SCL_FPGA
FMC.SDA_FPGA
PG_1V8
FMC.PG_1V8
FMC.AUXOUT0_P
FMC.AUXOUT0_N
FMC.AUXOUT1_P
FMC.AUXOUT1_N
FMC.AUXOUT2_P
FMC.AUXOUT2_N
FMC.AUXOUT3_P
FMC.AUXOUT3_N
AUXOUT0_P
AUXOUT0_N
AUXOUT1_P
AUXOUT1_N
AUXOUT2_P
AUXOUT2_N
AUXOUT3_P
AUXOUT3_N

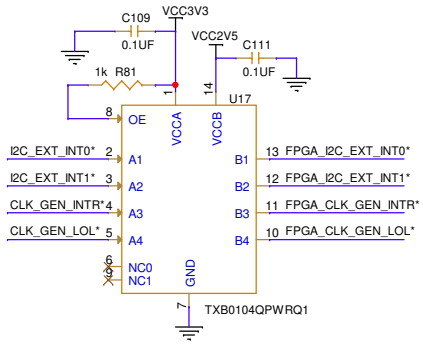

VCC3V3
C272
0.1UF
U46
SCL0
SDA0
SCL
SDA
VCC
INTR
3 TEMP_INTR*
TEMP_ADDR
A0
A1
A2
GND
R253
0 Ohm
LM75AIMX/NOPB
I2C ADDR = 0x48
Temp. Monitor
Note: Temperature measured
from component's die.


EEPROM
I2C ADDR = 0x50
R71
0 Ohm
R72
0 Ohm
R73
0 Ohm
U49
24AA025E48T-I/SN
A0_BID
A1_BID
A2_BID
A0
A1
A2
SCL_FPGA
SDA_FPGA
SCL
SDA
VCC
VSS
R75
DNP
R76
DNP
R77
DNP
VCC3V3
C108
0.1UF
25V
Board ID

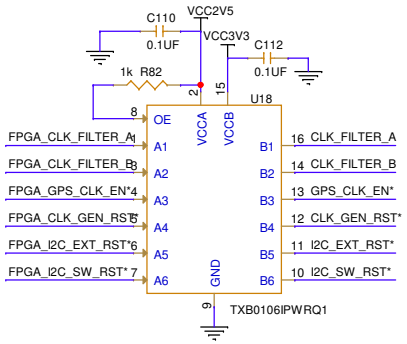

FPGA I/O
Voltage LEDs
VCC3V3
Q11
BSS138K
D14
GREEN
R74
75 Ohm
FPGA_IO_VOLTAGE
VCC3V3
U15
R78
97.6k
EN
VCC
OUT
SENSE
CT
GND
R79
20k
TPS3895ADRYR
Q12
BSS138K
D15
RED
R80
75 Ohm
-- When Illuminated --
FPGA I/O >2.5V
Change setting!


UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104
Design Title: GPS Interface Board
Schematic Title: 06. Utilities
Page Title: 11. Utilities
Size B
Date: Thursday, September 21, 2023
Document Number: <Doc>
Rev <RevCode>
Designer: Jon Sensenig
Sheet: 11 of 23

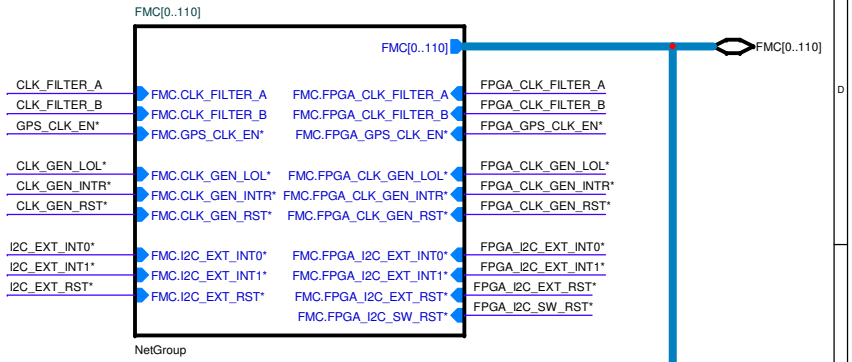
Level Translators



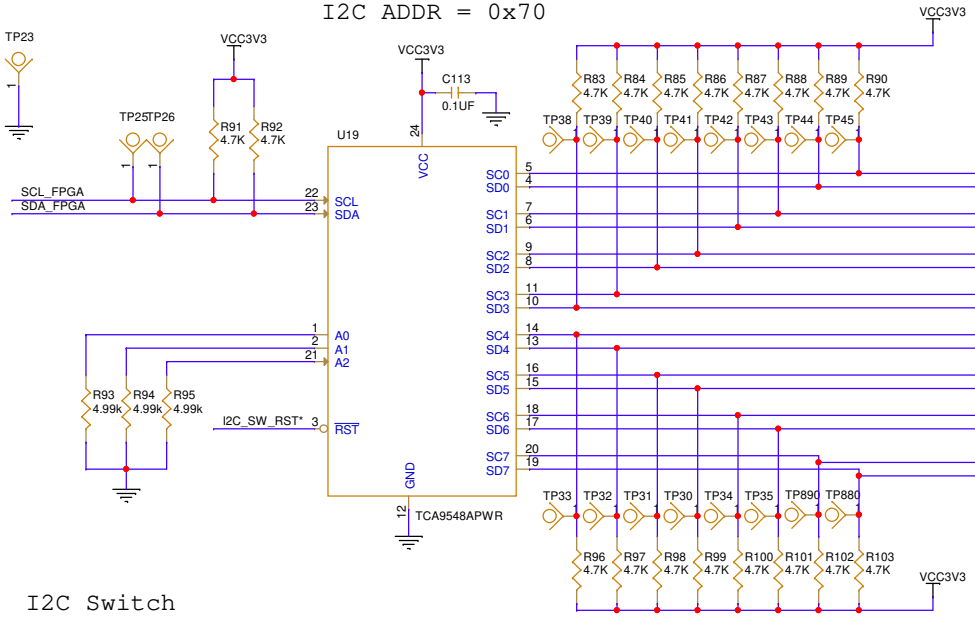
Board --> FPGA

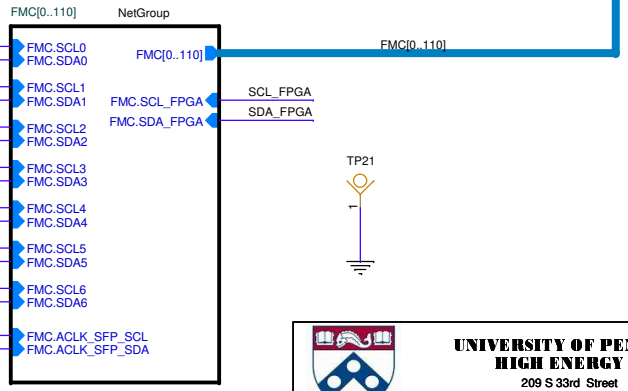


FPGA --> Board



I2C ADDR = 0x70





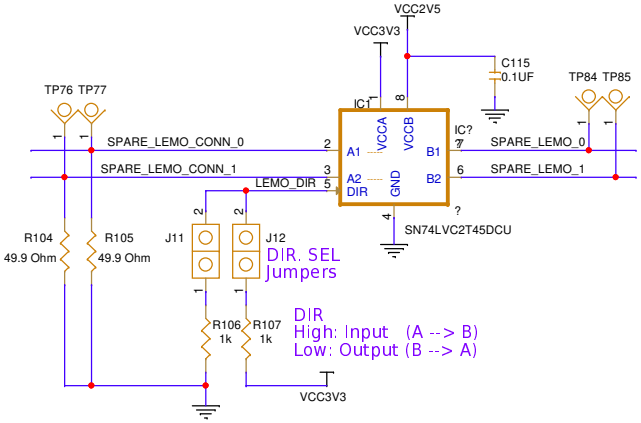
I2C Switch

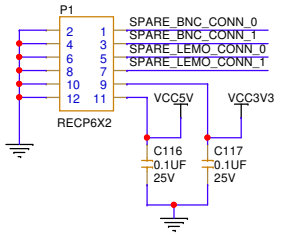
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104

Design Title:	GPS Interface Board
Schematic Title:	06. Utilities
Page Title:	12. Level Translators

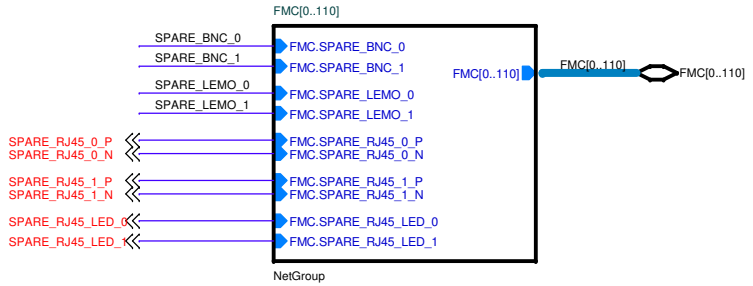
Size	Date:	Document Number:	Rev
B	Friday, September 22, 2023	<Doc>	<RevCode>
Designer: Jon Sensenig		Sheet: 12 of 23	

SPARE I/O
LEMO

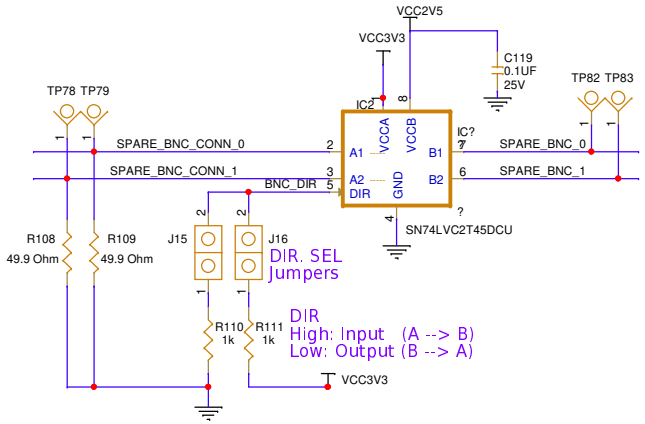


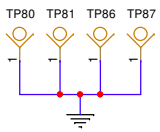


I/O Connector
to BNC & LEMO



SPARE I/O
BNC

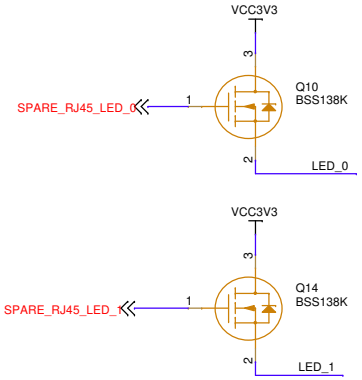


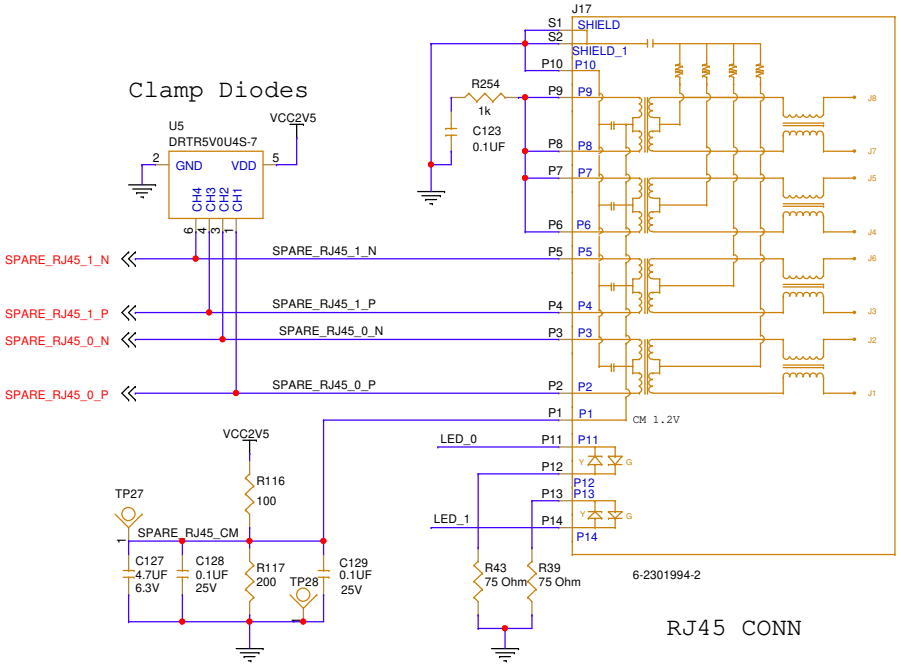


UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104

Design Title:	GPS Interface Board
Schematic Title:	06. Utilities
Page Title:	13. Spare I/O BNC/LEMO

Size: B	Date: Thursday, September 21, 2023	Document Number: <Doc>	Rev: <RevCode>
Designer: Jon Sensenig		Sheet: 13 of 23	

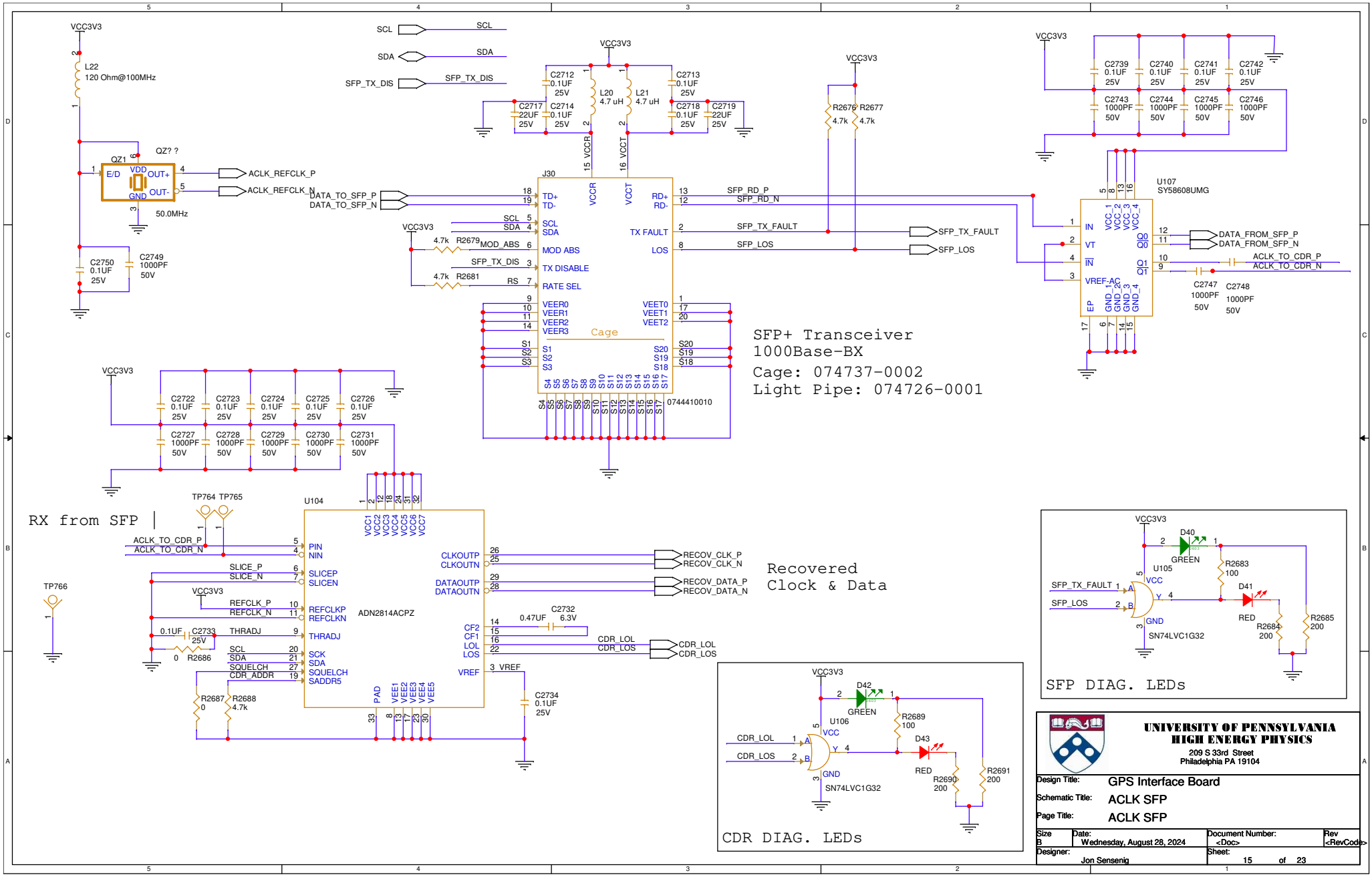


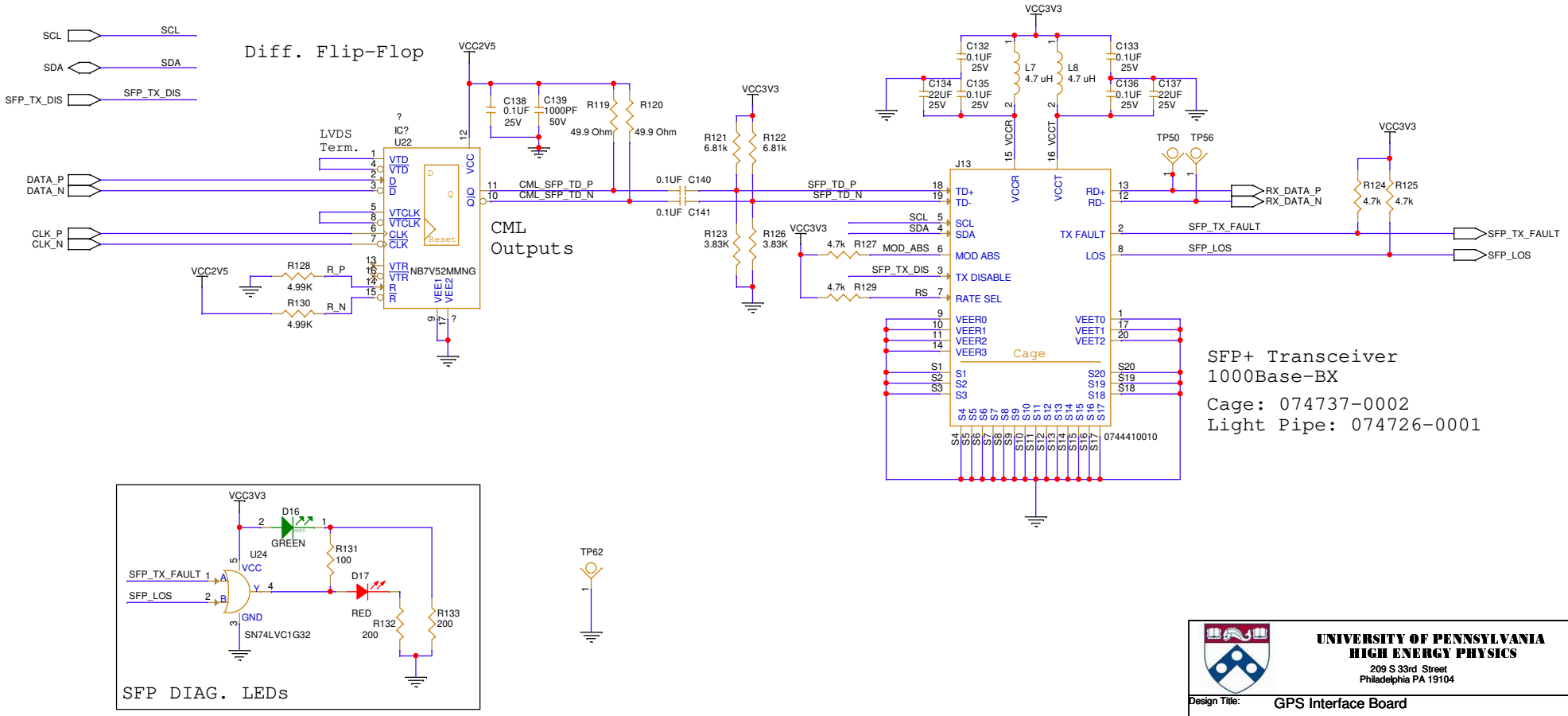


UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104

Design Title:	GPS Interface Board
Schematic Title:	06. Utilities
Page Title:	14. Spare I/O RJ45

Size	Date:	Document Number:	Rev
B	Thursday, September 21, 2023	<Doc>	<RevCode>
Designer: Jon Sensenig		Sheet: 14 of 23	

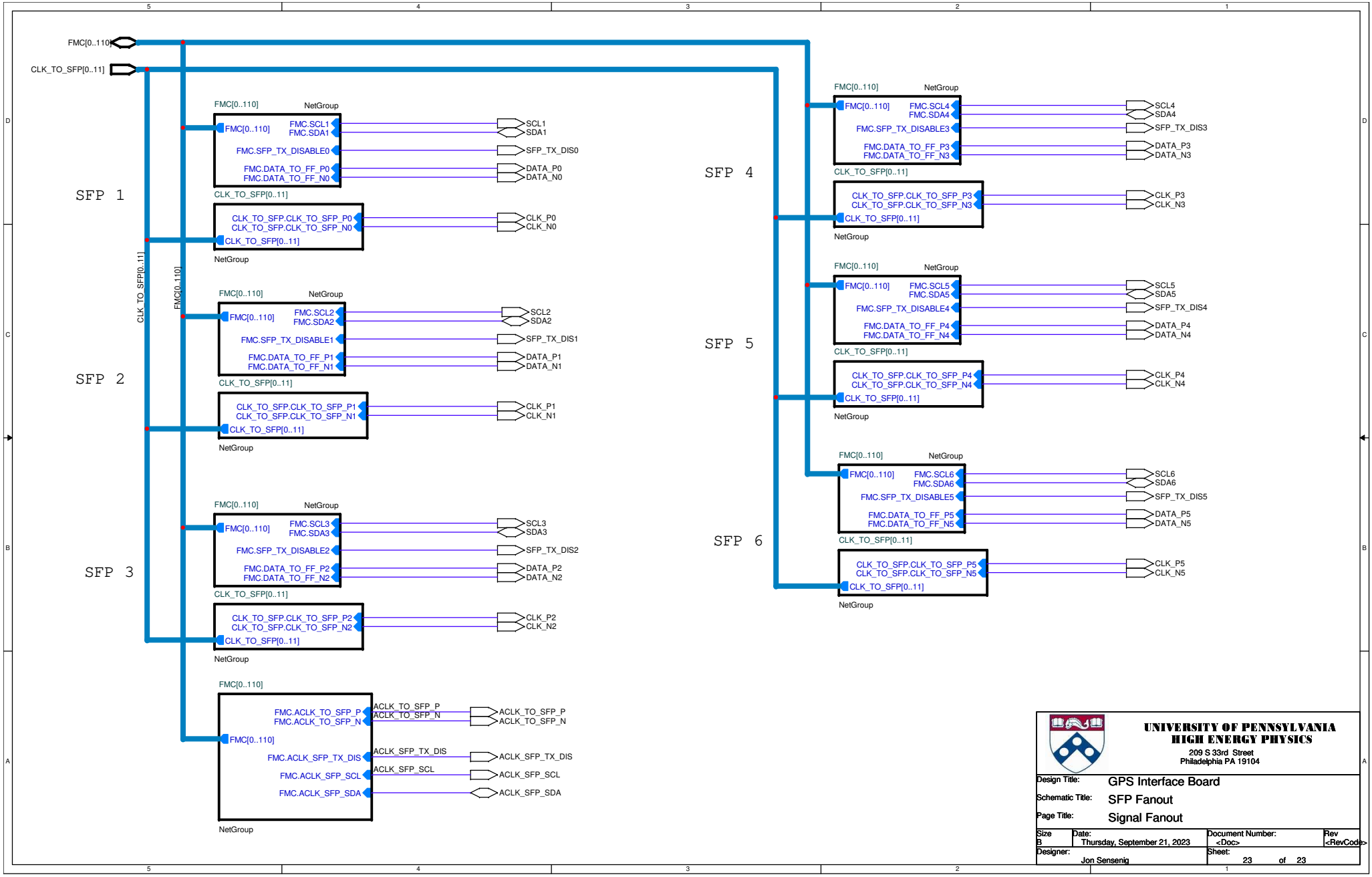

SFP+ Transceiver
1000Base-BX
Cage: 074737-0002
Light Pipe: 074726-0001
RX from SFP
Recovered
Clock & Data
SFP DIAG. LEDs
CDR DIAG. LEDs
UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104
Design Title: GPS Interface Board
Schematic Title: ACLK SFP
Page Title: ACLK SFP
Size B
Date: Wednesday, August 28, 2024
Document Number: <Doc>
Rev <RevCode>
Designer: Jon Sensenig
Sheet: 15 of 23



UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104

Design Title:	GPS Interface Board
Schematic Title:	SFP Block
Page Title:	SFP

Size	Date:	Document Number:	Rev
B	Friday, September 22, 2023	<Doc>	<RevCode>
Designer: Jon Sensenig		Sheet: 16 of 23	



UNIVERSITY OF PENNSYLVANIA
HIGH ENERGY PHYSICS
209 S 33rd Street
Philadelphia PA 19104

Design Title:	GPS Interface Board
Schematic Title:	SFP Fanout
Page Title:	Signal Fanout

Size: B	Date: Thursday, September 21, 2023	Document Number: <Doc>	Rev: <RevCode>
Designer: Jon Sensenig		Sheet: 23 of 23	