Generate 1V8 from SP header's 3V3 input using an LDO U1 LM1117-1.8 +178 GNDREF QSPI Mux: NC=SP connection (IN1 + IN2 Low) NO=SP3 connection (IN1 + IN2 High) +3.3V U2 ADG3308BRUZ SP Connection SP_FLASH_RESET_L_1V8 Matches gimletlet QSPI Header. XTRA7 is FLASH_RESET_L XTRA10 is SP_FLASH_MUX_SELECT SP_FLASH_DQ3_1V8 SP_FLASH_DQ2_1V8 SP_QSPI_CLK 19 SPI_FLASH_DQ3 SPI_FLASH_DQ2 D4 DQ3/HOLD COM1 C4 W/DQ2 D2 DQ1 SP_FLASH_DQ1_1V8 SPI_FLASH_DQ1 SP_QSPI_IO0 16 74 SP_QSPI_IO1 15 75 SP_QSPI_IO2 14 76 SP_QSPI_IO3 13 77 SP_FLASH_DQ0_1V8 SP_FLASH_CS_L_1V8 SPI_FLASH_D0 SP_FLASH_CLK_1V8 SPI_FLASH_CLK (SP_FLASH_RESET_L) EN 20 SPI_MUX_EN_L SP3_QSPI_I03 SP3_QSPI_I02 SP3_QSPI_I01 SP_TRANS_EN 10 EN GND 11 IN1 14 FLASH_MUX_SELECT SP3_QSPI_I00 SP3_QSPI_CS MT25QU256ABA8E12 SP3_QSPI_CLK GNDREF TS3A27518EPW GNDREF GNDREF GNDREF GNDREF AMD (SP3) Connection GNDREF Dupont header for connection to an SP3 dev system. Pin-out kept consistent with the Qspi but expects 1V8 voltage levels here Decoupling for ADG330BBCPZ Decoupling for Mux and Flash MountingHole_Pad GNDREF GNDREF GNDREF Manual Override Headers Jumper required! Install between Pins 1 and 2 for SP mux control Install between Pins 2 and 3 for J5 jumper control install Jumper to force Mux to AMD (SP3) but only if J6 is Jumpered between pins 2 and 3 also. Install jumper to disable SPI_MUX outputs. Use dupont wire on pin2 for for MUX_EN_L control SP_QSPI_XTRA10 Conn 01x02 SP_QSPI_XTRA10 1 FLASH_MUX_SELECT 2 MANUAL_MUX_SELECT 3 GNDRFF SP_TRANS_EN Install jumper to disable SPI Level translator outputs. Use dupont wire on pin1 for for SP_TRANS_EN control GNDRFF Sheet: / File: spimux.sch

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