Generate 1V8 from SP header's 3V3 input using an LDO
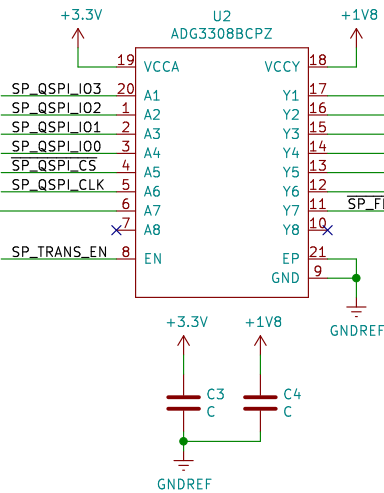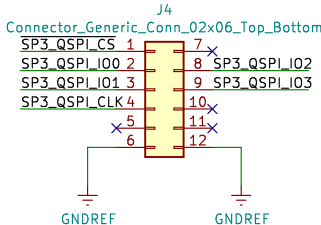
U1
LM1117-1.8
+3.3V → VI — VO → +1V8
GND

C1
10uF
C2
10uF

GNDREF
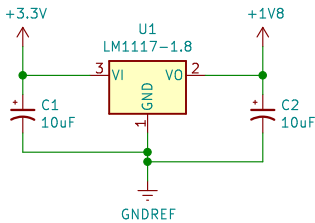
SP Connection

Matches gimlet QSPI Header.
XTRA7 is FLASH_RESET_L
XTRA10 is SP_FLASH_MUX_SELECT

J3
Connector_Generic_Conn_02x06_Top_Bottom

SP_QSPI_CS	1	7	SP_QSPI_XTRA7
SP_QSPI_IO0	2	8	SP_QSPI_IO2
SP_QSPI_IO1	3	9	SP_QSPI_IO3
SP_QSPI_CLK	4	10	SP_QSPI_XTRA10
+3.3V 5		11	+3.3V
6		12	

GNDREF   GNDREF

U2
ADG3308BCPZ

19 VCCA   VCCY 18
SP_QSPI_IO3 20 A1   Y1 17 → SP_FLASH_DQ3_1V8
SP_QSPI_IO2 1 A2   Y2 16 → SP_FLASH_DQ2_1V8
SP_QSPI_IO1 2 A3   Y3 15 → SP_FLASH_DQ1_1V8
SP_QSPI_IO0 3 A4   Y4 14 → SP_FLASH_DQ0_1V8
SP_QSPI_CS 4 A5   Y5 13 → SP_FLASH_CS_L_1V8
SP_QSPI_CLK 5 A6   Y6 12 → SP_FLASH_CLK_1V8
6 A7   Y7 11 → SP_FLASH_RESET_L_1V8
7 A8   Y8 10
SP_TRANS_EN 8 EN   EP 21
                     GND 9

+3.3V +1V8

C3 C4
C   C

GNDREF

Decoupling for ADG330BBCPZ
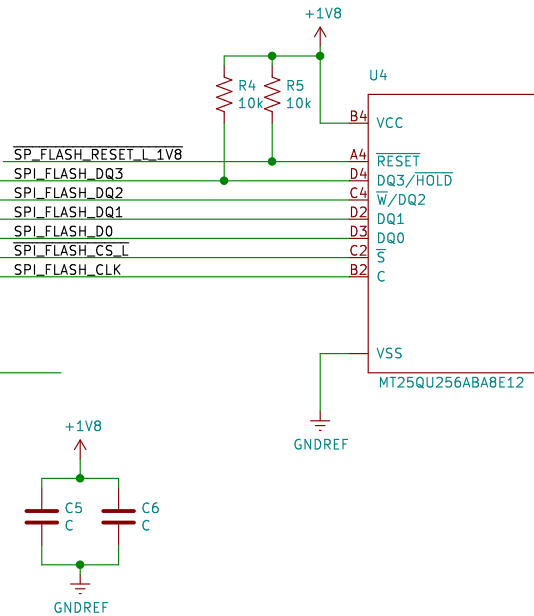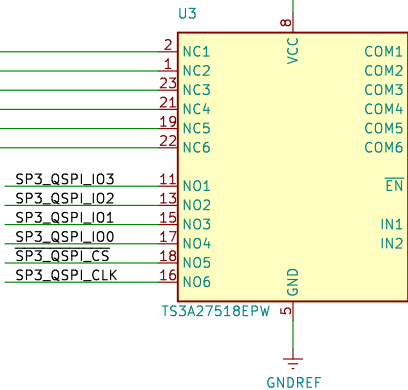
AMD (SP3) Connection

Dupont header for connection to an SP3 dev system.
Pin-out kept consistent with the Qspi but expects 1V8 voltage levels here

J4
Connector_Generic_Conn_02x06_Top_Bottom

SP3_QSPI_CS	1	7	
SP3_QSPI_IO0	2	8	SP3_QSPI_IO2
SP3_QSPI_IO1	3	9	SP3_QSPI_IO3
SP3_QSPI_CLK	4	10	
5		11	
6		12	

GNDREF   GNDREF

QSPI Mux:
NC=SP connection (IN1 + IN2 Low)
NO=SP3 connection (IN1 + IN2 High)

+1V8

U3
TS3A27518EPW

                    VCC 8
2 NC1   COM1 4 → SP_FLASH_RESET_L_1V8
1 NC2   COM2 6 → SPI_FLASH_DQ3
23 NC3   COM3 7 → SPI_FLASH_DQ2
21 NC4   COM4 9 → SPI_FLASH_DQ1
19 NC5   COM5 10 → SPI_FLASH_D0
22 NC6   COM6 12 → SPI_FLASH_CS_L
                        → SPI_FLASH_CLK
SP3_QSPI_IO3 11 NO1
SP3_QSPI_IO2 13 NO2   EN 20 → SPI_MUX_EN_L
SP3_QSPI_IO1 15 NO3
SP3_QSPI_IO0 17 NO4   IN1 1
SP3_QSPI_CS 18 NO5   IN2 24 → FLASH_MUX_SELECT
SP3_QSPI_CLK 16 NO6
                    GND 5

GNDREF

R4   R5
10k   10k

+1V8

U4
MT25QU256ABA8E12

B4 VCC
A4 RESET
D4 DQ3/HOLD
C4 W/DQ2
D2 DQ1
D3 DQ0
C2 CS
B2 C

VSS

GNDREF

SP_FLASH_RESET_L_1V8

+1V8

C5 C6
C   C

GNDREF

Decoupling for Mux and Flash

Manual Override headers

+1V8

J1
Conn_01x02
1
2

SPI_MUX_EN_L

R1
10k

GNDREF

Install jumper to disable SPI_MUX outputs.
Use dupont wire on pin2 for for MUX_EN_L control

+1V8

J2
Conn_01x02
1
2

R2
10k

SP_TRANS_EN

GNDREF

Install jumper to disable SPI Level translator outputs.
Use dupont wire on pin1 for for SP_TRANS_EN control

Install Jumper to force Mux to AMD (SP3)
but only if J6 is Jumpered between pins
2 and 3 also.

+3.3V

J5
Conn_01x02
1
2

Jumper required!
Install between Pins 1 and 2 for SP mux control
Install between Pins 2 and 3 for J5 jumper control

SP_QSPI_XTRA10 1
FLASH_MUX_SELECT 2
MANUAL_MUX_SELECT 3

J6
Conn_01x03

R3
10k

GNDREF