

TC358840XBG/TC358870XBG

Functional Specification

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3. MIPI DSI, "MIPI Alliance Specification for Display Serial Interface (DSI) Version 1.1 Revision 22 Nov 2011"
4. HDMI, "High-Definition Multimedia Interface Specification Version 1.4a March 4, 2010"
5. I2C bus specification, version 2.1, January 2000, Philips Semiconductor

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1 Overview

TC358840, Ultra HD to CSI-2, bridge converts high resolution (higher than 4Gbps) HDMI stream to MIPI CSI-2 Tx video. It is a follow up device of TC358743. The HDMI-RX runs at 297MHz to carry up to 7.2Gbps video stream. It requires dual link MIPI CSI-2 Tx, 1Gbps/data lane, to transmit out a maximum 7.2Gbps video data.

The bridge chip is necessary for current and next generation Application Processors which have been designed without video stream input port except CSI-2 Rx.

Alternatively, the CSI-2 Tx can be replaced by DSI Tx to drive a (dual) DSI link display directly.

TC358870 is the part number which embeds DSI Tx.

TC358840/70 system view block diagrams for CSI-2 and DSI outputs are shown in Figure 1-1 and Figure 1-2, respectively.

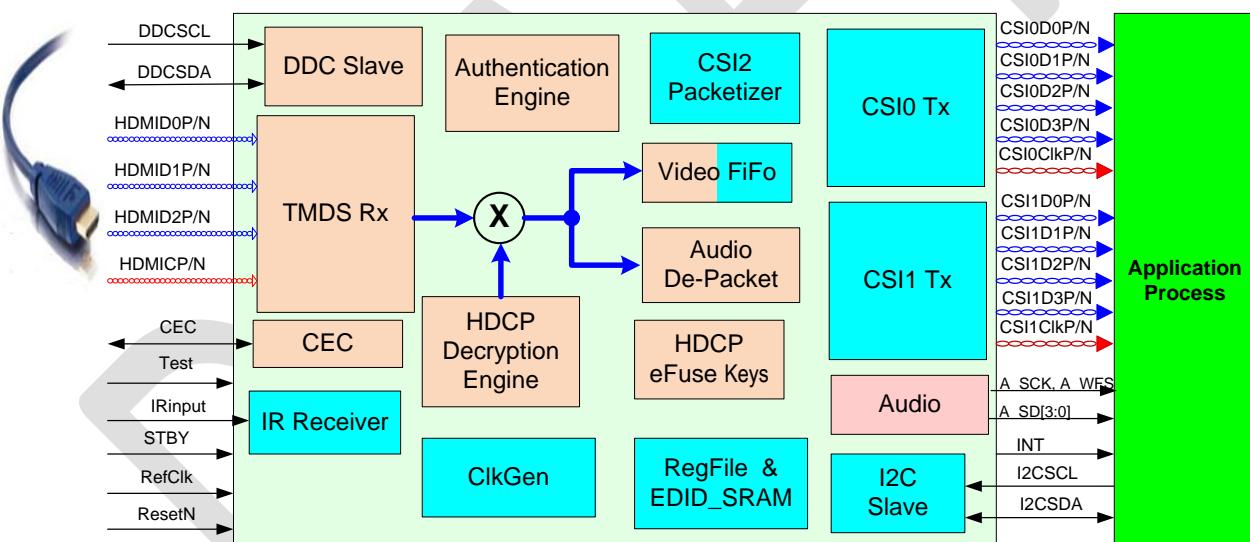


Figure 1-1 TC358840 System Overview (CSI-2 Output)

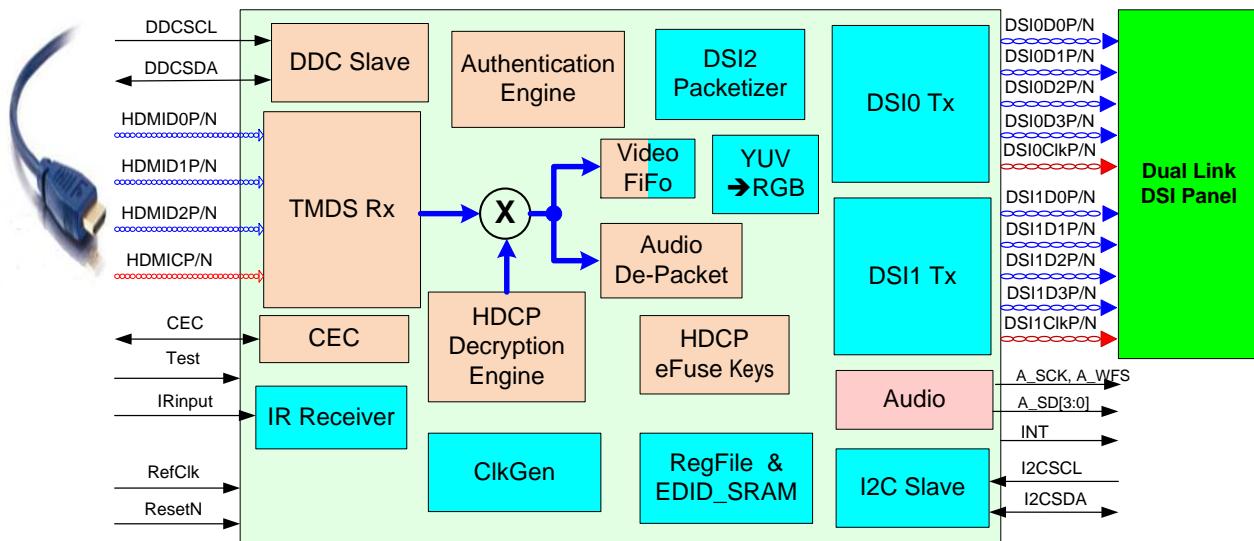


Figure 1-2 TC358870 System Overview (DSI Output)

2 Features

Below are the main features supported by TC358840/70.

HDMI-RX Interface

- ❖ HDMI 1.4b
 - Video Formats Support (Up to 4Kx2K), maximum 24 bps (bit-per-pixel) no deep color support
 - RGB, YCbCr444: 24-bpp @30fps
 - YCbCr422: 24-bpp @30fps
 - Color Conversion
 - 4:2:2 to 4:4:4 is supported
 - 4:4:4: to 4:2:2 is supported
 - RGB888 to YCbCr (4:4:4 / 4:2:2) is supported
 - YCbCr (4:4:4 / 4:2:2) to RGB888/666 is supported
 - ❖ Note: for RGB666 (R=R[5:0],2'b00, G=G[5:0],2'b00, B=G[5:0],2'b00)
 - Maximum HDMI clock speed: **297MHz**
 - Audio Supports
 - Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
 - 3D Support
 - Support HDCP1.4 decryptions
 - EDID Support, Release A, Revision 1 (Feb 9, 2000)
 - First 128 byte (EDID 1.3 structure)
 - First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
 - Embedded 1K-byte SRAM (EDID_SRAM)
 - ❖ Does not support Audio Return Path and HDMI Ethernet Channels

CSI-2 TX Interface (This function is supported only by TC358840)

- ❖ MIPI CSI-2 compliant (Version 1.01 Revision 0.04 – 2 April 2009)
- ❖ Dual links CSI-2 (CSI0 and CSI1), each link supports 4 data lanes @ 1Gbps/data lane
 - CSI0 carries the left half data of HDMI Rx video stream and CSI1 carries the right one at the default configuration.
 - Left or right data can be assigned/programmed to either CSI-2 Tx [link](#)

- The maximum length of each half is limited to 2048-pixel, CSI0 data length could be different from that of CSI1's
- The maximum Hsync skew between CSI0 and CSI1 can be less than 10 ByteClk
- ❖ Single link CSI-2, maximum horizontal pixel width
 - 2558 pixels (24-bit per pixel)
 - 3411 pixels (16-bit per pixel)
- ❖ HDMI InfoFrame data can be transmit over MIPI CSI-2 at the beginning of each frame (after FS short packet)
- ❖ Supports video data formats
 - RGB666, RGB888, YCbCr444, YCbCr 422 24-bit and YCbCr 422 16-bit
 - YCbCr inputs can be converted into RGB before outputting and vice versa.

DSI TX Interface (This function is supported only by TC358870)

- ❖ MIPI DSI compliant (Version 1.1 22 November 2011)
- ❖ Dual links DSI (DSI0 and DSI1), each link supports 4 data lanes @1Gbps/ data lane
 - DSI0 carries the left half data of HDMI Rx video stream and DSI1 carries the right one at the default configuration.
 - Left or right data can be assigned/programmed to either DSI Tx [link](#)
 - The maximum length of each half is limited to 2048-pixel plus up to 32-pixel overlap, DSI0 data length could be different from that of DSI1's
 - The maximum Hsync skew between DSI0 and DSI1 can be less than 10 ByteClk
- ❖ Single link DSI, maximum horizontal pixel width
 - 2558 pixels (24-bit per pixel)
 - 3411 pixels (16-bit per pixel)
- ❖ Supports video data formats
 - RGB666, RGB888, YCbCr444, YCbCr 422 16-bit and YCbCr 422 24-bit
 - YCbCr inputs can be converted into RGB before outputting

I2C Interface

- ❖ Support for normal (100KHz), fast mode (400 KHz) and ultrafast mode (2MHz)
- ❖ Slave Mode
 - To be used by an external Master to configure all TC358840/70 internal registers, including EDID_SRAM and panel control
 - Support 2 I2C Slave Addresses (7'h0F & 7'h1F) selected through boot-strap pin (INT)

Audio Output Interface

- ✧ Up to four I2S data lines for supporting multi-Channel audio data (5.1 and 7.1)
- ✧ Maximum audio sample frequency supported is 192KHz @8 CH
- ✧ Support 16, 18, 20 or 24-bit data (depend on HDMI input stream)
- ✧ Support Master Clock output only
- ✧ Support 32 bit-wide time-slot only
- ✧ Output Audio Over Sampling clock (256fs)
- ✧ Either I2S or TDM Audio interface available (pins are multiplexed)
- ✧ I2S Audio Interface
 - Support Left or Right-justify with MSB first
- ✧ TDM (Time Division Multiplexed) Audio Interface
 - Fixed to 8 channels (depend on HDMI input stream)
- ✧ Digital Audio Interface
 - Supports HBR audio stream split across 4 I2S lines if bandwidth higher than 12MHz

InfraRed (IR)

- ✧ Support NEC InfraRed protocol.

Power supply inputs

- ✧ Core: 1.1V
- ✧ MIPI D-PHY: 1.2V
- ✧ I/O: 1.8V, 3.3V
- ✧ HDMI: 3.3V
- ✧ APLL: 3.3V

Power Consumption during typical operations

- ✧ 1920x1080 @60fps: 372.15mW (Dual D-PHY link)
- ✧ 2560x1600 @60fps: mW (Dual D-PHY link)
- ✧ 3840x2160 @30fps: 429.27mW (Dual D-PHY link)

		VDDC11	VDDIO33	VDDIO18	VDD12_MIPI	VDD33_HDMI	VDD11_HDMI	Total Power	Unit
		1.1	3.3	1.8	1.2	3.3	1.1		
1920x1080 @60Frames	Current (mA)	34.25	18.6	1.09	25.1	62.9	64.65	372.15	mW
	Power (W)	37.675	61.38	1.962	30.12	207.57	71.115		
2560x1600 @60fps	Current (mA)	56.72	18.87	1.15	49.9	62.58	85.7	425.01	mW
	Power (mW)	62.39	62.27	2.07	59.88	206.51	94.27		
4Kx2k @30Frames	Current (mA)	66.5	18.66	1.08	51.7	62.66	88.1	429.27	mW
	Power (mW)	73.15	61.578	1.962	62.04	206.778	96.91		
Sleep 0x0002 = 0x0001	Current (uA)								uW
	Power (uW)								

Note:

- ✧ Attention about ESD. This product is weak against ESD. Please handle it carefully.
- ✧ TC358840/70 does not perform YCbCr ⇔ YUV conversion. In this document, YCbCr HDMI terminology, is used to describe color space.

3 External Pins

TC358840/70 resides in BGA80 pin packages. The following table gives the signals of TC358840/70 and their function.

Table 3-1 TC358840/70 Functional Signal List

Group	Pin Name	Ball	I/O	Init (O)	Type (Note)	Function	Voltage Supply
System: Reset & Clock (4)	RESETN	K8	I		Sch	System reset input (active low)	VDDIO18
	REFCLK	K9	I		Sch	Reference clock input (40 – 50 MHz)	VDDIO18
	TEST	G5	I		N	Internal test terminal (Always must be fixed low externally)	VDDIO18
	INT	J3	O	L	N	Interrupt Output signal (active high) *1	VDDIO18
CDSI2 TX0 (10)	CDSI0CP	F10	O	H	MIPI-PHY	MIPI-CSI0/DSI0 clock positive	VDD12_MIPI0
	CDSI0CN	F9	O	H	MIPI-PHY	MIPI-CSI0/DSI0 clock negative	VDD12_MIPI0
	CDSI0D0P	H10	O	H	MIPI-PHY	MIPI-CSI0/DSI0 data 0 positive	VDD12_MIPI0
	CDSI0D0N	H9	O	H	MIPI-PHY	MIPI-CSI0/DSI0 data 0 negative	VDD12_MIPI0
	CDSI0D1P	G10	O	H	MIPI-PHY	MIPI-CSI0/DSI0 data 1 positive	VDD12_MIPI0
	CDSI0D1N	G9	O	H	MIPI-PHY	MIPI-CSI0/DSI0 data 1 negative	VDD12_MIPI0
	CDSI0D2P	E10	O	H	MIPI-PHY	MIPI-CSI0/DSI0 data 2 positive	VDD12_MIPI0
	CDSI0D2N	E9	O	H	MIPI-PHY	MIPI-CSI0/DSI0 data 2 negative	VDD12_MIPI0
	CDSI0D3P	D10	O	H	MIPI-PHY	MIPI-CSI0/DSI0 data 3 positive	VDD12_MIPI0
	CDSI0D3N	D9	O	H	MIPI-PHY	MIPI-CSI0/DSI0 data 3 negative	VDD12_MIPI0
CDSI2 TX1 (10)	CDSI1CP	A7	O	H	MIPI-PHY	MIPI-CSI1/DSI1 clock positive	VDD12_MIPI0
	CDSI1CN	B7	O	H	MIPI-PHY	MIPI-CSI1/DSI1 clock negative	VDD12_MIPI1
	CDSI1D0P	A9	O	H	MIPI-PHY	MIPI-CSI1/DSI1 data 0 positive	VDD12_MIPI1
	CDSI1D0N	B9	O	H	MIPI-PHY	MIPI-CSI1/DSI1 data 0 negative	VDD12_MIPI1
	CDSI1D1P	A8	O	H	MIPI-PHY	MIPI-CSI1/DSI1 data 1 positive	VDD12_MIPI1
	CDSI1D1N	B8	O	H	MIPI-PHY	MIPI-CSI1/DSI1 data 1 negative	VDD12_MIPI1
	CDSI1D2P	A6	O	H	MIPI-PHY	MIPI-CSI1/DSI1 data 2 positive	VDD12_MIPI1
	CDSI1D2N	B6	O	H	MIPI-PHY	MIPI-CSI1/DSI1 data 2 negative	VDD12_MIPI1
	CDSI1D3P	A5	O	H	MIPI-PHY	MIPI-CSI1/DSI1 data 3 positive	VDD12_MIPI1
	CDSI1D3N	B5	O	H	MIPI-PHY	MIPI-CSI1/DSI1 data 3 negative	VDD12_MIPI1
HDMI-RX (9)	HDMICP	C1	I		HDMI-PHY	HDMI clock channel positive	VDD33_HDMI
	HDMICN	C2	I		HDMI-PHY	HDMI clock channel negative	VDD33_HDMI
	HDMID0P	D1	I		HDMI-PHY	HDMI data 0 channel positive	VDD33_HDMI
	HDMID0N	D2	I		HDMI-PHY	HDMI data 0 channel negative	VDD33_HDMI
	HDMID1P	E1	I		HDMI-PHY	HDMI data 1 channel positive	VDD33_HDMI
	HDMID1N	E2	I		HDMI-PHY	HDMI data 1 channel negative	VDD33_HDMI
	HDMID2P	F1	I		HDMI-PHY	HDMI data 2 channel positive	VDD33_HDMI
	HDMID2N	F2	I		HDMI-PHY	HDMI data 2 channel negative	VDD33_HDMI
	REXT	A1	I		HDMI-PHY	External reference resistor (Connect 2kohm between this terminal and VDD33HDMI)	VDD33_HDMI
DDC (2)	DDC_SCL	A3	IO		Sch/5V/OD	DDC I2C slave clock	VDDIO33
	DDC_SDA	B3	IO		Sch/5V/OD	DDC I2C slave data	VDDIO33
CEC(1)	CEC	A2	IO		Sch/5V/OD	CEC signal	VDDIO33
HPD(2)	HPDI	A4	I		5V	5V power input	VDDIO33
	HPDO	B4	O	L	N	Hot plug detect output	VDDIO33
Audio (7)	A_SCK	K7	O	L	N	I2S/TDM bit clock signal	VDDIO18
	A_WFS	K5	O	L	N	I2S word clock TDM frame sync signal	VDDIO18
	A_SD3	J5	O	L	N	I2S data signal bit3	VDDIO18

Group	Pin Name	Ball	I/O	Init (O)	Type (Note)	Function	Voltage Supply
	A_SD2	J6	O	L	N	I2S data signal bit2	VDDIO18
	A_SD1	J8	O	L	N	I2S data signal bit1	VDDIO18
	A_SD0	J9	O	L	N	I2S data signal bit0 TDM data signal	VDDIO18
	A_OSCK	J4	O	L	N	Audio Over Sampling Clock	VDDIO18
IR(1)	IR	G6	I		N	InfraRed signal (Fix low externally,if not used)	VDDIO18
I2C (2)	I2C_SCL	K4	IO		Sch/OD	I2C slave clock	VDDIO18
	I2C_SDA	K3	IO		Sch/OD	I2C slave data	VDDIO18
Audio PLL (4)	BIASDA	J1	O	L	PLL	Audio PLL BIAS signal Connect to AVSS through 0.1uF when not used	VDDIO33
	DAOUT	J2	O	L	PLL	Audio PLL Clock Reference output clock Please leave open when not used	VDDIO33
	PCKIN	K1	I		PLL	Audio PLL Reference Input clock Connect to AVSS through 0.1uF when not used	VDDIO33
	PFIL	K2	O	L	PLL	Audio PLL Low Pass Filter signal Connect to AVSS through 0.1uF when not used	VDDIO33
POWER (10)	VDDC11	C10 K6	-		Power	1.1V Internal core power supply	-
	VDDIO18	J7	-		Power	1.8V IO power supply	-
	VDDIO33	H2	-		Power	3.3V IO power supply	-
	VDD33_HDMI	B1 G1	-		Power	HDMI Phy 3.3Vpower supply	-
	VDD11_HDMI	B2 G2	-		Power	HDMI Phy 1.1V power supply	-
	VDD12_MIPI0	J10	-		Power	MIPI CSI2(DSI) 1.2V power supply for link0	-
Ground (18)	VSS	A10					
		C9					
		D4					
		D5					
		D6					
		D7					
		E4					
		E5					
		E6					
		E7					
		F4					
		F5					
		F6					
		F7					
		G4					
		G7					
		H1					
		K10					
Total 80 pins							

Note: Descriptions mean below.

- N: Normal digital I/O
Sch: Schmitt trigger input
5V: 5V tolerant input
OD: Open drain
*1: Pull-Up to select 7'h1F for I2C Slave address
Pull-Down to select 7'h0F for I2C Slave address

Please consult a technical support representative before board design to determine whether pull-up or pull-down with external resistors.

3.1 TC358840/70 80-Pin Count Summary

Table 3-2 BGA80 Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	4	-
CDSI TX0	10	-
CDSI TX1	10	-
HDMI RX	9	-
DDC	2	-
CEC	1	-
Audio	7	-
I2C	2	-
IR	1	-
HPD	2	-
Audio PLL	4	-
POWER	10	IO, Core
GROUND	18	IO, Core, Analog
TOTAL	80	Func 52 + (10+18)

3.2 Pin Layout

Top view											
	CDSI1										
A	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	VSS
	REXT	CEC	DDC_SCL	HPDI	CDSI1DP3	CDSI1DP2	CDSI1CP	CDSI1DP1	CDSI1DP0		
B	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	
	VDD33_HDN	DD11_HDM	DC_SDA	HPDO	CDSI1DN3	CDSI1DN2	CDSI1CN	CDSI1DN1	CDSI1DN0	VDD12_MIPI_1	
C	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	
	HDMICP	HDMICN							VSS		VDDC11
D	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	
	HDMIDP0	HDMIDN0		VSS	VSS	VSS	VSS		CDSI0DN3	CDSI0DP3	
E	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	
	HDMIDP1	HDMIDN1		VSS	VSS	VSS	VSS		CDSI0DN2	CDSI0DP2	
F	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	
	HDMIDP2	HDMIDN2		VSS	VSS	VSS	VSS		CDSI0CN	CDSI0CP	
G	G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	
	VDD33_HDN	DD11_HDM		VSS	TEST	IR	VPGM		CDSI0DN1	CDSI0DP1	
H	HT	Hz	H3	H4	H5	H6	H7	H8	H9	H10	
	VSS	VDDIO33							CDSI0DN0	CDSI0DP0	
J	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	
	BIASDA	DACOUT	INT	A_OSCK	A_SD3	A_SD2	VDDIO18	A_SD_1	A_SD_0	VDD12_MIPL_0	
K	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	VSS
	PCLKIN	PFIL	I2C_SDA	I2C_SCL	A_WFS	VDDC11	A_SCK	RESETN	REFCLK		
APLL											

Figure 3-1 TC358840/70 80-Pin Layout (Top View)

4 Major Functional Blocks

TC358840/70 consists of the following major blocks: HDMI-RX, CSI2-TX, DSI Tx, EDID, DDC, CEC, Audio, INT and I2C I/F.

DDC, CEC and I2C slave controller are always enabled which is required for configure the TC358840/70 chip and to wake up TC358840/70 chip.

The following sections describe each block in detail. Addition, there is a section describes Clock generation block.

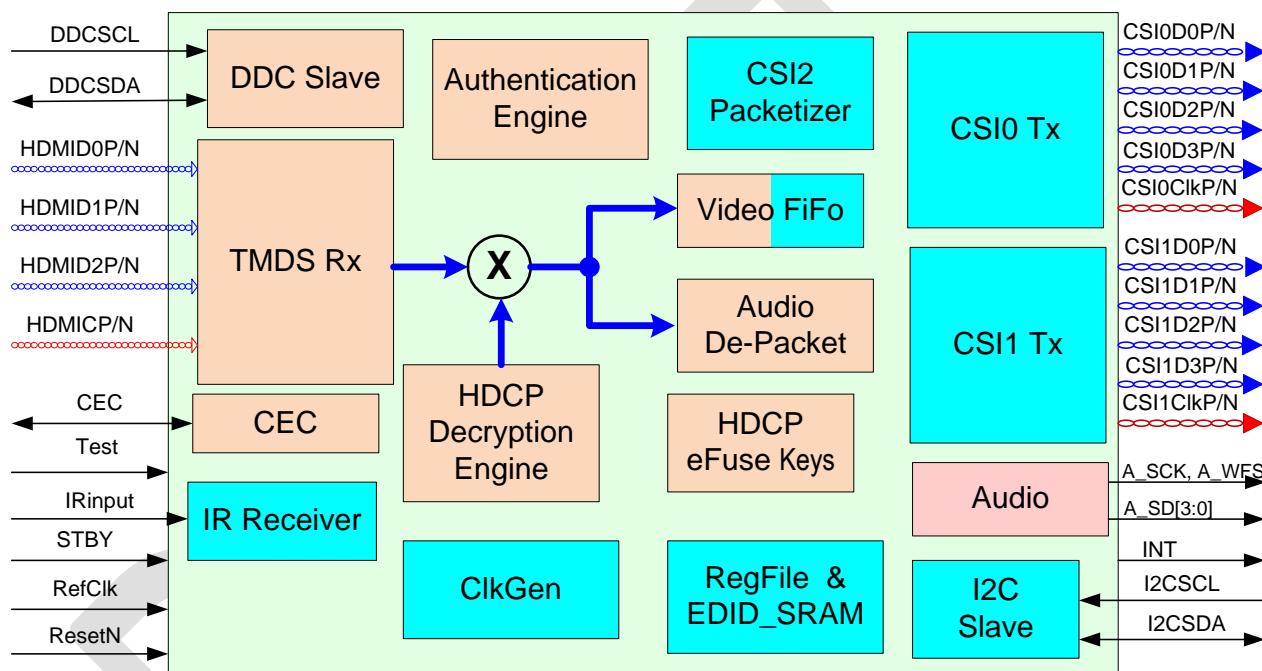


Figure 4-1 Block Diagram of TC358840/70

4.1 HDMI-RX

Primary features

- HDMI 1.4, maximum pixel clock frequency: 297MHz
- Video Format support
 - RGB, YCbCr444: 24-bpp
 - YCbCr422: 24-bpp
- Audio Support
- 3D Video Support

4.1.1 3D Support

HDMI 3D feature supports the following 3D structures.

Table 4-1 HDMI 3D Structure

3D_structureValue	Meaning
0000	Frame packing
0110	Top-and-Bottom
1000	Side-by-Side (Half)

4.1.2 InfoFrame Data Transfer

In HDMI streams, there are InfoFrame data. There are two methods at that the Application processor can get the InfoFrame data.

1. By reading TC358840/70 registers.
 - When TC358840/70 detected there are a change in the InfoFrame data, it asserts the INT so that Application processor can get the InfoFrame data by reading the registers.
2. By transmit InfoFrame data over CSI-2 protocol.
 - InfoFrame packet will be send over CSI-2 bus right after every FS packet. There are total 224 bytes of InfoFrame data.

Below is the order that InfoFrame data send over CSI-2 protocol and it also showed the register offset.

Table 4-2 InfoFrame Data Registers Summary

CSI-2 Byte#	Register Address Offset	Register name	Description
0	0x8710	AVI_0HEAD	861B AVI_info packet – Header byte 0 (= type)
1	0x8711	AVI_1HEAD	861B AVI_info packet – Header byte 1 (= version)
2	0x8712	AVI_2HEAD	861B AVI_info packet – Header byte 2 (= data length)
3	0x8713	AVI_0BYTE	861B AVI_info packet – Data byte 0 (= checksum)
19 - 4	0x8722 – 0x8714	AVI_xHEAD	861B AVI_info packet – Data byte 15 -1
31 – 20	0x872F – 0x8723	Reserved	Reserved
32	0x8730	AUD_0HEAD	861B AUD_info packet – Header byte 0 (= type)
33	0x8731	AUD_1HEAD	861B AUD_info packet – Header byte 1 (= version)
34	0x8732	AUD_2HEAD	861B AUD_info packet – Header byte 2 (= data length)
35	0x8733	AUD_0BYTE	861B AUD_info packet – Data byte 0 (= checksum)
45 - 36	0x873D – 0x8734	AUD_xBYTE	861B AUD_info packet – Data byte 10 – 1
47 - 46	0x873F – 0x873E	Reserved	Reserved
48	0x8740	MS_0HEAD	861B MS_info packet – Header byte 0 (= type)
49	0x8741	MS_1HEAD	861B MS_info packet – Header byte 1 (= version)
50	0x8742	MS_2HEAD	861B MS_info packet - Header byte 2 (= data length)
51	0x8743	MS_0BYTE	861B MS_info packet – Data byte 0 (= checksum)
61 – 52	0x874D – 0x8744	MS_xBYTE	861B MS_info packet – Data byte 10 – 1
63 – 62	0x874F – 0x874E	Reserved	Reserved
64	0x8750	SPD_0HEAD	861B SPD_info packet – Header byte 0 (= type)
65	0x8751	SPD_1HEAD	861B SPD_info packet – Header byte 1 (= version)
66	0x8752	SPD_2HEAD	861B SPD_info packet – Header byte 2 (= data length)
67	0x8753	SPD_0BYTE	861B SPD_info packet – Data byte 0 (= check sum)
94 – 68	0x876E – 0x8754	SPD_xBYTE	861B SPD_info packet – Data byte x
95	0x876F	Reserved	Reserved
96	0x8770	VS_0HEAD	861B VS_info packet – Header byte 0 (= byte)
97	0x8771	VS_1HEAD	861B VS_info packet – Header byte 1 (= version)
98	0x8772	VS_2HEAD	861B VS_info packet – Header byte 2 (= data length)
99	0x8773	VS_0BYTE	861B VS_info packet – Data byte 0 (= checksum)
126 – 100	0x878E – 0x8774	VS_xBYTE	861B VS_info packet – Data byte x
127	0x878F	Reserved	Reserved
128	0x8790	ACP_0HEAD	ACP packet – Header byte 0 (= type)
129	0x8791	ACP_1HEAD	ACP packet – Header byte 1
130	0x8792	ACP_2HEAD	ACP packet – Header byte 2
131	0x8793	ACP_0BYTE	ACP packet – Data byte 0
156 – 132	0x87AE – 0x8794	ACP_xBYTE	ACP packet – Data byte x
157	0x87AF	Reserved	Reserved
160	0x87B0	ISRC1_0HEAD	ISRC1 packet – Header byte 0
161	0x87B1	ISRC1_1HEAD	ISRC1 packet – Header byte 1

162	0x87B2	ISRC1_2HEAD	ISRC1 packet – Header byte 2
178 - 163	0x87C2 - 0x87B3	ISRC1_xBYTE	ISRC1 packet – Data byte x
191 - 179	0x87CF – 0x87C3	Reserved	Reserved
192	0x87D0	ISRC2_0HEAD	ISRC2 packet – Header byte 0
193	0x87D1	ISRC2_1HEAD	ISRC2 packet – Header byte 1
194	0x87D2	ISRC2_2HEAD	ISRC2 packet – Header byte 2
222 – 195	0x87EE – 0x87D3	ISRC2_xBYTE	ISRC2 packet – Data byte x
223	0x87EF	Reserved	Reserved

AVI: Auxiliary Video Information InfoFrame, InfoFrame_type = 0x02, HDMI Packet Type = 0x82

AUD: Audio InfoFrame, InfoFrame_type = 0x04, HDMI Packet Type = 0x84

MS: MPEG Source InfoFrame, InfoFrame_type = 0x05, HDMI Packet Type = 0x85

SPD: Source Product Description InfoFrame, InfoFrame_type = 0x03, HDMI Packet Type = 0x83

VS: Vendor Specific InfoFrame, InfoFrame_type = 0x01, HDMI Packet Type = 0x81

ACP: Audio Content Protection Packet, HDMI Packet Type = 0x4

ISRC1: International Standard Recoding Code, HDMI Packet Type = 0x5

ISRC2: International Standard Recoding Code, HDMI Packet Type = 0x6

4.1.3 Color Space Conversion

TC358840/70 provides color space conversion to transfer RGB888 data format to YCbCr444 or YCbCr422. It also provides conversions between YCbCr422 and YCbCr444. The register setting requirement for each conversion is listed below.

4.1.3.1 RGB888 to YCbCr422

0x8A00 = 8'h01

0x8A01 = 8'h14

0x8A08 = 8'h31

0x0004 [7:6] = 2'b11 (For CSITx)

4.1.3.2 RGB888 to YCbCr444

0x8A00 = 8'h01

0x8A01 = 8'h14

0x8A08 = 8'h11

0x0004 [7:6] = 2'b00 (For CSITx)

4.1.3.3 YCbCr444 to YCbCr422

0x8A00 = 8'h01

0x8A01 = 8'h14
0x8A08 = 8'h31
0x0004 [7:6] = 2'b11 (For CSI2 Tx)

4.1.3.4 YCbCr422 to YCbCr444

0x8A00 = 8'h00
0x8A01 = 8'h14
0x8A08 = 8'h11
0x0004 [7:6] = 2'b00 (For CSI2 Tx)

4.1.3.5 YCbCr444 to RGB888

0x8A00 = 8'h00
0x8A01 = 8'h14
0x8A08 = 8'h11
0x0004 [7:6] = 2'b00 (For CSI2 Tx)

4.1.3.6 YCbCr422 to RGB888

0x8A00 = 8'h00
0x8A01 = 8'h14
0x8A08 = 8'h11
0x0004 [7:6] = 2'b00 (For CSI2 Tx)

4.2 Line Split

We need dual link CSI-2/DSI Tx to transmit out HDMI Rx received 7.2Gbps (297MHz x 24bpp) video stream. The splitting of one (line of) video stream is performed by left and right halves. Left half data is sent to CSI0 link, while the right one is routed to CSI1 link.

1. Left half data can be assigned/programmed to either CSITx port
2. Left half data length could be different from that of right half one.
3. The maximum Hsync skew between CSI0 and CSI1 is less than 10 MIPI link ByteClk
4. The maximum length of each half is limited to 2048+32-pixel at 24bpp due to the 4Gbps D-PHY link speed per lane
5. The splitting for CSI-2 Tx and DSI Tx are shown graphically in Figure 4-2 and Figure 4-3, respectively.

6. Please note there is 1-line time delay between HDMI Rx and MIPI-Tx output due to the 2-line buffer implementation in CSI-2/DSI Tx block
7. For dual DSI link splitting, overlapped splitting shown in Figure 4-4 is also supported.

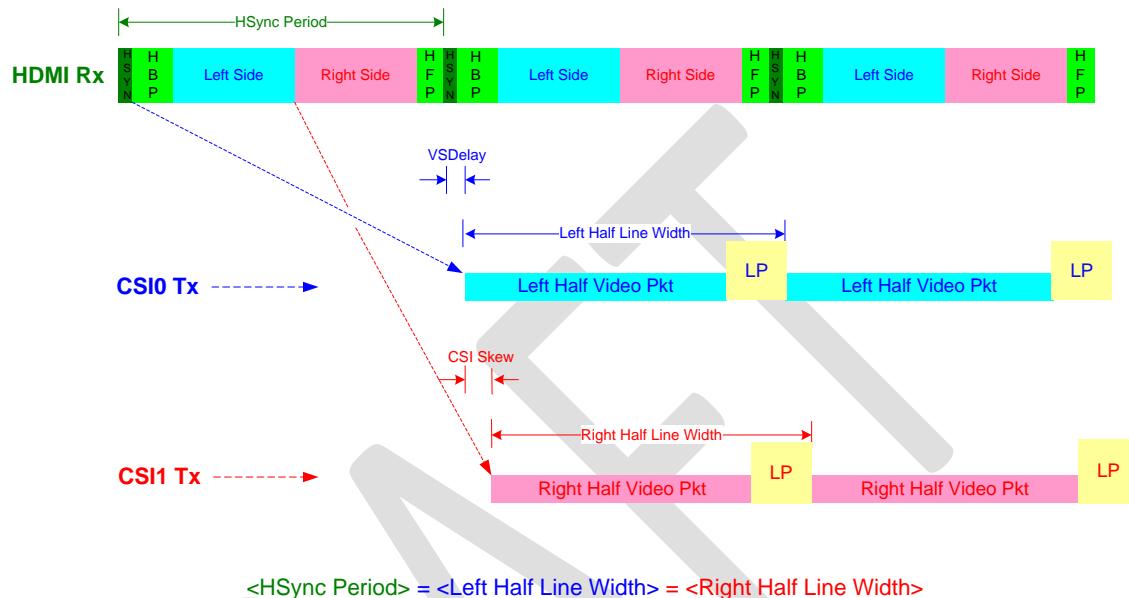


Figure 4-2 Line Splitting for Dual CSI-2 Link

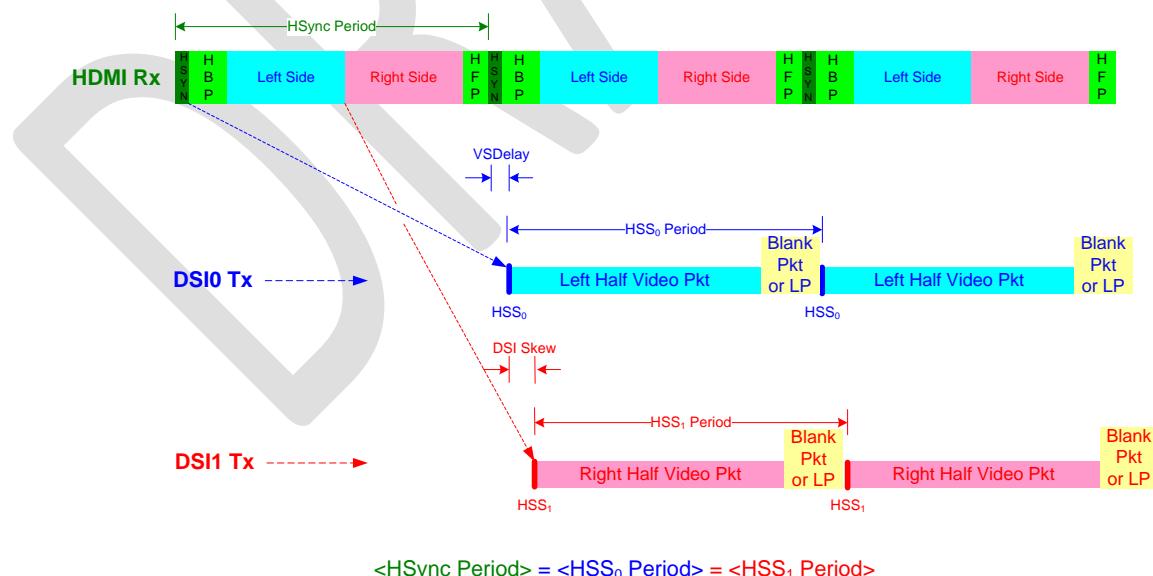


Figure 4-3 Line Splitting for Dual DSI Link

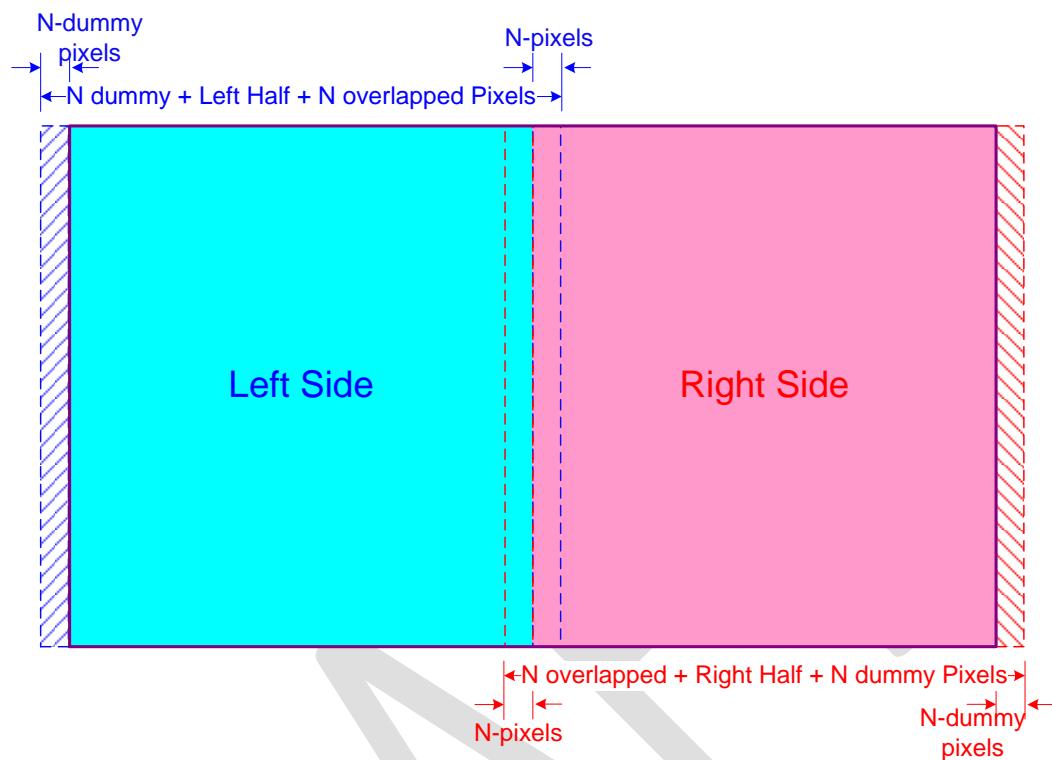


Figure 4-4 Line Overlap Splitting in Dual DSI Link

Please consult a technical support representative on a specific custom way of line splitting.

4.3 CSI-2 TX Controller (TC358840 only)

In addition to data formats specified by CSI-2 spec, TC358840 supports more data formats from HDMI input, including its data island data. Table below shows how TC358840 supports/allocates DataType for non-CSI-2 packets.

1. For interlace video, users should program their desired interlace stream DataID in register field PacketID1[VPID0] and PacketID1[VPID1] for top and bottom field, respectively.
2. For CSI-2 specified data formats, DataType follows CSI-2 standard
3. For non-CSI-2 supported YCbCr progressive data formats:
 - YCbCr444 (8-bit) uses 0x24, which is the same as that of CSI-2 RGB888.
 - YCbCr422 (12-bit) uses 0x2C, which is CSI-2 RAW12 data type.
 - The DataType for YCbCr422 (8-bit) depends on register bits set in ConfCtl[YCbCrFmt]
 - ConfCtl[YCbCrFmt] = 2'b10, uses the one in PacketID3[VPID2]. This is mainly to allow the use of User Defined data type, i.e., 0x30, 0x31, 0x32, etc.
 - ConfCtl[YCbCrFmt] = 2'b11, CSI-2 standard specified 0x1E will be used for YCbCr422 8-bit.

Table 4-3 Supported Data Types and Their Data ID fields

DataType ID Register	Description
0x00	Frame Start Code
0x01	Frame End Code
VPID0	For Interlaced frame Top field
VPID1	For Interlaced frame Bottom field
VPID2 (Register PacketID3)	- YCbCr422 12-bit data format packed as CSI-2 RAW12 data format. Data ID is 0x2C.
APID	Audio packet. Audio CSI-2 Packet ID is defined in PACKETID2 register (APID parameter)
IFPID	InfoFrame packet. CSI-2 packet ID is defined in PacketID2 register (IFPID parameter)

Note: YCbCr444 8-bit uses the same Data ID as that of RGB888, 0x24

4.3.1 CSI-2 TX Interface Block

Enable InfoFrame data to send over CSI-2 instead of Host reads Info Frame data over I2C I/F

- All InfoFrame data will send out right after FrameStart packet. Total there are 224 bytes of InfoFrame data

HDMI YCbCr444 data format (used RGB888 data format)

- Y mapped to G
- Cr mapped to R
- Cb mapped to B

HDMI YCbCr422 12-bit data format (used RAW12 data format)

- | | |
|-------------|----------------|
| - Cb0 = P1, | Cb2 = P5, |
| - Y0 = P2, | Y2 = P6, ... |
| - Cr0 = P3 | Cr2 = P7, |
| - Y1 = P4 | Y3 = P8 |

4.3.2 Frame Count

Frame count # can be embedded into Frame Start and Frame End packet (in WC field).

Frame count maximum value is defined in FCCtl register.

- When FrCnt = 0, WC field = 0
- When FrCnt = 1, WC field = 1,1,1,1,1,
- When FrCnt = 2, WC field = 1,2,1,2,1,2,.....
- When FrCnt = 3, WC field = 1,2,3,1,2,3,.....
-

Frame count is increment at every HDMI Vsync.

User is recommended to program FrCnt = 2 for interlace video streams. TC358840 counts 1 for the top field and 2 for bottom field.

4.4 DSI Tx Controller (TC358870 only)

4.4.1 DSI TX Application

TC358870 can also convert HDMI streams to DSI streams in order to display it directly on the DSI panel.

4.4.1.1 Program/Initialize DSI Panel

DSI panel might need to be programmed-initialized via DSI link.

1. TC358870 provides several **DSI_*** registers, which can be used to issue DSI command in order to program DSI panel. Please refer to section 4.4.2 for details.
2. These **DSICMD_*** registers can be written by an external micro-controller.
3. TC358870 uses DSIO to program panel.
 - a. TC358870 can also use DS11 to program panel with two LCD controllers
 - b. Simultaneously sending command to both DSI links are also supported to prevent left-right panel skew.

4.4.2 DSI TX Command Packet Operation

Below is the description of TC358870 sequence for transmitting out DSI, including DCS, Command over DSI TX. Host can use I2C interface to access TC358870 registers.

By programming the following register, TC358870 will generate/transmit DSI command packets. ECC and CRC are generated and attached automatically by the hardware.

- **DCS_CMDQ** (Register 0x0504)
 - DSI command queue

There is a 16-bit wide by 32 deep command queue FIFO for DSI command packets in the design.

When the last byte(s) of a packet is programmed, hardware will send out a packet with the content from the DSI command queue FIFO either at the beginning of vertical front porch or the beginning of vertical back porch selected by the **dcs_cm_act** register bit. Once the packet is sent out, hardware increments the **dcs_cmd_done** status bits by 1.

Host can write another packet to the **DCS_CMDQ** register as long as the command queue FIFO is not full. Command queue FIFO status can be monitored in the **DCSCMD_ST** register 0x0502. If there are multiple DSI command packets in the command queue FIFO, multiple DSI command packets will be sent out during either vertical front or back porch during video transmission.

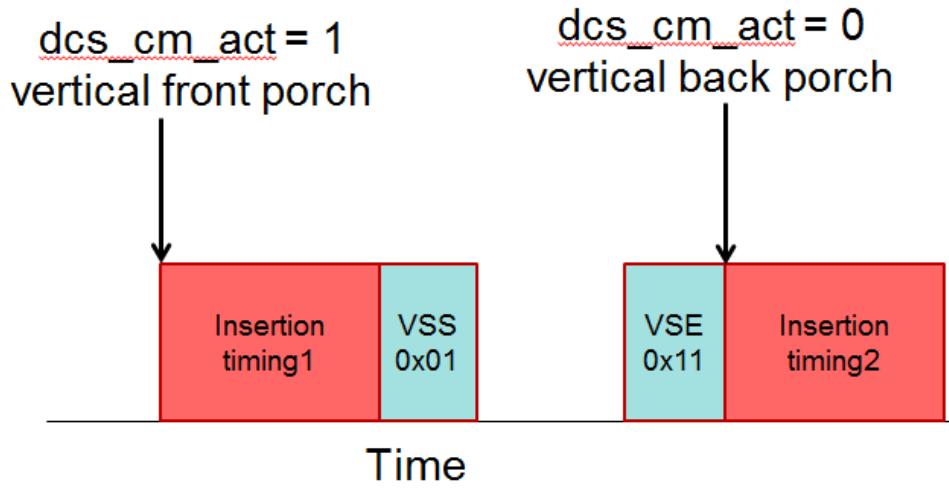


Figure 4-5 DSI Command Transmission Timing

4.4.3 TX Short Packet (DCS) Write Command

The relationship/assembly of a short DSI packet with respect to the **DCS_CMDQ** register are illustrated in Figure 4-6. The command code, either DCS command or Panel specific command, is stored in Data Byte 0 while Data Byte1 contains either command parameter or “0x00”.

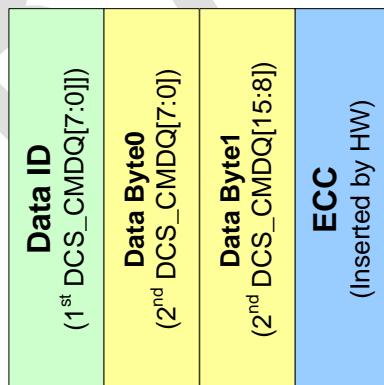


Figure 4-6 DSI Short Command Packet Assembly

The step-by-step procedure is listed below with two examples:

- 1 Choose desired DCS Short Write Command in register 1st **DCS_CMDQ[7:0]** = 0x05 or 0x15 for DCS Command without parameter or with 1 parameter, respectively.
Note that 1st **DCS_CMDQ[15]** is used to indicate if the packet is a short packet or long

packet: 0 means short packet and 1 means long packet
 1st **DCS_CMDQ[14:8]** is reserved and should be set to 0.

Write 0x00_05 to **DCS_CMDQ[15:0]** for DCS Short Write Command with 0 parameter packet – note bit 15 must be set to 0 for short packet

or

Write 0x00_15 to **DCS_CMDQ[15:0]** for DCS Short Write Command with 1 parameter packet – note bit 15 must be set to 0 for short packet

- 2 If 1st **DCS_CMDQ[7:0]** = 0x15, set DCS Command Parameter in 2nd DCS_CMDQ[15:8]. Otherwise set “0x00” in 2nd **DCS_CMDQ[15:8]**. Set 2nd **DCS_CMDQ[7:0]** to the DCS command.

Write {0x00, dcs_command[7:0]} to **DCS_CMDQ[15:0]** for DCS Command with 0 parameter or

Write {parameter[7:0], dcs_command[7:0]} to **DCS_CMDQ[15:0]** for DCS Command with 1 parameter

- 3 Check **DCSCDM_ST** register 0x0502 for command queue FIFO status:
 - dcs_cm_entry[5:0] indicates how many FIFO entries are still available for writing to.
 - dcs_cmd_done[1:0] is incremented by 1 when the DSI packet has been sent out on MIPI interface.
 Note that dcs_cmd_done[1:0] will wrap around to 0 when it is 3.
 - dcs_cmd_oflow indicates command queue FIFO has overflowed
 Write 1 to dcs_cmd_oflow to clear this bit.
 - dcs_cmd_empty indicates command queue FIFO is empty.
 - dcs_cmd_full indicates command queue FIFO is full.

Example1: TX DCS Short Command: Exit_Sleep_Mode (0x11), no parameter

0x0504 = 0x0005	(Short packet, Data ID = 0x05)
0x0504 = 0x0011	(WC1=0x00, WC0=0x11 for DSC Command)

Example2: TX DCS Short Command: Set_Pixel_Format (0x3A), 1 parameter (RGB888)

0x0504 = 0x0015	(Short packet, Data ID = 0x15)
0x0504 = 0x703A	(WC1=0x70 for RGB888, WC0=0x3A for DSC Command)

4.4.4 TX Long Packet Write Command (limited to 512-byte in length)

The relationship/assembly of a long DSI packet with respect to the **DSICMD_**** registers are illustrated in Figure 4-7. The command code, either DCS command or Panel specific command, is stored in Data Byte 0 while Data Byte1 to Data Byte 511 contains either command parameters. The maximum word count for DSI Long Command is limited to 512 bytes. For a single byte command code, the maximum parameters length can be 511 bytes.

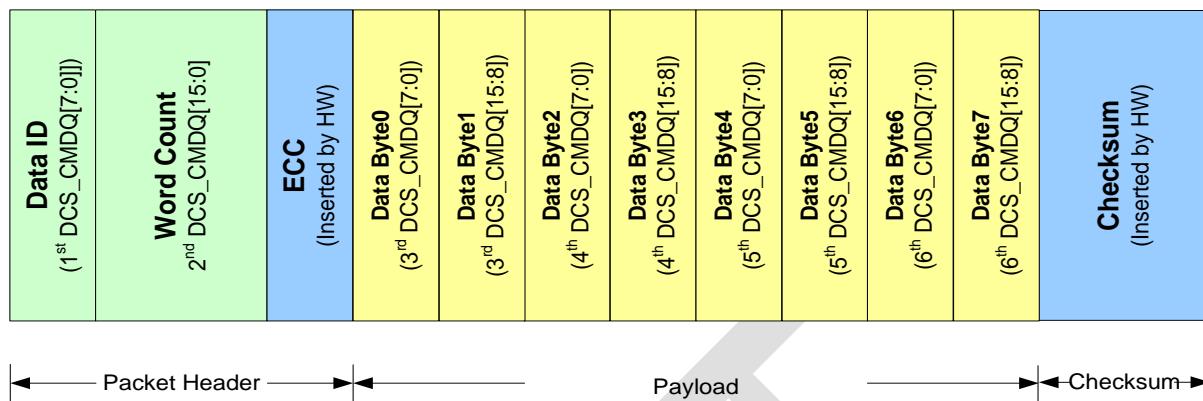


Figure 4-7 DSI Long Command Packet Assembly

The step-by-step procedure is listed below with an example:

- 1 Choose desired DSI Long Write Packet/Command, ex, 0x19 for Generic Long Write Packet, in register 1st **DCS_CMDQ[7:0]** field.
Note that 1st **DCS_CMDQ[15]** is used to indicate if the packet is a short packet or long packet: 0 means short packet and 1 means long packet
1st **DCS_CMDQ[14:8]** is reserved and should be set to 0.

For example, set register 1st **DCS_CMDQ[7:0]** to 0x040 for DSI long packet.

Write 0x8040 to **DCS_CMDQ[15:0]** for DSI long packet – note bit 15 must be set to 1 for long packet

- 2 Set 2nd **DCS_CMDQ** register to the correct word count, number of data bytes in the packet.
- 3 Check **DCSCDM_ST** register 0x0502 for command queue FIFO status:
 - dcs_cm_entry[5:0] indicates how many FIFO entries are still available for writing to.
 - dcs_cmd_done[1:0] is incremented by 1 when the DSI packet has been sent out on MIPI interface.
Note that dcs_cmd_done[1:0] will wrap around to 0 when it is 3.
 - dcs_cmd_oflow indicates command queue FIFO has overflowed
Write 1 to dcs_cmd_oflow to clear this bit.
 - dcs_cmd_empty indicates command queue FIFO is empty.
 - dcs_cmd_full indicates command queue FIFO is full.

Example: TX Generic Long Write Packet with 4 bytes of Data: 0x12, 0x34, 0x56, 0x78

0x0504 = 0x8029	(DSI Long Command/Packet, Data ID = 0x29)
0x0504 = 0x0004	(WC1,WC0)
0x0504 = 0x3412	(Data1,Data0)
0x0504 = 0x7856	(Data3,data2)

Note that for a long packet with WC of 0 please follow the procedure in 4.4.3 TX Short Packet (DCS) Write Command since there is no payload data to write. For example, to perform a DCS Long Write with WC of 0, the following sequence should be used:

0x0504 = 0x0039	(DCS Long Write, Data ID = 0x39) Note that bit 15 is 0 just like a short packet.
0x0504 = 0x0000	(WC1,WC0)

4.4.5 LPRX Packet Read Command

TC358870 provides a mechanism to receive long and short packets using interrupts and data FIFO. A 32 x 4byte FIFO is used to store long packets received during LPRX data transactions. Application may use combination of LPRX_PKT_START, LPRX_PKT_DONE and LPRX_THRESH_HIT interrupt to receive long packets of any size.

DSI_RX_STATE_INT_STAT.LPRX_THRESH_HIT interrupt is asserted when data in the DSIRX FIFO is greater than or equal to a programmable value DSI_LPRX_THRESH_COUNT (0x0C0). LPRX_PKT_DONE is asserted when the last data of the long packet is written to the RXFIFO or when a short packet is received. The diagram below shows LPRX packets may be processed by the application using the Register interface.

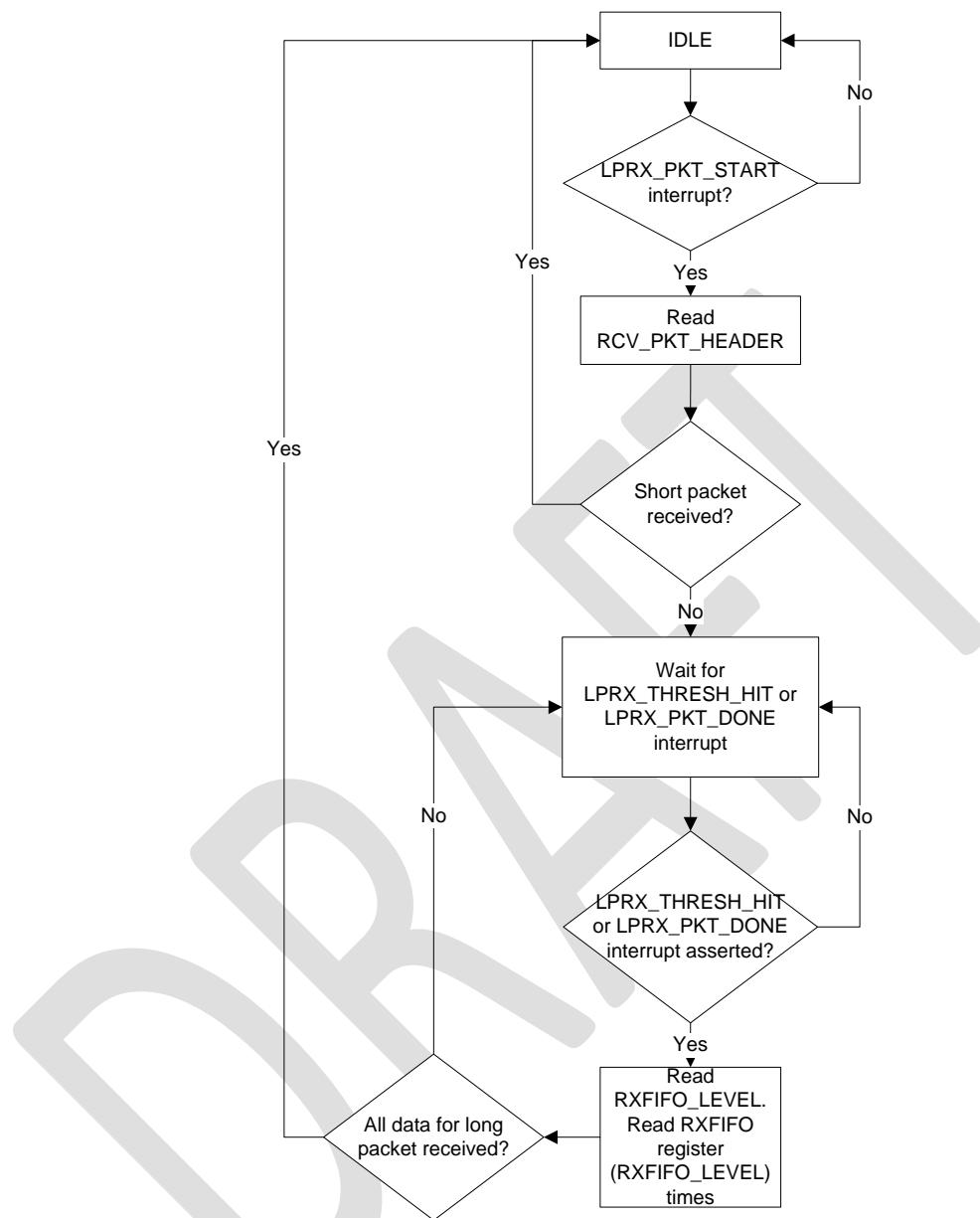


Figure 4-8 Flow diagram for LPRX data reception using Register interface

4.4.6 3D Support

For 3D video transmission on DSI, a two byte value continuing all information regarding the transport of stereoscopic content between host processor and display module is sent as part of the Vsync Start Packet. This two-byte value contains information regarding stereoscopic image

format, data order, whether or not the stereoscopic display panel is active, and the display orientation. Pls. refer to the MIPI DSI Spec. for 3D support for details on these parameters.

4.5 CEC Controller

CEC uses a single line to transfer data between TC358840/70 and a HDMI source. Messages are transferred as a single frame, which is built out of a start bit followed by data bits. The bit timing is clearly defined with different timings for the start bit and data bit period. Fixed bit timing is required, because no clock information is transferred over the CEC line.

Each transferred message starts with the transmission of a start bit, which is used to indicate the start of a message and which is also used for arbitration as several device could try to start a transfer. Once arbitration is won, the following information is transmitted in blocks (header block, opcode block and operand block). Each block consists of 8 data bits, one EOM – End Of Message indicator and an acknowledge bit period, where the acknowledge will be used by the addressed device to indicate successful transmission of each block.

TC358840/70 supports the Consumer Electronics Control Protocol as defined in HDMI specification. TC358840/70 offers the physical interface and low level support for data parsing.

4.5.1 Receive Operation Sequence

The following are the sequences for CEC Receive operation

- TC358840/70 collects CEC byte data into Receive FIFO (maximum 16 bytes)
- TC358840/70 asserts INT once it received a valid byte data in the Receive FIFO or after entire message has been received or there is an error condition on the CEC signal protocol.
- TC358840/70 will keep INT at High level until Host complete read out all the Receive data in the FIFO.

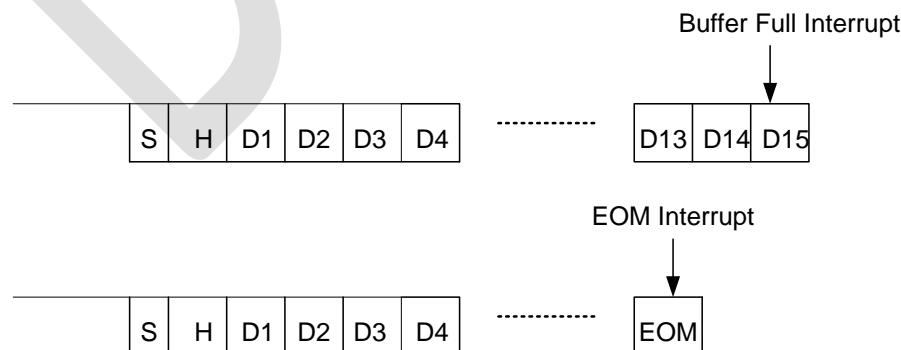


Figure 4-9 CEC reception overview

4.5.1.1 Noise cancellation time

The noise cancellation time is configurable with the CECHNC and CECLNC registers. The CEC line is monitored at each rising edge of the sampling clock. In the case that the CEC line has changed from "1" to "0", the change is fully recognized if "0"s of the same number as specified in the CECLNC bit are monitored. In the case that the CEC line has changed from "0" to "1", the change is fully recognized if "1"s of the same number as specified in the CECHNC bit are sampled.

The following figure illustrates the operation when the noise canceling is configured as CECHNC=10 (3 samplings) and CECLNC =011 (4 samplings). By canceling the noise, a signal "1" shift to "0" after "0" is sampled four times. The signal "0" shifts to "1" after "1" is sampled three times.

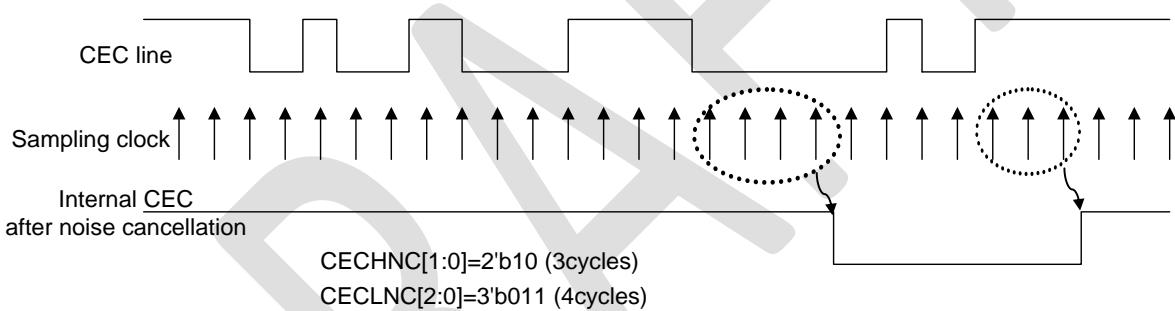


Figure 4-10 CEC noise cancellation example

4.5.1.2 Start bit detection

The following registers used to detect the start bit of CEC line.

- CECSWAV0 is used to specify the fastest start bit rising timing.
- CECSWAV1 specifies the latest start bit rising timing ((1) in the figure shown below).
- CECSWAV2 is used to specify the minimum number of cycles of a start bit (corresponds
 - to the length of a start bit measured in sampling clock cycles).
- CECSWAV3 specifies the maximum cycle of a start bit ((2) in the figure shown below).

The start bit is considered to be valid if a rising edge during the period (1) and a falling edge during the period (2) are detected.

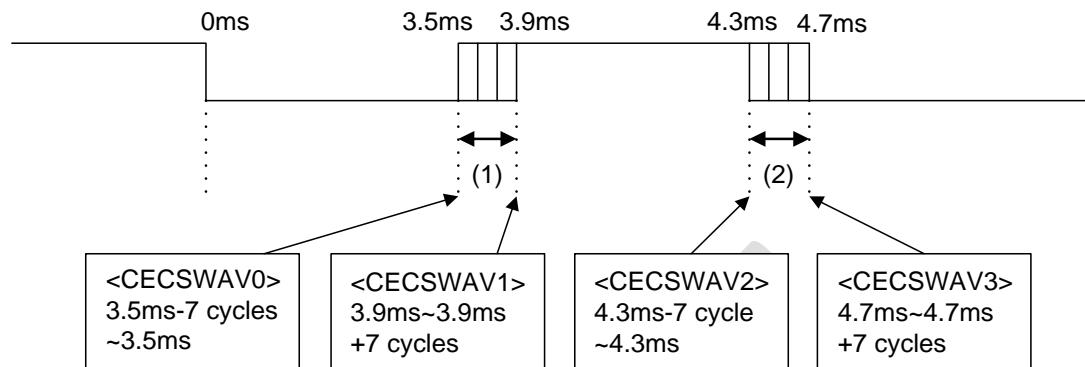


Figure 4-11 CEC start bit detection

4.5.1.3 Waveform Error Detection

The following registers CECWAV0, CECWAV1, CECWAV2 and CECWAV3 are used to detect logic transition on CEC line.

A waveform error interrupt is generated if a rising edge is detected during the period (1) or (2) shown below, or if no rising edge is detected in the timing described in (3).

- (1) period between the beginning of a bit and the fastest logical “1” rising timing
- (2) period between the latest logical “1” rising timing and the fastest logical “0” rising timing
- (3) the latest logical “0” rising time

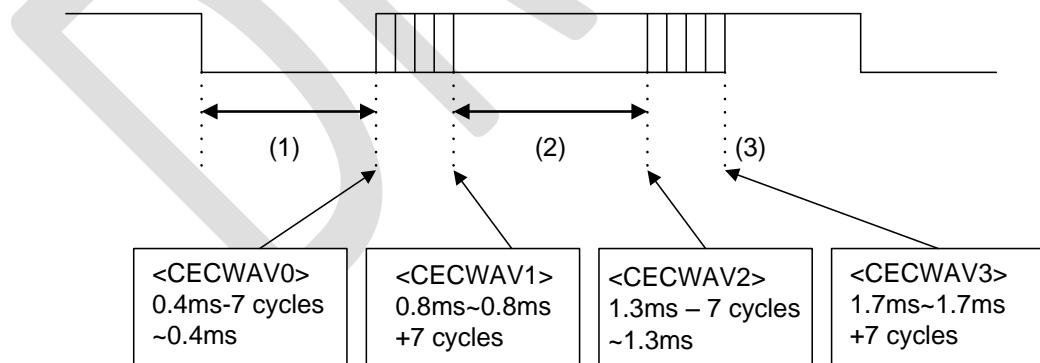


Figure 4-12 waveform error detection

4.5.1.4 Data sampling timing

The figure shown below illustrates a data sampling timing. The CECDAT register specifies the data sampling point per two sampling clock cycles within the range of + or - 6 cycles from the reference point (approx. 1.05 ms).

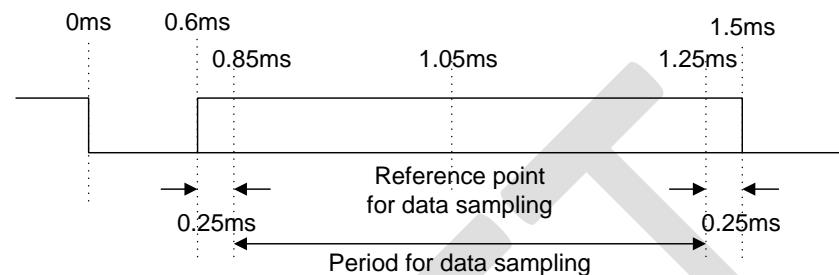


Figure 4-13 sampling time example

4.5.2 Transmit Operation Sequence

The following are the sequence for CEC transmit operation

- Write all transmit CEC byte data into Transmit FIFO (maximum 16 bytes)
- Write "1" to CEC_Conf register to start the operation
- TC358840/70 asserts INT once CEC transmit operation is completed or there is an error condition on the CEC signal protocol.
- Host must read the CEC_Status register to know the status of the transmitting operation and take appropriate action.

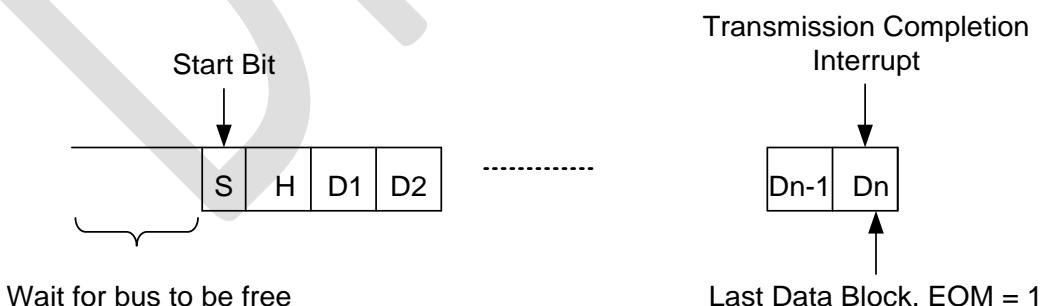


Figure 4-14 CEC transmission example

4.5.2.1 Wait Time for Bus to be Free

The wait time for a bus free check at transmission start is configured with the CECFREE register. It can be specified in a range from 1 to 16 sample clock cycles. Start point to check if a bus is free is the end of final bit. If a bus is free for specified bit cycles of “1”, transmission starts.

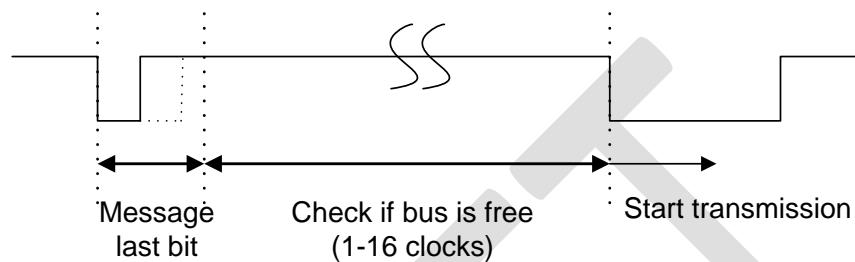


Figure 4-15 Transmission starts

4.5.2.2 Transmission Timing

The timing of the start and data bits can be adjusted with the registers as shown in the figure below

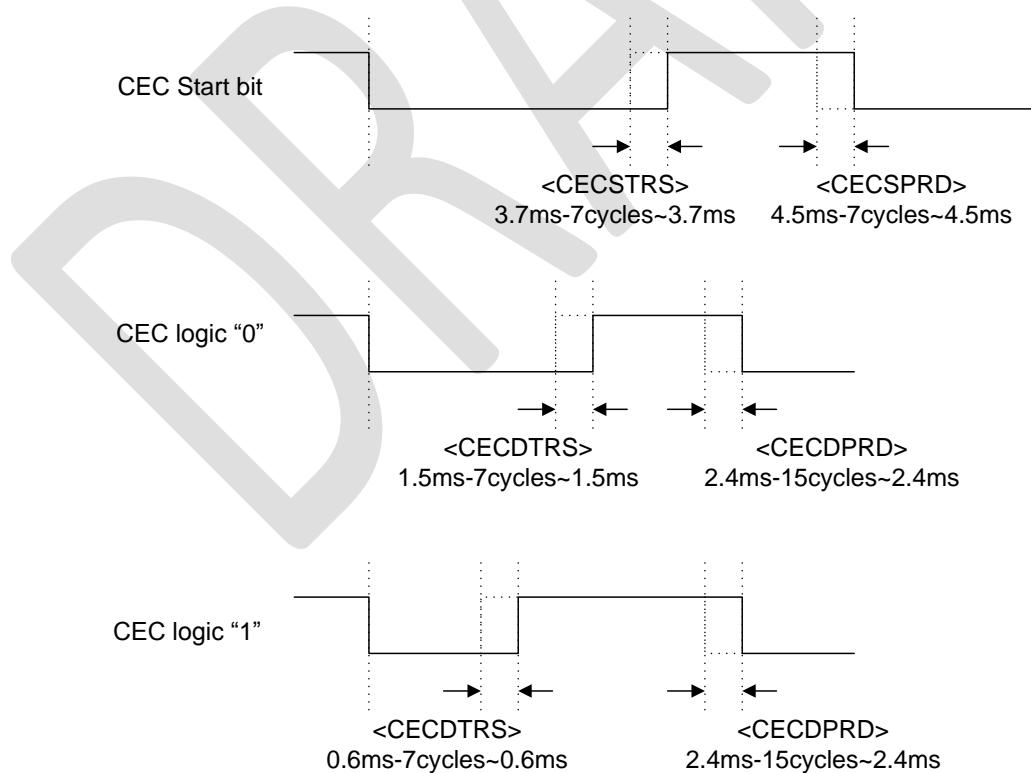


Figure 4-16 Transmission timing

4.5.3 Arbitration lost

An arbitration lost error occurs when CEC module detects “0” during the detection windows as shown in the figure below

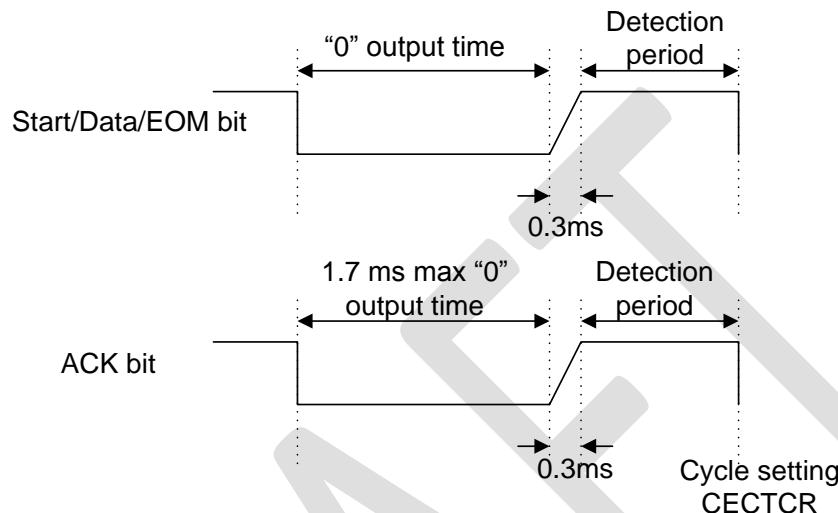


Figure 4-17 Arbitration Error check

4.5.4 Low level functions

In order to ensure transmission on the CEC line, the bridge serves the following low-level functions in accordance to the CEC standard:

- Monitoring of CEC line at all times for any incoming message except when CEC module is off (SET_CEC_ENABLE command).
- Line detection (free/occupied). This function tests the line if it is free to be used.
- Data/Frame parsing. Details of the CEC Frames (header, data blocks, EOM, ACK) will be split and stored.
- Acknowledgment of messages (positive/negative). Success or failure of message transmission will be notified to sender.
- Frame retransmission. Conditional retransmission of lost frames,
- Line error handling. Notification mechanism to inform about spurious pulses on the control signal line.
- Line Arbitration. Collision prevention mechanism.

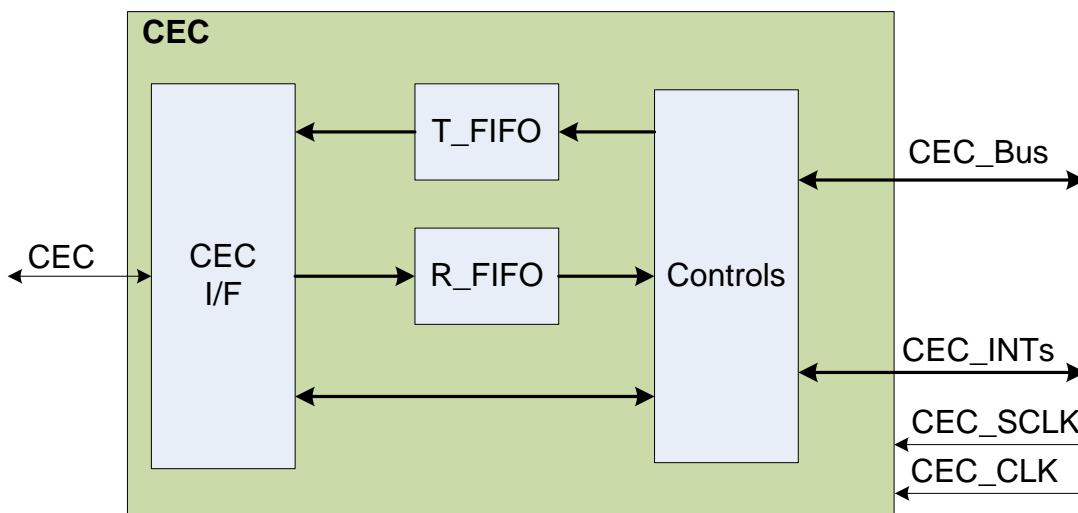


Figure 4-18 CEC Block diagram

4.6 Audio Output Function

TC358840/70 is capable of outputting audio data via I2S I/F, including TDM format, or SLIMbus I/F.

The sampling frequency ' f_s ' can be 22.05KHz, 24KHz, 32KHz, 44.1KHz, 48KHz, 88.2KHz, 96KHz, 176.4KHz, 192KHz.

TC358840/70 outputs Over-Sampling clock (A_OSCK) with frequency equal to $256f_s$ when applicable.

4.6.1 I2S Interface

The basic features of the I2S are outlined below:

- Up to 4 output lines (2 Audio channels per line = upto 8 channels)
- Support 16, 18, 20 or 24 bits data
- Support Left or Right-justify with MSB first
- Support 32 bit-wide time slot only.
- Support only Master Clock option
-

I2S bus in TC358840/70 is a 3-pin serial link consisting of a line for two time multiplexed data channels (left and right), a word select line and a clock line. Four more pins are provided for optionally providing 3 lines to send 6 additional audio channels and 1 line to provide the audio over-sampling clock. Since the transmitter and receiver have the same clock signal for data transmission, the transmitter as the master, has to generate the bit clock (SCK), and word-select (WS).

When Audio FIFO reaches certain (programmable) level, I2S controller will begin to fetch the data and transfer them over I2S interface. Once the Audio FIFO is empty, I2S controller will finish transfer the last bit of Audio data & then it will keep SCK LOW until it has more data.

Notes

- 1) The time-slot is 32 bit-wide. Input data could be 16, 18, 20 or 24 bits and could be left- or right-justify with MSB first or LSB first. There are three formats show in the below figures. Figure xx(a) illustrates Standard Data Format (Sony Format) with Left-Channel "H" and Right-channel "L", (b) Left Justified Format with Left-channel "L" and Right-channel "H". For I2S data format, there is one clock delay to latch the data bit.
- 2) I2S signals are multiplexed with TDM, & SLIMbus signals. Only one interface can be enabled at a time.

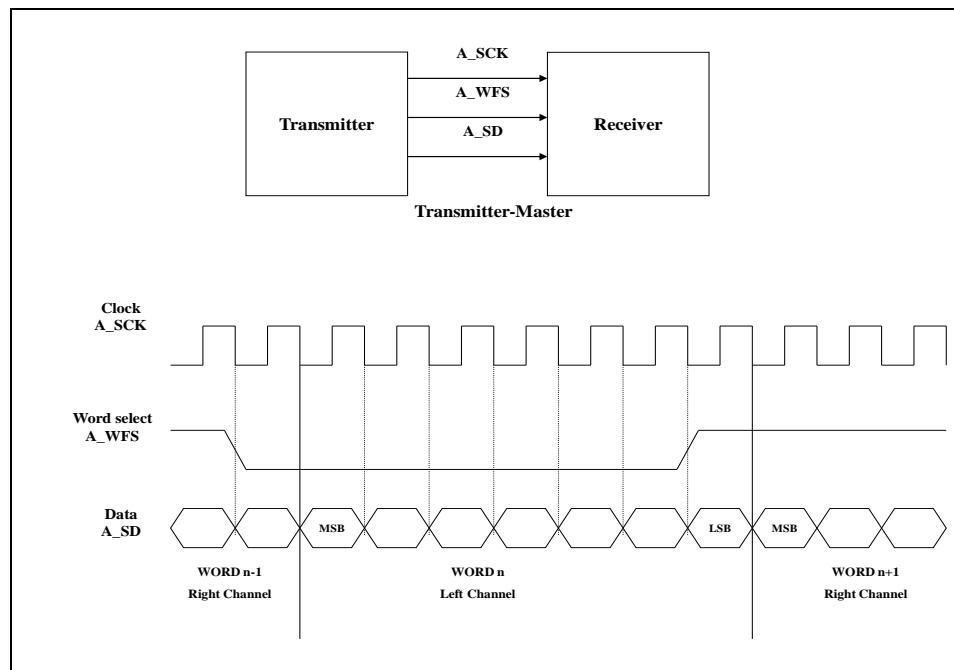


Figure 4-19 I2S Interface

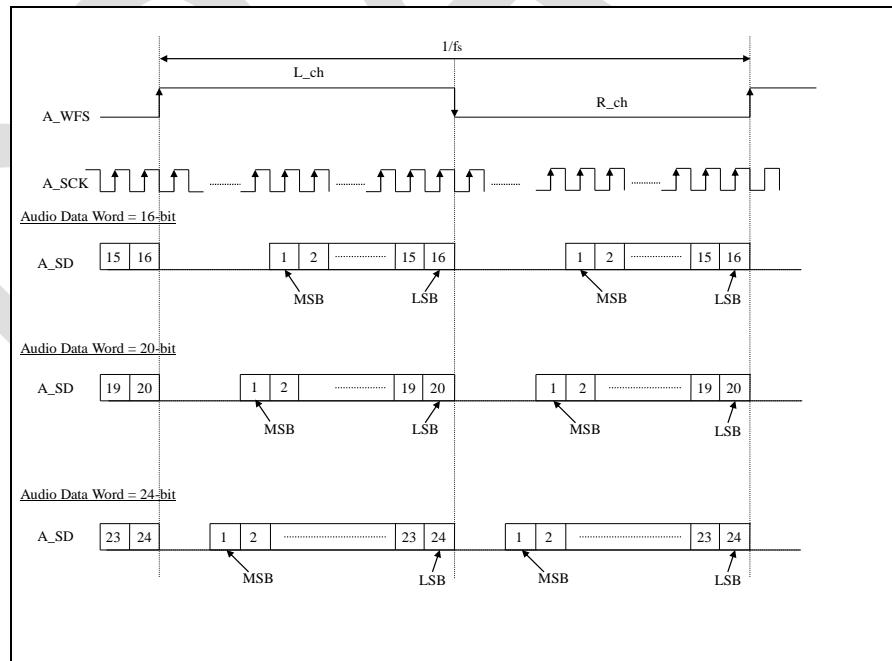
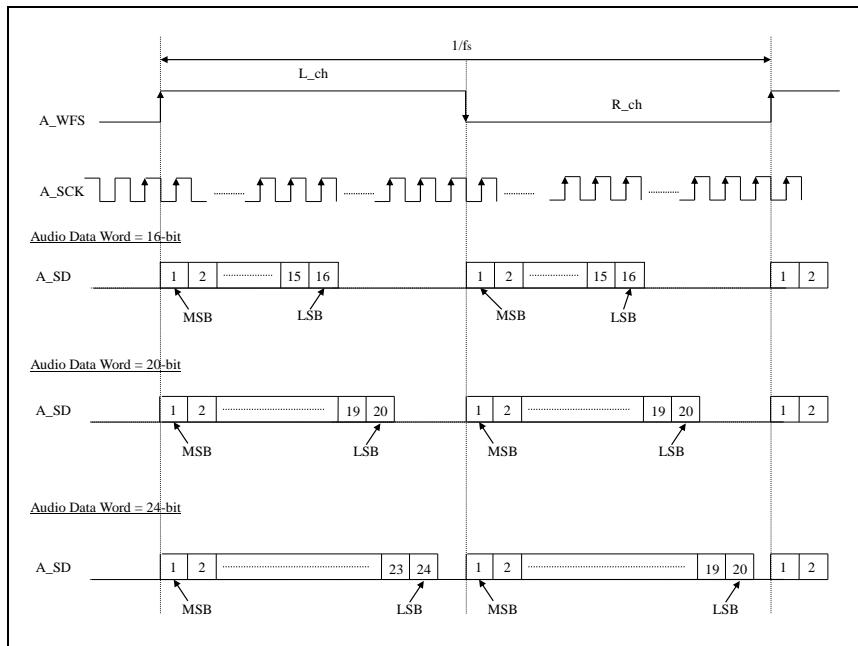
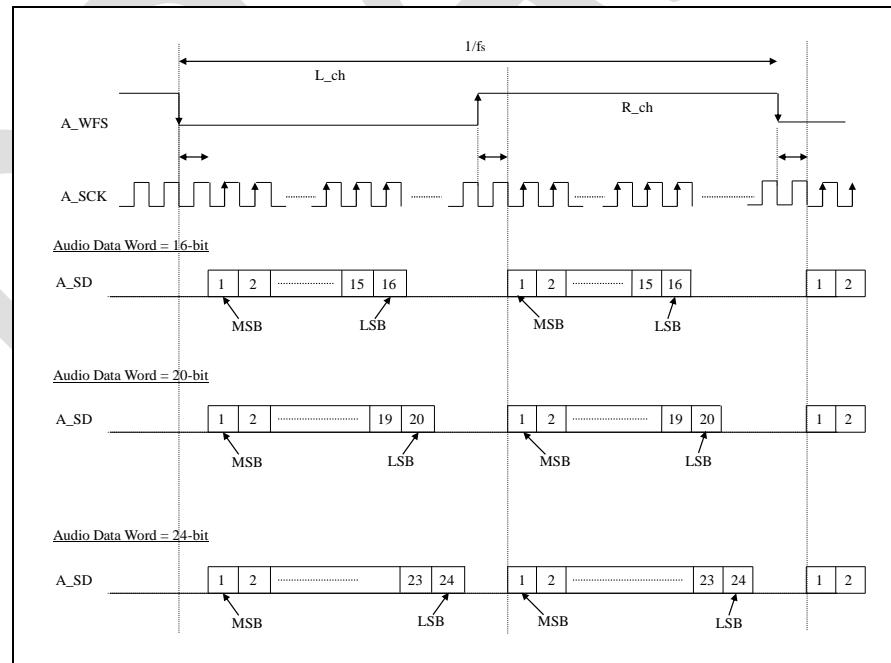


Figure 4-20 Data input timing of standard format (Sony format); L_ch=H, R_ch=L
 (SDO_MODE1.SDO_FMT=2'b00, ConfCtl.I2Sdlyopt=1'b0, SDO_MODE0.LR_POL=1'b1)



**Figure 4-21 Data input timing of Left-Justified format; L_ch=H, R_ch=L
(SDO_MODE1.SDO_FMT=2'b01, ConfCtl.I2Sdlyopt=1'b0, SDO_MODE0.LR_POL=1'b1)**



**Figure 4-22 Data input timing of I2S data format (Phillips format); L_ch=L, R_ch=H
(SDO_MODE1.SDO_FMT=2'b10, ConfCtl.I2Sdlyopt=1'b1, SDO_MODE0.LR_POL=1'b0)**

4.6.2 TDM (Time Division Multiplexed) Audio Interface

The basic features of the TDM are outlined below:

- Single output channel
- Support 16, 18, 20 or 24 bits data
- Support up to 8 channels
 - TDM output fixed at 8 channels
 - Fixed at 32 bit-time slot
- Support Master clock only

TDM interface allows multiple channels of data to be transmitted on a single data line. TDM interface is comprised of three signals: a frame synchronization pulse (WFS), serial clock (SCK) and serial audio data (SD).

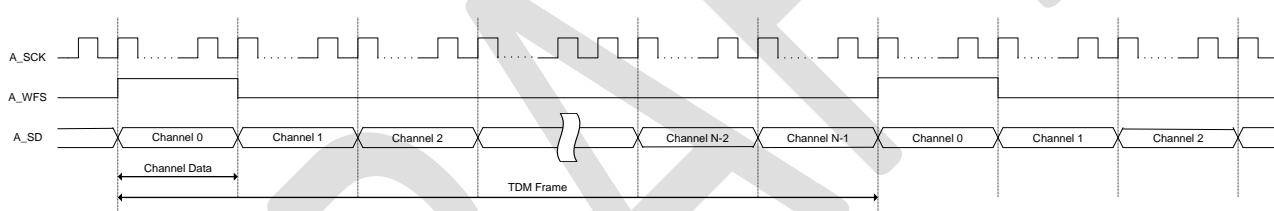


Figure 4-23 I2S N-Channel TDM timing

4.6.3 SLIMbus Audio

SLIMbus uses an un-encoded clock line and a NRZI encoded data line for signaling.

- Up to 8-channel data (2, 4, 6 or 8)
- Supports Active Framer (Host) mode as well as active Framer not present mode.
- Active Manager is not supported
- Supports Isochronous, Pushed and Pulled protocols
 - Isochronous protocol supported only in Active manager scenario
- Supports up to 28.8MHz Root Clock Frequency.
- Supports up to 22 MHz clock frequency on Clk lane.

For Framer, following options are supported:

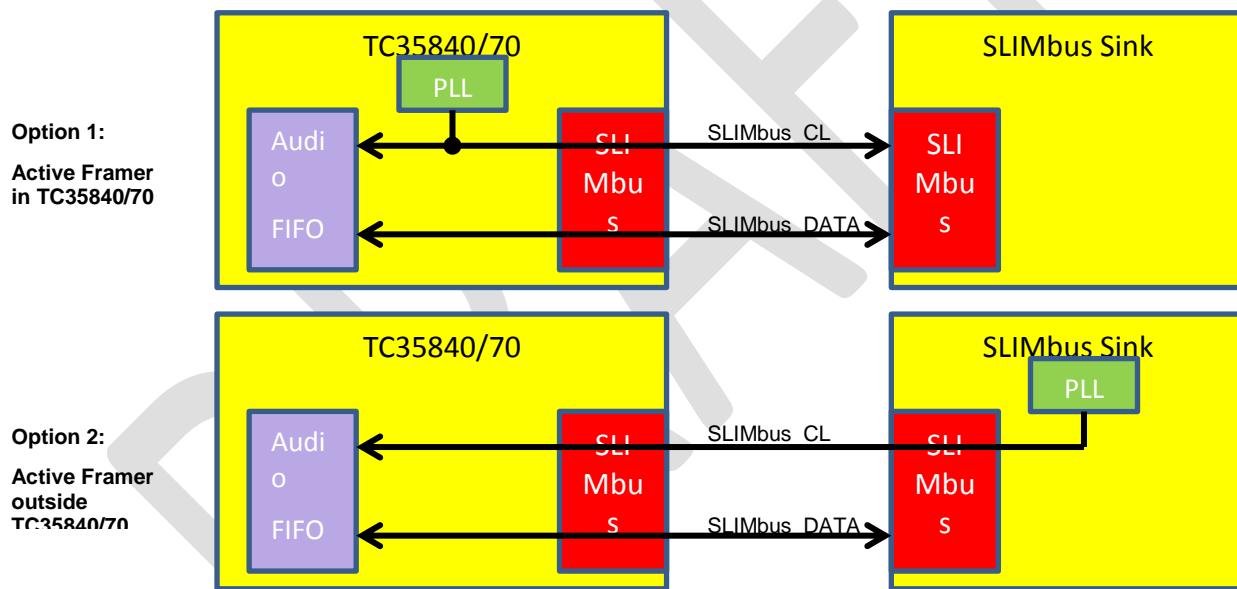


Figure 4-24 Framer configurations supported

Messages received by TC358840/70 on the SLIMbus cause TC358840/70 to send interrupts to the Host. The interrupts need to be responded to appropriately. As TC358840/70 does not have any intelligence associated, the onus of responding to the SLIMbus messages (by responding to TC358840/70 interrupts) lies with the Host. The Host is supposed to respond to the interrupts by reading the TC358840/70 registers to identify the actual cause of interrupts and then responding appropriately on SLIMbus (if required). Host interfaces with TC358840/70 through interrupt and I2C. As I2C interface is very slow compared to SLIMbus message speed, it is not possible for TC358840/70 to respond to every SLIMbus message in a timely manner while SLIMbus is operating

at nominal speeds of few MHz. To allow for TC358840/70 to respond properly to SLIMbus messages, following is proposed:

- Slow down SLIMbus clock at initialization time.
- During actual audio transfer, TC358840/70 can NOT guarantee quick response.

For Active Manager, options supported are shown below.

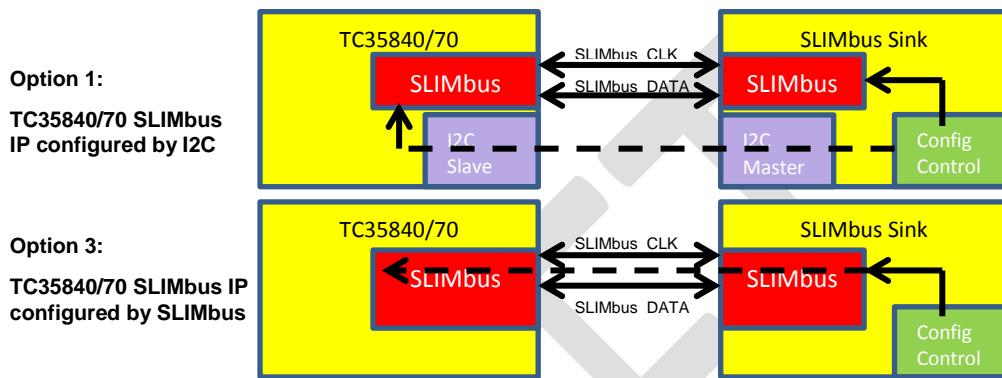


Figure 4-25 Manager configurations supported

4.6.3.1 Isochronous Protocol

Isochronous protocol does not provide any flow information nor flow control. It should be used to carry data whose rate matches exactly the channel rate, or where flow control is embedded in the data. There are no TAG bits used, therefore the length of the TAG field shall be zero on slots. A typical case is the transport of a 48 kHz sample rate PCM audio (samples available 48000 times per second) over a 48 khz channel rate (channel Segment available 48000 times per second).

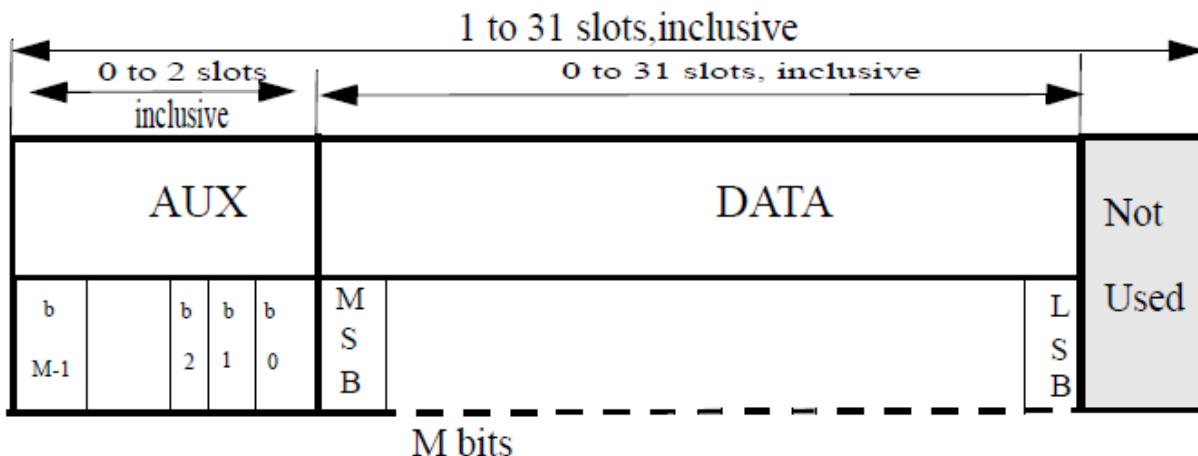


Figure 4-26 SLIMbus Isochronous Protocol

Refer SLIMbus specification for further details on different protocols.

4.6.3.2 Pushed Protocol

The pushed protocol includes flow information. It is used to carry data whose rate is equal to, or lower than the channel rate. TC358840/70 (source device for SLIMbus) drives the data flow and the TAG bits indicate availability of data in the DATA field.

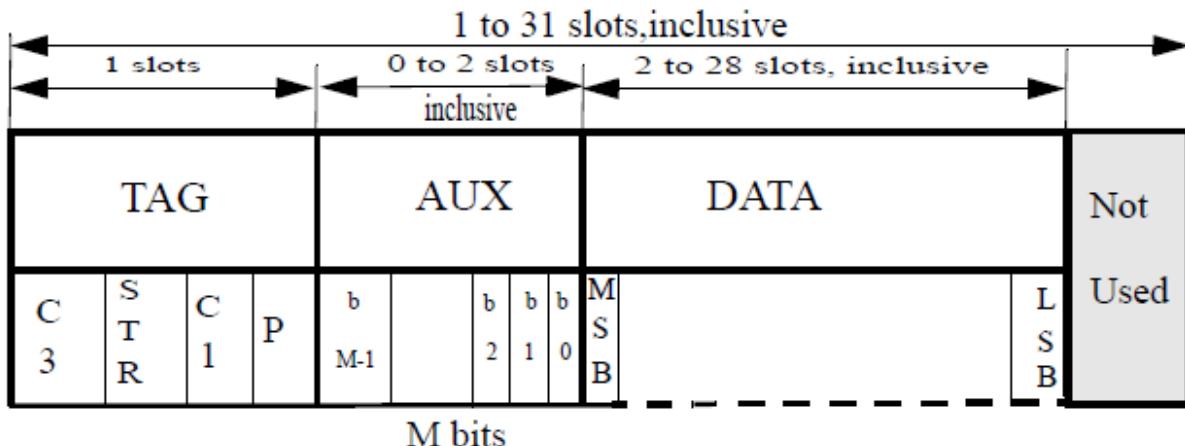


Figure 4-27 SLIMbus Pushed Protocol

Cell	Name	Source	Sink	Description
C3	-	Write	x	Reserved
C2	STR	Write	Read	STROBE bit,STR=1 indicates that data is expected to be present in the segment
C1	-	Write	x	Reserved
C0	P	Write	Read	PRESENCE bit P=1 indicates that data is present in the rest of the segment

Figure 4-28 TAG semantics for Pushed Protocol

Refer SLIMbus specification for further details on different protocols.

4.6.3.3 Pulled Protocol

The pulled Transport protocol provides a flow control mechanism where the sink device requests or pulls data from the TC358840/70 when needed. The TAG bits indicate availability of data in the DATA field. The sink should drive the SRQ (Sample request) bit and TC358840/70 will read the SRQ bit. In steady-state

operation, when SRQ=1 TC358840/70 will provide a valid sample in the current segment.

Whenever it provides a valid sample TC358840/70 shall set the P bit to indicate that the sample is present. When SRQ=0, TC358840/70 should not drive the remaining cells of the segment following C1. If, for any reason, TC358840/70 is not capable of servicing the sample request on time, it shall reset P to zero and write zeros to that segment AUX and DATA fields.

The pulled profile manages the frequency mismatch between the SLIMbus CLK line and the SLIMbus device's clock.

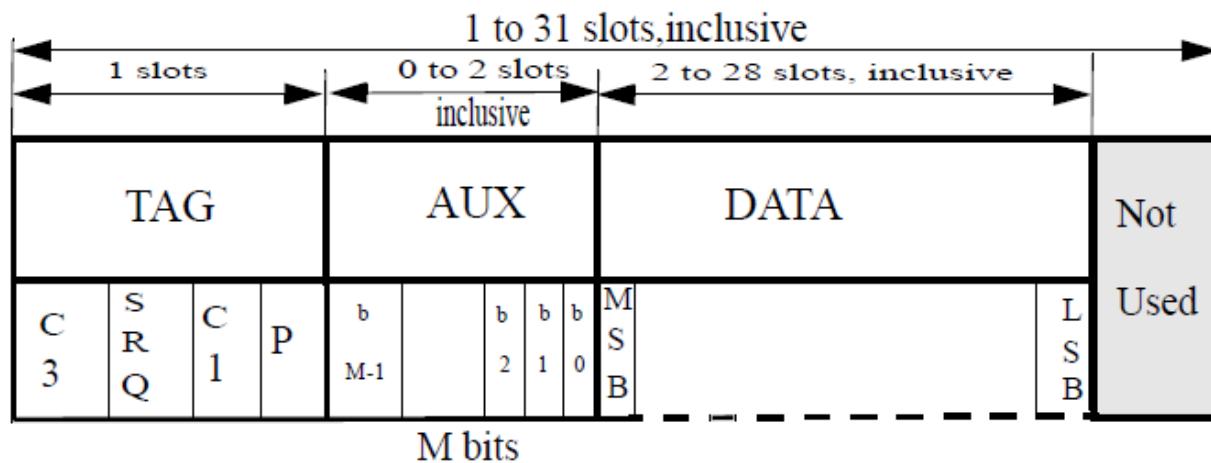


Figure 4-29 SLIMbus Pushed Protocol

Cell	Name	Source	Sink	Description
C3	--	Write	x	Reserved
C2	SRQ	Read	Write	Sample Request SRQ=1 requests a sample in the current segment
C!	--	Write	x	Reserved
C0	P	Write	Read	Presence bit,P=1 indicates that data is present in the DATA field.

Figure 4-30 TAG semantics for Pushed Protocol

Refer SLIMbus specification for further details on different protocols.

4.6.3.4 SlimBus Clock Generation

SLIMbus clock can be generated in 2 different ways in TC358840/70:

- HDMI Rx based
- External SLIMbus Active Framer

4.6.3.4.1 SlimBus Clock from HDMI Rx

SLIMbus Root Frequency Clock can also be generated from the audio over-sampling clock extracted from the HDMI Rx. In order for this mode, the following bits needs to be programmed:

- HDMI Rx audio over-sampling clock setting.

This mode supports different sampling rates from 22.05 KHz to 768 KHz based on the programming done to HDMI Audio_Div control registers (0x8666 – 0x866D).

Further, whenever the F_s changes on HDMI side, it is the responsibility of the Host software to broadcast this information well ahead on SLIMbus before actually affecting this change on HDMI side. How to handle this sequence of changing F_s and broadcasting of the message on SLIMbus is beyond the scope of this document. F_s change interrupt can be generated though if set properly.

SLIMbus protocols that can be supported in this mode are:

- Isochronous
- Pushed
- Pulled

In this mode, achieving overall clock sync is inherently built-in as shown in the diagram below.

- Active Framer (AF) is in TC358840/70 & HDMI clock is used
- Clock & Data rate – both accurate multiples of actual sampling frequency F_s .
- Clock extracted from HDMI Rx is in sync with HDMI Tx.
- Clock at all other points is in sync with clock in HDMI Tx.
- Audio data (extracted from HDMI Rx packets) is sent to AP via SLIMbus.
- No chance of drift due to frequency mismatch between HDMI source and SLIMbus sink.

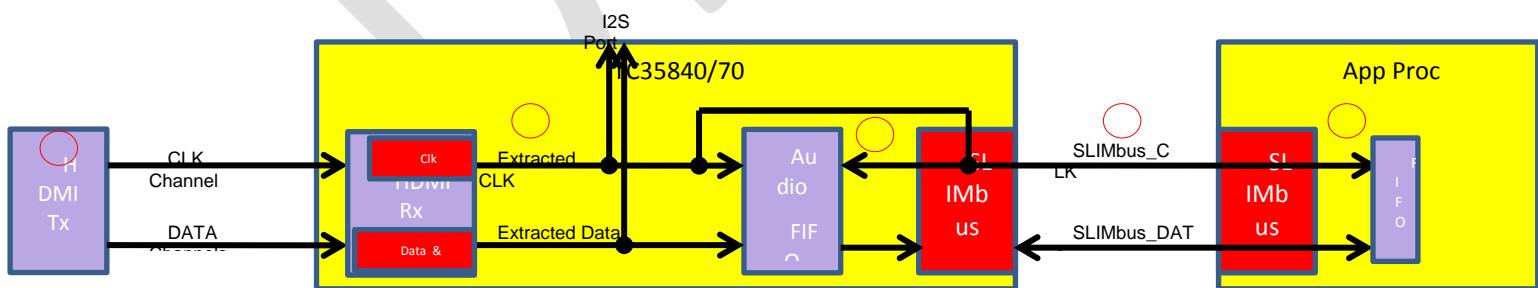


Figure 4-31 SLIMbus Clock source – HDMI Rx extracted clock in TC358840/70

4.6.3.4.1.1 *F_s* extraction programming

For proper generation of the *F_s* (sampling frequency) based on the audio stream input to HDMI Rx, proper dividers need to be programmed in HDMI Rx register space. Below are recommended divider values for different *F_s* values.

Table 4-4 HDMI *F_s* v/s divider values

F_s (KHz)	Divider
22.05	1/32
24	1/32
32	1/24
44.1	1/16
48	1/16
88.2	1/8
96	1/8
176.4	1/4
192	1/4
352.8	1/2
384	1/2
705.6	1/1
768	1/1

4.6.3.5 HBR Split over I2S

As a special case over I2S, the HBR audio stream can also be transmitted over the I2S.

But for HBR audio, the F_s is very high.

- $F_s = 768\text{kHz}$: $128\text{fs} \times 768\text{kHz} = 98.304\text{MHz}$
- $768\text{kHz} \times 64 = 49.152\text{ Mbit/lane}$.

In some scenarios, the I2S ports of the App Processor may not be able to handle this high data rate. To handle such scenarios, the HBR stream can be split across the four (4) I2S data lanes with data rate on each lane reduced by a factor of 4.

Figure below shows this feature conceptually.

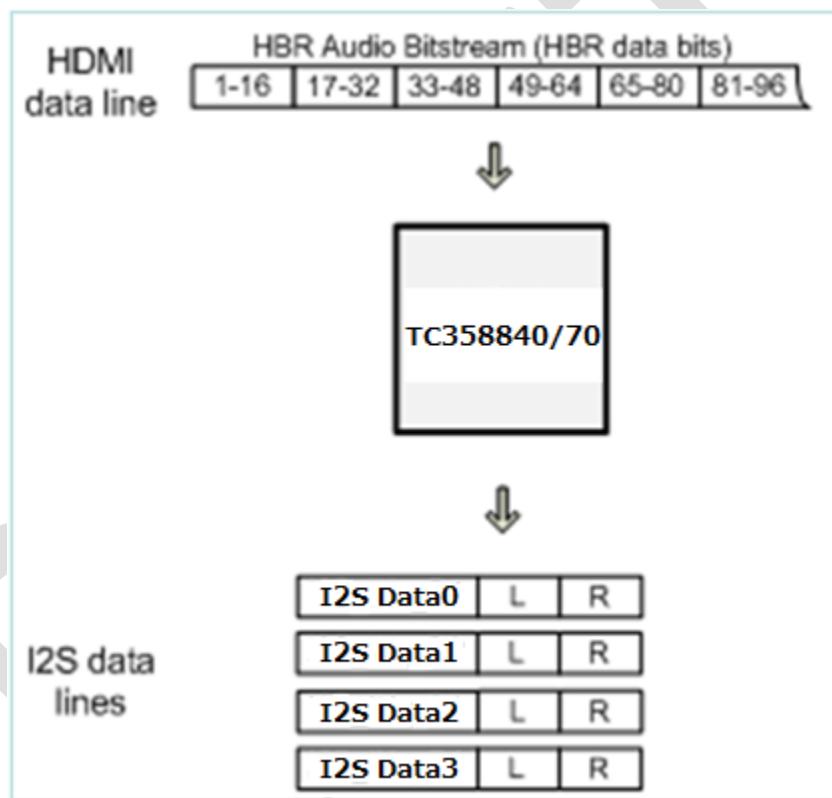


Figure 4-32 HBR Audio stream split over four (4) I2S data lanes

Figure below shows how the HBR audio stream will appear on I2S if not split across four (4) I2S data lanes.

Data Format for Dolby TrueHD HBR

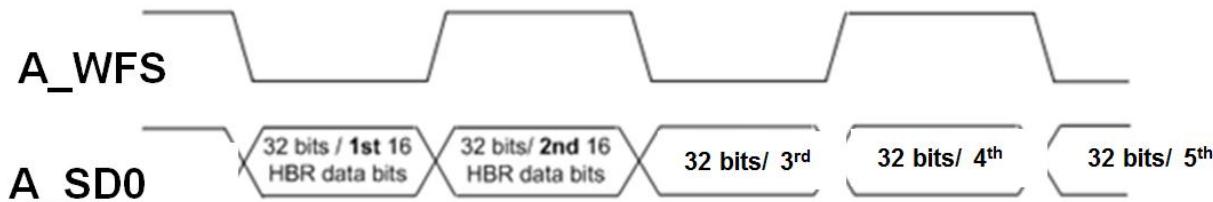


Figure 4-33 HBR Audio stream over 1 I2S lane

Figure below shows how the HBR audio stream will appear on I2S if split across four (4) data lanes.

Data Format for Dolby TrueHD HBR

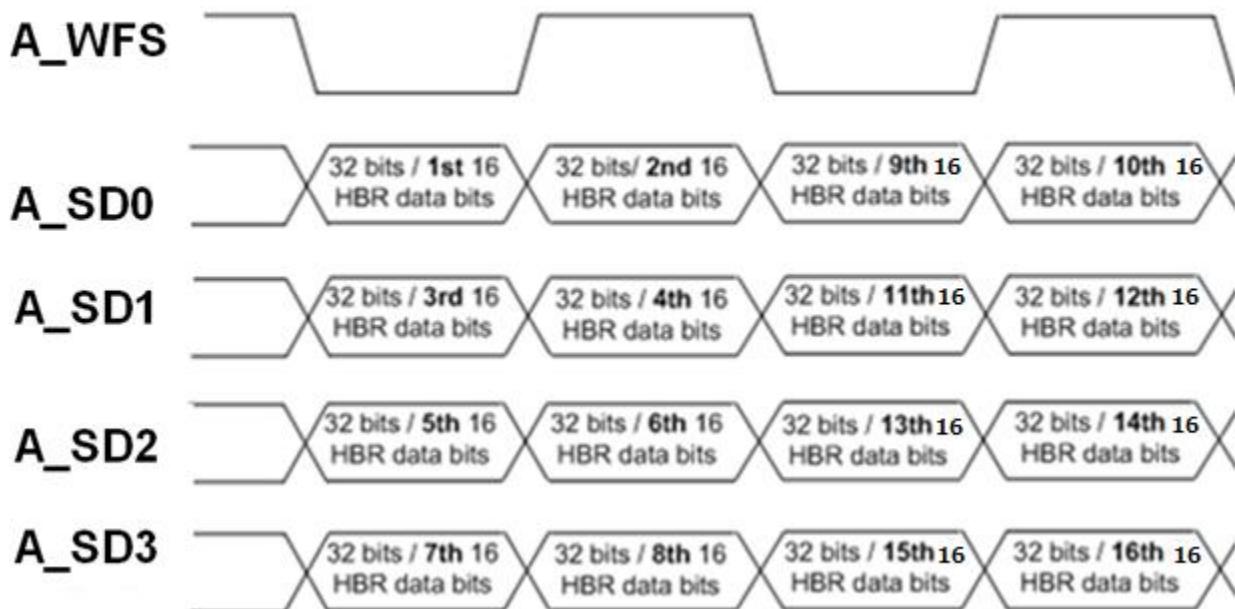


Figure 4-34 HBR Audio stream split over four (4) I2S lanes

4.6.4 Audio PLL LPF Configuration

The Audio PLL external terminal connections used in the Audio clock generation are shown in the Figure below.

In DAOUT output (PLL input), a low pass filter is installed in the LSI external area.

In addition, a low pass filter for cutting unnecessary components in phase comparator output in the PLL is also installed in the LSI external area.

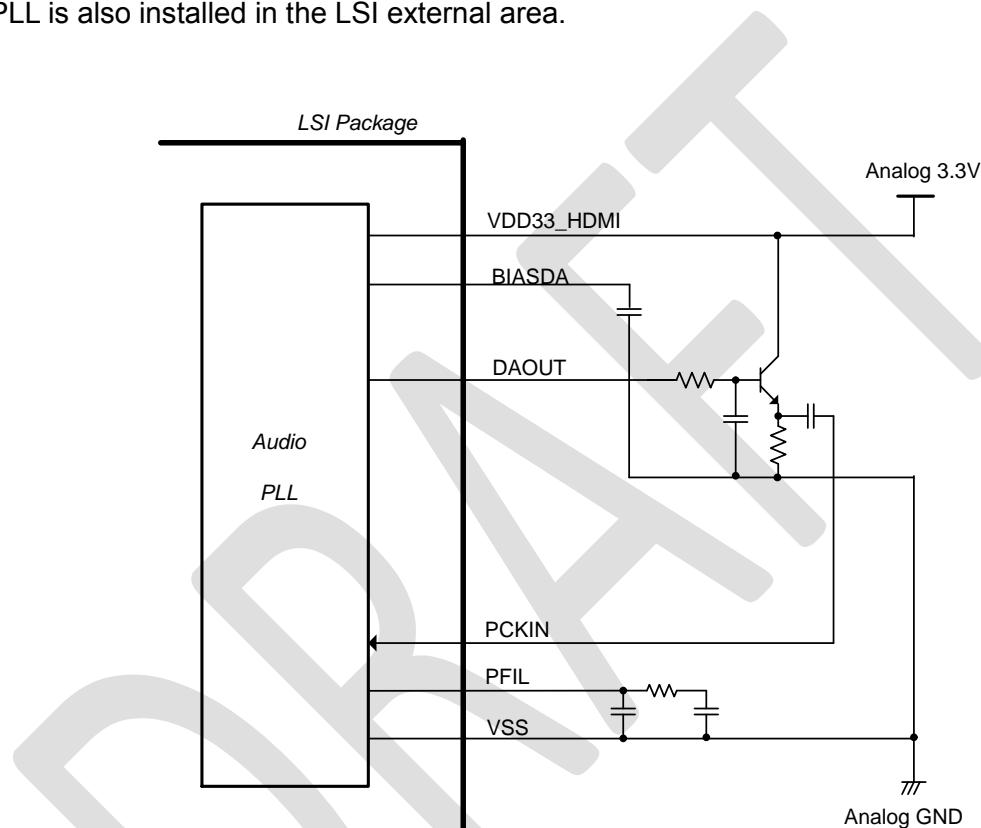


Figure 4-35 Audio Clock External LPF circuit block diagram

4.7 InfraRed (IR) Interface

The basic features of the IR are outlined below:

- Support NEC IR protocol
- Store up to 4 byte IR data
- Interrupt Host when IR address match and detect “end of message” transmission pulse.
- Programmable timing for Leading High time, Leading Low time, Logical “0” H and L time, Logical “1” H and L time.

Supports NEC IR transmission protocol which uses pulse distance encoding of the message bits. Below figures describes NEC InfraRed protocol.

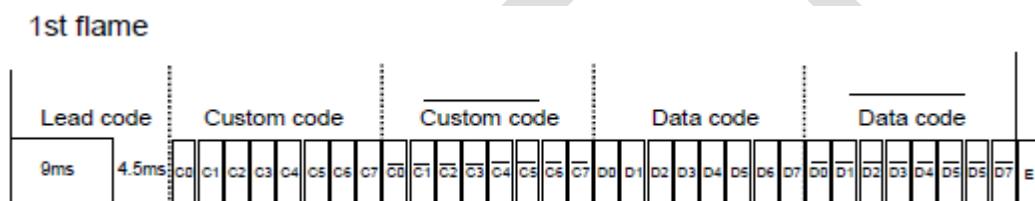


Figure 4-36 NEC Configuration of Frame

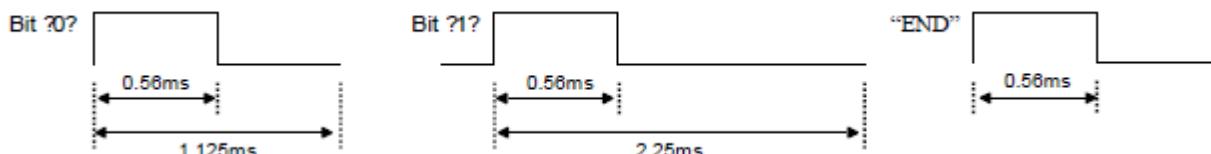


Figure 4-37 NEC Bit Description

The waveform is transmitted as long as a key is depressed

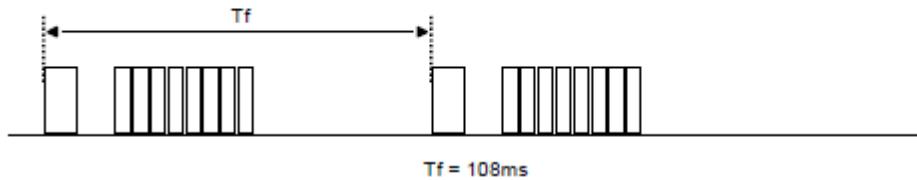


Figure 4-38 NEC Frame Interval (Tf)

4.7.1 Sampling Clock

IR lines are sampled by divide down Refclk (ir_clk).

ir_clk clock is generated from Refclk with divide option for High time and Low time. There are two parameters

1. reg_cech[10:0] contains the cec_clk HIGH time count (counts with RefClk). HIGH time has range of 1 to 2048 RefClk clock.
2. reg_cecl[10:0] contains the cec_clk LOW time count (counts with RefClk). LOW time has range of 1 to 2048 RefClk clock .

There are 12-bit counter to count the IR H time and L time with IR sampling clock. Host can config the appropriate frequency for the IR sampling clock (ir_clk).

4.7.2 Programmable timing

There are four programming timing parameters. IR modules use these timing parameters to detect Lead code, Bit H logic, Bit L logic and “END” flag. Below describes these four timing parameters

1. Detect Lead code when:
 - a. H count value is greater than LCHmin parameter (lchmin[11:0]) and smaller than LCHmax parameter (lchmax[11:0]).
 - b. L count value is greater than LCLmin parameter (lclmin[11:0]) and smaller than LCLmax parameter (lclmax[11:0]).
2. Detect “L” bit when:
 - a. H count value is greater than BitHHmin parameter (bhhmin[11:0]) and smaller than BitHHmax parameter (bhhmax[11:0]).
 - b. L count value is greater than BitHLmin parameter (bhlmin[11:0]) and smaller than BitHLmax parameter (bhlmax[11:0]).
3. Detect “H” bit when:
 - a. H count value is greater than BitLHmin parameter (blhmin[11:0]) and smaller than BitLHmax parameter (blhmax[11:0]).
 - b. L count value is greater than BitLLmin parameter (bllmin[11:0]) and smaller than BitLLmax parameter (bllmax[11:0]).
4. Detect “END” flag when:
 - a. After received Lead code – Custom code - /Custom code – Data code - /Data code
 - b. H count value is greater than EndHmin parameter (IR_EndHMIN[11:0]) and smaller than EndHmax parameter (IR_EndHMAX[11:0]).

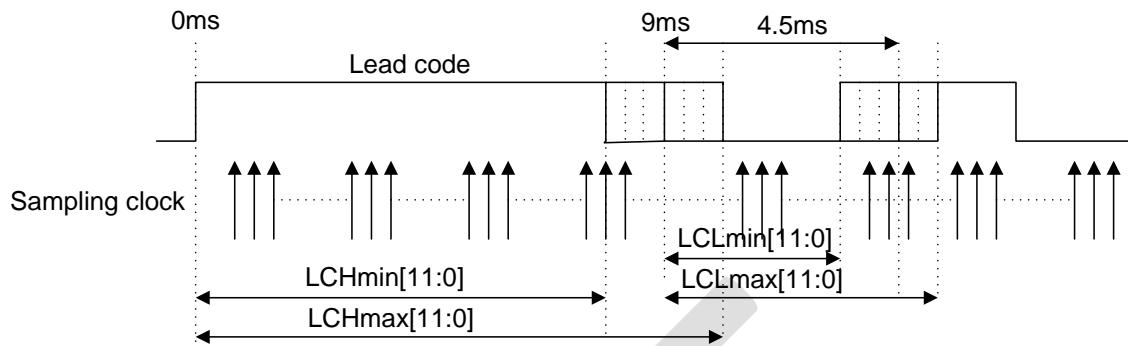


Figure 4-39 Example of Lead Code min/max values for H and L detection

4.7.3 Basic Operation

The following shows the IR sequences:

1. Detect Lead code
2. Receive 8-bit Custom code
3. Receive 8-bit /Custom code
4. IR logic compare the Receive Custom code against the programmable custom code in IR_ccode register. If they are match then IR controller continues to collect the data code. Otherwise it will ignore the IR data.
 - a. (Step 5 – 9 assumes Custom code match)
5. Receive 8-bit Data code
6. Receive 8-bit /Data code
7. Receive “End” code
8. After IR controller receive the “End” code, INT pin will be set (provided that IR_INT is not mask).
 - a. If “End” code is not receive – “End” code error flag will be set. INT pin will be set (provided that IR_Err is not mask)
9. Host need to read the 8-bit Data code through the I2C interface. Once the all the IR data code has been read host needs to clear the interrupt by writing “1” to the respective bit of the Interrupt Status register

Note: IR controller has buffer to store maximum 4 bytes of IR Data code and one 8-bit Custom code (for debugging purpose).

4.8 I2C

In addition to I2C function described in section 4.4.1, the I2C module can be addressed as a slave the following features:

- Up to 400 KHz fast mode operation
- Support special mode – Ultra fast mode 2MHz
- Supports 7 bit slave addresses recognition
 - Slave address = 7'h0F if INT = "0" during reset
 - Slave address = 7'h1F if INT = "1" during reset
- No support for general call address
- Supports 16 bit index value for TC358840/70 I2C slave access

The I2C slave function supports a fixed slave address only and does not support general call address. The I2C slave function does not require any programmable configuration parameters.

4.8.1 Providing Register Address over I2C Bus

The I2C slave function requires the interfacing I2C master to provide the register address of the TC358840/70 register to be accessed. The I2C slave function loads the first two bytes following a write command as the register address (address index) to be accessed (see Figure 4-40 and Figure 4-41).

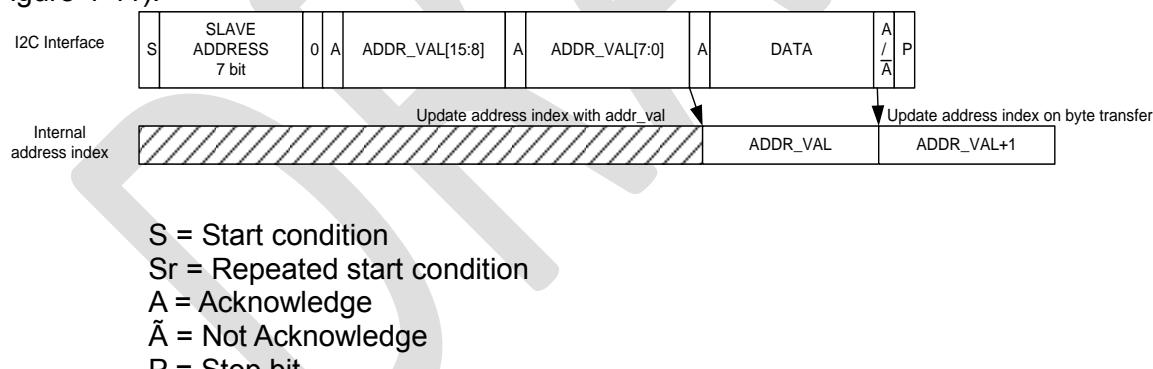


Figure 4-40 Register Write Transfer over I2C Bus

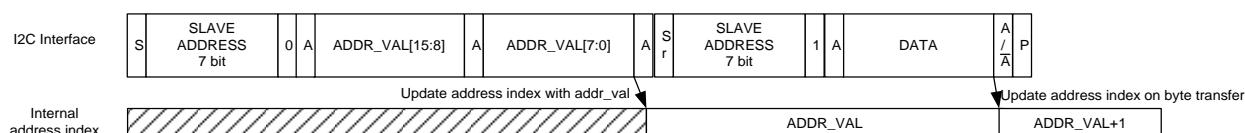


Figure 4-41 Random Register Read Transfer over I2C Bus

I²C slave function supports random write accesses and both random and continuous read accesses (see Figure 4-42).

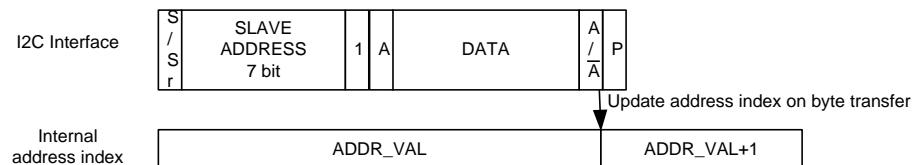


Figure 4-42 Continuous Register Read Transfer over I2C Bus

4.8.2 I²C Write Access Translation

Registers in TC358840/70 are 8, 16 and 32 bit aligned. This implies that I²C accesses to registers should always be done on 8, 16 or 32 bit boundaries depend on register group. The I²C slave controller is always operated in byte boundary. Bus management controller will pack the data to either 8, 16 or 32-bit and write into the register group accordingly.

Note that data transferred on the I²C bus is sent LSB first.

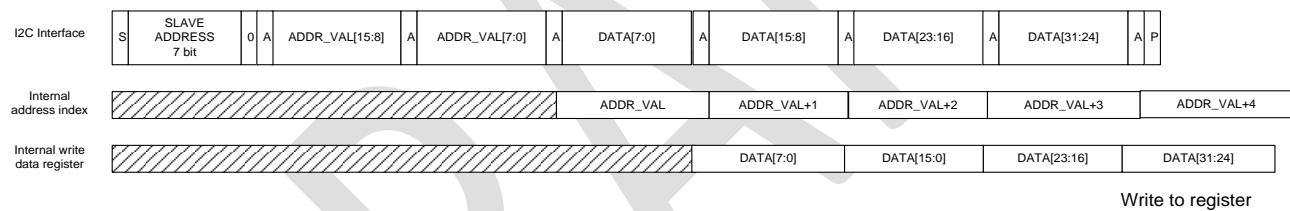


Figure 4-43 I²C Write Transfers Translated to Register Write Accesses

4.8.3 I²C Read Access Translation

Registers in TC358840/70 are 8, 16 and bit aligned. This implies that I²C accesses to registers should always be done on 8, 16 or 32 bit boundaries depend on register group. The I²C slave controller is always operated in byte boundary. Bus management controller will read the 8, 16 or 32 bit data, un-pack the data to 8-bit and send to I²C controller.

Note that data transferred on the I²C bus is sent LSB first.

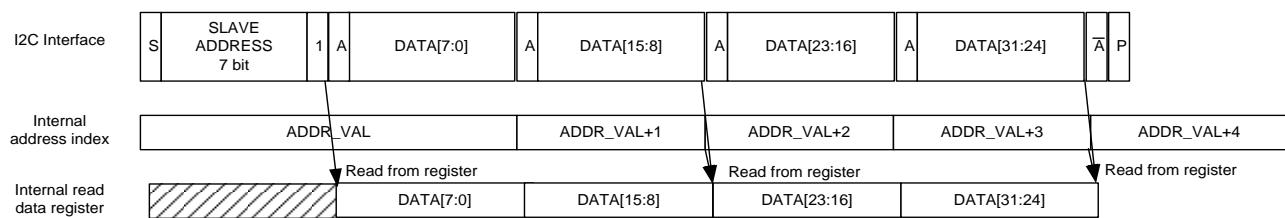
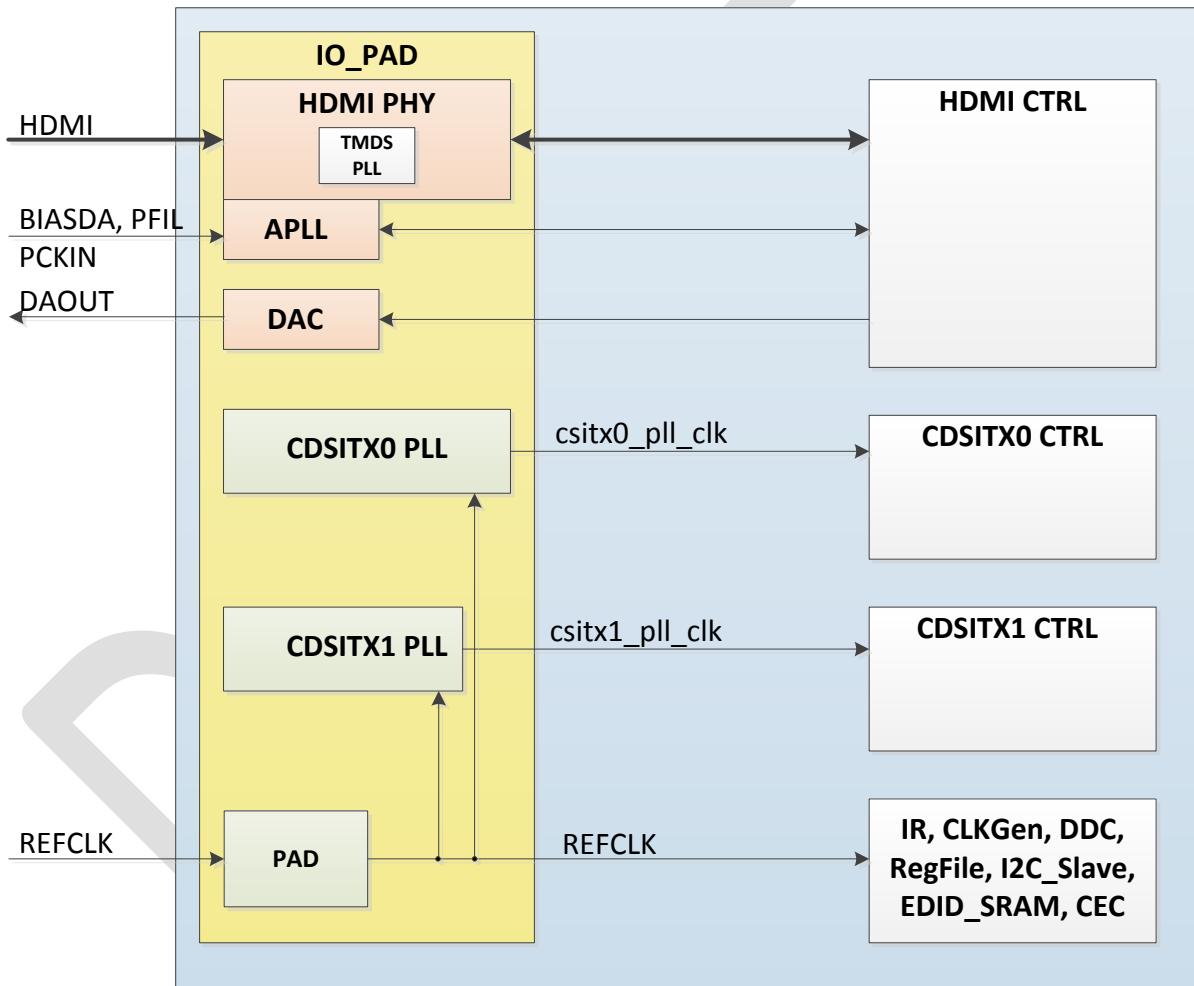


Figure 4-44 I2C Read Transfers to Register Read Accesses

5 Clock and System

TC358840/70 uses totally 4 PLLs.

- One PLL is inside the HDMI Rx PHY and is used to recover the clock from the HDMI stream.
- One PLL is inside the CSI-2/DSI0 Tx and is used to generate the high speed MIPI Tx clock.
- One PLL is inside the CSI-2/DSI1 Tx and is used to generate the high speed MIPI Tx clock.
- One PLL is used to generate the Audio over-sampling clock for audio data recovery.



CG supports three powers states RESET, FULLY ACTIVE and SLEEP where clocks are disabled or PLL is disabled to reduce power consumption. SLEEP state is controlled by register bit (reg_sleep).

In RESET: PLL is disabled and no clocks are output. During this state, TC358840/70 will not be able to function.

In FULLY ACTIVE: PLL and TC358840/70 system clock are enabled. Depending on the configuration, I2C controllers may also be enabled.

In SLEEP: PLL is disabled and no clocks are output. During this state,

- Only I2C slave, IR, DDC and CEC interfaces are enabled.
- To wake up TC358840/70
 - Application processor must wake up TC358840/70 by programming “0” to **SLEEP** bit (reg_sleep).
 - During Sleep state, TC358840/70 will interrupt Host if either DDC or CEC accesses to TC358840/70.
- This state may be used by TC358840/70 to safely update PLL parameters when required by the application processor.

CG uses an external input clock REFCLK (40MHz to 50 MHz) to generate clocks required by internal controllers.

5.1 Example of PLL Generated Clock Frequency

The possible clock frequencies generated from the CSITX-PLL are achieved by varying the values in registers **PLLFB**D and **PLLDiv**.

$$\text{csitx_pll_clk} = \text{REFCLK} * [(FBD + 1) / (PRD + 1)] * [1 / (2^FRS)]$$

Table 5-1 provides possible frequencies that may be used in TC358840/70.

Table 5-1 Possible CSITX_PLL parameters

Reference clock (MHz)	FBD	PRD	FRS	csitx_pll_clk (MHz)
40	255	7	1	640
	319	5	2	533.33
	319	6	2	457.143
	319	7	2	400.00

5.2 Output Clocks Generation

CEC_DIV:

cec_clk clock is generated from Refclk with divide option for High time and Low time.
There are two parameters

- 1) reg_CecHclk[10:0] contains the cec_clk HIGH time count (counts with RefClk). HIGH time has range of 1 to 2048 RefClk clock.
- 2) reg_CecLclk[10:0] contains the cec_clk LOW time count (counts with RefClk). LOW time has range of 1 to 2048 RefClk clock .

IR_DIV:

ir_clk clock is generated from Refclk with divide option for High time and Low time.
There are two parameters

- 1) reg_IrHclk[10:0] contains the cec_clk HIGH time count (counts with RefClk). HIGH time has range of 1 to 2048 RefClk clock.
- 2) reg_IrLclk[10:0] contains the cec_clk LOW time count (counts with RefClk). LOW time has range of 1 to 2048 RefClk clock.

CSICLK:

CSICLK is the CSI Tx clock generated by the CSI Tx PLL and is used for reading data from the final video and audio buffers and for handling the data through the CSI/DSI Tx stage.

Table 5-2 Controllers' Operating Frequency

Controllers	Operating Frequency		Source
	min (MHz)	max (MHz)	
HDMI-RX	---	297	HDMI Clock
CSI2/DSI2-TX	---	125	CSI2/DSI-TX byte clock(*)
DDC, CEC, RegFile, I2C Slave, IR Receiver	40	50	RefClk

(*) CSI2/DSI -TX byte clock is 1/8 of *csitx_pll_clk*.

5.3 TC358840/70 Power Up Procedure

The following sequence should happen before TC358840/70 is able to operate properly:

1. Provide voltage and clock sources to TC358840/70.
 - Keep all the input signals at either “Hi-z” or “logic low” state before powering on TC358840/70.
2. For voltage source, it is desired to turn on core power (1.1V) source first, then Analog PHY and IO (1.8V) power as shown in Figure 5-1 Power On Sequence.
3. REFCLK clock source can be 40 – 50 MHz.
4. The timing parameters for Figure 5-1 are tabulated in Table 5-3.

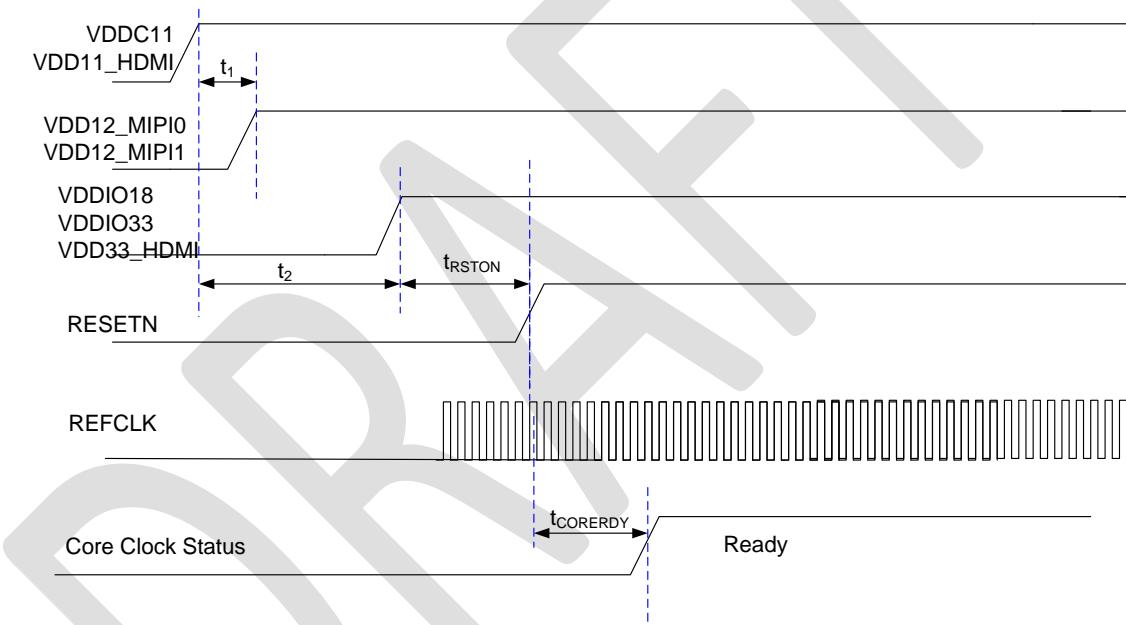


Figure 5-1 Power On Sequence

Table 5-3 Power On Sequence Timing

Parameters	Description	Min.	Typ.	Max.	Units
RefClk	Reference clock frequency	40	---	50	MHz
t_1	VDD12_MIPI0/1 on delay from VDDC11.	0	---	10	msec
t_2	VDDIO18, VDDIO33, VDD33_HDMI on delay from VDDC11, VDD11_HDMI	0	---	10	msec
t_{RSTON}	RESET width period	200	---	---	nsec
$t_{CORERDY}$	Period after reset de-assertion when TC358840/70 clocks are stable (Dependent on RefClk frequency)	0.7	---	1	msec

5.4 TC358840/70 Power Down Procedure

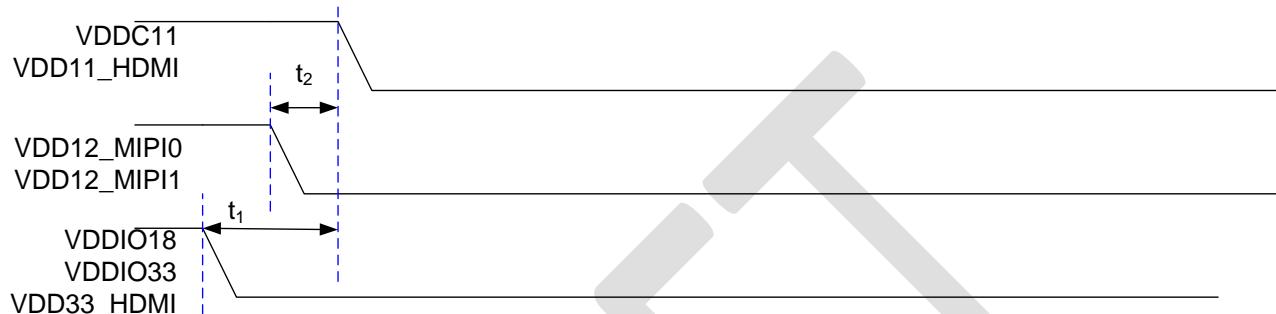


Figure 5-2 Power Down Sequence

Table 5-4 Power Down Sequence Timing

Parameters	Description	Min.	Typ.	Max.	Units
t_1	VDDC11, VDD11_HDMI off delay from VDDIO18/33, VDD33_HDMI	0	---	10	msec
t_2	VDD12_MIPI0/1 off delay from VDDC11 off	0	---	10	msec

6 RegFile Block (Reg)

The application processor (ISP) accesses TC358840/70 RegFile block to read status and/or write control registers through the I2C slave interface.

6.1 Register Map

The Overall I2C Offset address map table is provided in below Tables.

Table 6-1 Global Register Map

Segment Address	Module
0x0000 – 0x0013	Global Control Register
0x0014 – 0x001F	Interrupt Register
0x0028 – 0x002B	CEC Clock Control Register
0x002C – 0x00DF	IR Control Register
0x0080 – 0x008F	IO Control Register
0x0100 – 0x02FF	CSI2/DSI_0-TX Control Register
0x0300 – 0x04FF	CSI2/DSI_1-TX Control Register
0x0500 – 0x05FF	CDSI-TX Wrapper Register
0x0600 – 0x06FF	CEC Register
0x0700 – 0x07FF	Reserved
0x0800 – 0x4FFF	Reserved
0x5000 – 0x5FFF	Splitter registers
0x6000 – 0x6FFF	Reserved
0x7000 – 0x709F	Internal Color Bar Control Register
0x70A0 – 0x7FFF	Reserved
0x8000 – 0x9FFF	HDMIRX
0xA000 -	Reserved

Table 6-2 Detail Register Map

Group	Address	Register	Description
Global (16-bit addressable)	0x0000	ChipID	Chip and Revision ID
	0x0002	SysCtl	System Control Register
	0x0004	ConfCtl0	Configuration Control Register 0
	0x0006	ConfCtl1	Configuration Control Register 1
	0x0008	AWCnt	Audio Word Count Register
	0x000A	VWCnt	Video Word Count Register
	0x000C	PacketID1	Packet ID Register 1
	0x000E	PacketID2	Packet ID Register 2
	0x0010	PacketID3	Packet ID Register 3
	0x0012	FCCtl	Frame Count Ctrl Register
	0x001C	AudFrPrem	Audio Frame Preamble Register
	0x001E	SLmbConfig	SLIMbus Configuration Control Register
	0x0020		
	0x0022		
	0x0024		
	0x0026		
	0x0060	CSITX_MISC_CTRL	CSITx Miscellaneous Control Register
	0x0070	SLMB_AB_THRESH	SLIMbus audio threshold Register
	0x0072	I2S_IO_CTL	I2S IO Control Register
	0x0080	IOCtl0	IO control Register 0
	0x0082	IOCtl1	IO control Register 1
	0x0084	I2SPUDCTL	I2S Pull Up/Down Control Register
	0x7082	I2S_CONTROL	I2S Polarity Control
INT (16-bit addressable)	0x0014	IntStatus	Interrupt Status Register
	0x0016	IntMask	Interrupt Mask Register
	0x0018	IntFlag	Interrupt Flag Register
	0x001A	IntSYSStatus	SYS Interrupt status register
IR (16-bit addressable)	0x002C	IrHclk	IR Clock High Time register
	0x002E	IrLclk	IR Clock Low Time register
	0x0034	LCHmin	IR Lead Code Hmin register
	0x0036	LCHmax	IR Lead Code HMax register
	0x0038	LCLmin	IR Lead Code LMin register
	0x003A	LCLmax	IR Lead Code LMax register
	0x003C	BHHmin	IR Bit "H" Hmin register
	0x003E	BHHmax	IR Bit "H" Hmax register
	0x0040	BHLmin	IR Bit "H" Lmin register
	0x0042	BHLmax	IR Bit "H" Lmax register
	0x0044	BLHmin	IR Bit "L" Hmin register
	0x0046	BLHmax	IR Bit "L" Hmax register
	0x0048	BLLmin	IR Bit "L" Lmin register
	0x004A	BLLmax	IR Bit "L" Lmax register
	0x004C	EndHmin	IR "END" Hmin register
	0x004E	EndHmax	IR "END" Hmax register
	0x0050	RCLmin	IR Repeat Code LMin register
	0x0052	RCLmax	IR Repeat Code LMax register
	0x0058	IRCtl	IR Control register
	0x005A	IRRData	IR Receive Data register
	0x7082	IR_CONTROL	IR Input Polarity Control

Group	Address	Register	Description
CEC (16-bit addressable)	0x0028	CecHclk	CEC Clock High Time register
	0x002A	CecLclk	CEC Clock Low Time register
CSI2/DSI_0-TX	0x0104	ADDRESS_CONFIG	Address_Config register
	0x0108	CDSITX_CLKEN	CDSITX CLK Enable register
CSI2/DSI_1-TX	0x0304	ADDRESS_CONFIG	Address_Config register
	0x0308	CDSITX_CLKEN	CDSITX CLK Enable register
CDSI-TX Wrapper	0x0500	STX_Ctrl	CDSITX Control Register
CEC (32-bit addressable)	0x0600	CECEN	CEC Enable Register
	0x0604	CECADD	CEC Logical Address Register
	0x0608	CECRESET	CEC Reset Register
	0x060C	CECREN	CEC Receive Enable Register
	0x0610	--	Reserved
	0x0614	CECRCR1	CEC Receive Control Register 1
	0x0618	CECRCR2	CEC Receive Control Register 2
	0x061C	CECRCR3	CEC Receive Control Register 3
	0x0620	CECTEN	CEC Transmit Enable Register
	0x0628	CECTCR	CEC Transmit Control Register
	0x062C	CECRSTAT	Receive Interrupt Status Register
	0x0630	CECTSTAT	Transmit Interrupt Status Register
	0x0634	CECRBUF01	CEC Receive Buffer Register 1
	CEC Receive Buffer Register ...
	0x0670	CECRBUF16	CEC Receive Buffer Register 16
	0x0674	CECTBUF01	CEC Transmit Buffer Register 1
	CEC Transmit Buffer Register ...
	0x06B0	CECTBUF16	CEC Transmit Buffer Register 16
	0x06B4	CECRCTR	CEC Receive Byte Counter
	0x06B8	CECTESTR	CEC Test Purpose Register
	0x06C0	CECIMSC	CEC interrupt mask control register
	0x06CC	CECICR	CEC interrupt clear control register
	0x06D0 – 0x4FFF	---	Reserved
Splitter (16-bit addressable)	0x5000 – 0x5FFF		
	0x6000 – 0x6FFF	Reserved	
Internal Colorbar & Debug Registers (16-bit addressable)			
	0x7018 – 0x7FFF	Reserved	
HDMI RX Interrupts (8-bit addressable)	0x8000 – 0x9FFF		

Note:

- HDMI registers are 8-bit register.
- CEC registers are 32-bit register. Host must write two consecutive 16-bit register write to form 32-bit access.
- Note: CSI/DSI registers cannot be accessed when video transfer is in progress.

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The following sections provide a detailed description of the registers.

6.2 Global

6.2.1 Chip and Revision ID (ChipID: 0x0000)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name					ChipID			
Type					RO			
Default					0x47			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name					RevID			
Type					RO			
Default					0x0			

Register Field	Bit	Description
ChipID	[15:8]	Chip ID Chip ID assigned for this device by Toshiba.
RevID	[7:0]	Revision ID Revision ID for this device assigned by Toshiba.

6.2.2 System Control Register (SysCtl: 0x0002)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved	ABRst	SLMBRst	SPLRst	IRRst	CecRst	CTXRst	HdmiRst
Type	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I2S_Dis				Reserved			SLEEP
Type	R/W				RO			R/W
Default	0x1				0x0			0x1

Register Field	Bit	Description
Reserved	[15]	
ABRst	[14]	Audio Block Software Reset (Active high) This bit is set to force Audio Block logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation Software needs to clear ABRst when set.
SLMBRst	[13]	SLIMbus Software Reset (Active high) This bit is set to force SLIMbus logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation Software needs to clear SLMBRst when set.
SPLRst	[12]	SPLITter Software Reset (Active high) This bit is set to force VIP logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation Software needs to clear VIPRst when set.
IRRst	[11]	IR Software Reset (Active high) This bit is set to force IR logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation Software needs to clear IRReset when set.
CecRst	[10]	CEC Software Reset (Active high) This bit is set to force CEC logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation Software needs to clear CECReset when set.
CTXRst	9	CSI2-TX Software Reset (Active high) This bit is set to force CSI2-TX0 and CSI2-TX1 logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation Software needs to clear CReset when set.

Register Field	Bit	Description
HdmiRst	8	HDMI-RX Software Reset (Active high) This bit is set to force HDMI-RX logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation Software needs to clear HReset when set.
I2S_Dis	7	I2S Interface Disable (Active high) Control to disable I2S output interface (applies when ConfCtl.SLMB_en=0) 0: Enable I2S output interface 1: Disable I2S output interface Software needs to enable this (disabled by default).
Reserved	[6:1]	
SLEEP	0	SLEEP control 0: Normal operation 1: Sleep mode

6.2.3 Configuration Control Register 0 (ConfCtl0: 0x0004)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	TX_msel	SLMB_en	IECEn	AClkOpt	AudChNum	AudChSel	I2SDlyOpt	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	YCbCrFmt		ABuf_en		AudOutSel	AutoIndex	Vtx1_en	Vtx0_en
Type	R/W		R/W		R/W	R/W	R/W	
Default	0x0		0x0		0x0	0x0	0x0	

Register Field	Bit	Description
TX_msel	[15]	CDSITX Mode Select 1'b0: DSI-TX mode 1'b1: CSI-TX mode
SLMB_en	[14]	SLIMbus Enable 1'b0: Disable SLIMbus output 1'b1: Enable SLIMbus output
IECEn	[13]	IEC60958 Audio enable on CSI Tx 1'b0: Disable IEC60958 framing on CSI Tx and follow other controls for audio over CSI Tx 1'b1: Enable IEC60958 framing over CSI Tx (assuming input stream is in SPDIF format) – This function is not supported.
AClkOpt	[12]	Audio Bit Clock Option 1'b0: I2S/TDM clock are free running 1'b1: I2S/TDM clock stops when Mute active
AudChNum	[11:10]	Audio Channel Output Channels 2'b00: Enable 8 Audio channels 2'b01: Enable 6 Audio channels 2'b10: Enable 4 Audio channels 2'b11: Enable 2 Audio channels Note: valid only AudChSel = 1
AudChSel	[9]	Audio Channel Number Selection Mode 1'b0: Auto detect by HW 1'b1: Select by AudChNum register bits Note: valid only when AudOutSel[4] = 0
I2SDlyOpt	[8]	I2S/TDM Data Delay Option 1'b0: No delay 1'b1: Delay by 1 clock
YCbCrFmt	[7:6]	YCbCr Video Output Format select 2'b00: Select YCbCr444 data format 2'b01: Select YCbCr422 12-bit data format 2'b10: Select VPID2 parameter as data format 2'b11: Select YCbCr422 8-bit (HDMI YCbCr422 12-bit data format, discard last 4 data bits) Note: RGB data, this field has to be set to 2'b00
ABuf_en	[5]	Audio TX Buffer Enable 1'b0: disable

Register Field	Bit	Description
		1'b1: enable Note: enable only after HDMIRX and CSITX register have been setup.
AudOutSel	[4:3]	Audio Output option 2'b00: Audio output to CDSI-TX0 I/F 2'b01: Audio output to CDSI-TX1 I/F 2'b10: Audio output to I2S I/F 2'b11: Audio output to TDM I/F
AutoIndex	[2]	I2C slave index increment 1'b0: I2C address index does not increment on every data byte transfer 1'b1: I2C address index increments on every data byte transfer
VTX1_En	[1]	Video TX1 Enable 1'b0: disable 1'b1: enable Note: enable only after HDMIRX and CDSITX1 register have been setup.
VTX0_En	[0]	Video TX0 Enable 1'b0: disable 1'b1: enable Note: enable only after HDMIRX and CDSITX0 register have been setup.

6.2.4 Configuration Control Register 1(ConfCtl1: 0x0006)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							ef_bdone
Type	RO							RO
Default	0x0							0x?
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			dcs_clks	tx_msen	tx_ofmt		
Type	RO			R/W	R/W	R/W		
Default	0x0			0x0	0x0	0x0		

Register Field	Bit	Description
Reserved	[31:3]	
ef_bdone	[8]	eFuse SF_ATBOOTDONE status
Reserved	[7:3]	
dcs_clks	[3]	DCS Command Clock Source 1'b0: HDMIRX Pxclk 1'b1: Refclk Note: When no transfer video, must program this bit to "1"
tx_msen	[2]	Magic Square Enable 1'b0: Disable 1'b1: Enable (for RGB666 only)
tx_ofmt	[1:0]	CDSITX Output Format select 2'b0x: RGB888 2'b10: RGB666 packed 2'b11: RGB666 loosely packed

6.2.5 Audio Frame Preamble Register (AudFrPrem: 0x001C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					prem_m		
Type	RO					R/W		
Default	0x0					0x1		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	prem_w					prem_b		
Type	R/W					R/W		
Default	0x2					0x0		

Register Field	Bit	Description
Reserved	[15:12]	
prem_m	[11:8]	Preamble M Value used to indicate Preamble M
prem_w	[7:4]	Preamble W Value used to indicate Preamble W
prem_b	[3:0]	Preamble B Value used to indicate Preamble B

6.2.6 SLIMbus Configuration Control Register (SlmbConfig: 0x001E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved		sbrc_src		ext_sync_pulse_en			
Type	RO		R/W		R/W			
Default	0x0		0x1		0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					ready_sync		
Type	RO					R/W		
Default	0x00					0x1		

Register Field	Bit	Description
Reserved	[15:14]	
SBRC_SRC	[13:12]	SLIMbus Root Frequency Clock Source 2'b00: Reserved 2'b01: HDMI Rx based 2'b10: External Active Framer based 2'b11: Reserved
ext_sync_pulse_en	[11:8]	Enable for connecting HDMI Rx word select clock to the ext_presence_rate_clk i/p of SLIMbus IP
Reserved	[7:2]	
ready_sync	[1:0]	Number of slmb_clock clock cycles after negedge of audio sync pulse to next data launch

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6.2.7 SLMB_AB_THRES (SLMB_AB_THRES: 0x0070)

Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	RO	RO	RO	RO	RO	RO	RO	RO	
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved	slmb_ab_thres							
Type	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	

Register Field	Bit	Description
Reserved	[15:7]	
slmb_ab_thres	[6:0]	SLIMbus audio threshold For testing only.

6.2.8 I2S_IO_CTL (I2S_IO_CTL: 0x0072)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				I2SCtl4	I2SCtl3	I2SCtl2	I2SCtl1
Type	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description
Reserved	[15:4]	
I2SCtl4	[3]	I2S Ctl4 CTL4 of A_SCK, A_OSCK, A_WFS, A_SD_0, A_SD_1, A_SD_2 and A_SD_3 pins
I2SCtl3	[2]	I2S Ctl3 CTL3 of A_SCK, A_OSCK, A_WFS, A_SD_0, A_SD_1, A_SD_2 and A_SD_3 pins
I2SCtl2	[1]	I2S Ctl2 CTL2 of A_SCK, A_OSCK, A_WFS, A_SD_0, A_SD_1, A_SD_2 and A_SD_3 pins
I2SCtl1	[0]	I2S Ctl1 CTL1 of A_SCK, A_OSCK, A_WFS, A_SD_0, A_SD_1, A_SD_2 and A_SD_3 pins

6.2.9 I2SPUDCTL (I2SPUDCTL: 0x0084)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved		A_SD_3Pu	A_SD_3Pd	A_SD_2Pu	A_SD_2Pd	A_SD_1Pu	A_SD_1Pd
Type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	A_SD_0Pu	A_SD_0Pd	A_WFSPu	A_WFSPd	A_SCKPu	A_SCKPd	A_OSCKPu	A_OSCKPd
Type	R/W							
Default	0x0	0x1	0x0	0x0	0x0	0x1	0x0	0x0

Register Field	Bit	Description
Reserved	[15:14]	These bits are writeable but the writes are ignored as these bits are not used anywhere.
A_SD_3Pu	[13]	A_SD_3 Pull Up
A_SD_3Pd	[12]	A_SD_3 Pull Down
A_SD_2Pu	[11]	A_SD_2 Pull Up
A_SD_2Pd	[10]	A_SD_2 Pull Down
A_SD_1Pu	[9]	A_SD_1 Pull Up
A_SD_1Pd	[8]	A_SD_1 Pull Down
A_SD_0Pu	[7]	A_SD_0 Pull Up
A_SD_0Pd	[6]	A_SD_0 Pull Down
A_WFSPu	[5]	A_WFS Pull Up
A_WFSPd	[4]	A_WFS Pull Down
A_SCKPu	[3]	A_SCK Pull Up
A_SCKPd	[2]	A_SCK Pull Down
A_OSCKPu	[1]	A_OSCK Pull Up
A_OSCKPd	[0]	A_OSCK Pull Down

6.2.10 I2S Control Register (I2SCtl: 0x7082)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					I2SWFSInv	Reserved	I2SSCKInv
Type	RO					R/W	R/W	R/W
Default	0x00					0	0x0	0

Register Field	Bit	Default	Description
Reserved	[15:3]	0x0	These bits used by IR Control Register
I2SWFSInv	2	0x0	I2SWFSInv (Option to use inverted or non-inverted I2S Word Select Clock) 1: Invert I2S WFS Polarity
Reserved	1	0x0	These bits used by IR Control Register
I2SSCKInv	0	0x0	I2SSCKInv (Option to use inverted or non-inverted I2S Shift Clock) 1: Invert I2S Shift Clock Polarity

Note: This register shares the address with the IR Control Register

6.3 Interrupt Registers

6.3.1 Interrupt Status Register (IntStatus: 0x0014)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				CSITX1_INT	AMUTE_INT	HDMI_INT	CSITX0_INT
Type	RO				W1C	W1C	W1C	W1C
Default	0x0				0x0	0x0	0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SLMB_INT	Reserved	SYS_INT	CEC_EINT	CEC_TINT	CEC_RINT	IR_EINT	IR_DINT
Type	R/W1C	RO	W1C	W1C	W1C	W1C	W1C	W1C
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description
Reserved	[15:12]	
CSITX1_INT	[11]	CSI2-TX1 Interrupt Status
AMUTE_INT	[10]	Audio Mute Interrupt Status 1'b0: Normal 1'b1: Audio change from Normal to Mute Default = 0 (Value immediately becomes '1' after reset)
HDMI_INT	[9]	HDMI-RX Interrupt Status Note: all HDMI interrupt flags defined in HDMI register space
CSITX0_INT	[8]	CSI2-TX0 Interrupt Status
SLMB_INT	[7]	SLIMbus General Interrupt Status
Reserved	[6]	
SYS_INT	[5]	TC358840/70 System Interrupt Status 1'b0: Normal 1'b1: Video/Audio Overflow/Underflow/WakeUp occurs
CEC_EINT	[4]	CEC Error Interrupt Status 1'b0: Normal 1'b1: CEC Errors occurs
CEC_TINT	[3]	CEC Transmit Interrupt Status 1'b0: Idle 1'b1: Transmit completed/done
CEC_RINT	[2]	CEC Receive Interrupt Status 1'b0: Idle 1'b1: Data Received
IR_EINT	[1]	IR Error Interrupt Status 1'b0: No Error 1'b1: Error occurs (overflow error)
IR_DINT	[0]	IR Data Interrupt Status 1'b0: Idle 1'b1: Interrupt occurs (IR Data available)

Note: Write "1" to clear Interrupt. Interrupt is only active when INT_MASK = 1'b0.

Note: Pls. clear the interrupt source first (e.g. CEC interrupt bit in CEC interrupt clear register) before clearing the status bit in this register.

6.3.2 Interrupt Mask Register (IntMask: 0x0016)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				CSITX1_MSK	AMUTE_MSK	HDMI_MSK	CSITX0_MSK
Type	RO				R/W	R/W	R/W	R/W
Default	0x0				0x0	0x1	0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SLMB_MSK	Reserved	SYS_MSK	CEC_EMSK	CEC_TMSK	CEC_RMSK	IR_EMSK	IR_DMSK
Type	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description
Reserved	[15:12]	
CSITX1_MSK	[11]	CSI2-TX1 Interrupt Mask
AMUTE_MSK	[10]	Audio Mute Interrupt Mask
HDMI_MSK	[9]	HDMI-RX Interrupt Mask
CSITX0_MSK	[8]	CSI2-TX0 Interrupt Mask
SLMB_MSK	[7]	SLIMbus General Interrupt Mask
Reserved	[6]	
SYS_MSK	[5]	SYS Interrupt Mask
CEC_EMSK	[4]	CEC Error Interrupt Mask
CEC_TMSK	[3]	CEC Transmit Interrupt Mask
CEC_RMSK	[2]	CEC Receive Interrupt Mask
IR_EMSK	[1]	IR Error Interrupt Mask
IR_DMSK	[0]	IR Data Interrupt Mask 1'b0: Enable Interrupt 1'b1: Mask Interrupt

Note: if *MSK=1'b1 then *INT is never asserted

6.3.3 Interrupt Flag Register (IntFlag: 0x0018)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				CSITX1_FLG	AMUTE_FLG	HDMI_FLG	CSITX0_FLG
Type	RO				RO	RO	RO	RO
Default	0x0				0x0	0x0	0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SLMB_FLG	Reserved	SYS_FLG	CEC_EFLG	CEC_TFLG	CEC_RFLG	IR_EFLG	IR_DFLG
Type	RO_S	RO	RO	RO	RO	RO	RO	RO
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description
Reserved	[15:12]	
CSITX1_FLG	[11]	CSI2-TX1 Interrupt Flag
AMUTE_FLG	[10]	Audio Mute Interrupt Flag Default = 0 (Value immediately becomes '1' after reset)
HDMI_FLG	[9]	HDMI-RX Interrupt Flag
CSITX0_FLG	[8]	CSI2-TX0 Interrupt Flag
SLMB_FLG	[7]	SLIMbus General Interrupt Flag
Reserved	[6]	
SYS_FLG	[5]	SYS Interrupt Flag
CEC_EFLG	[4]	CEC Error Interrupt Flag
CEC_TFLG	[3]	CEC Transmit Interrupt Flag
CEC_RFLG	[2]	CEC Receive Interrupt Flag
IR_EFLG	[1]	IR Error Interrupt Flag
IR_DFLG	[0]	IR Data Interrupt Flag 1'b0: Idle 1'b1: Interrupt occurs (Data available)

Note: *MASK does not affect these flag status

6.3.4 SYS Interrupt Status Register (IntSYSStatus: 0x001A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name				Reserved				
Type				RO				
Default				0x0				
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name				Reserved				HPI_chg
Type				RO				RO
Default				0x0				0x0

Register Field	Bit	Description
Reserved	[15:1]	
HPI_chg	[0]	HPDI status 0: Normal 1: change Note: only valid during sleep mode. Use to wake up the host when HDPI is changing.

Note: These status will be clear when write "1" to SYS_INT register bit in IntStatus register.

6.4 IR Registers

6.4.1 IR Clock High Time Register 0 (IrHclk: 0x002C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						irhclk	
Type	RO						R/W	
Default	0x0						0x2	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	irhclk							
Type	R/W							
Default	0x29							

Register Field	Bit	Description
Reserved	[15:11]	
irhclk	[10:0]	IR Clock High Time 0: Disable 1: 1 RefClk 2: 2 RefClk

6.4.2 IR Clock Low Time Register 0 (IrLclk: 0x002E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						irclk	
Type	RO						R/W	
Default	0x0						0x2	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	irclk							
Type	R/W							
Default	0x29							

Register Field	Bit	Description
Reserved	[15:11]	
Irclk	[10:0]	IR Clock Low Time 0: Disable 1: 1 RefClk 2: 2 RefClk

6.4.3 IR Lead Code HMin Register (LCHmin: 0x0034)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name		Reserved					lchmin	
Type		RO					R/W	
Default		0x0					0x1	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name					lchmin			
Type					R/W			
Default					0x50			

Register Field	Bit	Description
Reserved	[15:12]	
lchmin	[11:0]	IR Lead Code H Minimum Count 0: Not valid 1: 1 count 2: 2 count

6.4.4 IR Lead Code HMax Register (LCHmax: 0x0036)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						lchmax	
Type	RO						R/W	
Default	0x0						0x1	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	lchmax							
Type	R/W							
Default	0x64							

Register Field	Bit	Description
Reserved	[15:12]	
lchmax	[11:0]	IR Lead Code H Maximum Count 0: Not valid 1: 1 count 2: 2 count

6.4.5 IR Lead Code LMin Register (LCLmin: 0x0038)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						lclmin	
Type	RO						R/W	
Default	0x0						0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	lclmin							
Type	R/W							
Default	0xA3							

Register Field	Bit	Description
Reserved	[15:12]	
lclmin	[11:0]	IR Lead Code L Minimum Count 0: Not valid 1: 1 count 2: 2 count

6.4.6 IR Lead Code LMax Register (LCLmax: 0x003A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						lclmax	
Type	RO						R/W	
Default	0x0						0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	lclmax							
Type	R/W							
Default	0xB7							

Register Field	Bit	Description
Reserved	[15:12]	
lclmax	[11:0]	IR Lead Code L Maximum Count 0: Not valid 1: 1 count 2: 2 count

6.4.7 IR Bit “H” HMin Register (BHHmin: 0x003C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					bhhmin		
Type	RO					R/W		
Default	0x0					0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	bhhmin							
Type	R/W							
Default	0x0C							

Register Field	Bit	Description
Reserved	[15:12]	
bhhmin	[11:0]	IR Bit H H Minimum Count 0: Not valid 1: 1 count 2: 2 count

6.4.8 IR Bit “H” H Max Register (BHHmax: 0x003E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				bhhmax			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	bhhmax							
Type	R/W							
Default	0x20							

Register Field	Bit	Description
Reserved	[15:12]	
bhhmax	[11:0]	IR Bit H H Maximum Count 0: Not valid 1: 1 count 2: 2 count

6.4.9 IR Bit “H” LMin Register (BHLmin: 0x0040)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					bhlmin		
Type	RO					R/W		
Default	0x0					0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	bhlmin							
Type	R/W							
Default	0x0C							

Register Field	Bit	Description
Reserved	[15:12]	
bhlmin	[11:0]	IR Bit H L Minimum Count 0: Not valid 1: 1 count 2: 2 count

6.4.10 IR Bit “H” LMax Register (BHLmax: 0x0042)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						bhlmax	
Type	RO						R/W	
Default	0x0						0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	bhlmax							
Type	R/W							
Default	0x20							

Register Field	Bit	Description
Reserved	[15:12]	
bhlmax	[11:0]	IR Bit H L Maximum Count 0: Not valid 1: 1 count 2: 2 count

6.4.11 IR Bit “L” HMin Register (BLHmin: 0x0044)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						blhmin	
Type	RO						R/W	
Default	0x0						0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	blhmin							
Type	R/W							
Default	0x37							

Register Field	Bit	Description
Reserved	[15:12]	
blhmin	[11:0]	IR Bit L H Minimum Count 0: Not valid 1: 1 count 2: 2 count

6.4.12 IR Bit “L” HMax Register (BLHmax: 0x0046)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						blhmax	
Type	RO						R/W	
Default	0x0						0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	blhmax							
Type	R/W							
Default	0x4B							

Register Field	Bit	Description
Reserved	[15:12]	
blhmax	[11:0]	IR Bit L H Maximum Count 0: Not valid 1: 1 count 2: 2 count

6.4.13 IR Bit “L” LMin Register (BLLmin: 0x0048)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					bllmin		
Type	RO					R/W		
Default	0x0					0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	bllmin							
Type	R/W							
Default	0x0C							

Register Field	Bit	Description
Reserved	[15:12]	
bllmin	[11:0]	IR Bit L L Minimum Count 0: Not valid 1: 1 count 2: 2 count

6.4.14 IR Bit “L” LMax Register (BLLmax: 0x004A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						bllmax	
Type	RO						R/W	
Default	0x0						0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	bllmax							
Type	R/W							
Default	0x20							

Register Field	Bit	Description
Reserved	[15:12]	
bllmax	[11:0]	IR Bit L L Maximum Count 0: Not valid 1: 1 count 2: 2 count

6.4.15 IR “END” HMin Register (EndHmin: 0x004C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						endhmin	
Type	RO						R/W	
Default	0x0						0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	endhmin						R/W	
Type								
Default	0x0C							

Register Field	Bit	Description
Reserved	[15:12]	
endhmin	[11:0]	IR “END” H Minimum Count 0: Not valid 1: 1 count 2: 2 count

6.4.16 IR “END” HMax Register (EndHmax: 0x004E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						endhmax	
Type	RO						R/W	
Default	0x0						0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	endhmax						R/W	
Type								
Default	0x20							

Register Field	Bit	Description
Reserved	[15:12]	
endhmax	[11:0]	IR “END” H Maximum Count 0: Not valid 1: 1 count 2: 2 count

6.4.17 IR Repeat Code LMin Register (RCLmin: 0x0050)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						rclmin	
Type	RO						R/W	
Default	0x0						0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	rclmin							
Type	R/W							
Default	0x4C							

Register Field	Bit	Description
Reserved	[15:12]	
rclmin	[11:0]	IR Repeat Code L Minimum Count 0: Not valid 1: 1 count 2: 2 count

6.4.18 IR Repeat Code LMax Register (RCLmax: 0x0052)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						rclmax	
Type	RO						R/W	
Default	0x0						0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	rclmax							
Type	R/W							
Default	0x60							

Register Field	Bit	Description
Reserved	[15:12]	
rclmax	[11:0]	IR Repeat Code L Maximum Count 0: Not valid 1: 1 count 2: 2 count

6.4.19 IR Control Register (IRCtl: 0x0058)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	ir_ccode							
Type	R/W							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					ir_ccodem	Reserved	
Type	RO					R/W	RO	
Default	0x0					0x0	0x0	

Register Field	Bit	Description
ir_ccode	[15:8]	IR Custom code TC358840/70 collects ir data only if the receive “custom code” match this ir_ccode (ir_ccodem=1'b0)
Reserved	[7:2]	
ir_ccodem	[1]	IR Custom Code Mask 0: Match 1: No Match (mask)
Reserved	[0]	

6.4.20 IR Data Register (IRData: 0x005A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name					ir_rccode			
Type					RO			
Default					0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name					ir_rdata			
Type					RO			
Default					0x0			

Register Field	Bit	Description
ir_rccode	[15:8]	IR Receive custom code data
ir_rdata	[7:0]	IR Receive data

6.4.21 IR CONTROL REGISTER (IR_CONTROL: 0x7082)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						IRInv	Reserved
Type	RO						R/W	RO
Default	0x00						0	0

Register Field	Bit	Default	Description
Reserved	[15:2]	0x0	Reserved
IRInv	1	0x0	IRInv (Option to use inverted or non-inverted polarity) 1: Invert IR Polarity
Reserved	0	0x0	These bits used by I2S Control Register

Note: This register shares the address with the I2S Control Register

6.5 CSI2/DSI-TX0 Registers

When reserved bits are read, the value is 0. Writing Reserved bits are invalid and no affects.

6.5.1 CSI2/DSI-TX0 Control Registers

6.5.1.1 ADDRESS_CONFIG (0x0104)

This register is used only when I2C access is used.

Do not access when CFG_IFSELI2C signal is 0.

field	31								24	23							16
field name	Reserve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

field	15								8	7								0
field name	SubSelR eturnW	Reserve d	Reserve d	Reserve d	Reserve d	SubSel3	SubSel2	SubSel1	Reserve d	MainSel								
field access	W	----	----	----	----	W	W	W	----	----	----	----	----	----	----	----	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	

Bit [31:16]: Reserved

Bit [15]: SubSelReturnW. Return selection from Sub Slave Device to Main Slave Device.

When MainSel bit is 0, this bit is valid.

This bit cannot be read as 1 after writing 1 to this bit by I2C access.

This bit can be read as 0 always by I2C access.

When MainSel bit is 1, writing to this bit is invalid and read data is always 0.

- 1:
When this device is a selected Sub Slave Device, by writing this bit to High, the I2C sub slave selection is returned to Main Slave Device. In another words, when 1 is set, SUBSELReturnW signal is set to High.
Writing 1 is automatically cleared when Main Slave Device receives SUBSELReturnW signal and Main Slave Device de-asserts SUBSELR signal.
- 0:
Writing 0 is no affect.

Bit [14:11]: Reserved

Bit [10:8]: SubSel [2:0]: I2C Sub Slave Device Selection.

This setting is valid when CFGIFSEL signal is '1' and CFGI2CDefSLMAIN signal is High.

- 000:
Reserved. When CFGI2CDefSLMAIN is High, keep '000'. When CFGI2CDefSLMAIN is Low, change the setting to either of '001', '010', or '100'.

001:
Sub Slave Device 1 is selected.

010:
Sub Slave Device 2 is selected.

100:
Sub Slave Device 3 is selected.

011:	Reserved. Do not set this value.
101:	Reserved. Do not set this value.
111:	Reserved. Do not set this value.
Bit [7:1]:	Reserved
Bit [0]:	MainSel
	This register shows the value from CFGI2CDefSLMAIN input signal.
1:	CFGI2CDefSLMAIN is High.
0:	CFGI2CDefSLMAIN is Low.

6.5.1.2 CDSITX_CLKEN (0x0108)

Field	31								24	23							16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	Reserve d	CDSITXEn															
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit [31:1]: Reserved

Bit [0]: CDSITXEn: CDSITX Enable.

0: The clocks are gated and not provided inside of CDSITX except for [[CDSITX_CLKEN \(0x0108\)](#)] register and [[ADDRESS_CONFIG \(0x0104\)](#)]. AddrConf [1:0] register bits setting for power saving.

1: The clocks are not clock gated.

6.5.1.3 CDSITX_CLKSEL (0x010C)

Field	31								24	23							16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	Reserve d	Reserve d	Reserve d	Reserve d	PPI SYS DTC IkSe I1	PPI SYS DTC IkSe I0	PPI SYS CLC IkSe I1	PPI SYS CLC IkSe I0	Reserve d	PPI HsT xClk En							
field access	-----	-----	-----	-----	R/W	R/W	R/W	R/W	-----	-----	-----	-----	-----	-----	-----	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:12]: Reserved

Bit [11:10] PPISYSDTClkSel [1:0] Clock Selection SYSDTClk clock for PPI block.
PPI High Speed Data Receive Interface for CDSI shall use the same selected clock.
Change these bits while PPIHsTxClkEn is Low.

- 00: HSCKBY8 clock is set for HSTX clock in D-PHY PPI block.
- 01: HSCKBY4 clock is set for HSTX clock in D-PHY PPI block.
- 10: HSCKBY2 clock is set for HSTX clock in D-PHY PPI block.
- 11: Reserved. Do not set.

Bit [9:8] PPISYSCLClkSel [1:0] Clock Selection SYSCLClk clock for PPI block.
PPI High Speed Data Receive Interface for CDSI shall use the same selected clock.
Change these bits while PPIHsTxClkEn is Low.

- 00: HSCKBY8 clock is set for HSTX clock in D-PHY PPI block.
- 01: HSCKBY4 clock is set for HSTX clock in D-PHY PPI block.
- 10: HSCKBY2 clock is set for HSTX clock in D-PHY PPI block.
- 11: Reserved. Do not set.

Bit [7:1]: Reserved

Bit [0] PPIHsTxClkEn: Clock Enable signal to provide the selected HSTX clock to D-PHY PPI block.
0: Clock is gated and clock is not provided.
1: Clock is not gated and clock is provided.

6.5.1.4 MODE_CONFIG (0x0110)

Field	31								24	23							16
field name	Res erve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	Res erve d	Ind Mod e	DTV ALI D_P OL SW	HSY NC POL SW	VSY NC POL SW	CSI2 Mod e											
field access	----	----	----	----	----	----	----	----	----	----	----	R/W	R/W	R/W	R/W	R/W	0
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit [31:5]: Reserved

Bit[4]: IndMode (To select LP or HS transmission mode for Sync Independent Data)

This is invalid if CDSITX IP is used for CSI-2. In case of CSI-2, Sync independent data will always be transmitted in HS mode only.

- 0: Sync independent data transmitted in HS mode.
- 1: Sync independent data transmitted in LP mode.

Bit[3]: DTVALID_POL_SW (PIC_SYN_DVALID_A Polarity Switch)

This is invalid if CDSITX IP is used for CSI-2

- 0: Data Valid Active High Polarity.
- 1: Data Valid Active Low Polarity.

Bit[2]: HSYNC_POL_SW (PIC_SYN_LINE_A Polarity Switch)

This is invalid if CDSITX IP is used for CSI-2

- 0: HSync Active Low Polarity.
- 1: HSync Active High Polarity.

Bit[1]: VSYNC_POL_SW (PIC_COM_FRAME_A Polarity Switch)

This is invalid if CDSITX IP is used for CSI-2

- 0: VSync Active Low Polarity.
- 1: VSync Active High Polarity.

Bit [0]: CSI2Mode: CSI-2 Mode Selection.

Unselected function shall be disabled and clock shall not be provided to the modules to support only unselected function. The registers which support unselected function shall be able to be accessed with read or write but the write access is invalid and read data shall be default value.

- 0: CDSI works as DSI TX.

When FORCE_CSI2_MODE signal is High, this register bit is invalid.
1: CDSI works as CSI-2 TX.

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6.5.1.5 CDSITX_SYSTEM_INIT (0x0114)

Field	31								24	23							16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	Reserve d	SysInit															
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:1]: Reserved

Bit [0]: SysInit: CDSI System Initialization.

When this bit is read, the value is 0.

0: No affection for write.

1: CDSI System is initialized.

This bit can be asserted only after contention detection or timeout is detected in order to initialize CDSI internal states. The registers are not intentionally initialized but Current Status Registers may be changed by the initialization.

6.5.1.6 LANE_ENABLE (0x0118)

Field	31								24	23							16
field name	Reserve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	Reserve d	CLaneEn	Reserve d	DTLaneEn2	DTLaneEn1	DTLaneEn0											
field access	----	----	----	----	----	----	----	----	----	----	----	----	R/W	----	R/W	R/W	R/W
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit [31:5]: Reserved

Bit [4]: CLaneEn: Clock Lane Enable

In order to transmit HSTX data, Clock Lane shall be enabled.

0: Lane operation disabled (default). Line is allowed at high impedance.

1: Lane operation enabled

Bit [2:0] DTLaneEn: Data Lane Enable

In order to transmit data, at least Data Lane 0 shall be enabled.

000: All data lane is disabled.

001: Data Lane 0 is enabled.

010: Data Lane 0 and 1 are enabled.

011: Data Lane 0, 1 and 2 are enabled.

100: Data Lane 0, 1, 2 and 3 are enabled.

101: Reserved. Do not set.

110: Reserved. Do not set.

111: Reserved. Do not set.

6.5.1.7 CDSITX_START (0x011C)

Field	31								24	23							16
field name	Reserve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	Reserve d	CDSITXStart															
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	R/W
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit [31:1]: Reserved

Bit [0]: CDSITXStart: This bit is used to enable CDSITX for data transmission. This bit is output to STARTPPI signal. Application shall configure this bit only when CDSITX is in idle mode. CDSITX should discard transmit or received data if this bit is set to zero.

0: CDSITX is stopped.

1: CDSITX is started for data transmission after line initialization is done.

6.5.1.8 LINE_INIT_COUNT (0x0120)

Field	31								24	23							16
field name	Reserve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	LIN EINI TCN T15	LIN EINI TCN T14	LIN EINI TCN T13	LIN EINI TCN T12	LIN EINI TCN T11	LIN EINI TCN T10	LIN EINI TCN T9	LIN EINI TCN T8	LIN EINI TCN T7	LIN EINI TCN T6	LIN EINI TCN T5	LIN EINI TCN T4	LIN EINI TCN T3	LIN EINI TCN T2	LIN EINI TCN T1	LIN EINI TCN T0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit [31:4]: Reserved

Bit [15:0]: LINEINITCNT: Line Initialization Wait Counter.
This counter is used for line initialization.
The value is set in LINEINITCOUNT signal. MIPI specification requires that slave device needs to observe LP-11 for 100 us and ignore the received data before the period at initialization time. The count value depends on SYSINITClk and the value needs to be set to achieve more than 100 us. The counter starts after the PPIStart bit of the CDSITX_START register is set. The Master device needs to output LP-11 for 100 us in order for the slave device to observe LP-11 for the period.

6.5.1.9 HSTX_TO_COUNT (0x0124)

This register is invalid if CDSITX is used for CSI-2.

Field	31							24	23								16
field name	HST oCn t31	HST oCn t30	HST oCn t29	HST oCn t28	HST oCn t27	HST oCn t26	HST oCn t25	HST oCn t24	HST oCn t23	HST oCn t22	HST oCn t21	HST oCn t20	HST oCn t19	HST oCn t18	HST oCn t17	HST oCn t16	
field access	R/W																
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Field	15							8	7								0
field name	HST oCn t15	HST oCn t14	HST oCn t13	HST oCn t12	HST oCn t11	HST oCn t10	HST oCn t9	HST oCn t8	HST oCn t7	HST oCn t6	HST oCn t5	HST oCn t4	HST oCn t3	HST oCn t2	HST oCn t1	HST oCn t0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Bit [31:0]: HSToCnt: Time Out counter for High Speed Transmission.
This counter is counted by TxByteClkHs. Set the counter before PPIStart.
This timer is used to monitor the TX on the length of HS transmission

6.5.1.10 FUNC_ENABLE (0x0128)

Field	31							24	23								16
field name	Deb ugMdEn	Res erved	InitInt_E n	App Side Errl nt_E n	DsiP rTol nt_E n	Dsir xErr Int_E n	DsiL ptxl nt_E n	Dsir xTrigInt_E n	DSI RxS tate lnt_E n								
field access	R/W	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Res erved	PRE SP_TO_E n	PR_TO_E n	TA_TO_E n	LRX_H_TO_E n	HST_X_T_O_E n	IndT_O_E n	Ind Mod eSel	VFH SYN CM ASK_E n	Res erved	VHD elay En						
field access	-----	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-----	-----	-----	-----	-----	-----	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31]: DebugMdEn: Debug Mode Enable.

Only developers can set the bit to be enabled. This bit selects enable or disable of the debug function including synchronizers. The clock shall not be provided when disabled. The debug function is defined in [**CDSI_DEBUG1 (0x02C0)**], [**CDSI_DEBUG2 (0x02C4)**], [**PPI_DEBUG1 (0x02C8)**], and [**PPI_DEBUG2 (0x02CC)**]. This is invalid if CDSITX IP is used for CSI-2.

0: Debug Mode is disabled.

1: Debug Mode is enabled.

Bit [30:23]: Reserved

Bit [22]: InitInt_E n

This bit selects enable or disable of INIT interrupt. When related interrupt mask bit is changed dynamically during working, the mask bit shall be changed while this Enable bit is set to low.

Bit [21]: AppSideErrInt_E n: Application Side Error Interrupt Enable.

This bit selects enable or disable of Application Error Interrupt.

When related interrupt mask bit is changed dynamically during working, the mask bit shall be changed while this Enable bit is set to low.

Bit [20]: DsiPrToInt_E n: DSI PRTO Interrupt Enable.

This bit selects enable or disable of DSI PRTO Interrupt.

When related interrupt mask bit is changed dynamically during working, the mask bit shall be changed while this Enable bit is set to low.

Bit [19]: DsirxErrInt_E n: DSI_RXERR Interrupt Enable

This bit selects enable or disable of DSI_RXERR Interrupt.

When related interrupt mask bit is changed dynamically during working, the mask bit shall be changed while this Enable bit is set to low.

Bit [18]: DsiLptxInt_En: DSI_LPTX Interrupt Enable

This bit selects enable or disable of DSI_LPTX Interrupt. This bit should be set to 1 while transmitting LPTX Data through LPTX register interface.

When related interrupt mask bit is changed dynamically during working, the mask bit shall be changed while this Enable bit is set to low.

Bit [17]: DsirxTrigInt_En: DSI_RXTRIG Interrupt Enable

This bit selects enable or disable of DSI_RXTRIG Interrupt.

When related interrupt mask bit is changed dynamically during working, the mask bit shall be changed while this Enable bit is set to low.

Bit [16]: DsiRxStateInt_En: DSI_RX_STATE Interrupt Enable.

This bit selects enable or disable of DSI_RX_STATE Interrupt.

When related interrupt mask bit is changed dynamically during working, the mask bit shall be changed while this Enable bit is set to low.

Bit[15]: Reserved.

Bit[14]: PRESP_TO_En. This is invalid if CDSITX IP is used for CSI-2.

- 0: Disable the PRESP_TO timer.
- 1: Enable the PRESP_TO timer.

Bit[13]: PR_TO_En. This is invalid if CDSITX IP is used for CSI-2.

- 0: Disables the PR_TO timer
- 1: Enables the PR_TO timer

Bit[12] TA_TO_En. This is invalid if CDSITX IP is used for CSI-2.

- 0: Disables the TA_TO timer
- 1: Enables the TA_TO timer

Bit[11] LRX-H_TO_En. This is invalid if CDSITX IP is used for CSI-2.

- 0: Disables the LRX-H_TO timer
- 1: Enables the LRX-H_TO timer

Bit[10] HSTX_TO_En. This is invalid if CDSITX IP is used for CSI-2.

- 0: Disables the HSTX_TO timer
- 1: Enables the HSTX_TO timer

Bit [9]: IndTO_En: Sync Independent Time Out Enable

- 0: Disable the IND_TO timer
- 1: Enable the IND_TO timer

Bit[8] : IndModeSel (To select between input port or register bit)

This bit is invalid if CDSITX IP is used for CSI-2.

- 0: “IND_LPMODE_A” input port will be used to select between LP or HS mode transmission.
- 1: “IndMode” register bit will be used to select between LP or HS mode transmission.

Bit[7]: VFHSYNCMASK_En. Enable VFHSYNCMASK feature. This is invalid if CDSITX IP is used for CSI-2.
0: VFHSYNCMASK feature is not enabled.
1: VFHSYNCMASK feature is enabled. When current line counter is equal or greater than VHMask_lcnt in DSI_VFHSYNCMASK register, all HSYNC packets will not be transmitted.

Bit[6:1]: Reserved
Bit [0]: VHDelayEn: Enable the APF_VDELAYCNT (0x0170) and APF_HDELAYCNT (0x0174) registers
Vertical and Horizontal DELAY Counts can be selected from APF_VDELAYCNT (0x0170) and APF_HDELAYCNT (0x0174) registers or from input ports.
0: VHDELAY Counts are from port inputs.
1: VHDELAY Counts are from registers.

6.5.1.11 DSI_LPTX_MODE (0x012C)

Field	31								24	23							16
field name	Reserve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	LPT_XTR_ANS_MIT_LIN_ENU_M12	LPT_XTR_ANS_MIT_LIN_ENU_M11	LPT_XTR_ANS_MIT_LIN_ENU_M10	LPT_XTR_ANS_MIT_LIN_ENU_M9	LPT_XTR_ANS_MIT_LIN_ENU_M8	LPT_XTR_ANS_MIT_LIN_ENU_M7	LPT_XTR_ANS_MIT_LIN_ENU_M6	LPT_XTR_ANS_MIT_LIN_ENU_M5	LPT_XTR_ANS_MIT_LIN_ENU_M4	LPT_XTR_ANS_MIT_LIN_ENU_M3	LPT_XTR_ANS_MIT_LIN_ENU_M2	LPT_XTR_ANS_MIT_LIN_ENU_M1	LPT_XTR_ANS_MIT_LIN_ENU_M0	LPT_X_time1	LPT_X_time0	Fro mRe g	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit[31:3] Reserved

Bit[15:3]: LPTXTRANSMITLINENUM

Line number for schedule the LP packet to be sent through register interface

Bit[2:1]: LPTX_time [1:0]: period time to transmit LPTX packet which generated by register.

00: LPTX packet will be transmitted during VFP (Vertical Front Porch).

01: LPTX packet will be transmitted during the line number equals to LPTXTRANSMITLINENUM [12:0] input.

10: LPTX packet can be transmitted as soon as possible at any non-image period.

11: Reserved.

Bit [0]: FromReg: From Register.

This bit indicate if the LPTX command can be from Register or Input

0: LPTX command is from Input.

1: LPTX command is from DSI LPTX Registers.

6.5.1.12 DSI_TATO_COUNT (0x0130)

This register is invalid if CDSITX is used for CSI-2.

Field	31							24	23								16
field name	TaTo Cnt3 1	TaTo Cnt3 0	TaTo Cnt2 9	TaTo Cnt2 8	TaTo Cnt2 7	TaTo Cnt2 6	TaTo Cnt2 5	TaTo Cnt2 4	TaTo Cnt2 3	TaTo Cnt2 2	TaTo Cnt2 1	TaTo Cnt2 0	TaTo Cnt1 9	TaTo Cnt1 8	TaTo Cnt1 7	TaTo Cnt1 6	
field access	R/W																
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Field	15							8	7								0
field name	TaTo Cnt1 5	TaTo Cnt1 4	TaTo Cnt1 3	TaTo Cnt1 2	TaTo Cnt1 1	TaTo Cnt1 0	TaTo Cnt9	TaTo Cnt8	TaTo Cnt7	TaTo Cnt6	TaTo Cnt5	TaTo Cnt4	TaTo Cnt3	TaTo Cnt2	TaTo Cnt1	TaTo Cnt0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Bit [31:0]: TaToCnt: Counter value for Turnaround Acknowledge time out

This counter is counted by SYSINITClk

Set the counter before CDSITX starts.

6.5.1.13 DS1_PRESP_BTA_COUNT (0x0134)

Field	31							24	23								16
field name	PRE SPB TAC nt31	PRE SPB TAC nt30	PRE SPB TAC nt29	PRE SPB TAC nt28	PRE SPB TAC nt27	PRE SPB TAC nt26	PRE SPB TAC nt25	PRE SPB TAC nt24	PRE SPB TAC nt23	PRE SPB TAC nt22	PRE SPB TAC nt21	PRE SPB TAC nt20	PRE SPB TAC nt19	PRE SPB TAC nt18	PRE SPB TAC nt17	PRE SPB TAC nt16	
field access	R/W																
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Field	15							8	7								0
field name	PRE SPB TAC nt15	PRE SPB TAC nt14	PRE SPB TAC nt13	PRE SPB TAC nt12	PRE SPB TAC nt11	PRE SPB TAC nt10	PRE SPB TAC nt9	PRE SPB TAC nt8	PRE SPB TAC nt7	PRE SPB TAC nt6	PRE SPB TAC nt5	PRE SPB TAC nt4	PRE SPB TAC nt3	PRE SPB TAC nt2	PRE SPB TAC nt1	PRE SPB TAC nt0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Bit [31:0]: PRESPBTACnt: Counter value for Peripheral Response time out for Bus Turn Around request.
 This counter is counted by SYSINITClk.
 Set the counter before CDSITX starts.

6.5.1.14 DS1_PRESP_LPR_COUNT (0x0138)

Field	31							24	23								16
field name	PRE SPL PRC nt31	PRE SPL PRC nt30	PRE SPL PRC nt29	PRE SPL PRC nt28	PRE SPL PRC nt27	PRE SPL PRC nt26	PRE SPL PRC nt25	PRE SPL PRC nt24	PRE SPL PRC nt23	PRE SPL PRC nt22	PRE SPL PRC nt21	PRE SPL PRC nt20	PRE SPL PRC nt19	PRE SPL PRC nt18	PRE SPL PRC nt17	PRE SPL PRC nt16	
field access	R/W																
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Field	15							8	7								0
field name	PRE SPL PRC nt15	PRE SPL PRC nt14	PRE SPL PRC nt13	PRE SPL PRC nt12	PRE SPL PRC nt11	PRE SPL PRC nt10	PRE SPL PRC nt9	PRE SPL PRC nt8	PRE SPL PRC nt7	PRE SPL PRC nt6	PRE SPL PRC nt5	PRE SPL PRC nt4	PRE SPL PRC nt3	PRE SPL PRC nt2	PRE SPL PRC nt1	PRE SPL PRC nt0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Bit [31:0]: PRESPLPRCn_t: Counter value for Peripheral Response time out for LPDT read request.
This counter is counted by SYSINITClk
Set the counter before CDSITX starts.

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6.5.1.15 DS1_PRESP_LPW_COUNT (0x013C)

Field	31							24	23								16
field name	PRE SPL PW Cnt3 1	PRE SPL PW Cnt3 0	PRE SPL PW Cnt2 9	PRE SPL PW Cnt2 8	PRE SPL PW Cnt2 7	PRE SPL PW Cnt2 6	PRE SPL PW Cnt2 5	PRE SPL PW Cnt2 4	PRE SPL PW Cnt2 3	PRE SPL PW Cnt2 2	PRE SPL PW Cnt2 1	PRE SPL PW Cnt2 0	PRE SPL PW Cnt1 9	PRE SPL PW Cnt1 8	PRE SPL PW Cnt1 7	PRE SPL PW Cnt1 6	
field access	R/W																
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Field	15							8	7								0
field name	PRE SPL PW Cnt1 5	PRE SPL PW Cnt1 4	PRE SPL PW Cnt1 3	PRE SPL PW Cnt1 2	PRE SPL PW Cnt1 1	PRE SPL PW Cnt1 0	PRE SPL PW Cnt9	PRE SPL PW Cnt8	PRE SPL PW Cnt7	PRE SPL PW Cnt6	PRE SPL PW Cnt5	PRE SPL PW Cnt4	PRE SPL PW Cnt3	PRE SPL PW Cnt2	PRE SPL PW Cnt1	PRE SPL PW Cnt0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Bit [31:0]: PRESPLPWCnt: Counter value for Peripheral Response time out for LPDT write request.

This counter is counted by SYSINITClk.

Set the counter before CDSITX starts.

6.5.1.16 DS1_PRESP_HSR_COUNT (0x0140)

Field	31							24	23								16
field name	PRE SPH SRC nt31	PRE SPH SRC nt30	PRE SPH SRC nt29	PRE SPH SRC nt28	PRE SPH SRC nt27	PRE SPH SRC nt26	PRE SPH SRC nt25	PRE SPH SRC nt24	PRE SPH SRC nt23	PRE SPH SRC nt22	PRE SPH SRC nt21	PRE SPH SRC nt20	PRE SPH SRC nt19	PRE SPH SRC nt18	PRE SPH SRC nt17	PRE SPH SRC nt16	
field access	R/W																
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Field	15							8	7								0
field name	PRE SPH SRC nt15	PRE SPH SRC nt14	PRE SPH SRC nt13	PRE SPH SRC nt12	PRE SPH SRC nt11	PRE SPH SRC nt10	PRE SPH SRC nt9	PRE SPH SRC nt8	PRE SPH SRC nt7	PRE SPH SRC nt6	PRE SPH SRC nt5	PRE SPH SRC nt4	PRE SPH SRC nt3	PRE SPH SRC nt2	PRE SPH SRC nt1	PRE SPH SRC nt0	

field access	R/W															
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit [31:0]: PRESPHSRCnt: Counter value for Peripheral Response time out for HS Read request.
This counter is counted by SYSINITClk. Set the counter before CDSITX starts.

DRAFT

6.5.1.17 DS1_PRESP_HSW_COUNT (0x0144)

Field	31							24	23								16
field name	PRE SPH SW Cnt 31	PRE SPH SW Cnt 30	PRE SPH SW Cnt 29	PRE SPH SW Cnt 28	PRE SPH SW Cnt 27	PRE SPH SW Cnt 26	PRE SPH SW Cnt 25	PRE SPH SW Cnt 24	PRE SPH SW Cnt 23	PRE SPH SWC nt22	PRES PHSW Cnt21	PRE SPH SWC nt20	PRE SPH SW Cnt 19	PRE SPH SW Cnt 18	PRE SPH SW Cnt 17	PRE SPH SW Cnt 16	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W									
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Field	15							8	7								0
field name	PRE SPH SW Cnt1 5	PRE SPH SW Cnt1 4	PRE SPH SW Cnt1 3	PRE SPH SW Cnt1 2	PRE SPH SW Cnt1 1	PRE SPH SW Cnt1 0	PRE SPH SW Cnt9	PRE SPH SW Cnt8	PRE SPH SW Cnt7	PRE SPH SW Cnt6	PRE SPH SW Cnt5	PRE SPH SW Cnt4	PRE SPH SW Cnt3	PRE SPH SW Cnt2	PRE SPH SW Cnt1	PRE SPH SW Cnt0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Bit [31:0]: PRESPHSWCnt: Counter value for Peripheral Response time out for HS Write request.

This counter is counted by SYSINITClk. Set the counter before CDSITX starts.

6.5.1.18 DS1_PR_TO_COUNT (0x0148)

This register is invalid if CDSITX is used for CSI-2.

Field	31							24	23								16
field name	PRT OCn t31	PRT OCn t30	PRT OCn t29	PRT OCn t28	PRT OCn t27	PRT OCn t26	PRT OCn t25	PRT OCn t24	PRT OCn t23	PRT OCn t22	PRT OCn t21	PRT OCn t20	PRT OCn t19	PRT OCn t18	PRT OCn t17	PRT OCn t16	
field access	R/W																
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Field	15							8	7								0
field name	PRT OCn t15	PRT OCn t14	PRT OCn t13	PRT OCn t12	PRT OCn t11	PRT OCn t10	PRT OCn t9	PRT OCn t8	PRT OCn t7	PRT OCn t6	PRT OCn t5	PRT OCn t4	PRT OCn t3	PRT OCn t2	PRT OCn t1	PRT OCn t0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Bit [31:0]: PRTOCnt: Counter value for Peripheral Reset time out.

This counter is counted by SYSINITClk. Set the counter before CDSITX starts.

This counter starts counting automatically upon receiving Reset trigger from either LPTX I/F or Sync independent I/F.

In order to enable this function, **FUNC_ENABLE (0x0128)**.DsiPrToInt_En bit needs to be set before transmitting Reset trigger. CDSITX sets **DSI_PRTO_INT_STAT (0x0208)**.PrTo bit when this counter is expired. It is application layers responsibility to not to transmit any packets during CDSITX is counting PR_TO.

6.5.1.19 DSI_LRX-H_TO_COUNT (0x014C)

This register is invalid if CDSITX is used for CSI-2.

Field	31							24	23							16
field name	LRX - HTO Cnt3 1	LRX - HTO Cnt3 0	LRX - HTO Cnt2 9	LRX - HTO Cnt2 8	LRX - HTO Cnt2 7	LRX - HTO Cnt2 6	LRX - HTO Cnt2 5	LRX - HTO Cnt2 4	LRX - HTO Cnt2 3	LRX - HTO Cnt2 2	LRX - HTO Cnt2 1	LRX - HTO Cnt2 0	LRX - HTO Cnt1 9	LRX - HTO Cnt1 8	LRX - HTO Cnt1 7	LRX - HTO Cnt1 6
field access	R/W															
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field	15							8	7							0
field name	LRX - HTO Cnt1 5	LRX - HTO Cnt1 4	LRX - HTO Cnt1 3	LRX - HTO Cnt1 2	LRX - HTO Cnt1 1	LRX - HTO Cnt1 0	LRX - HTO Cnt9	LRX - HTO Cnt8	LRX - HTO Cnt7	LRX - HTO Cnt6	LRX - HTO Cnt5	LRX - HTO Cnt4	LRX - HTO Cnt3	LRX - HTO Cnt2	LRX - HTO Cnt1	LRX - HTO Cnt0
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit [31:0]: LRX-HTOCnt: Counter value for LP-RX Timeout at the Host side.

This counter is counted by SYSINITClk Set the counter before CDSITX starts.

6.5.1.20 FUNC_MODE (0x0150)

Field	31							24	23								16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	CLForceTxStopModeEn	CntAutoTxMd	ECCDis	Reserve d	CrcDis	HsCKMd	Reserve d	Reserve d	Reserve d	Reserve d	EoTpEn					
field access	-----	-----	-----	-----	-----	R/W	R/W	-----	R/W	R/W	-----	-----	-----	-----	-----	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:10]: Reserved

Bit [10] CLForceTxStopModeEn

0: Clock Lanes will not be forced to STOP state when ForceTxStopmode signal is asserted internally

1: Clock Lanes will be forced to STOP state when ForceTxStopmode signal is asserted internally.

Bit [9] CntAutoTxMd

0: When Contention is detected, the mode is automatically changed from LPTX to stop state (LP-11). The Contention Error flag will be generated in this mode.

1: When Contention is detected, the mode is not automatically changed from LPTX to stop state (LP-11). This means the CDSITX continues LPTX transmission and ignores contention. The Contention Error flag is generated in this mode.

Bit [8] EccDis : ECC Disable

This bit sets operation for when there are multiple-bit ECC errors in the received data.

If multiple-bit ECC errors are detected in received packet, the ECC Error multi bit (bit 9) bit of the DSI_RXERR register is asserted to “1” regardless of this bit’s setting.

In the case of ECC single-bit errors, the setting of this bit has no effect on the operation. Single-bit errors can be corrected, so the corrected data can be stored in the Receive FIFO regardless of this bit’s setting. At this time, the ECC Error single bit (bit 8) bit of the DSI_RXERR is asserted to “1”

0: If there are multiple-bit ECC errors in the received data, subsequent processes including the fetching of data from the peripheral interface are terminated and wait for the LP Stop state.

Loading to the Receive FIFO of the corresponding packets is not performed.

1: Even if multiple-bit ECC errors are detected in the received data, subsequent processes including the fetching of data from the peripheral interface continue. Either the packet in which multiple bit ECC errors were detected is loaded into the Receive FIFO or the corresponding package waits for a valid Data Type. If the Data Type is invalid, the DSI Data Type no recognized (bit 11) bit of the DSI_RXERR register is set to “1” and the packet is discarded. If a valid Data Type is recognized, the packet is stored in the Receive FIFO. In the case of a long packet, processing continues up to the reception of the data payload.

Bit [7]	Reserved
Bit [6]	CrcDis. CRC Disable checking. Operation for when a CRC error was found in the received data is set. (For long receive packets only)
0:	CRC checking of received long packets is performed. If CRC errors exist in the received data, the CRC Error bit (bit 10) of the DSI_RXERR register is asserted to "1".
1:	Transfers to the Receive FIFO for the received data are performed. CRC checking of received long packets is not performed. Even if there are CRC errors in the received data, no notification is made to the DSI_RXERR register. The CRC errors are ignored and transfers to the Receive FIFO for the received data are performed.
Bit [5]	HsCkMd: HS Clock Mode
0:	Operation in discontinuous clock mode.
1:	Operation in continuous clock mode.
Bit [0]:	EoTpEn: EoT packet Enable. This bit is valid when [MODE_CONFIG (0x0110)].CSI2Mode is Low. This bit selects if the CDSI generate the EoTp at the end of HS transmission.
0:	CDSI does not generate EoTp at the end of HS transmission and also not expects EoTp at the end of HS reception.
1:	CDSI generates EoTp at the end of HS transmission.

6.5.1.21 DSIRX_VC_ENABLE (0x0154)

Field	31								24	23								16
field name	Reserve d																	
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15								8	7								0
field name	Reserve d	RXV_C3_EN	RXV_C2_EN	RXV_C1_EN	RXV_C0_EN													
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:4]:	Reserved
Bit [3]:	RXVC0_EN: Virtual Channel-3 supported in LPRX path
Bit [2]:	RXVC0_EN: Virtual Channel-2 supported in LPRX path
Bit [1]:	RXVC0_EN: Virtual Channel-1 supported in LPRX path
Bit [0]:	R XVC0_EN: Virtual Channel-0 supported in LPRX path

6.5.1.22 IND_TO_COUNT (0x0158)

Field	31							24	23								16
field name	IND_TO_Cnt3_1	IND_TO_Cnt3_0	IND_TO_Cnt2_9	IND_TO_Cnt2_8	IND_TO_Cnt2_7	IND_TO_Cnt2_6	IND_TO_Cnt2_5	IND_TO_Cnt2_4	IND_TO_Cnt2_3	IND_TO_Cnt2_2	IND_TO_Cnt2_1	IND_TO_Cnt2_0	IND_TO_Cnt1_9	IND_TO_Cnt1_8	IND_TO_Cnt1_7	IND_TO_Cnt1_6	
field access	R/W																
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Field	15							8	7								0
field name	IND_TO_Cnt1_5	IND_TO_Cnt1_4	IND_TO_Cnt1_3	IND_TO_Cnt1_2	IND_TO_Cnt1_1	IND_TO_Cnt1_0	IND_TO_Cnt9	IND_TO_Cnt8	IND_TO_Cnt7	IND_TO_Cnt6	IND_TO_Cnt5	IND_TO_Cnt4	IND_TO_Cnt3	IND_TO_Cnt2	IND_TO_Cnt1	IND_TO_Cnt0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Bit [31:0]: IND_TO_COUNT: Counter value for Sync Independent Interface at the Host side.
 This counter is counted by SYSClk. This counter is used to terminate the Sync Independent Interface transaction if the interface does not provide enough data as per WC. The counter will start counting during Independent Interface transaction and IND_DVALID_A is LOW. It will reset when IND_DVALID_A is HIGH.

6.5.1.23 INIT_INT_STAT (0x0160)

The following status bits show the unmasked status regardless the interrupt mask.

Writing 1 to the status bits clears the bit to 0.

Field	31								24	23							16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	Aut oCal Done	HsTxVRegR dy	Line InitD one													
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:3]: Reserved

Bit [2]: AutoCalDone: LPRX Auto Calibration Finish.

This is invalid if CDSITX IP is used for CSI-2

0: Calibration is not completed.

1: Auto calibration completed.

Bit [1]: HsTxVRegRdy: Voltage regulator count done signal when PPI_HSTXVREGCNT is counted.

0: Voltage regulator count not done.

1: Voltage regulator count done.

Bit [0]: LineInitDone: Line Initialization Done.

0: Line is not initialized.

1: Line is initialized.

There is restriction about status bits. TBD

6.5.1.24 INIT_INT_MASK (0x0164)

Field	31								24	23							16
field name	Res erve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	Res erve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	R/W	R/W
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit [31:3]: Reserved

Bit [2]: MaskAutoCalDone: LPRX Auto Calibration Finish.

Please set to High if CDSITX IP is used for CSI-2.

0: No Mask.

1: Mask.

Bit [1]: Mask_HsTxVRegRdy: Voltage regulator count done signal when PPI_HSTXVREGCNT is counted.

0: No Mask

1: Mask.

Bit [0]: Mask_LineInitDone: Line Initialization Done.

0: No Mask

1: Mask.

6.5.1.25 DSI_HSYNC_STOP_COUNT (0x0168)

This register is invalid if CDSITX is used for CSI-2.

Field	31							24	23								16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	HSync_nc_Cnt15	HSync_nc_Cnt14	HSync_nc_Cnt13	HSync_nc_Cnt12	HSync_nc_Cnt11	HSync_nc_Cnt10	HSync_nc_Cnt9	HSync_nc_Cnt8	HSync_nc_Cnt7	HSync_nc_Cnt6	HSync_nc_Cnt5	HSync_nc_Cnt4	HSync_nc_Cnt3	HSync_nc_Cnt2	HSync_nc_Cnt1	HSync_nc_Cnt0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:16]: Reserved.

Bit [15:0]: HSync Counter value is used for detecting stop condition when DSITX_MODE (0x017C).DSI_Stop_Mode = 2'b01. Please refer section エラー! 参照元が見つかりません。 for more detail.

6.5.2 APF Configuration Registers

6.5.2.1 APF_VDELAYCNT (0x0170)

This register specifies the delay from VSYNC start and end to transmit the Sync packet from APF to CDSI layer in case of CSI2. LSB 18 bits of this register are used to configure VHDELAY value in case of DSI mode. VHDELAY value is used to delay the transmission of complete Line data (Sync + Video Data). Please refer section エラー! 参照元が見つかりません。 for more information about VHDELAY setting.

Field	31							24	23								16
field name	VDL_EN_D_C_NT1_5	VDL_EN_D_C_NT1_4	VDL_EN_D_C_NT1_3	VDL_EN_D_C_NT1_2	VDL_EN_D_C_NT1_1	VDL_EN_D_C_NT1_0	VDL_EN_D_C_NT9	VDL_EN_D_C_NT8	VDL_EN_D_C_NT7	VDL_EN_D_C_NT6	VDL_EN_D_C_NT5	VDL_EN_D_C_NT4	VDL_EN_D_C_NT3	VDL_EN_D_C_NT2	VDL_EN_D_C_NT1	VDL_EN_D_C_NT0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	

Field	15							8	7								0
field name	VDL_ST_R_C_NT1_5	VDL_ST_R_C_NT1_4	VDL_ST_R_C_NT1_3	VDL_ST_R_C_NT1_2	VDL_ST_R_C_NT1_1	VDL_ST_R_C_NT1_0	VDL_ST_R_C_NT9	VDL_ST_R_C_NT8	VDL_ST_R_C_NT7	VDL_ST_R_C_NT6	VDL_ST_R_C_NT5	VDL_ST_R_C_NT4	VDL_ST_R_C_NT3	VDL_ST_R_C_NT2	VDL_ST_R_C_NT1	VDL_ST_R_C_NT0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	

Bit [31:16]: VDL_END_CNT[15:0] Vertical Sync End Delay Count in case of CSI2 mode.

Bit [15:0]: VDL_STR_CNT[15:0] Vertical Sync Start Delay Count in case of CSI2 mode.

APF_VDELAYCNT [17:0] is used to program VHDELAY value in case of DSI mode.

6.5.2.2 APF_HDELAYCNT (0x0174)

This register specifies the delay from HSYNC to transmit the Sync packet from APF to CDSI layer. These counters use TxByteClkHS. This register is invalid if CDSITX IP is used for DSI.

Field	31							24	23							16
field name	Reserve d															
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15							8	7								0
field name	HDL_CNT 15	HDL_CNT 14	HDL_CNT 13	HDL_CNT 12	HDL_CNT 11	HDL_CNT 10	HDL_CNT 9	HDL_CNT 8	HDL_CNT 7	HDL_CNT 6	HDL_CNT 5	HDL_CNT 4	HDL_CNT 3	HDL_CNT 2	HDL_CNT 1	HDL_CNT 0	
field access	-----	-----	-----	-----	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	

Bit [31:16]: Reserved

Bit [15:0]: HDL_CNT[15:0] Horizontal Sync Delay Count

6.5.2.3 APF_VC_CONFIG (0x0178)

Field	31								24	23							16
field name	Res erve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	Res erve d	VC _VAL 1	VC _VAL 0	VC _Sel													
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	R/W	R/W	R/W
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit [31:3]: Reserved

Bit [2:1]: VCVal: Virtual Channel number configuration for port A.

Bit [0]: VCSel: Virtual Channel selection from input port or register.

0: Virtual Channel value from input port

1: Virtual Channel value from this register bits [2:1]

6.5.2.4 DSITX_MODE (0x017C)

Field	31							24	23								16
field name	Res erve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Res erve d	Blan kPkt _En	Res erve d	Res erve d	Res erve d	Res erve d	DSI _STO P_M ODE 1	DSI _STO P_M ODE 0	DSI TXM d								
field access	----	----	----	----	----	----	----	R/W	----	----	----	----	R/W	R/W	R/W	0	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:8]: Reserved

Bit [7]: BlankPkt_En; Enable to transmit HSA, HBP as a long blank packet.

In DSI specification, the HSA and HBP can be a long blank packet concatenate with HSS, HSE and video packet in a single HS transmission. The WC of HSA, HBP is from **DSI_HSYNC_WIDTH (0x018C)** and **DSI_HBPR (0x0190)** registers, respectively. It is application layer's responsibility to configure these register for CDSI layer to transmit these packet in single HS period. But there is one exception. If application layer schedules LPTX data transmission in video active region when this bit set to 1, CDSITX shall transmit LPTX data in HBP period and ignores this bit value.

0 : HSA, HBP are in Low Power period. No long blank packet for HSA, HBP

1: This feature is enabled.

Bit [6:3]: Reserved.

Bit [2:1]: DSI Stop Mode Selection bits. Please refer section エラー! 参照元が見つかりません。 for more detail.

00: Based on VSync Fall after PIC_COM_START_A deassertion.

01: Based on Hsync Counter Value.

10: Immediate Stop based on PIC_COM_START_A deassertion.

11: Reserved.

Bit [0]: DSITXMd; DSI Video Transmit mode

0: Pulse mode.

1: Event mode.

6.5.2.5 DSI_HSYNC_WIDTH (0x018C)

This register specifies the horizontal blank width count in term of byte length used for HSA period in pulse mode. In the pulse mode APF will transmit the blank packet with the WC as defined in this register. Refer to Section 8.11 in [MIPI04].

Field	31							24	23								16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	HS_W15	HS_W14	HS_W13	HS_W12	HS_W11	HS_W10	HS_W9	HS_W8	HS_W7	HS_W6	HS_W5	HS_W4	HS_W3	HS_W2	HS_W1	HS_W0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	

Bit [31:16]: Reserved.

Bit [15:0]: This field gives the word count of the blanking packet that may be transmitted during Horizontal Sync width period when DSITX_MODE (0x017C).BlankPkt_En = 1. Alternatively, this field gives the period in DSI byte clocks for which CDSITX is to transition to LP mode when DSITX_MODE (0x017C).BlankPkt_En = 0.

HS_W [15:0] equal to zero is invalid for pulse mode.

6.5.2.6 DSI_HBPR (0x0190)

This register specifies the Horizontal Back Porch width in term of byte length used for HBP period in pulse mode.

Field	31								24	23							16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15								8	7							0
field name	HBP_W1_5	HBP_W1_4	HBP_W1_3	HBP_W1_2	HBP_W1_1	HBP_W1_0	HBP_W9	HBP_W8	HBP_W7	HBP_W6	HBP_W5	HBP_W4	HBP_W3	HBP_W2	HBP_W1	HBP_W0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	

Bit [31:16]: Reserved.

Bit [15:0]: This field gives the word count of the blanking packet that may be transmitted during Horizontal Back Porch period when DSITX_MODE (0x017C).BlankPkt_En = 1. Alternatively, this field gives the period in DSI byte clocks for which CDSITX is to transition to LP mode when DSITX_MODE (0x017C).BlankPkt_En = 0.

6.5.2.7 DSI_VFHSYNCMASK (0x0194)

Field	31								24	23							16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15								8	7							0
field name	VHM ask_lcnt_15	VHM ask_lcnt_14	VHM ask_lcnt_13	VHM ask_lcnt_12	VHM ask_lcnt_11	VHM ask_lcnt_10	VHM ask_lcnt_9	VHM ask_lcnt_8	VHM ask_lcnt_7	VHM ask_lcnt_6	VHM ask_lcnt_5	VHM ask_lcnt_4	VHM ask_lcnt_3	VHM ask_lcnt_2	VHM ask_lcnt_1	VHM ask_lcnt_0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:16]: Reserved

Bit [15:0]: VHMask_lcnt:

This counter is used to mask the HSYNC packet in DSI. CDSITX keeps an internal counter that is reset to 1

when Vsync assertion is detected on the V/H interface and increments by 1 when Hsync assertion is detected asserted. If the current line counter is equal or greater than the VHMask_lcnt then APF will not transmit Horizontal Sync Start/End packets. Note that Vertical Sync Start/End packets are always transmitted.

DRAFT

6.5.3 RX Event Registers

6.5.3.1 DSI_RX_STATE_INT_STAT (0x01A0)

The following status bits show the unmasked status regardless the interrupt enable mask.

Writing 1 to the status bits clears the bit to 0.

Field	31							24	23								16
field name	Reserve d																
Field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	LPR_X_PKT_START	LPR_X_PKT_DONE	LPR_X_THRESH_HIT	DirectionFall	DirectionRise											
field access	----	----	----	----	----	----	----	----	----	----	----	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:4]: Reserved

Bit [4]: LPRX_PKT_START

This is invalid if CDSITX IP is used for CSI-2

- 0: No new packet received or LPRX packet reception not complete
- 1: Indicates start of LPRX packet.

Bit [3]: LPRX_PKT_DONE

This is invalid if CDSITX IP is used for CSI-2

- 0: Not end of packet.
- 1: Indicates end of packet.

Bit [2]: LPRX_THRESH_HIT

This is invalid if CDSITX IP is used for CSI-2

- 0: Data Less than Threshold Count.
- 1: Data equal or greater than threshold Count.

Bit [1]: DirectionFall: Fall edge detection of Direction signal on Data Lane 0 from PPI.

This is invalid if CDSITX IP is used for CSI-2

- 0: No detection.
- 1: Fall edge detection. This means BTA is done from Peripheral to Host.

- Bit [0]: DirectionRise: Rise edge detection of Direction signal on Data Lane 0 from PPI.
This is invalid if CDSITX IP is used for CSI-2
- 0: No detection.
- 1: Rise edge detection. This means BTA is done from Host to Peripheral.

DRAFT

6.5.3.2 DSI_RX_STATE_INT_MASK (0x01A4)

Field	31							24	23								16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	MaskLP RX_PKT_START	MaskLP RX_PKT_DONE	MaskLP RX_THRESH_HIT	MaskDirectionFall	MaskDirectionRise											
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W	R/W	R/W	R/W
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit [31:4]: Reserved

Bit [4]: MaskLPRX_PKT_START

Please set to High if CDSITX IP is used for CSI-2.

- 0: No Mask
- 1: Mask.

Bit [3]: MaskLPRX_PKT_DONE

Please set to High if CDSITX IP is used for CSI-2.

- 0: No Mask
- 1: Mask.

Bit [2]: MaskLPRX_THRESH_HIT

Please set to High if CDSITX IP is used for CSI-2.

- 0: No Mask.
- 1: Mask.

Bit [1]: MaskDirectionFall: Fall edge detection of Direction signal on Data Lane 0 from PPI.

Please set to High if CDSITX IP is used for CSI-2

- 0: No Mask.
- 1: Mask.

Bit [0]: MaskDirectionRise: Rise edge detection of Direction signal on Data Lane 0 from PPI.

Please set to High if CDSITX IP is used for CSI-2

- 0: No Mask.
- 1: Mask.

6.5.3.3 DSI_RXTRIG_INT_STAT (0x01A8)

The following status bits show the unmasked status regardless the interrupt enable mask.

Writing 1 to the status bits clears the bit to 0.

This register is invalid if CDSITX IP is used for CSI-2

Field	31							24	23								16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	L0RxTrigger 3	L0RxTrigger 2	L0RxTrigger 1	L0RxTrigger 0												
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:4]: Reserved

Bit [3]: L0RxTrigger3: Reception of RxTrigger [3] on Data Lane 0.

Bit [2]: L0RxTrigger2: Reception of RxTrigger [2] on Data Lane 0.

Bit [1]: L0RxTrigger1: Reception of RxTrigger [1] on Data Lane 0.

Bit [0]: L0RxTrigger0: Reception of RxTrigger [0] on Data Lane 0.

0: No reception.

1: Reception.

6.5.3.4 DSI_RXTRIG_INT_MASK (0x01AC)

This register is invalid if CDSITX IP is used for CSI-2.

Please set to High if CDSITX IP is used for CSI-2

Field	31							24	23								16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	MaskL0RxTrigger3	MaskL0RxTrigger2	MaskL0RxTrigger1	MaskL0RxTrigger0												
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W	R/W	R/W
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit [31:4]: Reserved

Bit [3]: MaskL0RxTrigger3: Reception of RxTrigger [3] on Data Lane 0.

Bit [2]: MaskL0RxTrigger2: Reception of RxTrigger [2] on Data Lane 0.

Bit [1]: MaskL0RxTrigger1: Reception of RxTrigger [1] on Data Lane 0.

Bit [0]: MaskL0RxTrigger0: Reception of RxTrigger [0] on Data Lane 0.

0: No Mask.

1: Mask.

6.5.3.5 CDSITX_INTERNAL_STAT (0x01B0)

Writing the status bits is invalid and no affect.

Field	31							24	23								16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	APF_Lptx_Stat	APF_VHIF_Ind_Stat	APF_VHIF_Sync_Stat	PPI_RxEsc_Busy	PPI_Init_Busy	PPI_Byt e_Busy	PPI_TxEsc_Busy	PPI_CL_Busy	PPI_DT_Busy	CDS_I_St ate						
field access	-----	-----	-----	-----	-----	-----	R	R	R	R	R	R	R	R	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:9]: Reserved

Bit [9]: APF_Lptx_Stat: APF LPTX Internal state

- 0: All All state in APF LPTX module is idle state at the moment.
1: All state in APF LPTX module is not idle state at the moment.

Bit [8]: APF_VHIF_Ind_Stat: APF VHIF Ind Internal State.

- 0: All state in APF VHIF Ind module is idle state at the moment.
1: All state in APF VHIF Ind module is not idle state at the moment.

Bit [7]: APF_VHIF_Sync_Stat: APF VHIF Sync Internal State.

- 0: All state in APF VHIF Sync module is idle state at the moment.
1: All state in APF VHIF Sync module is not idle state at the moment.

Bit [6]: PPI_RxEsc_Busy: PPI is busy in RxByteClkEsc domain.

- 0: Not busy.
1: Busy.

Bit [5]: PPI_Init_Busy: PPI is busy in SysInitClk domain.

- 0: Not busy.
1: Busy.

Bit [4]: PPI_Byt e_Busy: PPI is busy in TxByteClkHs domain.

- 0: Not busy.

- 1: Busy.
- Bit [3]: PPI_TxEsc_Busy: PPI is busy in TxClkEsc domain.
0: Not busy.
1: Busy.
- Bit [2]: PPI_CL_Busy: PPI is busy in SYSCLClk domain.
0: Not busy.
1: Busy.
- Bit [1]: PPI_DT_Busy: PPI is busy in SYSDTClk domain.
0: Not busy.
1: Busy.
- Bit [0]: CDSI_Stat: CDSI Internal State.
0: All state in CDSI module is idle state at the moment.
1: All state in CDSI module is not idle state at the moment.

6.5.3.6 DSI_ACKERROR (0x01B4)

This register holds the content of Acknowledge packets having a report of the last error received. This register will be cleared when it is read.

Field	31							24	23							16
field name	Reserve d															
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15							8	7								0
field name	Ack Err_repo rt15	Ack Err_repo rt14	Ack Err_repo rt13	Ack Err_repo rt12	Ack Err_repo rt11	Ack Err_repo rt10	Ack Err_repo rt9	Ack Err_repo rt8	Ack Err_repo rt7	Ack Err_repo rt6	Ack Err_repo rt5	Ack Err_repo rt4	Ack Err_repo rt3	Ack Err_repo rt2	Ack Err_repo rt1	Ack Err_repo rt0	
field access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:16]: Reserved

Bit [15:0]: AckErr_report:

The content of the Acknowledge packet with report of the last error received is held. The meaning of these bits are in Table 20 of DSI specification.

6.5.3.7 DSI_RXFIFO (0x01B8)

These register is invalid if CDSITX IP is used for CSI-2.

Field	31							24	23								16
field name	RXD ATA 31	RXD ATA 30	RXD ATA 29	RXD ATA 28	RXD ATA 27	RXD ATA 26	RXD ATA 25	RXD ATA 24	RXD ATA 23	RXD ATA 22	RXD ATA 21	RXD ATA 20	RXD ATA 19	RXD ATA 18	RXD ATA 17	RXD ATA 16	
field access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	RXD ATA 15	RXD ATA 14	RXD ATA 13	RXD ATA 12	RXD ATA 11	RXD ATA 10	RXD ATA 9	RXD ATA 8	RXD ATA 7	RXD ATA 6	RXD ATA 5	RXD ATA 4	RXD ATA 3	RXD ATA 2	RXD ATA 1	RXD ATA 0	
field access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:0]: RXDATA

Data received from the peripheral interface via the DSI link is written to a 32 deep Data FIFO. This register is written with the data in the Data FIFO corresponding to the current read pointer. Reads to this register will increment the Data FIFO read pointer.

6.5.3.8 DSI_RX_HEADER (0x01BC)

These register is invalid if CDSITX IP is used for CSI-2

Field	31							24	23							16
field name	Reserve d	RXV C1	RXV CO	RXD T5	RXD T4	RXD T3	RXD T2	RXD T1	RXD T0							
field access	-----	-----	-----	-----	-----	-----	-----	R	R	R	R	R	R	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7							0
field name	RX WC1 5	RX WC1 4	RX WC1 3	RX WC1 2	RX WC1 1	RX WC1 0	RX WC9	RX WC8	RX WC7	RX WC6	RX WC5	RX WC4	RX WC3	RX WC2	RX WC1	RX WC0
field access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit [31:24] Reserved

Bit [23:22] RXVC: Virtual channel Identifier of received packet

Bit [21:16] RXDT: Data Identifier of received packet

Data Identifier of the data received from the peripheral interface via the DSI link is written to this register.

Bit [15:0]: RXWC: Word count of received packet

Word count of the data received from the peripheral interface via the DSI link is written to this register.

6.5.3.9 DSI_LPRX_THRESH_COUNT (0x01C0)

These register is invalid if CDSITX IP is used for CSI-2.

Field	31							24	23							16
field name	Reserve d															
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7							0
field name	Reserve d	RX_THRESH_CNT_T4	RX_THRESH_CNT_T3	RX_THRESH_CNT_T2	RX_THRESH_CNT_T1	RX_THRESH_CNT_T0										
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W	R/W	R/W	R/W
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit [31:5]: Reserved.

Bit [4:0]: RX_THRESH_CNT. Threshold value to assert LPRX_THRESH_HIT interrupts.

LPRX_THRESH_HIT interrupt is asserted when data in the DSIRX FIFO is greater than or equal to a programmable value in this register.

6.5.3.10 DSI_LPRX_FIFO_LEVEL (0x01C4)

These register is invalid if CDSITX IP is used for CSI-2.

Field	31							24	23							16
field name	Reserve d															
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7							0
field name	Reserve d	RX_FIFO_LVL_EVE_L4	RX_FIFO_LVL_EVE_L3	RX_FIFO_LVL_EVE_L2	RX_FIFO_LVL_EVE_L1	RX_FIFO_LVL_EVE_L0										
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R	R	R	R	R
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit [31:5]: Reserved.

Bit [4:0]: RX_FIFO_LEVEL. RX_FIFO_LEVEL value indicates number of 32-bit data entries in RX FIFO.

6.5.4 Error Experience Registers

6.5.4.1 DSI_PRTO_INT_STAT (0x0208)

The following status bits show the unmasked status regardless the interrupt enable mask.

Writing 1 to the status bits clears the bit to 0.

Field	31							24	23								16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	LRX - H_T o	PRe spT o	PrTo	HsT xTo	TaTo											
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:5] Reserved

Bit [4]: LRX-H_To: LP-RX Host Processor time out

This is invalid if CDSITX IP is used for CSI-2

- 0: No Timeout
- 1: Timeout.

Bit [3]: PRe spT o: Peripheral Response time out.

This is invalid if CDSITX IP is used for CSI-2

- 0: No Timeout
- 1: Timeout.

Bit [2]: PrTo: Peripheral Reset time out.

This is invalid if CDSITX IP is used for CSI-2.

- 0: No Timeout
- 1: Timeout.

Bit [1]: HsTxTo: HSTX time out.

This is invalid if CDSITX IP is used for CSI-2.

- 0: No Timeout
- 1: Timeout.

- Bit [0]: TaTo: Turnaround Acknowledge time out.
 This is invalid if CDSITX IP is used for CSI-2.
 If the BTA sequence is observed not to complete (by the previously-transmitting PHY) within the specified time period, the timer TA_TO expires.
 If the peripheral does not return the BTA response, this timeout is set.
- 0: No Timeout
 1: Timeout.

There is restriction about status bits. TBD

6.5.4.2 DSI_PRTO_INT_MASK (0x020C)

Field	31							24	23								16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Field	15							8	7								0
field name	Reserve d	MaskLRX-H_To	MaskPrTo	MaskPrT	MaskHsTxT	MaskTaT											
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W	R/W	R/W	R/W	
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

- Bit [31:5]: Reserved
 Bit [4]: MaskLRX-H_To: LP-RX Host Processor time out.
 Bit [3]: MaskPrTo: Peripheral response time out.
 Bit [2]: MaskPrTo: Peripheral reset time out.
 Bit [1]: MaskHsTxTo: HSTX time out.
 Bit [0]: MaskTaTo: Turnaround Acknowledge time out.
 Please set to High if CDSITX IP is used for CSI-2
- 0: No Mask.
 1: Mask.

There is restriction. TBD

6.5.4.3 APP_SIDE_ERR_INT_STAT (0x0210)

Writing 1 to the status bits clears the bit to 0.

Field	31							24	23								16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	Ind_Wrng_E n	Line_Buf_Rd_Wrt_Violat ion	Reserve d	ErrRxIfOv f	Reserve d	SynBuf_Ovf_Err	IndBuf_Ovf_Err	LineBuf_Ovf_err	ErrWC	ErrDT						
field access	-----	-----	-----	-----	-----	-----	RW	RW	-----	R/W	-----	RW	RW	RW	RW	RW	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:10]: Reserved

Bit [9]: Ind_Wrng_En: Assertion of incorrect IND_EN

- 0: IND_EN is asserted correctly
- 1: IND_EN is asserted incorrectly

Bit [8]: Line_Buf_Rd_Wrt_Violation: Read and Write happens simultaneously from one of the Line Buffers.

- 0: No Violation
- 1: Line Buffer Read and Write Violation

Bit [7]: Reserved

Bit [6]: ErrRx_fifoOvf: Rx FIFO Overflow.

This is invalid if CDSITX IP is used for CSI-2.

- 0: No Overflow.
- 1: Overflow.

Bit [5]: Reserved

Bit [4]: SyncBuf_Ovf_Err: Sync Packet Gen FIFO Overflow

- 0: No Overflow
- 1: Overflow

Bit [3]: IndBuf_Ovf_Err: Sync Independent FIFO Overflow

0: No Overflow
1: Overflow

Bit [2]: LineBuf_Ovf_Err: Line Buffer FIFO Overflow.

0: No Overflow.
1: Overflow.

Bit [1]: ErrWC. The WC and data valid input is not matched. Either expected data is shorter or longer than WC. This error bit is used for both VHIF or IND IF.

1: Error.
0: No Error.

Bit [0]: ErrDT; Error on Data type input.

1: Data type input is not supported.
0: No error.

6.5.4.4 APP_SIDE_ERR_INT_MASK (0x0214)

Field	31								24	23								16
field name	Reserve d																	
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Field	15							8	7									0
field name	Reserve d	Mask_Ind_Wrng_En	Mask_Line_Buf_Rd_Wrt_Violation	Reserve d	Mask_ErrRxFifoOv	Reserve d	Mask_SyncBuf_Ovf_Err	Mask_IndBuf_Ovf_Err	MaskLineBuf_Ovf_Err	MaskErrWC	MaskErrDT							
field access	-----	-----	-----	-----	-----	-----	R/W	R/W	-----	R/W	-----	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Bit [31:10]:Reserved

Bit [9]: Mask_Ind_Wrng_Err: Sync Independing incorrect assertion of IND_EN

- 1: Mask error on incorrect assertion of IND_EN
- 0: No Mask

Bit [8]: Mask_Line_Buf_Rd_Wrt_Violation: Line Buffer Read/Write Violation

- 1: Mask error on Violation.
- 0: No Mask

Bit [7]: Reserved

Bit [6]: Mask_ErrRxFifoOv: Rx FIFO Overflow

- 1: Mask error on RX FIFO Overflow
- 0: No Mask

Bit [5]: Reserved

Bit [4]: Mask_SyncBuf_Ovf_Err: Sync Packet Gen FIFO Overflow

- 1: Mask error on Sync Packet Gen FIFO Overflow
- 0: No Mask

Bit [3]: MaskIndBuf_Ovf_Err: Sync Independent FIFO Overflow

- 1: Mask error on Sync Independent FIFO Overflow
- 0: No Mask

Bit [2]: MaskLineBuf_Ovf_Err: Line Buffer Overflow.
1: Mask error on Line Buffer Overflow.
0: No mask.
Bit [1]: MaskErrWC.
1: Mask error on WC.
0: No mask.
Bit [0]: MaskErrDT; Mask Error on Data type.
1: Mask error on Data type input.
0: No mask.

DRAFT

6.5.4.5 DSI_RX_ERR_INT_STAT (0x0218)

This register is invalid if CDSITX IP is used for CSI-2.

Writing 1 to the status bits clears the bit to 0.

Field	31							24	23								16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	Reserve d	Err_repo rt13	Err_repo rt12	Err_repo rt11	Err_repo rt10	Err_repo rt9	Err_repo rt8	Err_repo rt7	Err_repo rt6	Reserve d	Err_repo rt4	Err_repo rt3	Reserve d	Reserve d	Reserve d	
field access	-----	-----	RW	RW	RW	RW	RW	RW	RW	RW	-----	RW	RW	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

- Bit [31:14]: Reserved
- Bit [13] Invalid Data Length
- Bit [12] DSI VC ID Invalid
- Bit [11] DSI Data Type not recognized.
- Bit [10] CRC Error (Long packet only).
- Bit [9] ECC Error: Multiple bit.
- Bit [8] ECC Error: Single-bit
- Bit [7] Contention Detection Error
- Bit [6] False Control Error
- Bit [5] Reserved.
- Bit [4] Low Power Transmit Sync Error.
- Bit [3] Escape Mode Entry command error
- Bit [2:0] Reserved.

6.5.4.6 DSI_RX_ERR_INT_MASK (0x021C)

Please set to High if CDSITX IP is used for CSI-2

Field	31							24	23							16
field name	Reserve d															
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Field	15							8	7								0
field name	Reserve d	Reserve d	MskErr_repOrt13	MskErr_repOrt12	MskErr_repOrt11	MskErr_repOrt10	MskErr_repOrt9	MskErr_repOrt8	MskErr_repOrt7	MskErr_repOrt6	Reserve d	MskErr_repOrt4	MskErr_repOrt3	Reserve d	Reserve d	Reserve d	
field access	-----	-----	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-----	R/W	R/W	-----	-----	-----	
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Bit [31:14]: Reserved

Bit [13:3]: Err_report Mask.

- 1: Mask error
- 0: No mask

Bit [13] Invalid Data Length

Bit [12] DSI VC Invalid

Bit [11] DSI Data Type recognition error

Bit [10] CRC Error (Long packet only)

Bit [9] ECC Error: Multiple bit

Bit [8] ECC Error: Single-bit

Bit [7] Contention Detection Error

Bit [6] Faulty Control Error

Bit [5] Reserved.

Bit [4] LP transfer Sync Error

Bit [3] Escape Mode Entry command error

Bit [2:0] Reserved.

6.5.5 DSI LPTX Registers

6.5.5.1 DSI_LPTX_INT_STAT (0x0220)

The following status bits show the unmasked status regardless the interrupt enable mask.

Writing 1 to the status bits clears the bit to 0.

Field	31								24	23									16
field name	Reserve d																		
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7									0
field name	Reserve d	Payl oad 1Do ne	Payl oad 0Do ne	Reserve d	LpTxDo ne														
field access	-----	-----	-----	-----	-----	-----	R/W	R/W	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:10]: Reserved

Bit [9]: Payload1Done: LP Transmit Complete of Payload1.

0: LP data which is stored in [DSI_LPTX_PAYLOAD1 (0x0238)] is not completed yet.

1: LP data which is stored in [DSI_LPTX_PAYLOAD1 (0x0238)] is completed.

Bit [8]: Payload0Done: LP Transmit Complete of Payload0.

0: LP data which is stored in [DSI_LPTX_PAYLOAD0 (0x0234)] is not completed yet.

1: LP data which is stored in [DSI_LPTX_PAYLOAD0 (0x0234)] is completed.

Bit [7:1]: Reserved

Bit [0]: LpTxDone: LP Packet Transmit is completed.

0: LP Transmit is not completed yet.

1: LP Transmit is completed.

6.5.5.2 DSI_LPTX_INT_MASK (0x0224)

Field	31								24	23								16
field name	Reserve d																	
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15								8	7								0
field name	Reserve d	Mas kPa yloa d1D one	Mas kPa yloa d0D one	Reserve d	Mas kLp TxD one													
field access	-----	-----	-----	-----	-----	-----	R/W	R/W	-----	-----	-----	-----	-----	-----	-----	-----	R/W	
reset value	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	

Bit [31:10]: Reserved

Bit [9]: MaskPayload1Done: LP Transmit Complete of Payload1.

Bit [8]: MaskPayload0Done: LP Transmit Complete of Payload0.

0: No Mask.

1: Mask.

Bit [7:1]: Reserved

Bit [0]: MaskLpTxDone: LP Packet Transmit is completed.

0: No Mask.

1: Mask.

6.5.5.3 DSI_LPTX_REQ (0x0228)

If the [DIS_LPTX_MODE] bit [0] is ‘1’ then LPTX Command can be sent from registers in section 6.5.5.4, 6.5.5.5, 6.5.5.6 and 6.5.5.7.

Field	31							24	23								16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	LpTxReq															
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:1]: Reserved

Bit [0]: LpTxReq: LP Transmit Request.

Only write is valid,. After setting ‘1’ this bit becomes ‘0’ when LPTXDONE is received.

0: No affect.

1: Transmit data set by.

6.5.5.4 LPTX_TYPE (0x022C)

Field	31							24	23								16
field name	Reserve d	LPT XTrigSel 4	LPT XTrigSel 3	LPT XTrigSel 2	LPT XTrigSel 1	LPT XTrigSel 0											
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	RsTriggerSel1	RsTriggerSel0	LPDT	Targ et_Lane 2	Targ et_Iane 1	Targ et_Lane 0	LP_Command2	LP_Command1	LP_Command0	Turn Req						
field access	-----	-----	-----	-----	-----	-----	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:21]: Reserved

Bit [20:16]: LPTXTrigSel: LPTxTrigger encoding for CDSI block
These bits are not used for CSI-2. Set to all zero for CSI-2.

“LpTxTrigSel [4:0]” “TxTriggerEsc [3:0] output bit order”

00000	[3]	[2]	[1]	[0]
00001	[3]	[2]	[0]	[1]
00010	[3]	[1]	[2]	[0]
00011	[3]	[1]	[0]	[2]
00100	[3]	[0]	[2]	[1]
00101	[3]	[0]	[1]	[2]
00110	[2]	[3]	[1]	[0]
00111	[2]	[3]	[0]	[1]
01000	[2]	[1]	[3]	[0]
01001	[2]	[1]	[0]	[3]
01010	[2]	[0]	[3]	[1]
01011	[2]	[0]	[1]	[3]
01100	[1]	[3]	[2]	[0]
01101	[1]	[3]	[0]	[2]
01110	[1]	[2]	[3]	[0]
01111	[1]	[2]	[0]	[3]
10000	[1]	[0]	[3]	[2]
10001	[1]	[0]	[2]	[3]
10010	[0]	[3]	[2]	[1]
10011	[0]	[3]	[1]	[2]
10100	[0]	[2]	[3]	[1]
10101	[0]	[2]	[1]	[3]

10110	[0] [1] [3] [2]
10111	[0] [1] [2] [3]

Bit [15:10]: Reserved

Bit [9:8]: RsTrigSel[1:0] : Reset Trigger Select is used to select which Trigger is for Reset Trigger (This is used in CDSI block)

- 00: Trigger0 is a Reset Trigger
- 01: Trigger1 is a Reset Trigger
- 10: Trigger2 is a Reset Trigger
- 11: Trigger3 is a Reset Trigger

Bit [7] : LPDT Low power Data Transmission. This bit is used to indicate low power long/short packet data transmission through LPTX register interface. When TurnReq is High, this field is ignored. The command to disabled lanes is ignored.

Bit [6:4]: Target_Lane[2:0] LP_Command for Enter /Exit ULPS is executed to the following target lanes.
When TurnReq is High, this field is ignored. The command to disabled lanes are ignored.

- 000: Clock Lane
- 001: Data Lane 0
- 010: Data Lane 1
- 011: Data Lane 2
- 100: Data Lane 3
- 101: Reserved
- 110: ALL enabled Data Lanes
- 111: ALL enabled Lanes

Bit [3:1]: LP_Command[2:0]: Encoded Low Power Command Request.
When TurnReq is High, this field is ignored. The command to disabled lanes is ignored.
Please refer section エラー! 参照元が見つかりません。 for setting target lane when LP_Command = 110 or 111.

- 000: Reserved
- 001: Enter ULPS
- 010: Exit ULPS
- 011: Reserved
- 100: Transmit Trigger0
- 101: Transmit Trigger1
- 110: Transmit Trigger2
- 111: Transmit Trigger3

Bit [0]: TurnReq: BTA Turn Request.
0: No affect.
1: BTA Turn Request signal is asserted to D-PHY PPI.

6.5.5.5 DSI_LPTX_PKT_HDR (0x0230)

Field	31								24	23							16
field name	Res erve d	WC1 Data 7	WC1 Data 6	WC1 Data 5	WC1 Data 4	WC1 Data 3	WC1 Data 2	WC1 Data 1	WC1 Data 0								
field access	----	----	----	----	----	----	----	----	R/W								
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15								8	7							0
field name	WC0 Data 7	WC0 Data 6	WC0 Data 5	WC0 Data 4	WC0 Data 3	WC0 Data 2	WC0 Data 1	WC0 Data 0	VCI D1	VCI D0	Data Type 5	Data Type 4	Data Type 3	Data Type 2	Data Type 1	Data Type 0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:24]: Reserved

Bit [23:16]: WC1Data: Word Count 1 or Data 1.

The field is the either of WC1 for long packet, or Data 1 for short packet.

Bit [15:8]: WC0Data: Word Count 0 or Data 0.

The field is the either of WC0 for long packet, or Data 0 for short packet.

Bit [7:6]: VCID: Virtual Channel ID.

Bit [5:0]: DataType: Data Type.

Note: WC[15:0] = 0 or LPTX Long packet with WC=0 is not supported through LPTX register interface.

6.5.5.6 DSI_LPTX_PAYLOAD0 (0x0234)

Field	31							24	23							16
field name	PYLD0 [31:16]															
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15							8	7							0
field name	PYLD0 [15:0]															
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Payload data up to 8 bytes can be configured by [DSI_LPTX_PAYLOAD0 (0x0234)] and [DSI_LPTX_PAYLOAD1 (0x0238)]. If 9 bytes or more payload data has to be configured, it must be controlled with [DSI_LPTX_INT_STAT (0x0220)]. Payload1Done, Payload0Done in combination with the application layer. PLD0 is transmitted earlier than PLD1.

Data is transmitted from LSB byte.

Bit [31:0]: PYLD0: Return Long Packet Payload Data 0

Store the payload data to answer the read request long packet. Set the payload data up to the byte size configured in WC region of [DSI_LPTX_PKT_HDR].WC1Data and [DSI_LPTX_PKT_HDR].WC0Data. CRC is added automatically.

6.5.5.7 DSI_LPTX_PAYLOAD1 (0x0238)

Field	31							24	23							16
field name	PYLD1 [31:16]															
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15							8	7							0
field name	PYLD1 [15:0]															
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit [31:0]: PYLD1: Return Long Packet Payload Data 1

Store the payload data to answer the read request long packet. Set the payload data up to the byte size configured in WC0 and WC1 region of [DSI_LPTX_PKT_HDR (0x0230)].

6.5.6 D-PHY Control Registers (Toshiba D-PHY only)

6.5.6.1 PPI_DPHY_DLYCNTRL (0x0240)

Field	31							24	23								16
field name	Reserve d	CLS_DL_YCNTRL 3	CLS_DL_YCNTRL 2	CLS_DL_YCNTRL 1	CLS_DL_YCNTRL 0												
field access	----	----	----	----	----	----	----	----	----	----	----	----	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	D3S_DL_YCNTRL 3	D3S_DL_YCNTRL 2	D3S_DL_YCNTRL 1	D3S_DL_YCNTRL 0	D2S_DL_YCNTRL 3	D2S_DL_YCNTRL 2	D2S_DL_YCNTRL 1	D2S_DL_YCNTRL 0	D1S_DL_YCNTRL 3	D1S_DL_YCNTRL 2	D1S_DL_YCNTRL 1	D1S_DL_YCNTRL 0	D0S_DL_YCNTRL 3	D0S_DL_YCNTRL 2	D0S_DL_YCNTRL 1	D0S_DL_YCNTRL 0	
field access	R/W																
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:20]: Reserved

Bit [19:16]: CLS_DLYCNTRL [3:0]: Tuning of transmit window position.

The HS clock output can be delayed according to the setting.

The recommended value is implementation specific.

Bit [15:12]: D3S_DLYCNTRL [3:0]: Tuning of transmit window position.

The HS data lane 3 output can be delayed according to the setting.

The recommended value is implementation specific.

Bit [11:8]: D2S_DLYCNTRL [3:0]: Tuning of transmit window position.

The HS data lane 2 output can be delayed according to the setting.

The recommended value is implementation specific.

Bit [7:4]: D1S_DLYCNTRL [3:0]: Tuning of transmit window position.

The HS data lane 1 output can be delayed according to the setting.

The recommended value is implementation specific.

Bit [3:0]: D0S_DLYCNTRL [3:0]: Tuning of transmit window position.

The HS data lane 0 output can be delayed according to the setting.

The recommended value is implementation specific.

6.5.6.2 PPI_DPHY_LPRX_THSLD (0x0244)

This register is invalid if CDSITX IP is used for CSI-2

Field	31								24	23							16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	Reserve d	DOS_CUTRSEL	D0S_LP_RXVTHLOW														
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	

Bit [31:2]: Reserved

Bit [1]: D0S_CUTRSEL: LPRXVTHLOW CUTR value select for Data Lane 0.

1: LPRXVTHLOW value is set by CUTR cell.

0: LPRXVTHLOW value is set by D0S_LPRXVTHLOW.

Bit [0]: D0S_LPRXVTHLOW: LPRX input threshold select for Data Lane 0.

1: LPRX input threshold is low.

0: LPRX input threshold is high.

6.5.6.3 PPI_DPHY_LPRXCALCNTRL (0x0248)

This register is invalid if CDSITX IP is used for CSI-2. Do not change the default value.

Field	31							24	23							16
field name	Reserve d	AutoCal Cnt7	AutoCal Cnt6	AutoCal Cnt5	AutoCal Cnt4	AutoCal Cnt3	AutoCal Cnt2	AutoCal Cnt1	AutoCal Cnt0							
field access	-----	-----	-----	-----	-----	-----	-----	R/W								
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15							8	7								0
field name	Reserve d	LPR XCA LTRI M2	LPR XCA LTRI M1	LPR XCA LTRI M0	Reserve d	Reserve d	Reserve d	Reserve d									
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W	R/W	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	

Bit [31:24]: Reserved

Bit [23:16]: AutoCalCnt [7:0]: Auto Calibration Counter.

The counter is counted by CFGCLK.

The counter value shall generate the time be more than 500ns.

Bit [15:7]: Reserved.

Bit [6:4]: LPRXCALTRIM [2:0]: Calibration Trimmer.

Bit [3:0]: Reserved.

6.5.6.4 PPI_DPHY_LPRXAUTOCALST (0x024C)

Field	31								24	23							16
field name	Reserve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	Reserve d	LPR XCA LRE S	LPR XCA LEN	AutoCalStrt													
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:3]: Reserved

Bit [2] LPRXCALRES: LPRX Calibration Reset.

In order to reset auto calibration, set 1, and keep 1 for 500ns or more during LPRXCALEN = 0.

When auto calibration function is used, keep this bit to 0.

- 0: Not Reset
- 1: Reset calibration.

Bit [1] LPRXCALEN: LPRX Calibration Enable.

In order to execute calibration, set 1, and keep 1 for 500ns or more during LPRXCALRES = 0.

When auto calibration function is used, keep this bit to 0.

- 0: Calibration Switch OFF
- 1: Calibration Switch ON

Bit [0] AutoCalStrt: LPRX Auto Calibration Start.

When this bit is set to 1, LPRXCALRES and LPRXCALEN are ignored until the end of auto calibration.

- 0: Calibration is not started.
- 1: Start auto calibration.

When this bit is set to 1, the read value is 1 until auto calibration is finished. When autocalibration is finished, the bit is cleared to 0.

6.5.6.5 PPI_DPHY_MON (0x0250)

Field	31								24	23							16
field name	Res erve d	DOS LP CDE NM ON	DOS LP TXH IZM ON														
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	

Field	15								8	7							0
field name	Res erve d	CUT R_L PRX VTH LO W															
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	

Bit [31:18]: Reserved

Bit [23:18]: Reserved

Bit [17]: DOS_LPCDENMON

LPCDEN signal for Data Lane 0 is monitored by this bit. The signal is synchronized to CFGCLK.

Bit [16]: DOS_LPTXHIZMON

LPTXHIZ signal for Data Lane 0 is monitored by this bit. The signal is synchronized to CFGCLK.

Bit [15:1]: Reserved

Bit [0]: CUTR_LPRXVTHLOW: CUTR LPRXVTHLOW Monitor

This bit monitors ZEMIPICUTR calibration value. This signal from PHY is synchronized by CFGCLK.

6.5.6.6 PPI_DPHY_LPTXTIMECNT (0x0254)

Field	31								24	23							16
field name	Res erve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	

reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field	15							8	7								0
field name	Reserve d	Reserve d	Reserve d	Reserve d	LPT XTI MEC NT1 1	LPT XTI MEC NT1 0	LPT XTI MEC NT9	LPT XTI MEC NT8	LPT XTI MEC NT7	LPT XTI MEC NT6	LPT XTI MEC NT5	LPT XTI MEC NT4	LPT XTI MEC NT3	LPT XTI MEC NT2	LPT XTI MEC NT1	LPT XTI MEC NT0	
field access	----	----	----	----	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:12]: Reserved

Bit [11:0]: LPTXTIMECNT TLPX Period counter.

The counter generates a timing signal for the period of T_{LPX} .

This value is set to LPTXTIMECNT signal.

T_{LPX} period = $(1 + \text{LPTXTIMECNT}) * \text{SYSDTClk}$ for data Lane

T_{LPX} period = $(1 + \text{LPTXTIMECNT}) * \text{SYSCLClk}$ for data Lane

NOTE:

The minimum value for LPTXTIMECNT shall be two.

The time for $(\text{LPTXTIMECNT} + 1) * (\text{SYSDTClk}$ period) shall be more than 50ns.

The time for $(\text{LPTXTIMECNT} + 1) * (\text{SYSCLClk}$ period) shall be more than 50ns.

It is preferred $\text{SYSCLClk} = \text{SYSDTClk}$ to assure TLPX is same for both clock and data lanes.

6.5.6.7 PPI_DPHY_TCLK_HEADERCNT (0x0258)

Field	31							24	23								16
field name	Reserve d	TCL K_P REZ ERO CNT 7	TCL K_P REZ ERO CNT 6	TCL K_P REZ ERO CNT 5	TCL K_P REZ ERO CNT 4	TCL K_P REZ ERO CNT 3	TCL K_P REZ ERO CNT 2	TCL K_P REZ ERO CNT 1	TCL K_P REZ ERO CNT 0								
field access	----	----	----	----	----	----	----	R/W	R/W								
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	Reserve d	TCL K_P reC nt5	TCL K_P reC nt4	TCL K_P reC nt3	TCL K_P reC nt2	TCL K_P reC nt1	TCL K_P reC nt0	Reserve d	TCL K_P repa reC nt6	TCL K_P repa reC nt5	TCL K_P repa reC nt4	TCL K_P repa reC nt3	TCL K_P repa reC nt2	TCL K_P repa reC nt1	TCL K_P repa reC nt0	
field access	----	----	R/W	R/W	R/W	R/W	R/W	R/W	----	R/W							
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:24]: Reserved.

Bit [23:16]: TCLK_PREZEROCNT [7:0].

This counter is used for TCLK-ZERO parameter in Clock Lane. This counter is counted by SYSCLClk.

Set this register to satisfy the minimum of 300ns of (TCLK-ZERO + TCLK-PREPARE).

Bit [15:14] Reserved.

Bit [13:8] TCLK-PreCnt [5:0]. This counter is counted by SYSDTClk

Bit [7] Reserved.

Bit [6:0] TCLK_PrepCnt [6:0].

This counter is used for TCLK_PREPARE parameter. This counter is counted by SYSCLClk.

Set this register to satisfy the TCLK-PREPARE timing parameter in MIPI D-PHY specification, which is minimum 38ns and maximum 95ns.

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6.5.6.8 PPI_DPHY_TCLK_TRAILCNT (0x025C)

Field	31							24	23								16
field name	Reserve d	TCL_K_ExitCnt10	TCL_K_ExitCnt9	TCL_K_ExitCnt8	TCL_K_ExitCnt7	TCL_K_ExitCnt6	TCL_K_ExitCnt5	TCL_K_ExitCnt4	TCL_K_ExitCnt3	TCL_K_ExitCnt2	TCL_K_ExitCnt1	TCL_K_ExitCnt0					
field access	----	----	----	----	----	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	TCL_K_TrailCnt7	TCL_K_TrailCnt6	TCL_K_TrailCnt5	TCL_K_TrailCnt4	TCL_K_TrailCnt3	TCL_K_TrailCnt2	TCL_K_TrailCnt1	TCL_K_TrailCnt0								
field access	----	----	----	----	----	----	----	R/W	R/W								
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:27]: Reserved.

Bit [26:16]: TCLK_ExitCnt [10:0].

Bit [15:8]: Reserved.

Bit [7:0] TCLK_TrailCnt [7:0].

This counter is used for TCLK_TRAIL parameter. This counter is counted by SYSCLClk.

Set this register to satisfy the minimum of 60ns.

6.5.6.9 PPI_DPHY_THS_HEADERCNT (0x0260)

Field	31							24	23								16
field name	Reserve d	THS_PR_EZE_ROC_NT7	THS_PR_EZE_ROC_NT6	THS_PR_EZE_ROC_NT5	THS_PR_EZE_ROC_NT4	THS_PR_EZE_ROC_NT3	THS_PR_EZE_ROC_NT2	THS_PR_EZE_ROC_NT1	THS_PR_EZE_ROC_NT0								
field access	-----	-----	-----	-----	-----	-----	-----	R/W	R/W								
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	THS_PrepareCnt6	THS_PrepareCnt5	THS_PrepareCnt4	THS_PrepareCnt3	THS_PrepareCnt2	THS_PrepareCnt1	THS_PrepareCnt0									
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W							
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:24]: Reserved.

Bit [23:16]: THS_PREZEROCNT [7:0].

This counter is used for THS-ZERO parameter in DataLane. This counter is counted by SYSDTClk.

Set this register to satisfy the minimum of 145ns + 10*UI of (THS-ZERO + THS-PREPARE).

Bit [15:7] Reserved.

Bit [6:0] THS_PrepCnt [6:0].

This counter is used for THS_PREPARE parameter. This counter is counted by SYSDTClk.

Set this register to satisfy the THS-PREPARE timing parameter in MIPI D-PHY specification, which is minimum 40ns+4*UI and maximum 85ns+6*UI.

6.5.6.10 PPI_DPHY_TWAKEUPCNT (0x0264)

Field	31								24	23							16
field name	Reserve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	TWA KEU P_C nt15	TWA KEU P_C nt14	TWA KEU P_Cn t13	TWA AK EU P_C nt12	TWA AK EUP _Cn t11	TWA AKE UP_ Cnt1 0	TWA KEU P_C nt9	TWA KEU P_C nt8	TWA KEU P_C nt7	TWA KEU P_C nt6	TWA KEU P_C nt5	TWA KEU P_C nt4	TWA KEU P_C nt3	TWA KEU P_C nt2	TWA KEU P_C nt1	TWA KEU P_C nt0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:16]: Reserved.

Bit [15:0] TWAKEUP_Cnt[15:0].

This counter is used to exit ULPS State. TWAKEUP = TWAKEUP_Cnt * T_{Lpx} period.

6.5.6.11 PPI_DPHY_TCLK_POSTCNT (0x0268)

Field	31								24	23							16
field name	Reserve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	Reserve d	TCL K_P ostC nt10	TCL K_P ostC nt9	TCL K_P ostC nt8	TCL K_P ostC nt7	TCL K_P ostC nt6	TCL K_P ostC nt5	TCL K_P ostC nt4	TCL K_P ostC nt3	TCL K_P ostC nt2	TCL K_P ostC nt1	TCL K_P ostC nt0					
field access	----	----	----	----	----	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:11]: Reserved.

Bit [10:0]: TCLK-PostCnt[10:0].

This counter is used for TCLK-POSTparameter in Clock Lane. This counter is counted by SYSDTClk.
Set the value greater than (60ns +52*UI).

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6.5.6.12 PPI_DPHY_THSTRAILCNT (0x026C)

Field	31							24	23								16
field name	Reserve d	THS_ExitCnt 10	THS_ExitCnt 9	THS_ExitCnt 8	THS_ExitCnt 7	THS_ExitCnt 6	THS_ExitCnt 5	THS_ExitCnt 4	THS_ExitCnt 3	THS_ExitCnt 2	THS_ExitCnt 1	THS_ExitCnt 0					
field access	----	----	----	----	----	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	THS_TrailCnt 7	THS_TrailCnt 6	THS_TrailCnt 5	THS_TrailCnt 4	THS_TrailCnt 3	THS_TrailCnt 2	THS_TrailCnt 1	THS_TrailCnt 0								
field access	----	----	----	----	----	----	----	R/W	R/W								
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:27]: Reserved.

Bit [26:16]: THS_ExitCnt[10:0].

Bit [15:8]: Reserved.

Bit [7:0] THS_TrailCnt[7:0].

This counter is used for THS_TRAIL parameter. This counter is counted by SYSDTClk.

6.5.6.13 PPI_DPHY_HSTXVREGCNT (0x0270)

Field	31							24	23								16
field name	Reserve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	HST_XVR_EGC_NT1_5	HST_XVR_EGC_NT1_4	HST_XVR_EGC_NT1_3	HST_XVR_EGC_NT1_2	HST_XVR_EGC_NT1_1	HST_XVR_EGC_NT1_0	HST_XVR_EGC_NT9	HST_XVR_EGC_NT8	HST_XVR_EGC_NT7	HST_XVR_EGC_NT6	HST_XVR_EGC_NT5	HST_XVR_EGC_NT4	HST_XVR_EGC_NT3	HST_XVR_EGC_NT2	HST_XVR_EGC_NT1		
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-------------	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Bit [31:16]: Reserved.

Bit [15:0]: HSTXVREGCNT[15:0].

TX Voltage Regulator setup Wait Counter

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6.5.6.14 PPI_DPHY_HSTXVREGEN (0x0274)

Field	31								24	23							16
field name	Reserve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	Reserve d	D3M_HS	D2M_HS	D1M_HS	D0M_HS	CLM_HS											
field access	----	----	----	----	----	----	----	----	R/W	R/W	R/W	R/W	R/W				
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0				0

Bit [31:5]: Reserved

Bit [4]: D3M_HSTXVREGEN. Voltage regulator enable for HSTX Data Lane 3.

0: Disable.

1: Enable.

Bit[3]: D2M_HSTXVREGEN. Voltage regulator enable for HSTX Data Lane 2.

0: Disable.

1: Enable.

Bit[2]: D1M_HSTXVREGEN. Voltage regulator enable for HSTX Data Lane 1.

0: Disable.

1: Enable.

Bit[1]: D0M_HSTXVREGEN. Voltage regulator enable for HSTX Data Lane 0.

0: Disable.

1: Enable.

Bit[0]: CLM_HSTXVREGEN. Voltage regulator enable for HSTX Clock Lane.

0: Disable.

1: Enable.

6.5.6.15 PPI_DSI_BTA_COUNT (0x0278)

This register is invalid if CDSITX IP is used for CSI-2

Field	31							24	23							16
field name	Reserve d	TXT AG O10	TXT AG O9	TXT AG O8	TXT AG O7	TXT AG O6	TXT AG O5	TXT AG O4	TXT AG O3	TXT AG O2	TXT AG O1	TXT AG O0				
field access	-----	-----	-----	-----	-----	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15							8	7							0
field name	Reserve d	RXT ASU REC NT10	RXT ASU REC NT9	RXT ASU REC NT8	RXT ASU REC NT7	RXT ASU REC NT6	RXT ASU REC NT5	RXT ASU REC NT4	RXT ASU REC NT3	RXT ASU REC NT2	RXT ASU REC NT1	RXT ASU REC NT0				
field access	-----	-----	-----	-----	-----	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit [31:27]: Reserved

Bit [26:16]: TXTAGOCNT

This value is used to set cout up value to set TTA-GO period (LP-00 drive period) when this module release drive right by BTA.

The period to drive LP-00 for TTA-GO period is $4 * (\text{TXTAGOCNT} + 1) * (\text{SYSDTClk cycle})$.

Please set the value to be TTA-GO (= $4 * \text{TLPX}$) period which is MIPI specification.

Bit [15:11]: Reserved

Bit [10:0]: RXTASURECNT

This value is used to set counter value for the period to drive LP00 as TTA-SURE period when drive right is acquired by BTA.

The drive period is calculated by (BTA detection period + (RXTASURECNT + (3 or 2)) * (SYSDTClk cycle)).

Please set the period within TTA-SURE (Min TLPX, Max 2*TLPX), which is MIPI specification.

6.5.6.16 PPI_DPHYTX_ADJUST (0x027C)

Field	31							24	23								16
field name	ForceDPHYADVLd	Reserve d	FLP TXC URR EN1	FLP TXC URR EN0													
field access	R	----	----	----	----	----	----	----	----	----	----	----	----	----	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	CLS_LP_TXC_URR_EN1	CLS_LP_TXC_URR_EN0	D3S_LP_TXC_URR_EN1	D3S_LP_TXC_URR_EN0	D2S_LP_TXC_URR_EN1	D2S_LP_TXC_URR_EN0	D1S_LP_TXC_URR_EN1	D1S_LP_TXC_URR_EN0	D0S_LP_TXC_URR_EN1	D0S_LP_TXC_URR_EN0						
field access	----	----	----	----	----	----	R/W										
reset value	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	

- Bit [31]: ForceDPHYADVLd: Force D-PHY characteristic adjustment value from the input signals.
 This bit is a monitor bit of FORCE_DPHY_ADVLDEN signal. This bit is static and it is fixed before releasing Reset_N.
 Writing this bit is invalid.
- 0: FORCE_DPHY_ADVLDEN signal is Low.
 1: FORCE_DPHY_ADVLDEN signal is High.
- Bit [30:18]: Reserved
- Bit [17:16]: FLPTXCURREN [1:0]: Force D-PHY LPTX output current (TRLP/TFLP tuning) value from the input signals.
 The bits are monitor bits of FORCE_LPTX_CURREN signal.
 Writing the bits is invalid.
 The bits are used for Data Lane 0 when FORCE_DPHY_ADVLDEN is High.
- Bit [15:10]: Reserved.
- Bit [9:8]: CLS_LPTXCURREN: Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Clock Lane.
 The bits are output from CLS_LPTXCURR1EN and CLS_LPTXCURR0EN when FORCE_DPHY_ADVLDEN is Low.
 00: no additional output current
 01: A% additional output current
 10: A% additional output current
 11: B% additional output current
 When value is changed from 10 (default) to 00, rise/fall time is longer. When '11' is set, rise/fall time is shorter.
- Bit [7:6]: D3S_LPTXCURREN: Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 3.
 The bits are output from D3S_LPTXCURR1EN and D3S_LPTXCURR0EN when FORCE_DPHY_ADVLDEN

is Low.

- 00: no additional output current
- 01: A% additional output current
- 10: A% additional output current
- 11: B% additional output current

When value is changed from 10 (default) to 00, rise/fall time is longer. When '11' is set, rise/fall time is shorter.

Bit [5:4]: D2S_LPTXCURREN: Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 2.

The bits are output from D2S_LPTXCURR1EN and D2S_LPTXCURR0EN when FORCE_DPHY_ADVLDEN is Low.

- 00: no additional output current
- 01: A% additional output current
- 10: A% additional output current
- 11: B% additional output current

When value is changed from 10 (default) to 00, rise/fall time is longer. When '11' is set, rise/fall time is shorter.

Bit [3:2]: D1S_LPTXCURREN: Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 1.

The bits are output from D1S_LPTXCURR1EN and D1S_LPTXCURR0EN when FORCE_DPHY_ADVLDEN is Low.

- 00: no additional output current
- 01: A% additional output current
- 10: A% additional output current
- 11: B% additional output current

When value is changed from 10 (default) to 00, rise/fall time is longer. When '11' is set, rise/fall time is shorter.

Bit [1:0]: D0S_LPTXCURREN: Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 0.

The bits are output from D0S_LPTXCURR1EN and D0S_LPTXCURR0EN when FORCE_DPHY_ADVLDEN is Low.

- 00: no additional output current
- 01: A% additional output current
- 10: A% additional output current
- 11: B% additional output current

When value is changed from 10 (default) to 00, rise/fall time is longer. When '11' is set, rise/fall time is shorter.

Note:

1. FORCE_DPHY_ADVLDEN and FORCE_LPTX_CURREN [1:0] – Should be driven to 0 or 1 before Reset_N release, otherwise bit [31] & bits [17:16] will appear as 'Z' in simulation.

6.5.6.17 PPI_DPHY_POWERCNTRL (0x0284)

Field	31							24	23							16
field name	Reserve d															
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7							0
field name	Reserve d	EN_ZEMIPIV12	V12PEN	V12EN												
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	Selectable	Selectable	Selectable	

Bit [31:3]: Reserved

Bit [2]: EN_ZEMIPIV12: Control signal of EN of ZEMIPIV12 power cell.
 0: V12 power is turned off.
 1: V12 power is turned on.

Bit [1]: V12PEN: Control signal of V12PIN of ZEMIPIPLL.
 0: V12 power is turned off.
 1: V12 power is turned on.

Bit [0]: V12EN: Control signal of V12EN of ZEMIPI.
 0: V12 power is turned off.
 1: V12 power is turned on.

The default value for Bit[2:0] will be selected based on value of input port “CFGDEFSEL” during reset state only. Please refer section エラー! 参照元が見つかりません。 for more detail.

6.5.6.18 PPI_DPHY_CAP (0x0288)

Field	31							24	23								16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	CLS_CA_P1	CLS_CA_P0	D3S_CA_P1	D3S_CA_P0	D2S_CA_P1	D2S_CA_P0	D1S_CA_P1	D1S_CA_P0	D0S_CA_P1	D0S_CA_P0						
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
reset value	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	

Bit [31:10]: Reserved

Bit [9:8]: CLS_CAP [1:0] Select output capacitors for Clock Lane.

Bit [7:6]: D3S_CAP [1:0] Select output capacitors for Data Lane 3.

Bit [5:4]: D2S_CAP [1:0] Select output capacitors for Data Lane 2.

Bit [3:2]: D1S_CAP [1:0] Select output capacitors for Data Lane 1.

Bit [1:0]: D0S_CAP [1:0] Select output capacitors for Data Lane 0.

6.5.7 Current Status Registers

6.5.7.1 LANE_STATUS_HS (0x0290)

Writing the status bits is invalid and no affect.

Field	31							24	23								16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Reserve d	CLActiveHS	Reserve d	Reserve d	Reserve d	D3TxActiveHS	D2TxActiveHS	D1TxActiveHS	D0TxActiveHS								
field access	-----	-----	-----	-----	-----	-----	R	R	-----	-----	-----	R	R	R	R	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:18]: Reserved

Bit [7]: CLActiveHS: High Speed State of Clock Lane.

0: LP state.

1: HS state.

When the line transition from LP11 to LP00 through LP01 is detected, this bit is set.

When Stopstate is detected, this bit is cleared to 0.

Bit [6:4]: Reserved

Bit [3]: D3TxActiveHS: High Speed State of Data Lane 3.

The explanation is the same as CLActiveHS.

Bit [2]: D2TxActiveHS: High Speed State of Data Lane 2.

The explanation is the same as CLActiveHS.

Bit [1]: D1TxActiveHS: High Speed State of Data Lane 1.

The explanation is the same as CLActiveHS.

Bit [0]: D0TxActiveHS: High Speed State of Data Lane 0.

The explanation is the same as CLActiveHS.

6.5.7.2 LANE_STATUS_LP (0x0294)

Writing the status bits is invalid and no affect.

Field	31							24	23								16
field name	Reserve d	L0Direction	Reserve d	Reserve d	L3UI psEsc	L2UI psEsc	L1UI psEsc	L0UI psEsc									
field access	-----	-----	-----	-----	-----	-----	-----	-----	R	-----	-----	R	R	R	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	CIUI psA ctive	Reserve d	Reserve d	Reserve d	L3UI psA ctive	L2UI psA ctive	L1UI psA ctive	L0UI psA ctive	CIS t opSt ate	Reserve d	Reserve d	Reserve d	L3St opSt ate	L2St opSt ate	L1St opSt ate	L0St opSt ate	
field access	R	-----	-----	-----	R	R	R	R	-----	-----	-----	R	R	R	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

This register shows the current status and the bit value changes dynamically.

When the lanes are disabled, the status of the lane is invalid.

Bit [31:24]: Reserved

Bit [23]: Reserved

Bit [22]: L0Direction: Direction bit status of Data Lane 0.
This register is invalid if CDSITX IP is used for CSI-2.

0: Direction signal is 0. This means that CDSI detects BTA from host and Data Lane 0 is in LPTX mode, or in LPRX mode, at which host device has not received BTA return from CDSI.

1: Direction signal is 1. This means that Data Lane 0 is in LPRX mode.

Bit [21:20]: Reserved

Bit [19]: L3UlpsEsc: Data Lane 3 Rx Ulps Esc

The explanation is the same as CIUlpsEsc.

0: Indicates that Data Lane is neither of ULPS state or Mark-1 state which is an intermediate state to exit ULPS.
1: Indicates that Data Lane is in ULPS state, including Mark-1 state which is an intermediate state to exit ULPS.

Bit [18]: L2UlpsEsc: Data Lane 2 Rx Ulps Esc:

The explanation is the same as L3UlpsEsc.

Bit [17]: L1UlpsEsc: Data Lane 1 Rx Ulps Esc:

The explanation is the same as L3UlpsEsc.

Bit [16]: L0UlpsEsc: Data Lane 0 Rx Ulps Esc:

The explanation is the same as L3UlpsEsc.

- Bit [15]: ClUlpsActive: Clock Lane Rx Ulps Active
0: Indicates that Clock Lane is not in ULPS state.
1: Indicates that Clock Lane is in ULPS state.
- Bit [14:12]: Reserved
- Bit [11]: L3UlpsActive: Data Lane 3 Rx Ulps Active
0: Indicates that Data Lane 3 is not in ULPS state.
1: Indicates that Data Lane 3 is in ULPS state.
- Bit [10]: L2UlpsActive: Data Lane 2 Rx Ulps Active
The explanation is the same as L3UlpsActive.
- Bit [9]: L1UlpsActive: Data Lane 1 Rx Ulps Active
The explanation is the same as L3UlpsActive.
- Bit [8]: L0UlpsActive: Data Lane 0 Rx Ulps Active
The explanation is the same as L3UlpsActive.
- Bit [7]: ClStopState: Clock Lane Stop State
The initial value depends on the lane status.
0: Indicates that Clock Lane is not in Stop state.
1: Indicates that Clock Lane is in Stop state.
- Bit [6:4]: Reserved
- Bit [3]: L3StopState: Data Lane 3 Stop State
The initial value depends on the lane status.
0: Indicates that Data Lane 3 is not in Stop state.
1: Indicates that Data Lane 3 is in Stop state.
- Bit [2]: L2StopState: Data Lane 2 Stop State
The explanation is the same as L3StopState.
- Bit [1]: L1StopState: Data Lane 1 Stop State
- Bit [0]: L0StopState: Data Lane 0 Stop State

6.5.8 MIPI PLL Control Registers

6.5.8.1 MIPI_PLL_CTRL (0x02A0)

PLL Control register settings.

Field	31							24	23								16
field name	Res erve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	Res erve d	MP CKE N	MP ENAB LE														
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit [31:2]: Reserved

Bit [1]: MP_CKEN:
Clock enable of HSCK, HSCKB, HSBYTECK, HSCKBY2, HSCKBY4 and HSCKBY8

Bit [0]: MP_Enable:
MIPI PLL Enable

6.5.8.2 MIPI_PLL_LOCKCNT (0x02A4)

PLL lock counter. The counter to count to wait for PLL lock detection

Field	31							24	23								16
field name	Reserve d																
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	MP LOC KCN T15	MP LOC KCN T14	MP LOC KCN T13	MP LOC KCN T12	MP LOC KCN T11	MP LOC KCN T10	MP LOC KCN T9	MP LOC KCN T8	MP LOC KCN T7	MP LOC KCN T6	MP LOC KCN T5	MP LOC KCN T4	MP LOC KCN T3	MP LOC KCN T2	MP LOC KCN T1	MP LOC KCN T0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Bit [31:16]: Reserved

Bit [15:0]: MP_LOCKCNT

MIPI PLL Lock count. Counter to wait until MIPI PLL lock is detected.

This counter is counted by MP_CKREF.

6.5.8.3 MIPI_PLL_LOCK (0x02A8)

Field	31								24	23							16
field name	Res erve d																
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15								8	7							0
field name	Res erve d	MP LOC KUP DON E															
field access	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	R
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit [31:1]: Reserved

Bit [0]: MP_LOCKUPDONE: PLL lock done indication.
Indicates PLL lock wait counter has expired.

6.5.8.4 MIPI_PLL_CONF (0x02AC)

PLL parameter settings.

Field	31							24	23								16
field name	Reserve d	MP_LB_W1	MP_LB_W0														
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	

Field	15							8	7								0
field name	MP_PRD_3	MP_PRD_2	MP_PRD_1	MP_PRD_0	MP_FRS_1	MP_FRS_0	MP_LFBREN	MP_FBD_8	MP_FBD_7	MP_FBD_6	MP_FBD_5	MP_FBD_4	MP_FBD_3	MP_FBD_2	MP_FBD_1	MP_FBD_0	
field access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
reset value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	

Bit [31:18]: Reserved

Bit [17:16]: MP_LBW[1:0]:

Low Bandwidth setting

2'b00: 25% of maximum loop bandwidth.

2'b01: 33% of maximum loop bandwidth.

2'b10: 50% of maximum loop bandwidth.

2'b00: maximum loop bandwidth.

Bit [15:12]: MP_PRD[3:0]:

Input Divider Value; Division ration = (MP_PRD[3:0] + 1)

Bit [11:10]: MP_FRS[1:0]:

Frequency range setting (post divider) for HSCK.

2'b00: 500MHz ... 1GHz

2'b01: 250MHz ... 500MHz

2'b10: 125MHz ... 250MHz

2'b11: 62.5MHz...125MHz

Bit [9]: MP_LFBREN:

Lower Frequency Bound Removal enable

Bit [8:0]: MP_FBD[8:0]:

Feedback divider value. Division ratio = (MP_FBD[8:0] + 1)

6.5.8.5 MIPI_PLL_DEBUG (0x02B0)

PLL Debug register settings.

Field	31							24	23							16
field name	Reserve d															
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	15							8	7								0
field name	Reserve d	MP_TESTEN	MP_TCKS	MP_TCKEN	MP_EXTFBEN	MP_CKTRISTATE	MP_BYPCKEN										
field access	-----	-----	-----	-----	-----	-----	-----	-----	-----	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:6]: Reserved

Bit [5]: MP_TESTEN:
Test Mode enable. Use only for test purpose.

Bit [4]: MP_TCKS:
Test clock output select. Use only for test purpose.
0 : output of input divider transferred to TCK
1 : output of feedback divider transferred to TCK.

Bit [3]: MP_TCKEN:
Test clock output enable. Use only for test purpose.

Bit [2]: MP_EXTFBEN:
Clock feedback is used for testing. Use only for test purpose.

Bit [1]: MP_CKTRISTATE:
MIPI PLL clock outputs are in high impedance.
Do not write High to MP_CKTRISTATE.

Bit [0]: MP_BYPCKEN:
Bypass clock enable. Use only for test purpose.

6.5.9 Debug Registers

6.5.9.1 CDSI_DEBUG1 (0x02C0)

When the bits are read, the read data is always 0.

Field	31							24	23								16
field name	CDS_I_D1_31	CDS_I_D1_30	CDS_I_D1_29	CDS_I_D1_28	CDS_I_D1_27	CDS_I_D1_26	CDS_I_D1_25	CDS_I_D1_24	CDS_I_D1_23	CDS_I_D1_22	CDS_I_D1_21	CDS_I_D1_20	CDS_I_D1_19	CDS_I_D1_18	CDS_I_D1_17	CDS_I_D1_16	
field access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	CDS_I_D1_15	CDS_I_D1_14	CDS_I_D1_13	CDS_I_D1_12	CDS_I_D1_11	CDS_I_D1_10	CDS_I_D1_9	CDS_I_D1_8	CDS_I_D1_7	CDS_I_D1_6	CDS_I_D1_5	CDS_I_D1_4	CDS_I_D1_3	CDS_I_D1_2	CDS_I_D1_1	CDS_I_D1_0	
field access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:0]: CDSI_D1 [31:0] CDSI block debug 1 registers.

Actual bit assign is defined by implementation.

6.5.9.2 CDSI_DEBUG2 (0x02C4)

When the bits are read, the read data is always 0.

Field	31							24	23								16
field name	CDS_I_D2_31	CDS_I_D2_30	CDS_I_D2_29	CDS_I_D2_28	CDS_I_D2_27	CDS_I_D2_26	CDS_I_D2_25	CDS_I_D2_24	CDS_I_D2_23	CDS_I_D2_22	CDS_I_D2_21	CDS_I_D2_20	CDS_I_D2_19	CDS_I_D2_18	CDS_I_D2_17	CDS_I_D2_16	
field access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	CDS_I_D2_15	CDS_I_D2_14	CDS_I_D2_13	CDS_I_D2_12	CDS_I_D2_11	CDS_I_D2_10	CDS_I_D2_9	CDS_I_D2_8	CDS_I_D2_7	CDS_I_D2_6	CDS_I_D2_5	CDS_I_D2_4	CDS_I_D2_3	CDS_I_D2_2	CDS_I_D2_1	CDS_I_D2_0	

field access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit [31:0]: CDSI_D2 [31:0] CDSI block debug 2 registers.

Actual bit assign is defined by implementation.

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6.5.9.3 PPI_DEBUG1 (0x02C8)

When the bits are read, the read data is always 0.

Field	31							24	23								16
field name	PPI_D1_31	PPI_D1_30	PPI_D1_29	PPI_D1_28	PPI_D1_27	PPI_D1_26	PPI_D1_25	PPI_D1_24	PPI_D1_23	PPI_D1_22	PPI_D1_21	PPI_D1_20	PPI_D1_19	PPI_D1_18	PPI_D1_17	PPI_D1_16	
field access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	PPI_D1_15	PPI_D1_14	PPI_D1_13	PPI_D1_12	PPI_D1_11	PPI_D1_10	PPI_D1_9	PPI_D1_8	PPI_D1_7	PPI_D1_6	PPI_D1_5	PPI_D1_4	PPI_D1_3	PPI_D1_2	PPI_D1_1	PPI_D1_0	
field access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:0]: PPI_D1 [31:0] D-PHY PPI block debug 1 registers.

Actual bit assign is defined by implementation.

6.5.9.4 PPI_DEBUG2 (0x02CC)

When the bits are read, the read data is always 0.

Field	31							24	23								16
field name	PPI_D2_31	PPI_D2_30	PPI_D2_29	PPI_D2_28	PPI_D2_27	PPI_D2_26	PPI_D2_25	PPI_D2_24	PPI_D2_23	PPI_D2_22	PPI_D2_21	PPI_D2_20	PPI_D2_19	PPI_D2_18	PPI_D2_17	PPI_D2_16	
field access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Field	15							8	7								0
field name	PPI_D2_15	PPI_D2_14	PPI_D2_13	PPI_D2_12	PPI_D2_11	PPI_D2_10	PPI_D2_9	PPI_D2_8	PPI_D2_7	PPI_D2_6	PPI_D2_5	PPI_D2_4	PPI_D2_3	PPI_D2_2	PPI_D2_1	PPI_D2_0	
field access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit [31:0]: PPI_D2 [31:0] D-PHY PPI block debug 2 registers.

Actual bit assign is defined by implementation.

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6.6 CSI2/DSI-TX1 Registers

CSI2/DSI-TX1 registers are identical as in CSI2/DSI-TX0 register description. Only different are the segment address assignment. TX1 registers are 0x0200 + those of TX0's.

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6.7 CDSI-TX Wrapper Registers

6.7.1 STX_Ctrl (STX_Ctrl:0x0500)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	R/W							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				dcs_cm_act	dcs_cm_sel	Reserved	
Type	RO				R/W	R/W	RO	
Default	0				0	0	0	

Register Field	Bit	Description
Reserved	[15:4]	
dcs_cm_act	[3]	DCS Command Active Option 1'b0: Send DCS command at Vertical Front Porch 1'b1: Send DCS command at Vertical Back Porch
dcs_cm_sel	[2:1]	DCS Command Select 2'b00: Select DSITX0 I/F 2'b01: Select DSITX1 I/F 2'b1x: Select both DSITX0 and DSITX1 I/F Note: when select 2'b1x, when write to DCSCMD_ID, DCSCMD_WC and DCSCMD_WDn will write to both DSITX0 and DSITX1.
Reserved	[0]	

6.7.2 DCSCMD_ST (DCSCMD_ST:0x0502)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved		dcs_cm_entry					
Type	R/W		RO					
Default	0		32					
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			dcs_cmd_done		dcs_cmd_ofl_ow	dcs_cmd_empty	dcs_cm_full
Type	RO			RO		RO	RO	RO
Default	0			0		0	1	0

Register Field	Bit	Description
Reserved	[15:14]	
dcs_cm_entry	[13:8]	DCS Command Entry available for writing in the command queue FIFO Command queue FIFO is 32 deep. So valid value is 0 to 32.
Reserved	[7:5]	
dcs_cmd_done	[4:3]	DCS Command done count Note: Wrap around counter that increments by 1 for every DSI command ths send out on MIPI I/F
dcs_cmd_oflow	[2]	DCS Command FIFO overflow 1'b0: Normal 1'b1: Overflow Write 1 to this bit to clear overflow flag. Note that all data written that cause overflow are dropped. Host should take care not to cause overflow. Unexpected behavioral can result because of overflow.
dcs_cmd_empty	[1]	DCS Command FIFO empty 1'b0: Fifo not empty 1'b1: Fifo empty
dcs_cmd_full	[0]	DCS Command FIFO Full 1'b0: Not full 1'b1: Fifo full

6.7.3 DCS Command Q Register (DCSCMD_Q: 0x0504)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name				dcs_cmdq				
Type				WO				
Default				0x0				
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name				dcs_cmdq				
Type				WO				
Default				0x0				

Register Field	Bit	Default	Description
dcs_cmdq	[15:0]	0x0	DCS Command Queue Write to this will write to the DCS command queue (32 deep) Note: check dcscmd_st to know the command queue status

6.7.4 STX0_MAXFCNT (STX0_MAXFCNT:0x0510)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name				Stx0_maxfcnt[15:8]				
Type				R/W				
Default				0x0				
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name				Stx0_maxfcnt[7:0]				
Type				R/W				
Default				0				

Register Field	Bit	Default	Description
Stx0_maxfcnt	[15:0]	0	STX0 CDSITX Maximum Frame Count

6.7.5 STX1_MAXFCNT (STX1_MAXFCNT:0x0514)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Stx1_maxfcnt[15:8]							
Type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Stx1_maxfcnt[7:0]							
Type	R/W							
Default	0							

Register Field	Bit	Description
Stx1_maxfcnt	[15:0]	STX1 CDSITX Maximum Frame Count

6.7.6 STX0_3Dreg0 (STX0_3Dreg0:0x0580)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Stx0_3d_en		Reserved	Stx0_3dcm_line[12:8]				
Type	R/W		RO	R/W				
Default	0x0		0x0	0x0				
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Stx0_3dcm_line[7:0]							
Type	R/W							
Default	0							

Register Field	Bit	Description
Stx0_3d_en	[15:14]	DSI 3D command mode 00: No 3D Mode VSS/DCS command 01: 3D Mode VSS transmit enable 10: 3D Mode Command Transmit enable 11: Reserved
Reserved	[13]	
Stx0_3dcm_line	[12:0]	STX0 CDSITX Maximum Frame Count

6.7.7 STX0_3Dreg1 (STX0_3Dreg1:0x0582)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Stx0_3d_lpldt[15:8]							
Type	R/W							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Stx0_3d_lpldt[7:0]							
Type	R/W							
Default	0							

Register Field	Bit	Description
Stx0_3d_lpldt	[15:0]	DSITX0 3d Mode VSS payload or 3D Mode DCS command payload

6.7.8 STX0_3Dreg2 (STX0_3Dreg2:0x0584)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Stx0_3dcm_di[7:0]							
Type	R/W							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Stx0_3d_upldt[7:0]							
Type	R/W							
Default	0							

Register Field	Bit	Description
Stx0_3dcm_di	[15:8]	DSITX0 3D DCS Command Data Identifier [7:6]: VC [5:0]: Data Type
Stx0_3d_upldt	[7:0]	DSITX0 3d Mode VSS payload or 3D Mode DCS command payload - Upper 8-bits

6.7.9 STX0_dsiphy_ctrl0 (STX0_dsiphy_ctrl0:0x0590)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Stx0_auto_cal_cnt[7:0]							
Type	R/W							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		Stx0_flprx_caltrim_data			Stx0_flprx_caltrim	Stx0_flprx_cal_cn	Stx0_auto_cal_st
Type	RO		R/W			R/W	R/W	R/W
Default	0		0			0	0	0

Register Field	Bit	Description
Stx0_auto_cal_cnt	[15:8]	Set the count up value for auto calibration
Reserved	[7:6]	
Stx0_flprx_caltrim_dat_a	[5:3]	Force LPRXCALTRIM data
Stx0_flprx_caltrim	[2]	Force LPRXCALTRIM signals 0: Not Force 1: Force
Stx0_flprx_cal_ctrl	[1]	Enable force LPRXCAL signal control 0: LPRXCALEn and LPRXCALRES are control by CDSI internal logic 1: LPRXCALEn and LPRXCALRES signals are controlled by FORCE_LPRX_CALEN and FORCE_LPRX_CALRES
Stx0_auto_cal_st	[0]	Start of auto calibration of LPRX 0: Idle 1: Start

6.7.10 STX0_dsiphy_ctrl1 (STX0_dsiphy_ctrl1:0x0592)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			Stx0_flptx_curen		Stx0_fdphy_advlden	Stx0_flprx_calres	Stx0_flprx_calen
Type	RO		R/W		R/W		R/W	R/W
Default	0		0		0		0	0

Register Field	Bit	Description
Reserved	[15:5]	
Stx0_flptx_curen	[4:3]	Force D-Phy LPTXCURREN1 and LPTXCURREN0 signals when FORCE_DPHY_ADVLDEN is high
Stx0_fdphy_advlden	[2]	Force D-Phy characteristic adjustment value by the input signal
Stx0_flprx_calres	[1]	LPRX Calibration Reset
Stx0_flprx_calen	[0]	LPRX Calibration Enable

6.7.11 STX1_3Dreg0 (STX1_3Dreg0:0x05C0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Stx1_3d_en		Reserved			Stx1_3dcm_line[12:8]		
Type	R/W		RO			R/W		
Default	0x0		0x0			0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name				Stx1_3dcm_line[7:0]				
Type				R/W				
Default				0				

Register Field	Bit	Description
Stx1_3d_en	[15:14]	DSI 3D command mode 00: No 3D Mode VSS/DCS command 01: 3D Mode VSS transmit enable 10: 3D Mode Command Transmit enable 11: Reserved
Reserved	[13]	
Stx1_3dcm_line	[12:0]	STX1 CDSITX Maximum Frame Count

6.7.12 STX1_3Dreg1 (STX1_3Dreg1:0x05C2)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Stx1_3d_lpldt[15:8]							
Type	R/W							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Stx1_3d_lpldt[7:0]							
Type	R/W							
Default	0							

Register Field	Bit	Description
Stx1_3d_lpldt	[15:0]	DSITX1 3d Mode VSS payload or 3D Mode DCS command payload

6.7.13 STX1_3Dreg2 (STX1_3Dreg2:0x05C4)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Stx1_3dcmd_di[7:0]							
Type	R/W							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Stx1_3d_upldt[7:0]							
Type	R/W							
Default	0							

Register Field	Bit	Description
Stx1_3dcmd_di	[15:8]	DSITX1 3D DCS Command Data Identifier [7:6]: VC [5:0]: Data Type
Stx1_3d_upldt	[7:0]	DSITX1 3d Mode VSS payload or 3D Mode DCS command payload - Upper 8-bits

6.7.14 STX1_dsiphy_ctrl0 (STX1_dsiphy_ctrl0:0x05D0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Stx1_auto_cal_cnt[7:0]							
Type	R/W							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		Stx1_flprx_caltrim_data			Stx1_flprx_caltrim	Stx1_flprx_cal_cnt	Stx1_auto_cal_st
Type	RO		R/W			R/W	R/W	R/W
Default	0		0			0	0	0

Register Field	Bit	Description
Stx1_auto_cal_cnt	[15:8]	Set the count up value for auto calibration
Reserved	[7:6]	
Stx1_flprx_caltrim_dat a	[5:3]	Force LPRXCALTRIM data
Stx1_flprx_caltrim	[2]	Force LPRXCALTRIM signals 0: Not Force 1: Force
Stx1_flprx_cal_ctrl	[1]	Enable force LPRXCAL signal control 0: LPRXCALEn and LPRXCALRES are control by CDSI internal logic 1: LPRXCALEn and LPRXCALRES signals are controlled by FORCE_LPRX_CALEN and FORCE_LPRX_CALRES
Stx1_auto_cal_st	[0]	Start of auto calibration of LPRX 0: Idle 1: Start

6.7.15 STX1_dsiphy_ctrl1 (STX1_dsiphy_ctrl1:0x05D2)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			Stx1_flptx_curen		Stx1_fdphy_advlde_n	Stx1_flprx_calres	Stx1_flprx_calen
Type	RO		R/W		R/W		R/W	R/W
Default	0		0		0		0	0

Register Field	Bit	Description
Reserved	[15:5]	
Stx1_flptx_curen	[4:3]	Force D-Phy LPTXCURREN1 and LPTXCURREN0 signals when FORCE_DPHY_ADVIDEN is high
Stx1_fdphy_advlden	[2]	Force D-Phy characteristic adjustment value by the input signal
Stx1_flprx_calres	[1]	LPRX Calibration Reset
Stx1_flprx_calen	[0]	LPRX Calibration Enable

6.8 CEC Control Registers

6.8.1 CEC Clock High Time Register 0 (CecHclk: 0x0028)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						cechclk	
Type	RO						R/W	
Default	0x0						0x2	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cechclk							
Type	R/W							
Default	0x90							

Register Field	Bit	Description
Reserved	[15:11]	
cechclk	[10:0]	CEC Clock High Time 0: Disable 1: 1 RefClk 2: 2 RefClk

6.8.2 CEC Clock Low Time Register 0 (CecLclk: 0x002A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							ceclclk
Type	RO							R/W
Default	0x0							0x2
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ceclclk							
Type	R/W							
Default	0x90							

Register Field	Bit	Description
Reserved	[15:11]	
ceclclk	[10:0]	CEC Clock Low Time 0: Disable 1: 1 RefClk 2: 2 RefClk

6.8.3 CEC Enable Register (CECEN: 0x0600)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							
Type	RO							
Default	0x0							

Table 6-3 CEC Enable Register

Register Field	Bit	Description
Reserved	[15:1]	
CECEN	0	CEC operation 0: Disable 1: Enable

6.8.4 CEC Logical Address Register (CECADD: 0x0604)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	CECADD[15:8]							
Type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CECADD[7:0]							
Type	R/W							
Default	0x0							

Table 6-4 CEC Logical Address Register

Register Field	Bit	Description
CECADD[15:0]	[15:0]	Specify logical address assigned to CEC Each bit corresponds to individual address, therefore multiple addresses can be assigned to CEC logic

6.8.5 CEC Reset Register (CECRST: 0x0608)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							
Type	RO							
Default	0x0							

Table 6-5 CEC Reset Register

Register Field	Bit	Description
Reserved	[15:1]	Reserved
CECRST	[0]	<p>CEC soft reset 0: Disable 1: Enable</p> <p>Setting this bit to “1” affects the following:</p> <ul style="list-style-type: none"> - Reception: Stops immediately. The received data is discarded. - Transmission (including the CEC line): Stops immediately. - Registers: The following registers are initialized. (CECADD, CECREN, CECRCR1, CECRCR2, CECRCR3, CECTEN, CECTCR, CECRSTAT, CECTSTAT, CECRBUF01-16, CECTBUF01-16, CECRCTR)

6.8.6 CEC Receive Enable (CECREN: 0x060C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							
Type	RO							
Default	0x0							

Table 6-6 CEC Receive Enable Register

Register Field	Bit	Description
Reserved	[15:1]	Reserved
CECREN	[0]	CEC reception enable 0: Disable 1: Enable

6.8.7 CEC Receive Control Register 1 (CECRCTL1: 0x0614)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved						CECACKDIS	
Type	RO						R/W	
Default	0x0						0x0	
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved		CECHNC[1:0]		Reserved	CECLNC[2:0]		
Type	RO		R/W		RO	R/W		
Default	0x0		0x0		0x0	0x0		
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved	CECMIN[2:0]			Reserved	CECMAX[2:0]		
Type	RO	R/W			R	R/W		
Default	0x0	0x0			0x0	0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B6
Name	Reserved	CECDAT[2:0]			CECTOUT[1:0]		CECRIHLD	CECOTH
Type	RO	R/W			R/W		R/W	R/W
Default	0x0	0x0			0x0		0x0	0x0

Table 6-7 CEC Receive Control Register 1

Register Field	Bit	Description
Reserved	[31:25]	Reserved
CECACKDIS	[24]	Enable ACK transmission 0: Disable 1: Enable
Reserved	[23:22]	Reserved
CECHNC	[21:20]	Number of consecutive cycles sampling logical '1' for noise cancellation 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles
Reserved	[19]	Reserved
CECLNC	[18:16]	Number of consecutive cycles sampling logical '0' for noise cancellation 000: 1 cycle 001: 2 cycles 100: 3 cycles 100: 4 cycles 111: 8 cycles
Reserved	[15]	Reserved
CECMIN	[14:12]	The minimum time to detect valid bit value. Error is detected when signal changes earlier than the minimum value 000: 2.05ms 001: 2.05ms+1cycle 010: 2.05ms+2cycles 011: 2.05ms+3cycles 100: 2.05ms-1cycle 101: 2.05ms-2cycles 110: 2.05ms-3cycles

Register Field	Bit	Description
		111: 2.05ms-4cycles
Reserved	[11]	Reserved
CECMAX	[10:8]	The maximum time to detect valid bit value. Error is detected when signal does not change within the maximum time 000: 2.75ms 001: 2.75ms+1cycle 010: 2.75ms+2cycles 011: 2.75ms+3cycles 100: 2.75ms-1cycle 101: 2.75ms-2cycles 110: 2.75ms-3cycles 111: 2.75ms-4cycles
Reserved	[7]	Reserved
CECDAT	[6:4]	Time to detect CEC signal as valid (0 or 1) 000: 1.05ms 001: 1.05ms+2cycles 010: 1.05ms+4cycles 011: 1.05ms+6cycles 100: 1.05ms-2cycles 101: 1.05ms-4cycles 110: 1.05ms-6cycles 111: Reserved
CECTOUT	[3:2]	Number of cycles to determine timeout 00: 1 bit cycle 01: 2 bit cycles 10: 3 bit cycles 11: Reserved
CECRIHLD	[1]	Suspend CEC receive error interrupt 0: Disable 1: Enable
CECOTH	[0]	For Testing only. Enable the CEC reception when address does not match 0: Disable 1: Enable

6.8.8 CEC Receive Control Register 2 (CECRCTL2: 0x0618)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved	CECSWAV3[2:0]			Reserved	CECSWAV2[2:0]		
Type	RO	R/W			RO	R/W		
Default	0x0	0x0			0x0	0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	CECSWAV1[2:0]			Reserved	CECSWAV0[2:0]		
Type	RO	R/W			RO	R/W		
Default	0x0	0x0			0x0	0x0		

Table 6-8 CEC Receive Control Register 2

Register Field	Bit	Description
Reserved	[15]	Reserved
CECSWAV3	[14:12]	Maximum time to detect start bit 000: 4.7ms 001: 4.7ms+1cycle 010: 4.7ms+2cycles 011: 4.7ms+3cycles 100: 4.7ms+4cycles 101: 4.7ms+5cycles 110: 4.7ms+6cycles 111: 4.7ms+7cycles
Reserved	[11]	Reserved
CECSWAV2	[10:8]	Minimum time to detect start bit 000: 4.3ms 001: 4.3ms-1cycle 010: 4.3ms-2cycles 011: 4.3ms-3cycles 100: 4.3ms-4cycles 101: 4.3ms-5cycles 110: 4.3ms-6cycles 111: 4.3ms-7cycles
Reserved	[7]	Reserved
CECSWAV1	[6:4]	Maximum time to detect start bit rising 000: 3.9ms 001: 3.9ms+1cycle 010: 3.9ms+2cycles 011: 3.9ms+3cycles 100: 3.9ms+4cycles 101: 3.9ms+5cycles 110: 3.9ms+6cycles 111: 3.9ms+7cycles
Reserved	[3]	Reserved
CECSWAV0	[2:0]	Minimum time to detect start bit rising 000: 3.5ms 001: 3.5ms-1cycle 010: 3.5ms-2cycles 011: 3.5ms-3cycles

Register Field	Bit	Description
		100: 3.5ms-4cycles 101: 3.5ms-5cycles 110: 3.5ms-6cycles 111: 3.5ms-7cycles

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6.8.9 CEC Receive Control Register 3 (CECRCTL3: 0x061C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved	CECWAV3[2:0]			Reserved	CECWAV2[2:0]		
Type	RO	R/W			RO	R/W		
Default	0x0	0x0			0x0	0x0		
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved	CECWAV1[2:0]			Reserved	CECWAV0[2:0]		
Type	RO	R/W			R	R/W		
Default	0x0	0x0			0x0	0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B6
Name	Reserved			CECACKEI	CECMINEI	CECMAXEI	CECRSTEI	CECWAVEI
Type	RO			R/W	R/W	R/W	R/W	R/W
Default	0x0			0x0	0x0	0x0	0x0	0x0

Table 6-9 CEC Receive Control Register 3

Register Field	Bit	Description
Reserved	[31:23]	Reserved
CECWAV3	[22:20]	The latest rising timing of logical 0 000: 1.7ms 001: 1.7ms+1cycle 010: 1.7ms+2cycles 011: 1.7ms+3cycles 100: 1.7ms+4cycles 101: 1.7ms+5cycles 110: 1.7ms+6cycles 111: 1.7ms+7cycles
Reserved	[19]	Reserved
CECWAV2	[18:16]	The fastest rising timing of a logical 0 000: 1.3ms 001: 1.3ms-1cycle 010: 1.3ms-2cycles 011: 1.3ms-3cycles 100: 1.3ms-4cycles 101: 1.3ms-5cycles 110: 1.3ms-6cycles 111: 1.3ms-7cycles
Reserved	[15]	Reserved
CECWAV1	[14:12]	The latest rising timing of logical 1 000: 0.8ms 001: 0.8ms+1cycle 010: 0.8ms+2cycles 011: 0.8ms+3cycles 100: 0.8ms+4cycles 101: 0.8ms+5cycles

Register Field	Bit	Description
		110: 0.8ms+6cycles 111: 0.8ms+7cycles
Reserved	[11]	Reserved
CECWAV0	[10:8]	The fastest rising of a logical 1 000: 0.4ms 001: 0.4ms-1cycle 010: 0.4ms-2cycles 111: 0.4ms-3cycles 100: 0.4ms-4cycles 101: 0.4ms-5cycles 110: 0.4ms-6cycles 111: 0.4ms-7cycles
Reserved	[7:5]	Reserved
CECACKEI	[4]	ACK collision error interrupt enable 0: Disable 1: Enable
CECMINEI	[3]	Minimum timing error detection interrupt enable 0: Disable 1: Enable
CECMAXEI	[2]	Maximum timing error detection interrupt enable 0: Disable 1: Enable
CECRSTEI	[1]	Start bit interrupt enable 0: Disable 1: Enable
CECWAVEI	[0]	Waveform error interrupt enable 0: Disable 1: Enable

6.8.10 CEC Transmit Enable Register (CECTEN: 0x0620)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						CECTBusy	CECTEN
Type	RO						RO	R/W
Default	0x0						0x0	0x0

Table 6-10 Audio Data Double Word Count Register 2

Register Field	Bit	Description
Reserved	[15:2]	Reserved
CECTBusy	[1]	CEC transmit state (read only) 0: idle 1: active
CECTEN	[0]	CEC transmission control 0: Disable 1: Enable

6.8.11 CEC Transmit Control Register (CECTCTL: 0x0628)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name					Reserved			
Type					RO			
Default					0x0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved		CECSTRS[2:0]		Reserved		CECSPRD[2:0]	
Type	RO		R/W		RO		R/W	
Default	0x0		0x0		0x0		0x0	
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved		CECDTRS[2:0]				CECDPRD[3:0]	
Type	RO		R/W				R/W	
Default	0x0		0x0				0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name		Reserved		CECBRD			CECFREE[3:0]	
Type		RO		R/W			R/W	
Default		0x0		0x0			0x0	

Table 6-11 CEC Transmit Control Register

Register Field	Bit	Description
Reserved	[31:23]	Reserved
CECSTRS	[22:20]	Rising cycle time of the start bit – between the default values and 0-7 cycles 000: default value (~ 3.7ms) 001: default value – 1 cycle 010: default value – 2 cycles 011: default value – 3 cycles 100: default value – 4 cycles 101: default value – 5 cycles 110: default value – 6 cycles 111: default value – 7 cycles
Reserved	[19]	Reserved
CECSPRD	[18:16]	Start bit cycle time 000: RV 001: RV –1cycle 010: RV –2cycle 011: RV –3cycle 100: RV –4cycle 101: RV –5cycle 110: RV –6cycle 111: RV –7cycle
Reserved	[15]	Reserved
CECDTRS	[14:12]	Rising cycle time of data bit 000: RV 001: RV –1cycle 010: RV –2cycle 011: RV –3cycle 100: RV –4cycle 101: RV –5cycle 110: RV –6cycle

		111: RV –7cycle
CECDPRD	[11:8]	Data bit cycle time 0000: RV 1000: RV – 8 cycles 0001: RV – 1 cycle 1001: RV – 9 cycles 0010: RV – 2 cycles 1010: RV – 10 cycles 0011: RV – 3 cycles 1011: RV – 11 cycles 0100: RV – 4 cycles 1100: RV – 12 cycles 0101: RV – 5 cycles 1101: RV – 13 cycles 0110: RV – 6 cycles 1110: RV – 14 cycles 0111: RV – 7 cycles 1111: RV – 15 cycles
Reserved	[7:5]	Reserved
CECBRD	[4]	Broadcast transmit enable 1'b0: disable 1'b1: enable
CECFREE	[3:0]	Number of cycles for checking the line to be inactive before the start of transmission 0000: 1-bit cycle 1000: 9 bit cycle 0001: 2 bit cycle 1001: 10 bit cycle 0010: 3 bit cycle 1010: 11 bit cycle 0011: 4 bit cycle 1011: 12 bit cycle 0100: 5 bit cycle 1100: 13 bit cycle 0101: 6 bit cycle 1101: 14 bit cycle 0110: 7 bit cycle 1110: 15 bit cycle 0111: 8 bit cycle 1111: 16 bit cycle

6.8.12 CEC Receive Interrupt Status Register (CECRSTAT: 0x062C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	CECRIWA	CECRIOR	CECRIACK	CECRIMIN	CECRIMAX	CECRISTA	CECRIEND
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0x0	0x0	0x0	0x0	0x0	0x2	0x0	0x0

Table 6-12 CEC Receive Interrupt Status Register

Register Field	Bit	Description
Reserved	[15:7]	Reserved
CECRIWA	[6]	CEC Waveform error interrupt flag
CECRIOR	[5]	Receive buffer full flag
CECRIACK	[4]	ACK collision detection flag
CECRIMIN	[3]	Bit cycle time is less than minimum time flag
CECRIMAX	[2]	Bit cycle time is greater than maximum time flag
CECRISTA	[1]	Start bit detection flag
CECRIEND	[0]	Reception of CEC message with EOM

6.8.13 CEC Transmit Interrupt Status Register (CECTSTAT: 0x0630)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		CECTIUR	CECTIACK	CECTIAL	CECTIEND	Reserved	
Type	RO		RO	RO	RO	RO	RO	
Default	0x0		0x0	0x0	0x0	0x0	0x0	

Table 6-13 Interrupt Flag Register

Register Field	Bit	Description
Reserved	[15:5]	Reserved
CECTIUR	[4]	Transmission is completed and the transmit buffer is empty
CECTIACK	[3]	ACK error detection flag
CECTIAL	[2]	Arbitration loss flag ("0" is detected while transmit "1")
CECTIEND	[1]	Data block transmission completion flag
Reserved	[0]	Reserved

6.8.14 CEC Receive Buffer Registers (01-16) (CECRBUF01-16: 0x0634-0x0670)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						CECRACK	CECEOM
Type	RO						RO	RO
Default	0x0						0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CECRBYTE[7:0]							
Type	RO							
Default	0x0							

Table 6-14 CEC Receive Buffer Registers (01-16)

Register Field	Bit	Description
Reserved	[15:10]	Reserved
CECRACK	[9]	ACK bit received
CECEOM	[1]	EOM bit received
CECRBYTE	[7:0]	CEC byte received

6.8.15 CEC Transmit Buffer Registers (01-16) (CECTBUF01-16: 0x0674-0x06B0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							CECTEOM
Type	RO							R/W
Default	0x0							0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CECTBYTE[7:0]							
Type	R/W							
Default	0x0							

Table 6-15 CEC Transmit Buffer Registers (01-16)

Register Field	Bit	Description
Reserved	[15:9]	Reserved
CECTEOM	[8]	EOM bit value to be transmitted
CECTBYTE	[7:0]	Byte data to be transmitted

6.8.16 CEC Receive Byte Counter Register (CECRCTR: 0x06B4)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name					Reserved			
Type					RO			
Default					0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name		Reserved					CECRCTR[4:0]	
Type		RO					RO	
Default		0x0					0x0	

Table 6-16 Interrupt Flag Register

Register Field	Bit	Description
Reserved	[15:5]	Reserved
CECRCTR	[4:0]	Numbers of bytes received

6.8.17 CEC Interrupt Enable Register (CECIMSK: 0x06C0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					CECTIM	CECRIM	
Type	RO					R/W	R/W	
Default	0x0					0x0	0x0	

Table 6-17 CEC Interrupt Enable Register

Register Field	Bit	Description
Reserved	[15:2]	Reserved
CECTIM	[1]	CEC Transmit status interrupt enable 1'b0: disable 1'b1: enable
CECRIM	[0]	CEC Receive status interrupt enable 1'b0: disable 1'b1: enable

6.8.18 CEC Interrupt Clear Register (CECICLR: 0x06CC)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					CECTClr	CECRCIrl	
Type	RO					WO	WO	
Default	0x0					0x0	0x0	

Table 6-18 CEC Interrupt Enable Register

Register Field	Bit	Description
Reserved	[15:2]	Reserved
CECTIM	[1]	Host writes “1” to this bit to clear CEC Transmit status interrupt
CECRIM	[0]	Host writes “1” to this bit to clear CEC Receive status interrupt

6.9 Splitter Control Registers

6.9.1 STX0_CTRL (STX0_CTRL:0x5000)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							Stx0_spbp
Type	RO							R/W
Default	0x0							0x1
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							Stx0_ifen
Type	RO							R/W
Default	0x0							0x0

Register Field	Bit	Description
Reserved	[15:9]	Reserved
Stx0_spbp	[8]	STX0 Splitter bypass 0: Enable Split 1: Bypass
Reserved	[7:2]	Reserved
stx0_ifen	[1]	CDSITX 0 InfoFrame Enable 1'b0: Do not send InfoFrame data out to CSI2-TX0 1'b1: Send InfoFrame data out to CSI2-TX0
Stx0_lcd_csel	[0]	STX0 LCD Controller Clock Select (CSITX0 video path) 0: 2 x CSI Clock (Default) 1: 1 x CSI Clock

6.9.2 STX0 Packet ID Register 1 (STX0_PacketID1: 0x5002)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Stx0_VPID1							
Type	R/W							
Default	0x34							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Stx0_VPID0							
Type	R/W							
Default	0x35							

Register Field	Bit	Description
Stx0_VPID1	[15:8]	CDSITX0 Video Packet ID 1 Note: For interlace mode only, this ID is for Bottom video field.
Stx0_VPID0	[7:0]	CDSITX0 Video Packet ID 0 Note: For interlace mode only, this ID is for Top video field

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6.9.3 STX0 Packet ID Register 2 (STX0_PacketID2: 0x5004)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Stx0_IFPID							
Type	R/W							
Default	0x36							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Stx0_APID							
Type	R/W							
Default	0x37							

Register Field	Bit	Description
stx0_ifpid	[15:8]	CDSITX0 InfoFrame Packet ID
Stx0_APID	[7:0]	CDSITX0 CSI Audio Packet ID (Same pkt. ID is used for SPDIF as I2S over CSI) – This function is not supported.

6.9.4 STX0 Packet ID Register 3 (STX0_PacketID3: 0x5006)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	stx0_vpid2							
Type	R/W							
Default	0x24							

Register Field	Bit	Description
Reserved	[15:8]	
stx0_vpid2	[7:0]	CDSITX0 Video Packet ID Note: Use for YCbCr 12-bit video data format and when YCbCrFmt[1:0] = 2'b10

6.9.5 STX0_WC (STX0_WC:0x5008)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	stx0_wc							
Type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	stx0_wc							
Type	R/W							
Default	0x0							

Register Field	Bit	Default	Description
stx0_wc	[15:0]	0x0	Splitter TX0 Line Word Count Defined total number of byte for each line. Note: only valid when stc0_wc is not equal to "0". Else TX WC is directly from HDMIRX source if only stx0_ehw = "1"

6.9.6 STX0_DPX (STX0_DPX:0x500A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved		stx0_de_px					
Type	RO		R/W					
Default	0x0		0x0					
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		stx0_db_px					
Type	RO		R/W					
Default	0		0x0					

Register Field	Bit	Default	Description
Reserved	[15:14]	0x0	
stx0_de_px	[13:8]	0x0	Splitter TX0 End Dummy Pixel 6'h00: No dummy pixel inserted 6'h01: Dummy pixel inserted 6'h2x: 32 Dummy pixels inserted (maximum) Note: These Dummy pixels inserted at the end of the line
Reserved	[7:6]	0x0	
stx0_db_px	[5:0]	0x0	Splitter TX0 Beginning Dummy Pixel 6'h00: No dummy pixel inserted 6'h01: Dummy pixel inserted 6'h2x: 32 Dummy pixels inserted (maximum) Note: These Dummy pixels inserted at the beginning of the line

6.9.7 STX0_FPX (STX0_FPX:0x500C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Stx_ehw	Stx_hsel	Reserved			stx_fpxv		
Type	R/W	R/W	RO			R/W		
Default	0x1	0x0	0x0			0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	stx0_fpxv							
Type	R/W							
Default	0x0							

Register Field	Bit	Default	Description
stx_ehw	[15]	0x0	Splitter TX HW enable 0: Select Manual setting (used stx0/1_fpxv, stx0/1_lpx parameters) 1: automatically split line into half for both stx0 and stx1
stx_hsel	[14]	0x0	Splitter TX L/R select 0: Select 1 st half of the line for STX0, 2 nd half for STX1 1: Select 2 nd half of the line for STX0, 1 st half for STX1 Note: 1) only valid when stx_ehw = 1 2) if stx_hsel=0 - stx0_db_px indicates # Dummy pixel inserted at beginning - stx0_de_px indicates # pixels overlap at the end (not Dummy pixel) if stx_hsel=1 - stx0/1_db_px indicates # pixels overlap at the beginning (Not Dummy pixel) - stx0/1_de_px indicates # Dummy pixels inserted at the end
Reserved	[13:12]	0x0	
stx0_fpxv	[11:0]	0x0	Splitter TX0 First Pixel Valid 12'h000: 1 st pixel in HDMIRX line 12'h001: 2 nd pixel in HDMIRX line 12'hFFF: 4096 pixel in HDMIRX line Note: Note: This parameter indicates the first pixel location to transmit to CDSITX0

6.9.8 STX0_LPX (STX0_LPX:0x500E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				stx0_lpxv			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	stx0_lpxv							
Type	R/W							
Default	0x0							

Register Field	Bit	Default	Description
Reserved	[15:12]	0x0	
stx0_lpxv	[11:0]	0x0	Splitter TX0 Last Pixel Valid 12'h000: 1 st pixel in HDMIRX line 12'h001: 2 nd pixel in HDMIRX line 12'hFFF: 4096 pixel in HDMIRX line Note: This parameter indicates the last pixel location to transmit to CDSITX0

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6.9.9 STX0_DRPX (STX0_DRPX:0x5010)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	stx0_dRpx							
Type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	stx0_dRpx							
Type	R/W							
Default	0x0							

Register Field	Bit	Default	Description
stx0_dRpx	[15:0]	0x0	TX0 Red Dummy Pixel

6.9.10 STX0_DGPX (STX0_DGPX:0x5012)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	stx0_dGpx							
Type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	stx0_dGpx							
Type	R/W							
Default	0x0							

Register Field	Bit	Default	Description
stx0_dGpx	[15:0]	0x0	TX0 Green Dummy Pixel

6.9.11 STX1_CTRL (STX1_CTRL:0x5080)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							Stx1_spbp
Type	RO							R/W
Default	0x0							0x1
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							Stx1_ifen Stx1_lcd_csel
Type	RO							R/W R/W
Default	0x0							0x0 0x0

Register Field	Bit	Description
Reserved	[15:9]	Reserved
Stx1_spbp	[8]	STX1 Splitter bypass

		0: Enable Split 1: Bypass
Reserved	[7:2]	Reserved
Stx1_ifen	[1]	CDSITX1 InfoFrame Enable 1'b0: Do not send InfoFrame data out to CSI2-TX0 1'b1: Send InfoFrame data out to CSI2-TX0
Stx1_lcd_csel	[0]	STX1 LCD Controller Clock Select (CSITX0 video path) 0: 2 x CSI Clock (Default) 1: 1 x CSI Clock

6.9.12 STX1 Packet ID Register 1 (STX1_PacketID1: 0x5082)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Stx1_VPID1							
Type	R/W							
Default	0x34							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Stx1_VPID0							
Type	R/W							
Default	0x35							

Register Field	Bit	Description
Stx1_VPID1	[15:8]	CDSITX1 Video Packet ID 1 Note: For interlace mode only, this ID is for Bottom video field.
Stx1_VPID0	[7:0]	CDSITX1 Video Packet ID 0 Note: For interlace mode only, this ID is for Top video field

6.9.13 STX0_DBPX (STX0_DBPX:0x5014)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	stx0_dbpx							
Type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	stx0_dbpx							
Type	R/W							
Default	0x0							

Register Field	Bit	Default	Description
stx0_dbpx	[15:0]	0x0	TX0 Blue Dummy Pixel

6.9.14 STX1 Packet ID Register 2 (STX1_PacketID2: 0x5084)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Stx1_IFPID							
Type	R/W							
Default	0x36							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Stx1_APID							
Type	R/W							
Default	0x37							

Register Field	Bit	Description
Stx1_ifpid	[15:8]	CDSITX1 InfoFrame Packet ID
Stx1_APID	[7:0]	CDSITX1 CSI Audio Packet ID (Same pkt. ID is used for SPDIF as I2S over CSI) – This function is not supported.

6.9.15 STX1 Packet ID Register 3 (STX1_PacketID3: 0x5086)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Stx1_vpid2							
Type	R/W							
Default	0x24							

Register Field	Bit	Description
Reserved	[15:8]	
Stx1_vpid2	[7:0]	CDSITX1 Video Packet ID Note: Use for YCbCr 12-bit video data format and when YCbCrFmt[1:0] = 2'b10

6.9.16 STX1_WC (STX1_WC:0x5088)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Stx1_wc							
Type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Stx1_wc							
Type	R/W							
Default	0x0							

Register Field	Bit	Default	Description
Stx1_wc	[15:0]	0x0	Splitter TX1 Line Word Count Defined total number of byte for each line. Note: only valid when Note: only valid when stc1_wc is not equal to "0". Else TX WC is directly from HDMIRX source if only stx1_ehw = "1"

6.9.17 STX1_DPX (STX1_DPX:0x508A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved		Stx1_de_px					
Type	RO		R/W					
Default	0x0		0x0					
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		Stx1_db_px					
Type	RO		R/W					
Default	0		0x0					

Register Field	Bit	Default	Description
Reserved	[15:14]	0x0	
Stx1_de_px	[13:8]	0x0	Splitter TX0 End Dummy Pixel 6'h00: No dummy pixel inserted 6'h01: Dummy pixel inserted 6'h2x: 32 Dummy pixels inserted (maximum) Note: These Dummy pixels inserted at the end of the line
Reserved	[7:6]	0x0	
Stx1_db_px	[5:0]	0x0	Splitter TX1 Beginning Dummy Pixel 6'h00: No dummy pixel inserted 6'h01: Dummy pixel inserted 6'h2x: 32 Dummy pixels inserted (maximum) Note: These Dummy pixels inserted at the beginning of the line

6.9.18 STX1_FPX (STX1_FPX:0x508C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				Stx1_fpxv			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Stx1_fpxv				R/W			
Type								
Default	0x0							

Register Field	Bit	Default	Description
Reserved	[15:12]	0x0	
Stx1_fpxv	[11:0]	0x0	<p>Splitter TX1 First Pixel Valid</p> <p>12'h000: 1st pixel in HDMIRX line 12'h001: 2nd pixel in HDMIRX line 12'hFFF: 4096 pixel in HDMIRX line</p> <p>Note: Note: This parameter indicates the first pixel location to transmit to CDSITX1</p>

6.9.19 STX1_LPX (STX1_LPX:0x508E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				Stx1_lpxv			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	stx0_lpxv				R/W			
Type								
Default	0x0							

Register Field	Bit	Default	Description
Reserved	[15:12]	0x0	
Stx1_lpxv	[11:0]	0x0	<p>Splitter TX1 Last Pixel Valid 12'h000: 1st pixel in HDMIRX line 12'h001: 2nd pixel in HDMIRX line 12'hFFF: 4096 pixel in HDMIRX line</p> <p>Note: This parameter indicates the last pixel location to transmit to CDSITX1</p>

6.9.20 STX1_DRPX (STX1_DRPX:0x5090)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	stx1_dRpx							
Type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	stx1_dRpx							
Type	R/W							
Default	0x0							

Register Field	Bit	Default	Description
stx1_dRpx	[15:0]	0x0	TX1 Red Dummy Pixel

6.9.21 STX1_DGPX (STX1_DGPX:0x5092)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	stx1_dGpx							
Type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	stx1_dGpx							
Type	R/W							
Default	0x0							

Register Field	Bit	Default	Description
stx1_dRpx	[15:0]	0x0	TX1 Green Dummy Pixel

6.9.22 STX1_DBPX (STX1_DBPX:0x5094)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	stx1_dBpx							
Type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	stx1_dBpx							
Type	R/W							
Default	0x0							

Register Field	Bit	Default	Description
stx1_dBpx	[15:0]	0x0	TX1 Blue Dummy Pixel

6.10 Internal Color Bar Generator

6.10.1 Color Bar Control Register 0 (CB_CTRL0: 0x7000)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				cb_csel	cb_type	cb_en	
Type	RO				RW	RW	RW	
Default	0x0				0x0	0x0	0x0	

Register Field	Bit	Description
Reserved	[15:4]	
Cb_clksel	[3]	Color Bar Clock Select 0: CSITX0 Byte clock 1: CSITX1 Byte clock
Cb_clksel	[2:1]	Color Bar Type 00: Normal operation 01: Solid color mode 10: Color bar mode 11: Color Checkers mode
Cb_en	[0]	Color Bar Enable 0: Disable 1: Enable

6.10.2 Color Bar Control Register 1 (CB_CTRL1: 0x7002)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	cb_blue							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cb_blue							
Type	RW							
Default	0x0							

Register Field	Bit	Description
Cb_blue	[15:0]	Color Bar – Blue color

6.10.3 Color Bar Control Register 2 (CB_CTRL2: 0x7004)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	cb_green							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cb_green							
Type	RW							
Default	0x0							

Register Field	Bit	Description
Cb_green	[15:0]	Color Bar – Green color

6.10.4 Color Bar Control Register 3 (CB_CTRL3: 0x7006)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	cb_red							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cb_red							
Type	RW							
Default	0x0							

Register Field	Bit	Description
Cb_red	[15:0]	Color Bar – Red color

6.10.5 Color Bar Control Register 4 (CB_CTRL4: 0x7008)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved	cb_hs_width						
Type	RO	RW						
Default	0x0	0x0						
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cb_hs_width							
Type	RW							
Default	0x0							

Register Field	Bit	Description
Reserved	[15]	
Cb_hs_width	[14:0]	Color Bar – HS Width

6.10.6 Color Bar Control Register 5 (CB_CTRL5: 0x700A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved	cb_vs_width						
Type	RO	RW						
Default	0x0	0x0						
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cb_vs_width							
Type	RW							
Default	0x0							

Register Field	Bit	Description
Reserved	[15]	
Cb_vs_width	[14:0]	Color Bar – VS Width

6.10.7 Color Bar Control Register 6 (CB_CTRL6: 0x700C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	cb_h_total							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cb_h_total							
Type	RW							
Default	0x0							

Register Field	Bit	Description
Cb_h_total	[15:0]	Color Bar – H Total

6.10.8 Color Bar Control Register 7 (CB_CTRL7: 0x700D)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	cb_v_total							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cb_v_total							
Type	RW							
Default	0x0							

Register Field	Bit	Description
Cb_v_total	[15:0]	Color Bar – V Total

6.10.9 Color Bar Control Register 8 (CB_CTRL8: 0x7010)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	cb_h_act							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cb_h_act							
Type	RW							
Default	0x0							

Register Field	Bit	Description
Cb_h_act	[15:0]	Color Bar – H Active

6.10.10 Color Bar Control Register 9 (CB_CTRL9: 0x7012)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	cb_v_act							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cb_v_act							
Type	RW							
Default	0x0							

Register Field	Bit	Description
Cb_v_act	[15:0]	Color Bar – V Active

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Color Bar Control Register 10 (CB_CTRL10: 0x7014)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	cb_h_start							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cb_h_start							
Type	RW							
Default	0x0							

Register Field	Bit	Description
cb_h_start	[15:0]	Color Bar – H Start

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Color Bar Control Register 11 (CB_CTRL11: 0x7016)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	cb_v_start							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cb_v_start							
Type	RW							
Default	0x0							

Register Field	Bit	Description
cb_v_start	[15:0]	Color Bar – V Start

6.10.13 Debug Control Register (DebCtl: 0x7080)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						db_clko	Reserved
Type	RO						R/W	RO
Default	0x0						0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	vworden	Reserved						
Type	R/W	RO						
Default	0x0	0x0						

Register Field	Bit	Description
Reserved	[15:11]	
db_clko	[10]	Debug clock output
Reserved	[9:8]	
vworden	[7]	Video Word count enable 0: normal 1: used Video word count register for CSITX word count
Reserved	[6:0]	

6.10.14 H2C Self Check Register1 (SchkReg1: 0x7084)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	hpdi_st	hpdi_tg	ir_st	ir_tg	cec_st	cec_tg	test_st	rst_tg
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	??	??	??	??	??	??	??	??
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							stst_en
Type	RO							R/W
Default	0x0							0x0

Table 6-19 Self Check Register1

Register Field	Bit	Description
hdpi_st	[15]	HPDI pin status
hdpi_tg	[14]	HPDI toggle status
ir_st	[13]	IR Pin status
ir_tg	[12]	IR toggle status 0: not toggle 1: detect IR toggle
cec_st	[11]	CEC Pin status
cec_tg	[10]	CEC toggle status 0: not toggle 1: detect CEC toggle
test_st	[9]	TEST Pin status Read TEST pin status
rst_tg	[8]	RESETN toggle status 0: Not toggle 1: Toggle Must Write "1" first then toggle RESET pin
Reserved	[7:1]	
stst_en	[0]	Self Check Enable 0: Disable 1: Enable

6.10.15

H2C Self Check Register2 (SchkReg2: 0x7086)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	asc_d							
Type	R/W							
Default	0x5A							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ddc_st							
Type	RO							
Default	0x0							

Table 6-20 Self Check Register1

Register Field	Bit	Description
asc_d	[15:8]	Audio Self Check Data - Channel 0 Left data = {asc_d,asc_d,asc_d,asc_d} - Channel 0 Right data = Inverted of Channel 0 Left data - Channel 1 Left data = Channel 0 Left data shift left by 1 (MSB → LSB) - Channel 1 Right data = Inverted Channel 1 Left data - Channel 2 Left data = Channel 1 Left data data shift left by 1 (MSB → LSB) - Channel 2 Right data = Inverted Channel 1 Left data - Channel 3 Left data = Channel 2 Left data shift left by 1 (MSB → LSB) - Channel 3 Right data = Inverted Channel 1 Left data
ddc_st	[7:0]	DDC first byte status

6.11 HDMI Rx System Control

6.11.1 INTERRUPT0 REGISTER (HDMI_INT0) (0x8500)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_KEY	Reserved					I_MISC	Reserved
Type	RO	RO					RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_KEY	7	0	KEY-EDID (address 0x85_0F) interrupt 0: No interrupt, 1: Interrupt generated
I_MISC	1	0	MISC (address 0x85_0B) interrupt 0: No interrupt, 1: Interrupt generated

6.11.2 INTERRUPT1 REGISTER (HDMI_INT1) (0x8501)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_GBD	I_HDCP	I_ERR	I_AUD	I_CBIT	I_PACKET	I_CLK	I_SYS
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_GBD	7	0	GBD (address 0x85_09) interrupt 0: No interrupt, 1: Interrupt generated
I_HDCP	6	0	HDCP (address 0x85_08) interrupt 0: No interrupt, 1: Interrupt generated
I_ERR	5	0	ERR (address 0x85_07) interrupt 0: No interrupt, 1: Interrupt generated
I_AUD	4	0	Audio Buffer (address 0x85_06) interrupt 0: No interrupt, 1: Interrupt generated
I_CBIT	3	0	Audio CBIT (address 0x85_05) interrupt 0: No interrupt, 1: Interrupt generated
I_PACKET	2	0	Info Packet (address 0x85_04) interrupt 0: No interrupt, 1: Interrupt generated
I_CLK	1	0	Pixel CLK (address 0x85_03) interrupt 0: No interrupt, 1: Interrupt generated
I_SYS	0	0	SYSTEM (address 0x85_02) interrupt 0: No interrupt, 1: Interrupt generated

6.11.3 SYSTEM INTERRUPT (SYS_INT) (0x8502)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_ACR_CTS	I_ACRN	I_DVI	I_HDMI	I_NOPMBDET	I_DPMBDET	I_TMDS	I_DDC
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_ACR_CTS	7	0	Receive CTS update interrupt 0: No interrupt 1: Interrupt generated
I_ACRN	6	0	Receive N update interrupt 0: No interrupt 1: Interrupt generated
I_DVI	5	0	HDMI→DVI change detection interrupt 0: No interrupt 1: Interrupt generated
I_HDMI	4	0	DVI→HDMI change detection interrupt 0: No interrupt 1: Interrupt generated
I_NOPMBDET	3	0	No Datasland Preamble detection interrupt 0: No interrupt 1: Interrupt generated
I_DPMBDET	2	0	With Datasland Preamble detection interrupt 0: No interrupt 1: Interrupt generated
I_TMDS	1	0	TMDS amplitude change interrupt 0: No interrupt 1: Presence change detected (PHY squelch ON/OFF changeddetected)
I_DDC	0	0	DDC power change detection interrupt 0: No interrupt 1: 0V↔5V change detected

6.11.4 CLOCK INTERRUPT (CLK_INT) (0x8503)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_OUT_D_E_CHG	I_OUT_H_CHG	I_IN_DE_CHG	I_IN_HV_CHG	I_DC_CHG	I_PXCLK_CHG	I_PHYCLK_CHG	I_TMDSC_LK_CHG

Type	W1C/R							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_OUT_DE_CHG	7	0	(Output side) DE size and position change detection interrupt 0: No interrupt 1: Interrupt generated
I_OUT_H_CHG	6	0	(Output side) H counter change detection interrupt 0: No interrupt 1: Interrupt generated
I_IN_DE_CHG	5	0	(Input side) DE size and position change detection interrupt 0: No interrupt 1: Interrupt generated
I_IN_HV_CHG	4	0	(Input side) HV counter change detection interrupt 0: No interrupt 1: Interrupt generated
I_DC_CHG	3	0	Deep Color mode change detection interrupt 0: No interrupt 1: Interrupt generated
I_PXCLK_CHG	2	0	Pixel CLK change detection interrupt 0: No interrupt 1: Interrupt generated
I_PHYCLK_CHG	1	0	PHY PLL CLK change detection interrupt 0: No interrupt 1: Interrupt generated
I_TMDSCLK_CHG	0	0	TMDS CLK change detection interrupt 0: No interrupt 1: Interrupt generated

6.11.5 PACKET INTERRUPT (PACKET_INT) (0x8504)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_PK_ISRC_2	I_PK_ISRC	I_PK_ACP	I_PK_VS	I_PK_SPD	I_PK_MS	I_PK_AUD	I_PK_AVI
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
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I_PK_ISRC2	7	0	ISRC2 packet update interrupt 0: No interrupt, 1: Interrupt generated
I_PK_ISRC	6	0	ISRC1 packet update interrupt 0: No interrupt, 1: Interrupt generated
I_PK_ACP	5	0	ACP packet update interrupt 0: No interrupt, 1: Interrupt generated
I_PK_VS	4	0	861B VS_info packet update interrupt 0: No interrupt, 1: Interrupt generated
I_PK_SPD	3	0	861B SPD_info packet update interrupt 0: No interrupt, 1: Interrupt generated
I_PK_MS	2	0	861B MS_info packet update interrupt 0: No interrupt, 1: Interrupt generated
I_PK_AUD	1	0	861B AUD_info packet update interrupt 0: No interrupt, 1: Interrupt generated
I_PK_AVI	0	0	861B AVI_info packet update interrupt 0: No interrupt, 1: Interrupt generated

※ Interrupt is generated only when receive content has changed.

If the same data is repeatedly received, interrupt is not generated.

6.11.6 CBIT INTERRUPT (CBIT_INT) (0x8505)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_AF_LOCK	I_AF_UNLOCK	Reserved	I_AU_DS_D	I_AU_HBR	I_CBIT_NLPCM	I_CBIT_FS	I_CBIT
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_AF_LOCK	7	0	Audio clock frequency lock detection interrupt 0: No interrupt 1: Interrupt generated
I_AF_UNLOCK	6	0	Audio clock frequency unlock detection interrupt 0: No interrupt 1: Interrupt generated

Reserved	5	0	
I_AU_DSD	4	0	DSD packet detection interrupt 0: No interrupt 1: Interrupt generated
I_AU_HBR	3	0	HBR packet detection interrupt 0: No interrupt 1: Interrupt generated
I_CBIT_NLPCM	2	0	Normal Audio LPCM↔NLPCM change detection interrupt 0: No interrupt 1: Interrupt generated
I_CBIT_FS	1	0	Receive data FS update interrupt 0: No interrupt 1: Interrupt generated
I_CBIT	0	0	Receive C_bit data [47:0] update interrupt 0: No interrupt 1: Interrupt generated

6.11.7 AUDIO Buffer INTERRUPT (AUDIO_INT) (0x8506)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_BUF_O VER	I_BUF_N O2	I_BUF_N O1	I_BUF_CE NTER	I_BUF_N U1	I_BUF_N U2	I_BUF_U NDER	I_BUFINI T_END
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_BUF_OVER	7	0	Buffer Over flow detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_NO2	6	0	Buffer Nearly Over (threshold 2) detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_NO1	5	0	Buffer Nearly Over (threshold 1) detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_CENTER	4	0	Buffer CENTER detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_NU1	3	0	Buffer Nearly Under (threshold 1) detection interrupt 0: No interrupt 1: Interrupt generated

I_BUF_NU2	2	0	Buffer Nearly Under (threshold 2) detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_UNDER	1	0	Buffer Under flow detection interrupt 0: No interrupt 1: Interrupt generated
I_BUFINIT_END	0	0	Buffer initial operation completed interrupt 0: No interrupt 1: Interrupt generated

6.11.8 ERROR INTERRUPT (ERR_INT) (0x8507)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_EESS_ERR	I_AU_FRAME	I_NO_ACP	I_NO_AVI	I_DC_NOCD	I_DC_DEERR	I_DC_BUERR	I_DC_PPERR
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_EESS_ERR	7	0	EESS error generation detection interrupt ×1 [6] W1C/R 1'b0 0: No interrupt 1: Interrupt generate
I_AU_FRAME	6	0	60958Frame discontinuous change detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_ACP	5	0	ACP Packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_AVI	4	0	AVI Packet receive cut detection interrupt 0: No interrupt 1: Interrupt generated
I_DC_NOCD	3	0	Deep Color CD=0 (or not defined) generates 24bit mode auto move 0: No interrupt 1: Interrupt generated
I_DC_DEERR	2	0	In Deep Color Packing Group, DE position abnormal generation 0: No interrupt 1: Interrupt generated
I_DC_BUERR	1	0	Deep Color FIFO flow generation 0: No interrupt 1: Interrupt generated
I_DC_PPERR	0	0	Deep Color UnPack phase dis-unified generation 0: No interrupt 1: Interrupt generated

※1 During HDMI(=EESS) mode, detects state where Enc_Disable, Enc_Enable can no longer be detected during HDCP decoding operation.

Used for detecting the abnormal state where HDCP goes OFF without te send side sending Enc_Disable.

6.11.9 HDCP INTERRUPT (HDCP_INT) (0x8508)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_AVM_S ET	I_AVM_C LR	I_LINKER R	I_SHA_E ND	I_RO_EN D	I_KM_EN D	I_AKSV_E ND	I_AN_EN D
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_AVM_SET	7	0	SET AVMUTE receive interrupt 0: No receive, 1: With receive
I_AVM_CLR	6	0	CLRAE AVMUTE receive interrupt 0: No receive, 1: With receive
I_LINKERR	5	0	Link error detection interrupt ※1 0: No link error 1: Link error generated
I_SHA_END	4	0	V' value operation ended interrupt 0: During idle or operation 1: Operation ended
I_RO_END	3	0	Ks', M0', R0' operation ended interrupt 0: During idle or operation 1: Operation ended
I_KM_END	2	0	Km' operation ended interrupt 0: During idle or operation 1: Operation ended
I_AKSV_END	1	0	AKSV write completed interrupt 0: During idle or write 1: Write completed notification
I_AN_END	0	0	AN write completed interrupt 0: During idle or write 1: Write completed notification

※1 This interrupt is generated when other device termination of HDCP encoding is detected.

(Detects IDLE State after HDCP certification No.3 part)

However, it may be set up even during HDMI SET_AVMUTE.

6.11.10 GBD INTERRUPT (GBD_INT) (0x8509)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_GBD_P KERR	I_GBD_A CLR	I_P1GBD _CHG	I_P0GBD _CHG	Reserved	I_P1GBD _DET	I_GBD_O FF	I_GBD_O N
Type	W1C/R	W1C/R	W1C/R	W1C/R	RO	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_GBD_PKERR	7	0	GBD packet receive ERR generation interrupt 0: No interrupt 1: Interrupt generated
I_GBD_ACLR	6	0	GBD packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated (cutoff generated)
I_P1GBD_CHG	5	0	Valid P1 GBD update interrupt 0: No interrupt 1: Interrupt generated (GBD-RAM update generated)
I_P0GBD_CHG	4	0	Valid P0 GBD update interrupt 0: No interrupt 1: Interrupt generated (GBD-RAM update generated)
I_P1GBD_DET	2	0	P1 GBD data receive generation interrupt 0: No interrupt 1: Interrupt generated 【Note】 Not related to change in packet content, generated each time packet is received.
I_GBD_OFF	1	0	Valid GBD yes→no change generation interrupt 0: No interrupt 1: Interrupt generated
I_GBD_ON	0	0	Valid GBD no→yes change generation interrupt 0: No interrupt 1: Interrupt generated

6.11.11 MISC INTERRUPT (MISC_INT) (0x850b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_AU_DS D_OFF	I_AU_HB R_OFF	I_VIDEO_ COLOR	I_AS_LAY OUT	I_NO_SP D	I_NO_VS	I_SYNC_C HG	I_AUDIO _MUTE
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_AU_DSD_OFF	7	0	Discontinuity of DSD packet detection interrupt 0: No interrupt 1: Interrupt generated
I_AU_HBR_OFF	6	0	Discontinuity of HBR packet detection interrupt 0: No interrupt 1: Interrupt generated
I_VIDEO_COLOR	5	0	Video Color Space (RGB, YCbCr444, YCbCr422) change detection interrupt 0: No interrupt 1: Interrupt generated
I_AS_LAYOUT	4	0	audio Layout Bit change detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_SPD	3	0	SPD_Info packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_VS	2	0	VS_Info packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated
I_SYNC_CHG	1	0	Video sync signal state change detection interrupt 0: No interrupt 1: Interrupt generated
I_AUDIO_MUTE	0	0	Audio MUTE generation interrupt 0: No interrupt 1: Interrupt generated

6.11.12 SYS INTERRUPT MASK (SYS_INTM) (0x8512)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_ACR_CTS	M_ACR_N	M_DVI_DET	M_HDMI_DET	M_NOP_MBDT	M_BPMB_DET	M_TMDS	M_DDC
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_ACR_CTS	7	1	Receive CTS update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_ACR_N	6	1	Receive N value update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

M_DVI_DET	5	1	HDMI→DVI change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_HDMI_DET	4	1	DVI→HDMI change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_NOPMBDET	3	1	No Datasland Preamble detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BPMBDET	2	1	With Datasland Preamble detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_TMDS	1	1	TMDS amplitude change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_DDC	0	1	DDC power change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

6.11.13 CLK INTERRUPT MASK (CLK_INTM) (0x8513)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	M_OUT_H_CHG	M_IN_DE_CHG	M_IN_HV_CHG	M_DC_C_HG	M_PXCLK_CHG	M_PHYCLK_CHG	M_TMDS_CHG
Type	R	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
Reserved	7	1	
M_OUT_H_CHG	6	1	(Output side) H counter change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_IN_DE_CHG	5	1	(Input side) DE size and position change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_IN_HV_CHG	4	1	(Input side) HV counter change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_DC_CHG	3	1	Deep Color change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

M_PXCLK_CHG	2	1	Pixel CLK change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PHYCLK_CHG	1	1	PHY PLL CLK change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_TMDS_CHG	0	1	TMDS CLK change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

6.11.14 PACKET INTERRUPT MASK (PACKET_INTM) (0x8514)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_PK_ISRC2	M_PK_ISRC	M_PK_ACP	M_PK_VS	M_PK_SPD	M_PK_MS	M_PK_AUD	M_PK_AVI
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_PK_ISRC2	7	1	ISRC2 packet receive interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PK_ISRC	6	1	ISRC1 packet receive interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PK_ACP	5	1	ACP packet receive interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PK_VS	4	1	861B VS_info packet update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PK_SPD	3	1	861B SPD_info packet update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PK_MS	2	1	861B MS_info packet update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PK_AUD	1	1	861B AUD_info packet update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PK_AVI	0	1	861B AVI_info packet update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

6.11.15 CBIT INTERRUPT MASK (CBIT_INTM) (0x8515)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_AF_LO CK	M_AF_U NLOCK	Reserved	M_AU_D SD	M_AU_H BR	M_CBIT_ NLPCM	M_CBIT_ FS	M_CBIT
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_AF_LOCK	7	1	Audio clock frequency lock detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AF_UNLOCK	6	1	Audio clock frequency unlock detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
Reserved	5	1	
M_AU_DSD	4	1	DSD Audio packet receive detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AU_HBR	3	1	HBR Audio packet receive detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_CBIT_NLPCM	2	1	Receive data LPCM↔NLPCM change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_CBIT_FS	1	1	Receive data FS update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_CBIT	0	1	Receive C_bit data [39:0] update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

6.11.16 AUDIO INTERRUPT MASK (AUDIO_INTM) (0x8516)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_BUF_ OVER	M_BUF_ NO2	M_BUF_ NO1	M_BUF_ CENTER	M_BUF_ NU1	M_BUF_ NU2	M_BUF_ UNDER	M_BUFIN IT_END
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_BUF_OVER	7	1	Buffer Over flow detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BUF_NO2	6	1	Buffer Nearly Over (Threshold 2) detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BUF_NO1	5	1	Buffer Nearly Over (Threshold 1) detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BUF_CENTER	4	1	Buffer CENTER detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BUF_NU1	3	1	Buffer Nearly Under (Threshold 1) detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BUF_NU2	2	1	Buffer Nearly Under (Threshold 2) detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BUF_UNDER	1	1	Buffer Under flow detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BUFINIT_END	0	1	Buffer initialization operation completed interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

6.11.17 ERR INTERRUPT MASK (ERR_INTM) (0x8517)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_EESS_ERR	M_AU_FRAME	M_NO_ACP	M_NO_AVI	M_DC_NOCD	M_DC_DEERR	M_DC_BUFERR	M_DC_PPERR
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_EESS_ERR	7	1	EES error occurrence detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AU_FRAME	6	1	Audio 60958Frame discontinuous detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_NO_ACP	5	1	ACP packet receive cutoff detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

M_NO_AVI	4	1	AVI packet receive cutoff detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_DC_NOCD	3	1	Deep color 24bit mode auto move occurrence interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_DC_DEERR	2	1	In Deep Color Packing Group, DE position abnormal occurrence interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_DC_BUFERR	1	1	Deep Color FIFO flow occurrence interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_DC_PPERR	0	1	Deep Color UnPack phase dis-unify occurrence 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

6.11.18 HDCP INTERRUPT MASK (HDCP_INTM) (0x8518)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_AVM_SET	M_AVM_CLR	M_LINKERR	M_SHA_END	M_RO_END	M_KM_END	M_AKSV_END	M_AN_END
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_AVM_SET	7	1	SET AVMUTE receive interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AVM_CLR	6	1	CLRAE AVMUTE receive interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_LINKERR	5	1	Link error detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_SHA_END	4	1	V' value operation completed interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_RO_END	3	1	Ks', M0', R0' operation completed interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_KM_END	2	1	Km' operation completed interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

M_AKSV_END	1	1	AKSV write completed interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AN_END	0	1	AN write completed interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

6.11.19 GBD INTERRUPT MASK (GBD_INTM) (0x8519)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_GBD_PKERR	M_GBD_ACLR	M_P1GBD_CHG	M_P0GBD_CHG	Reserved	M_P1GBD_DET	M_GBD_OFF	M_GBB_ON
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_GBD_PKERR	7	1	GBD packet receive error occurrence interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_GBD_ACLR	6	1	GBD packet receive cutoff detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_P1GBD_CHG	5	1	P1 GBD update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_P0GBD_CHG	4	1	P0 GBD update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_P1GBD_DET	2	1	P1 GBD data receive detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_GBD_OFF	1	1	No Valid GBD detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_GBB_ON	0	1	With valid GBD detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

6.11.20 MISC INTERRUPT MASK (MISC_INTM) (0x851b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_AU_D	M_AU_H	M_VIDEO	M_AS_LA	M_NO_S	M_NO_V	M_SYNC_	M_AUDI

	SD_OFF	BR_OFF	_COLOR	YOUT	PD	S	CHG	O_MUTE
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_AU_DSD_OFF	7	0	Discontinuity of DSD Audio packet receive detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AU_HBR_OFF	6	0	Discontinuity of HBR Audio packet receive interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_VIDEO_COLOR	5	1	Mask for Video Color (RGB, YCbCr444, YCbCr422) change interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AS_LAYOUT	4	1	audio Layout Bit change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_NO_SPD	3	1	SPD_Info packet receive cutoff detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_NO_VS	2	1	VS_Info packet receive cutoff detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_SYNC_CHG	1	1	Video sync signal state change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AUDIO_MUTE	0	1	Audio MUTE generation interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

6.11.21 SYS STATUS (SYS_STATUS) (0x8520)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_SYNC	S_AVMUTE	S_HDCP	S_HDMI	S_PHY_SCDT	S_PHY_PLL	S_TMDS	S_DDC5V
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_SYNC	7	0	Input Video sync signal status 0 : No sync signal (unstable) 1: With sync signal (stable) 【Note】 For the generation conditions for this status, follow the address 0x85A5 ~ 0x85AE settings.
S_AVMUTE	6	0	AVMUTE status 0: AVMUTE=OFF 1: AVMUTE=ON

S_HDCP	5	0	HDCP status 0: HDCP=OFF (no code) 1: HDCP=ON (with code)
S_HDMI	4	0	HDMI status 0: DVI 1: HDMI
S_PHY_SCDT	3	0	PHY DE detect status (PHY SCDT signal monitor) 0: No DE 1: With DE
S_PHY_PLL	2	0	PHY PLL status (PHY PLL_LOCK_IND signal monitor) 0: UnLock 1: Lock
S_TMDS	1	0	TMDS input amplitude status (PHY squelch signal monitor) 0: No input amplitude, 1: With input amplitude
S_DDC5V	0	0	DDC_Power (DDC5V) input status 0: No input, 1: With input

6.11.22 VIDEO INPUT STATUS (VI_STATUS) (0x8521)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_V_repeat							S_V_format
Type	RO							RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_V_repeat	7:4	0	Input Video signal status (Repetition) 0: No Repetition, 1: Repetition = 2, 2: Repetition = 3, 3: Repetition = 4, . . . , 9: Repetition = 10
S_V_format	3:0	0	Video format status detected from input DE size Shows the status before implementation of correction using repetition. 4'd1 : VGA (Horizontal 631~649, Vertical 471~489) 4'd2 : 240p/480i (Horizontal 1401~1449, Vertical 231~249) 4'd3 : 288p/576i (Horizontal 1401~1449, Vertical 279~297) 4'd4 : W240p/480i (Horizontal 2801~2899, Vertical 231~249) 4'd5 : W288p/576i (Horizontal 2801~2899, Vertical 279~297) 4'd6 : 480p (Horizontal 701~729, Vertical 471~489) 4'd7 : 576p (Horizontal 701~729, Vertical 567~585)

			4'd8 : W480p (Horizontal 1401~1449, Vertical 471~489) 4'd9 : W576p (Horizontal 1401~1449, Vertical 567~585) 4'd10 : WW480p (Horizontal 2801~2899, Vertical 471~489) 4'd11 : WW576p (Horizontal 2801~2899, Vertical 567~585) 4'd12 : 720p (Horizontal 1261~1289, Vertical 711~729) 4'd13 : 1035i (Horizontal 1911~1929, Vertical 507~527) 4'd14 : 1080i (Horizontal 1911~1929, Vertical 531~549) 4'd15 : 1080p (Horizontal 1911~1929, Vertical 1071~1089) 4'd0 : Other than above
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6.11.23 VIDEO INPUT STATUS1 (VI_STATUS1) (0x8522)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_V_GBD	Reserved			S_DeepColor	S_V_422	S_V_interlace	
Type	RO	RO			RO	RO	RO	
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_V_GBD	6:4	0	Effective GBD data status ^{※1} 0: No GBD, 1: With GBD
	3:2		Reserved
S_V_422	1	0	Input Video signal status (422 detection) ^{※3} 0 : 444, 1 : 422
S_V_interlace	0	0	Input Video signal status (Interlace detection) ^{※4} 0: Progressive, 1: Interlace

^{※1} During DVI input, judged to be No GBD.

^{※2} During DVI input, judged to be 24bit.

^{※3} During DVI input, judged to be 444. During HDMI input, judged from the AVI-Info value.

^{※4} Progressive/Interlace judgment method follows the address0x858e[4]bit setting.

6.11.24

AUDIO STATUS0 (AU_STATUS0) (0x8523)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_A_MUTE	S_A_P_Lock	S_A_F_Lock	Reserved	S_A_DSD	S_A_HBR	S_A_NLPCM	S_A_sample
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_A_MUTE	7	0	AUDIO auto mute status 0: Mute OFF, 1: Mute ON
S_A_P_Lock	6		AUDIO-PLL phase lock status 0: Unlock 1: Lock
S_A_F_Lock	5	0	AUDIO-PLL Frequency lock status 0: Unlock 1: Lock
Reserved	4	0	Reserved
S_A_DSD	3	0	1BIT Audio packet transmission status (1.5msec update) 0: No DSD transmission, 1: With DSD transmission
S_A_HBR	2	0	HBR Audio packet transmission status (1.5msec update) 0: No HBR transmission, 1: With HBR transmission
S_A_NLPCM	1	0	Normal AUDIO/HBR AUDIOPacket compression stream detection 0: LPCM, 1: Compression stream (61937-1)
S_A_sample	0	0	Normal AUDIO packet transmission status (1.5msec update) 0: No AUDIO transmission, 1: With AUDIO transmission Notes: When 1bit-audio is received, this bit is always 0.

6.11.25

AUDIO STATUS1 (AU_STATUS1) (0x8524)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	3D_STRUCTURE				S_VS	S_SPD	S_PKERR	S_ACP
Type	RO				RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
3D_STRUCTURE	7:4	0	3D transmission format information in VS info 0000: Frame packing 0001 Field alternative

			0010: Line alternative 0011: Side-by-Side(Full) 0100: L + depth 0101: L + depth + graphics + graphics-depth 0110: Top-and-Bottom 0111: Reserved 1000: Side-by-Side(Half) 1001-1110: Reserved 1111: Not used ※Valid when S_VS_VIC_3D(0x8525[5]) is 1
S_VS	3	0	VS packet transmission status 0: No VS transmission, 1: With VS transmission
S_SPD	2	0	SPD packet transmission status 0: No SPD transmission, 1: With SPD transmission
S_PKERR	1	0	Packet receive error occurrence status 0: No Packet receive error, 1: Packet receive error now occurring
S_ACP	0	0	ACP packet transmission status 0: No ACP transmission, 1: With ACP transmission

6.11.26 VIDEO INPUT STATUS2 (VI_STATUS2) (0x8525)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_FP_IP		S_VS_VIC_3D	Reserved				
Type	RO		RO	RO				
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_FP_IP	7:6	0	IP judgment result 0x8980[2] due to size (Vertical V size and vertical DE size) or VIC to select whether to use size or VIC to judge. Valid during Frame packing receive. 2'd0: Progressive 2'd1: Interlace 2'd2: VIC=39
S_VS_VIC_3D	5	0	3D format judgment result due to VS info ※ 0: Non-3D format 1: 3D format 【Note】 Valid during HDMI input only. During DVI input, fixed at 0. When VS Info packet HDMI Video format(PB4 [7:5]) = 3'b010,

			set o 1.
Reserved	[4:1]	0	
S_DC_NOCD	0	0	Status determining whether Color Depth used in current Deep Color unpack operation is in 24bit mode due to auto move 0: During normal operation (DVI mode or normal CD value) 1: CD=0 or CD=reserved or Operations due to No GC Packet

6.11.27 CLK STATUS (CLK_STATUS) (0x8526)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_V_3D_format				S_V_HPOL	S_V_VPOL	S_CLK_U_21M	S_CLK_D_C
Type	RO				RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_V_3D_format	7:4	0	<p>3D Video format status detected from input DE size ×1</p> <p>4'd1 : 3D 1080i Frame Packing (Horizontal 1911~1929, Vertical 2219~2237)</p> <p>4'd2 : 3D 1080p Frame Packing or L+depth (Horizontal 1911~1929, Vertical 2196~2214)</p> <p>4'd3 : 3D 720p Frame Packing or L+depth (Horizontal 1271~1289, Vertical 1461~1479)</p> <p>4'd4 : 3D 1080p Line alternative (Horizontal 1911~1929, Vertical 2151~2169)</p> <p>4'd5 : 3D 720p Line alternative (Horizontal 1271~1289, Vertical 1431~1449)</p> <p>4'd6 : 3D 1080i Side by Side(Full) (Horizontal 3831~3849, Vertical 531~549)</p> <p>4'd7 : 3D 1080p Side by Side(Full) (Horizontal 3831~3849, Vertical 1071~1089)</p> <p>4'd8 : 3D 720p Side by Side(Full) (Horizontal 2551~2569, Vertical 711~729)</p> <p>4'd9 : 3D 1080p L+depth+G+G_depth</p>

			(Horizontal 1911~1929, Vertical 4446~4464) 4'd10 : 3D 720p L+depth+G+G_depth (Horizontal 1271~1289, Vertical 2961~2979) 4'd0 : Other than above
S_V_HPOL	3	0	Input HSYNC polarity status 0: Low active 1: High active
S_V_VPOL	2	0	Input VSYNC polarity status 0: Low active 1: High active
S_CLK_U21M	1	0	TMDS clock detection status at less than 21MHz 0: 21MHz or more , 1: Less than 21MHz
S_CLK_DC	0	0	TMDS clock DC condition detection status 0: Non DC condition, 1: DC condition 【Note】 In reality, DC to frequency of about 1MHz or less is "1". Responds even when TMDS clock is not input (amplitude 0).

※1 3D 1080i Line alternative cannot identify 2D 1080p,

3D Side by Side (Half) cannot identify 2D format,

3D Top-and-Bottom cannot identify 2D format,

The above unidentifiable format is displayed as 4'd0.

6.11.28 VI STATUS3 (VI_STATUS3) (0x8528)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							S_V_color
Type	RO							RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_V_color	4:0	0	Input Video signal color space judgment status ※1 5'b00 000 RGB (Full) 5'b00 001 RGB (Limited) 5'b00 010 YCbCr601 (Full) 5'b00 011 YCbCr601 (Limited) 5'b00 110 YCbCr709 (Full) 5'b00 111 YCbCr709 (Limited) 5'b00 100 Adobe_RGB (Full) 5'b00 101 Adobe_RGB (Limited) 5'b01 010 xvYCC601 (Full) 5'b01 011 xvYCC601 (Limited) 5'b01 110 xvYCC709 (Full) 5'b01 111 xvYCC709 (Limited)

			5'b10 010 sYCC601 (Full) 5'b10 011 sYCC601 (Limited) 5'b11 010 Adobe_YCC601 (Full) 5'b11 011 Adobe_YCC601 (Limited) ※Values other than above are not generated 【Note】 Each bit has the following meaning. [0] Full/Limited identification bit [1] RGB/YCbCr identification bit [2] During RGB input, category identification bit During YCbCr input, 601/709 identification bit [4: 3] During RGB input, 00 fixed During YCbCr input, category identification bit
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※1 During DVI input, judged as RGB. For range identification, follow the address0x8570[3]bit setting.

During HDMI input, judged from AVI-Info value. If at AVI-Info judged to be RGB, for the range identification follow the address0x8570[2]bit.

6.11.29 SYS FREQ0 Register (SYS_FREQ0) (0x8540)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SYS_FREQ0							
Type	R/W							
Default	0x88							

Register Field	Bit	Default	Description
SYS_FREQ0	7:0	0x88	System clock frequency setting (lower bits) Set System clock frequency setting divide 10000 integer Ex. When system clock at 26MHz, 2600 = 16'h0A28 When system clock at 27MHz, 2700 = 16'h0A8C When system clock at 42MHz, 4200 = 16'h1068 When system clock at 50MHz, 4200 = 16'h1388

6.11.30 SYS FREQ1 Register (SYS_FREQ1) (0x8541)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SYS_FREQ1							
Type	R/W							
Default	0x13							

Register Field	Bit	Default	Description
SYS_FREQ1	7:0	0x13	System clock frequency setting (upper bits)

6.11.31 DDC CONTROL (DDC_CTL) (0x8543)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					DDC_ACT ION	DDC5V_MODE	
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	1	0

Register Field	Bit	Default	Description
	7:3		Reserved
DDC_ACTION	2	0	Selection of response method for DDC access from send side 0 : DDC is active only while HotPLUG is being output 1 : DDC is active when initialization completion INIT_END, 0x854A[0], is asserted
DDC5V_MODE	1:0	0	DDC5V_active detect delay setting To prevent chattering in the DDC5V input rising detection area, DDC5V is judged as avtime after a specified time from the rise detect point in time. 00: 0msec, 01: 50msec, 10: 100msec, 11: 200msec, 【 Note】 With this setting, the DDC5V detection interrupt, HOTPLUG automatic output, and PHY automatic power ON timing are all delayed.

6.11.32 HPD Control Register (HPD_CTL) (0x8544)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			HPD_CTL0	Reserved			HPD_OUT0
Type	RO				RO			
Default	0x0			0x1	0x0			0x0

Register Field	Bit	Default	Description
Reserved	7:5	0x0	
HPD_CTL0	4	0x1	HOTPLUG output ON/OFF control mode 0: Host manual setting 1: DDC5V detection interlock
Reserved	3:1	0x0	
HPD_OUT0	0	0x0	HOTPLUT Output setting

			0: HOTPLUG = "L" output 1: HOTPLUG = "H" output Note: When at DDC5V detection interlock setting, write is not valid. Become status monitor bit.
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6.11.33 INIT END REGISTER (INIT_END) (0x854A)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							INIT_END
Type	RO							RW
Default	0							0

Register Field	Bit	Default	Description
Reserved	7:1	0x0	
INIT_END	0	0x0	Initialization completed flag After completion of all initialization settings, write "1" to this register. If 0x8544[4] = 1, HPDO is asserted only when INIT_END is asserted. If 0x8543[2] = 1, DDC is active only when INIT_END is asserted

6.11.34 HDCP MODE Register (HDCP_MODE) (0x8560)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						AuthMod	
Type	RO		RW		RW		RW	
Default	0		1		0		1	

Register Field	Bit	Default	Description
Reserved	[7:2]	0	
Reserved	[1:0]	0	HDCP authentication mode setting 2'b00: Automatic authentication mode 0 (for receiver) (Aksv_write -> HDCP reset -> Km' calculation -> Ks', 0', R0' calculation) 2'b01: Automatic authentication mode 1 (for repeater) (Aksv_write -> HDCP reset -> Km' calculation -> Ks', M0', R0' calculation -> V' calculation)

			2'b1x: Host command mode The HOST issues commands sequentially according to interrupts.
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6.11.35 HDCP COMMAND Register (HDCP_CMD) (0x8561)

Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved					ShaS	CalParam	CalKm	UnAuth
Type	RO					RW	RW	RW	RW
Default	0x0					0	0	0	0

Register Field	Bit	Default	Description
Reserved	[7:4]	0	
ShaS	3	0	V' value calculation start command (After calculation completed, automatically clears) 1: Command issued
CalParam	2	0	Ks', M0', R0' calculation start command (After calculation completed, automatically clears) 1: Command issued Note) During Auto authorization mode (AUTHMOD_A=00 or 01), this command is invalid.
CalKm	1	0	Km calculation start command (After calculation completed, automatically clears) 1: Command issued Note) During Auto authorization mode (AUTHMOD_A=00 or 01), this command is invalid.
UnAuth	0	0	Unauthorized move command (automatic clear) 1: Command issued

6.11.1 VIDEO MUTE REGISTER1 (V_MUTE1) (0x857A)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			VAM_CLR_MODE			VAM_SYNC_EN	VAM_DATA_EN
Type	R		R/W		R		R/W	R/W
Default	0		0		0		0	0

Register Field	Bit	Default	Description
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Reserved	[7:6]	2'b0	
VAM_CLR_MODE	[5:4]	2'b0	Clearing method selection of Video Auto Mute 00: Manual Clearing 01: Auto Clearing by mute-timer 1x: Auto Clearing by mute-timer & Vsync active edge
Reserved	[3:2]		
VAM_SYNC_EN	1	0	VD_o/HD_o/DE_o auto mute setting 0: auto mute OFF 1: auto mute ON by selected Factors in address 0x857B
VAM_DATA_EN	0	0	Y_o/CB_o/CR_o auto mute setting 0: auto mute OFF 1: auto mute ON by selected Factors in address 0x857B

6.11.2 VIDEO MUTE REGISTER2 (V_MUTE2) (0x857B)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	VAM_FACTOR6	VAM_FACTOR5	VAM_FACTOR4	VAM_FACTOR3	VAM_FACTOR2	VAM_FACTOR1	VAM_FACTOR0
Type	R	R/W						
Default	0	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
Reserved	7	1'b0	
VAM_FACTOR6	6	1'b1	When TMDS signal existence (PHY Squelch) change is detected, Video_Mute is set automatically. 0: Not set, 1: Set
VAM_FACTOR5	5	1'b1	When DE size and position of Input side change is detected, Video_Mute is set automatically. 0: Not set, 1: Set
VAM_FACTOR4	4	1'b1	When HV counter of Input side change is detected, Video_Mute is set automatically. 0: Not set, 1: Set
VAM_FACTOR3	3	1'b1	When Deep Color mode change is detected, Video_Mute is set automatically. 0: Not set, 1: Set
VAM_FACTOR2	2	1'b1	When Pixel CLK change is detected, Video_Mute is set automatically. 0: Not set, 1: Set
VAM_FACTOR1	1	1'b1	When PHY PLL CLK Frequency change is detected, Video_Mute is set automatically. 0: Not set, 1: Set

VAM_FACTOR0	0	1'b1	When TMDS CLK change is detected, Video_Mute is set automatically. 0: Not set, 1: Set
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6.11.3 VIDEO MUTE Timer REGISTER1 (VMUTE_TIMER) (0x857C)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Video_mute_timer_Limit							
Type	R/W							
Default	0x14							

Register Field	Bit	Default	Description
Video_mute_timer_Limit	[7:0]	0x14	<p>Waiting time until Clearing of Video Mute status. 25.6ms ~ 6553msec. (set in 25.6ms units)</p> <p>Note) Setting of 0 sec. (00h) is prohibited</p>

6.11.4 VIDEO MUTE STATUS REGISTER (VMUTE_STATUS) (0x857D)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			SYNC_MUTE_STATUS	Reserved			DATA_MUTE_STATUS
Type	RO			R/W	RO			R/W
Default	0			0	0			0

Register Field	Bit	Default	Description
Reserved	[7:5]		
VAM_FACTOR4	4	1'b0	<p>Video SYNC (VD_o/HD_o/DE_o)auto mute status</p> <p>0: Mute OFF (VD_o/HD_o/DE_o = Normal output) 1: Mute ON (VD_o/HD_o/DE_o = Logic "L")</p> <p>Note) Only in the case of VAM_CLR_MODE = 2'b00, Host can write "0". HOST always cannot write "1."</p>
Reserved	[3:1]		
VAM_FACTOR0	0	1'b0	<p>Video DATA (Y_o/CB_o/CR_o)auto mute status</p> <p>0: Mute OFF (Y_o/CB_o/CR_o = Normal output) 1: Mute ON (Y_o/CB_o/CR_o = Black)</p>

			Note) Only in the case of VAM_CLR_MODE = 2'b00, Host can write "0". HOST always cannot write "1."
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6.11.5 VIDEO MUTE AUTO REGISTER2 (VMUTE_AUTO) (0x857F)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUTO_VI_MUTE1	AUTO_VI_MUTE0	Reserved	VI_MUTE		Reserved		VI_BLACK
Type	R/W	R/W	R	R/W		R		RW
Default	1	1	0	0		0		0

Register Field	Bit	Default	Description
AUTO_VI_MUTE1	7	1'b1	Auto mute of HD_o/VD_o/DE_o when No TMDS (PHY Squelch) detected 0: No Mute, 1: Mute Note) Use the initial value.
AUTO_VI_MUTE0	6	1'b1	Auto mute of HD_o/VD_o/DE_o when No DDC5V detected 0: No Mute, 1: Mute Note) Use the initial value.
Reserved	5	1'b0	
VI_MUTE	4	1'b0	Manual Mute setup of HD_o/VD_o/DE_o 0: OFF (Normal) 1: Mute (HD_o/VD_o/DE_o "0" fixed) Note) HOST always can write "1" or "0".
Reserved	[3:1]	1'b0	
VI_BLACK	0	1'b0	Manual Black screen output setup 0: OFF (Normal) 1: Black screen output Note) HOST always can write "1" or "0".

6.11.6 EDID MODE REGISTER (EDID_MODE) (0x85E0)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							EDID_MODE
Type	RO							R/W

Default	0x0			0x0
---------	-----	--	--	-----

Register Field	Bit	Default	Description		
Reserved	[7:2]	0x0			
EDID_MODE	1:0	0x0	EDID access response mode selection 00: DDC line direct connection EEPROM mode (Absolutely no response to EDID access from DDC line) 01: Internal EDID-RAM & DDC2B mode (No response to 0x60slave => Returns NACK) 1x: Internal EDID-RAM & E-DDC mode		

6.11.7 EDID Length REGISTER 1 (EDID_LEN1) (0x85E3)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	EDID_LEN[7:0]							
Type	R/W							
Default	0x00							

Register Field	Bit	Default	Description
EDID_LEN[7:0]	7:0	0x00	EDID data size stored in RAM Note: Sets Data byte number Read from EEPROM Note: If EDID_LEN[10:0]=0 is set, no read Note: if EDID_LEN[10:0]>0x400 (1024 or more) is set, 1024 bytes only are Read Note: If EEPROM not used, and data is written directly to RAM from HOST, data size is set

6.11.8 EDID Length REGISTER 2 (EDID_LEN2) (0x85E4)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							EDID_LEN[10:8]
Type	RO							R/W
Default	0x00							0x0

Register Field	Bit	Default	Description
Reserved	7:3	0x00	Reserved
EDID_LEN[10:8]	2:0	0x0	EDID data size stored in RAM (upper address bits)

6.12 HDMI Rx Audio Control

6.12.1 FORCE MUTE (FORCE_MUTE) (0x8600)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			FORCE_A MUTE	Reserved			FORCE_D MUTE
Type	RO			RW	RO			RW
Default	0	0	0	1	0	0	0	1

Register Field	Bit	Default	Description
FORCE_AMUTE	4	0x1	Forced AMUTEOUT terminal control 0 : Mute OFF, 1 : Mute ON 【Note】 Setting and clear is possible at HOST only 【Note】 For Mute ON polarity, follow the 0x8608[5] setting
FORCE_DMUTE	0	0x1	Forced data MUTE control 0 : Mute OFF, 1 : Mute ON 【Note】 Setting and clear is possible at HOST only 【Note】 For Mute signal, follow the 0x8608[2:0] setting

6.12.2 CMD AUD (CMD_AUD) (0x8601)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			CMD_BU FINIT	CMD_LO CKDET	CMD_M UTE		
Type	RO			RW	RW	RW		
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
CMD_BUFINIT	2	0	Buffer initialization start command 1 : Command issued 【Note】 After buffer initialization completed, automatically clears 【Note】 When in automatic command issue mode (address0x8604[2:1]≠2'b00), issue of commands from HOST is prohibited. 【Note】 When issuing commands from HOST, always issue the MUTE startcommand first.

CMD_LOCKDET	1	0	<p>Audio clock frequency lock detection start command 1 : Command issued 【Note】 The reproduced Audio clock frequency detects unification with FS information transmitted by Cannel Status bit, and issues interrupt. For observation cycle and detection precision, follow the address0x8630~33 setting. 【Note】 After frequency lock detection, automatically clears ※Use not recommended</p>
CMD_MUTE	0	0	<p>MUTE start command 1 : Command issued 【Note】 Automatic command issue mode exists. For automatic issue condition, follow the AUTO_CMD0,1(address0x8602, 0x8603) setting. 【Note】 When AUTO_PLAY3 setting ON, automatically clears to "0" whenBuffer initialization completed. 【Note】 For Mute signal, follow the 0x8608[2:0] setting 【Note】 For AMUTE terminal output polarity, follow the 0x8608[5] setting</p>

6.12.3 AUDIO AUTO MUTE Command REGISTER (AMute_Auto) (0x8602)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Auto_Mute7	Auto_Mute6	Auto_Mute5	Auto_Mute4	Auto_Mute3	Auto_Mute2	Auto_Mute1	Auto_Mute0
Type	RW							
Default	1	1	1	1	0	0	1	1

Register Field	Bit	Description
Auto_Mute7	7	In PHY-A/B switch, automatically set CMD_MUTE 0: Not set, 1: Set
Auto_Mute6	6	In LPCM/NLPCM change detection, automatically set CMD_MUTE 0: Not set, 1: Set 【Note】 OR conditions for LPCM→NLPCM detect and NLPCM→LPCM detect
Auto_Mute5	5	In FS change detection, automatically set CMD_MUTE 0: Not set, 1: Set

Auto_Mute4	4	In PHY output clock change detection, automatically set CMD_MUTE 0: Not set, 1: Set
Auto_Mute3	3	In Non LPCM detection period, automatically set CMD_MUTE 0: Not set, 1: Set
Auto_Mute2	2	In Audio clock frequency unlock detect period, automatically set CMD_MUTE 0: Not set, 1: Set ※Use not recommended
Auto_Mute1	1	In PHY no output clock detect period, automatically set CMD_MUTE 0: Not set, 1: Set
Auto_Mute0	0	In DVI mode period, or in DDC5V =0V period, automatically set CMD_MUTE 0: Not set, 1: Set

6.12.4 Auto Command REGISTER 0 (AUTO_CMD1) (0x8603)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name					Reserved	Auto_Mute10	Auto_Mute9	Auto_Mute8
Type					RO	RW	RW	RW
Default					0x00	0	1	0

Register Field	Bit	Description
Reserved	[7:3]	
Auto_Mute10	2	In 60958 frame discontinuous detect, automatically issue CMD_MUTE 0: Not issue, 1: Issue
Auto_Mute9	1	In SET_AVMUTE receive period, automatically issue CMD_MUTE 0: Not issue, 1: Issue
Auto_Mute8	0	In buffer flow detect, automatically issue CMD_MUTE 0: Not issue, 1: Issue

6.12.5 Auto Command REGISTER 0 (AUTO_CMD2) (0x8604)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name					Auto_Play3	Auto_Play2		Reserved
Type					RO	RW	RW	RO
Default					0x0	1	1	0x0

Register Field	Bit	Description
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Reserved	[7:4]	
Auto_Play3	3	In Buffer initialization end detect, automatically clears MUTE_CMD 0: Not clear, 1: Clear
Auto_Play2	2	After generation of MUTE factor selected in AUTO_MUTE setting “after fixed time B” automatically issue CMD_BUFINIT 0: Not issue, 1: Issue 【Note】Priority over frequency lock detect (=equivalent to lock detect time limit) 【Note】If MUTE factor continues for fixed period, issue command at end edge of factor. 【Note】If MUTE factor is generated during fixed time measurement, restart time measurement from beginning.
Reserved	[1:0]	

6.12.6 Buffer Initialization Start Period (BUFINIT_START) (0x8606)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	BUFINIT_START							
Type	RW							
Default	0x0A							

Register Field	Bit	Description
BUFINIT_START	[7:0]	Wait time setting until Buffer initialization start in AUTO_PLAY2 → “fixed time B” 0.1 ~ 25.5sec. (set in 0.1 sec. units) 【Note】Setting of 0 sec. (00h) is prohibited

6.12.7 FS MUTE REGISTER (FS_MUTE) (0x8607)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	FS_else_MUTE	FS22_MUTE	FS24_MUTE	FS88_MUTE	FS96_MUTE	FS176_MUTE	FS192_MUTE	FS_NO_MUTE
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
FS_else_MUTE	7	0x1	Other than FS = 22k,24k,32k,44k,48k,88k,96,176k,192k 0 : Do not Mute, 1 : Mute

FS22_MUTE	6	0x1	When at FS = 22.05KHz, routinely 0 : Do not Mute, 1 : Mute
FS24_MUTE	5	0x1	When at FS = 24KHz, routinely 0 : Do not Mute, 1 : Mute
FS88_MUTE	4	0x1	When at FS = 88.2KHz, routinely 0 : Do not Mute, 1 : Mute
FS96_MUTE	3	0x1	When at FS = 96KHz, routinely 0 : Do not Mute, 1 : Mute
FS176_MUTE	2	0x1	When at FS = 176.4KHz, routinely 0 : Do not Mute, 1 : Mute
FS192_MUTE	1	0x1	When at FS = 192KHz, routinely 0 : Do not Mute, 1 : Mute
FS_NO_MUTE	0	0x1	When at FS = not indicated, routinely 0 : Do not Mute, 1 : Mute

Write FS Bit corresponding to set specification to "0".

FS=48KHz, 44.1KHz, 32KHz are outside FS_MUTE applicability. (In the standard, 48KHz, 44.1KHz, 32KHz must be reproduced)

6.12.8 AUDIO MUTE MODE REGISTER (MUTE_MODE) (0x8608)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AMUTE_DLY	AMUTE_POL	O_AMUTE_EN	reserved	MUTE_LRCK	MUTE_BCK	MUTE_SDO	
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	2'b01	1	1	0	0	0	0	1

Register Field	Bit	Default	Description
AMUTE_DLY	[7:6]	2'b01	When MUTE cleared, AMUTE output delay adjustment (※2) 00 : No delay 01 : 100msec delay 10 : 200msec delay 11 : 300msec delay
AMUTE_POL	5	1'b1	AMUTE polarity (※1) 0:"0" output 1:"1" output
O_AMUTE_EN	4	1'b1	AMUTE signal ON/OFF when MUTE ON (※1) 0:OFF ("0" output fixed) 1:ON
Reserved	3	1'b0	
MUTE_LRCK	2	1'b0	LRCK output when MUTE ON (※1) 0: Do not Mute 1: Mute

MUTE_BCK	1	1'b0	BCK output when MUTE ON (※1) 0: Do not Mute 1: Mute
MUTE_SDO	0	1'b1	SDO/DADO output when MUTE ON (※1) 0: Do not Mute 1: Mute

※1 Actually setting to MUTE ON occurs when any of the following ① ~ ④ occur.

- ① When HOST sets FORCE_MUTE (address0x8600)
- ② When HOST sets CMD_MUTE (address0x8601[0])
- ③ When factor selected in AUTO_MUTE (address0x8602 ~ 0x8603) is generated
- ④ When other than FS received in FS_MUTE(address0x8607) is selected

※2 If using AMUTEOUT to perform transistor mute at set output stage, this setting can also be used to delay the Mute clear timing.

6.12.9 AUDIO SAMPLE FREQUENCY MODE REGISTER (FS_SET) (0x8621)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			NLPCM	FS			
Type	RW			RW	RW			
Default	0			0	0x2			

Register Field	Bit	Description
Reserved	[7:5]	
NLPCM	4	Normal Audio linear PCM/nonlinear PCM identification information extraction result 0: LPCM 1: Compression stream 【Note】 When 0x8620[6]==0, Follow the 0x8620[5:4] setting, and HW automatically set, write from Host is invalid. If 0x8620[6]==1, HOST determines and sets. 【Note】 LPCM/NLPCM change interrupt (address0x8505[3:2]) is generated when this register has a change.
FS	[3:0]	AUDIO sampling frequency information extraction result 4'h0: 44.1KHz, 4'h2: 48KHz, 4'h3: 32KHz, 4'h4: 22.05KHz, 4'h6: 24KHz, 4'h8: 88.2KHz, 4'hA: 96KHz, 4'hC: 176.4KHz, 4'hE: 192KHz, 4'h9: 768KHz 4'h5: 384KHz, 4'h7: 352.8KHz, 4'hB: 705.6KHz 【Note】 If 0x8620[3]==0, Follow 0x8620[2:0] setting, HW is automatically set, write from

		Host is invalid. If 0x8620[3]==1, Host determines and sets. 【Note】FS change interrupt (address0x08505[1]) is generated when this register has a change.
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6.12.10 CBIT Byte 0 (CBIT_BYTE0) (0x8622)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CBIT_BYTE0							
Type	RW							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CBIT_BYTE0	[7:0]	Channel Status bit [7:0]

6.12.11 CBIT Byte 1 (CBIT_BYTE1) (0x8623)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CBIT_BYTE1							
Type	RW							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CBIT_BYTE1	[7:0]	Channel Status bit [15:8]

6.12.12 CBIT Byte 2 (CBIT_BYTE2) (0x8624)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CBIT_BYTE2							
Type	RW							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CBIT_BYTE2	[7:0]	Channel Status bit [23:16]

6.12.13 CBIT Byte 3 (CBIT_BYTE3) (0x8625)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CBIT_BYTE3							
Type	RW							
Default	0	0	0	0	0	0	1	0

Register Field	Bit	Description
CBIT_BYTE3	[7:0]	Channel Status bit [31:24]

6.12.14 CBIT Byte 4 (CBIT_BYTE4) (0x8626)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CBIT_BYTE4							
Type	RW							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CBIT_BYTE4	[7:0]	Channel Status bit [39:32]

6.12.15 CBIT Byte 5 (CBIT_BYTE5) (0x8627)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CBIT_BYTE5							
Type	RW							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CBIT_BYTE5	[7:0]	Channel Status bit [47:40]

6.12.16 Audio Sample Counter Register 0 (Audio_Counter0) (0x862E)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AS_COUNT							
Type	R							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
AS_COUNT	[7:0]	Audio sample count measurement result during 100msec

6.12.17 Audio Sample Counter Register 1 (Audio_Counter1) (0x862F)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AS_COUNT							
Type	R							

Default	0	0	0	0	0	0	0	0
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Register Field	Bit	Description
AS_COUNT	[15:8]	Audio sample count measurement result during 100msec

6.12.18 AUDIO OUTPUT MODE 0 Register (SDO_MODE0) (0x8651)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					BCK_POL	BCK_FS	LR_POL
Type	RW							
Default	0	0	0	0	0	0	1	0

Register Field	Bit	Default	Description
	7:3	0	Reserved
BCK_POL	2	0	BCK polarity selection 0: Normal (ASDO data changed at down edge) 1: Inverted (ASDO data changed at up edge)
BCK_FS	1	1	BCK frequency selection 0: 32fs 1: 64fs
LR_POL	0	0	LRCK polarity selection 0: Normal (sample period: 1 st half=L, 2 nd half = H) 1: Inverted (sample period: 1 st half = H, 2 nd half = L)

6.12.19 AUDIO OUTPUT MODE 1 Register (SDO_MODE1) (0x8652)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	SDO_BIT LENG					HBR_OUT_MODE	I2S_MODE
Type	RO	R/W					R/W	R/W
Default	0	3'b110					0	2'b00

Register Field	Bit	Description
	7	Reserved
SDO_BIT LENG	6:4	ASDO output data Bit Length setting 000: 16bit (lower 8bit discarded) 001: 16bit (lower 8bit + 1 discarded) 010: 18bit (lower 6bit discarded)

		011: 18bit (lower 6bit + 1 discarded) 100: 20bit (lower 4bit discarded) 101: 20bit (lower 4bit + 1 discarded) 110: 24bit no rounding 111: Output OFF (Mute)
HBR_OUT_MODE	3	HBR Audio output format setting 0 : HBR output which uses only ASDO[0]. LRCK = 768KHz 1 : HBR output which uses ASDO[3:0], LRCL = 768KHz/4 = 192KHz
I2S_MODE	2	ASDO output format setting 3'b000: standard Back(Right) justified 3'b001: standard Front(Left) justified 3'b01x: standard I2S 3'b10x: 60958 over I2S (without 1bit delay) 3'b11x: 60958 over I2S (with 1bit delay)
SDO_FMT	1:0	

6.12.20 AUDIO PLL Setting Register (NCO_F0_MOD) (0x8670)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						NCO_F0_MOD	
Type	RO						R/W	
Default	0x0						2'b10	

Register Field	Bit	Description
Reserved	7:2	
NCO_F0_MOD	1:0	<p>NCO standard frequency setting for Audio PLL</p> <p>00: For REFCLK = 42MHz 01: For REFCLK = 27MHz 1x: Register setting value uses 28bit setting for 48KHz series use, for 44.1KHz series use. (address 0x8671~78)</p> <p>【Note】</p> <ol style="list-style-type: none"> 1. NCO standard frequency setting value calculation 48KHz series : $6.144\text{MHz} \times 2^{28} \div (\text{RefClk frequency})$ 44.1KHz series : $5.6448\text{MHz} \times 2^{28} \div (\text{RefClk clock frequency})$ 2. For 26MHz RefClk: <ul style="list-style-type: none"> • Set this field to 2'b10 f • 0x8671-74: NCO_48F0[27:0] = 0x3_C7_EA_93 • 0x8675-78: NCO_44F0[27:0] = 0x3_79_45_EA

6.12.21 AUDIO PLL Setting Register (NCO_48F0A) (0x8671)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_48F0[7:0]							
Type	RW							
Default	0x05							

Note: $6.144\text{MHz} \times 2^{28} \div (\text{System clock frequency})$

6.12.22 AUDIO PLL Setting Register (NCO_48F0B) (0x8672)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_48F0[15:8]							
Type	RW							
Default	0x51							

6.12.23 AUDIO PLL Setting Register (NCO_48F0C) (0x8673)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_48F0[23:16]							
Type	RW							
Default	0xF7							

6.12.24 AUDIO PLL Setting Register (NCO_48F0D) (0x8674)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							
Type	RO							
Default	0x0							

Note: $6.144\text{MHz} \times 2^{28} \div (\text{System clock frequency})$

6.12.25 AUDIO PLL Setting Register (NCO_44F0A) (0x8675)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_48F0[7:0]							
Type	RW							
Default	0x09							

Note: $5.6448\text{MHz} \times 2^{28} \div (\text{System clock frequency})$

6.12.26 AUDIO PLL Setting Register (NCO_44F0B) (0x8676)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_48F0[15:8]							
Type	RW							

Default	0x6C
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6.12.27 AUDIO PLL Setting Register (NCO_44F0C) (0x8677)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_48F0[23:16]							
Type	RW							
Default	0xCE							

6.12.28 AUDIO PLL Setting Register (NCO_44F0D) (0x8678)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							
Type	RO							
Default	0x0							

Note: $5.6448\text{MHz} \times 2^{28} \div (\text{System clock frequency})$

6.13 HDMI Rx InfoFrame Data

6.13.1 Clear InfoFrame Packet Register (CLR_INFO) (0x8700)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_CLR	ISRC1_CLR	ACP_CLR	VS_CLR	SPD_CLR	MS_CLR	AUD_CLR	AVI_CLR
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
ISRC2_CLR	7	All-zero clear command for ISRC2(ETC) packet data When this bit is set to 1, Address 0x87D0 ~ 0x87EE are cleared to All-zero.
ISRC1_CLR	6	All-zero clear command for ISRC1 packet data When this bit is set to 1, Address 0x87B0 ~ 0x87C2 are cleared to All-zero.
ACP_CLR	5	All-zero clear command for ACP packet data When this bit is set to 1, Address 0x8790 ~ 0x87AE are cleared to All-zero.
VS_CLR	4	All-zero clear command for VS_info packet data When this bit is set to 1, Address 0x8770 ~ 0x878E are cleared to All-zero.
SPD_CLR	3	All-zero clear command for SPD_info packet data When this bit is set to 1, Address 0x8750 ~ 0x876E are cleared to All-zero.

MS_CLR	2	All-zero clear command for MS_info packet data When this bit is set to 1, Address 0x8740 ~ 0x874D are cleared to All-zero.
AUD_CLR	1	All-zero clear command for AUD_info packet data When this bit is set to 1, Address 0x8730 ~ 0x873D are cleared to All-zero.
AVI_CLR	0	All-zero clear command for AVI_info packet data When this bit is set to 1, Address 0x8710 ~ 0x8723 are cleared to All-zero.

6.13.2 VS INFO PACKET TYPE CODE SETTING (TYP_VS_SET) (0x8701)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_VS_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_VS_SET	7:0	X	VS_info Packet Type code setting

6.13.3 AVI INFO PACKET TYPE CODE SETTING (TYP_AVI_SET) (0x8702)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_AVI_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X
Register Field	Bit	Default	Description					
TYP_AVI_SET	7:0	X	AVI_info Packet Type code setting					

6.13.4 SPD INFO PACKET TYPE CODE SETTING (TYP_SPD_SET) (0x8703)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_SPD_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_SPD_SET	7:0	X	SPD_info Packet Type code setting

6.13.5 AUD INFO PACKET TYPE CODE SETTING (TYP_AUD_SET) (0x8704)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_AUD_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_AUD_SET	7:0	X	AUD_info Packet Type code setting

6.13.6 MS INFO PACKET TYPE CODE SETTING (TYP_MS_SET) (0x8705)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_MS_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_MS_SET	7:0	X	MS_info Packet Type code setting

6.13.7 ACP INFO PACKET TYPE CODE SETTING (TYP_ACP_SET) (0x8706)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_ACP_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_ACP_SET	7:0	X	ACP Packet Type code setting

6.13.8 ISRC1 INFO PACKET TYPE CODE SET. (TYP_ISRC1_SET) (0x8707)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_ISRC1_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_ISRC1_SET	7:0	X	ISRC1 Packet Type code setting

6.13.9 ISRC2 INFO PACKET TYPE CODE SETTING (TYP_ISRC2_SET) (0X8708)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_ISRC2_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_ISRC2_SET	7:0	X	ISRC2 Packet Type code setting

6.13.10 PACKET INTERRUPT MODE (PK_INT_MODE) (0x8709)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_IN_T_MODE	ISRC_INT_MODE	ACP_INT_MODE	VS_INT_MODE	SPD_INT_MODE	MS_INT_MODE	AUD_INT_MODE	AVI_INT_MODE
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
PK_INT_MODE	7:0	X	Packet Interrupt Mode

ISRC2_INT_MODE	7	0	Action setting during ISRC2_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
ISRC_INT_MODE	6	0	Action setting during ISRC 1 packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
ACP_INT_MODE	5	0	Action setting during ACP packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
VS_INT_MODE	4	0	Action setting during VS_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
SPD_INT_MODE	3	0	Action setting during SPD_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
MS_INT_MODE	2	0	Action setting during MS_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
AUD_INT_MODE	1	0	Action setting during AUD_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
AVI_INT_MODE	0	0	Action setting during AVI_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST

6.13.11 PACKET AUTO CLEAR (PK_AUTO_CLR) (0x870a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	PK_AUTO_CLR7	PK_AUTO_CLR6	PK_AUTO_CLR5	PK_AUTO_CLR4	PK_AUTO_CLR3	PK_AUTO_CLR2	PK_AUTO_CLR1	PK_AUTO_CLR0
Type	RW							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
PK_AUTO_CLR7	7	0	When DVI received, ISRC2_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR6	6	0	When DVI received, ISRC packet data cleared 1: Clear 0: Do not clear

PK_AUTO_CLR5	5	0	When DVI received, ACP packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR4	4	0	When DVI received, VS_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR3	3	0	When DVI received, SPD_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR2	2	0	When DVI received, MS_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR1	1	0	When DVI received, AUD_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR0	0	0	When DVI received, AVI_info packet data cleared 1: Clear 0: Do not clear

6.13.12 NO PACKET LIMIT (NO_PK_LIMIT) (0x870B)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NO_ACP_LIMIT							NO_AVI_LIMIT
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
NO_ACP_LIMIT	7:4	0	<p>After receiving ACP packet, when ACP packet not received during settingvalue*80msec period, ACP receive interrupt occurs.</p> <p>【Note】 At 4'b0000 setting, interrupt does not occur.</p> <p>【Note】 At 4'b0000 setting, ACP packet receive status action does not occur.</p> <p>【Note】 When DVI received, interrupt does not occur.</p>
NO_AVI_LIMIT	3:0	0	<p>When AVI packet not received during setting value*80msec period, AVI receive interrupt occurs.</p> <p>【Note】 At 4'b0000 setting, interrupt does not occur.</p> <p>【Note】 When DVI received, interrupt does not occur.</p>

6.13.13 NO PACKET CLEAR (NO_PK_CLR) (0x870c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	NO_VS_C_LR	NO_SPD_CLR	NO_ACP_CLR	Reserved		NO_AVI_CLR1	NO_AVI_CLR0
Type	RW	RW	RW	RW	RO		RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
NO_VS_CLR	6	0	When VS receive interrupt is detected, VS storage register automatic clear setting 0: During receive interrupt, no automatic clear 1: During receive interrupt, automatic clear
NO_SPD_CLR	5	0	When SPD receive interrupt is detected, SPD storage register automatic clear setting 0: During receive interrupt, no automatic clear 1: During receive interrupt, automatic clear
NO_ACP_CLR	4	0	When ACP receive interrupt is detected, ACP storage register automatic clear 1: Clear 0: Do not clear
NO_AVI_CLR1	1	0	When AVI receive interrupt occurs, judge input video signal with RGB and no Repetition 1: Judge 0: No judge (preserve in status before interruption)
NO_AVI_CLR0	0	0	When AVI receive interrupt is detected, AVI storage register automatic clear 1: Clear 0: Do not clear

6.13.14 ERROR PACKET LIMIT (ERR_PK_LIMIT) (0x870d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ERR_PK_MOD	ERR_PK_LIMIT						
Type	RW	RW						
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
ERR_PK_MOD	7	0x1	Packet continuing receive error detection start conditions 0: If error is included in either header/data 1: If correctable error was included in header

ERR_PK_LIMIT	6:0	0x7f	Packet continuing receive error occurrence detection threshold If error packet is continually received up to set Packet number value, Set Packet receive error status to "1". If absolutely no error Packet is received, return Packet receive error status for both header/data to "0". In 0 setting, detection OFF
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6.13.15 NO PACKET LIMIT (NO_PK_LIMIT2) (0x870E)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NO_VS_LIMIT							NO_SPD_LIMIT
Type	RW							RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
NO_VS_LIMIT	7:4	0	If no VS packet is received during setting value*80msec periodjudge receive interrupt has occurred. At 0000 setting, receiveinterrupt detect is OFF.
NO_SPD_LIMIT	3:0	0	If no SPD packet is received during setting value*80msec periodjudge receive interrupt has occurred. At 0000 setting, receiveinterrupt detect is OFF.

6.13.16 VS IEEE SELECT (VS_IEEE_SEL) (0x870f)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							VS_IEEE_SEL
Type	RO							RW
Default	0	0	0	0	0	0	0	1

Register Field	Bit	Default	Description
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VS_IEEE_SEL	0	0x1	Extraction operation selection for VS Info packet stored at HDMI_VSInfo receive register (address0x8770~8e). 1: Store only when IEEE Registration Identifier is 0x000C03 VS_Infopacket only. 0: Freely store VS_Info packet regardless of IEEE Registration Identifier. 【Note】 This register setting is valid only at address 0x8701[7:0]=81h. When address 0x8701[7:0]≠81h, this register setting is ignored, and the specified Type Packet is stored at address 0x8770~8e each time it is received.
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6.13.17 AVI INFO PACKET HEADER BYTE 0 (PK_AVI_0HEAD) (0x8710)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_OHEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_OHEAD	7:0	X	861B AVI_info packet Header byte 0 (= type)

6.13.18 AVI INFO PACKET HEADER BYTE 1 (PK_AVI_1HEAD) (0x8711)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_1HEAD	7:0	X	861B AVI_info packet Header byte 1 (= version)

6.13.19

AVI INFO PACKET HEADER BYTE 2 (PK_AVI_2HEAD) (0x8712)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_2HEAD	7:0	X	861B AVI_info packet Header byte 2 (= data length)

6.13.20

AVI INFO PACKET DATA BYTE 0 (PK_AVI_0BYTE) (0x8713)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_0BYTE	7:0	X	861B AVI_info packet Data byte 0 (= checksum)

6.13.21

AVI INFO PACKET DATA BYTE 1 (PK_AVI_1BYTE) (0x8714)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_1BYTE	7:0	X	861B AVI_info packet Data byte 1

6.13.22

AVI INFO PACKET DATA BYTE 2 (PK_AVI_2BYTE) (0x8715)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_2BYTE							
Type	RO							

Default	X	X	X	X	X	X	X	X
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Register Field	Bit	Default	Description					
AVI_2BYTE	7:0	X	861B AVI_info packet Data byte 2					

6.13.23 AVI INFO PACKET DATA BYTE 3 (PK_AVI_3BYTE) (0x8716)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
AVI_3BYTE	7:0	X	861B AVI_info packet Data byte 3					

6.13.24 AVI INFO PACKET DATA BYTE 4 (PK_AVI_4BYTE) (0x8717)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
AVI_4BYTE	7:0	X	861B AVI_info packet Data byte 4					

6.13.25 AVI INFO PACKET DATA BYTE 5 (PK_AVI_5BYTE) (0x8718)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
Confidential								

AVI_5BYTE	7:0	X	861B AVI_info packet Data byte 5
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6.13.26

AVI INFO PACKET DATA BYTE 6 (PK_AVI_6BYTE) (0x8719)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_6BYTE	7:0	X	861B AVI_info packet Data byte 6

6.13.27

AVI INFO PACKET DATA BYTE 7 (PK_AVI_7BYTE) (0x871a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_7BYTE	7:0	X	861B AVI_info packet Data byte 7

6.13.28

AVI INFO PACKET DATA BYTE 8 (PK_AVI_8BYTE) (0x871b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_8BYTE	7:0	X	861B AVI_info packet Data byte 8

6.13.29 AVI INFO PACKET DATA BYTE 9 (PK_AVI_9BYTE) (0x871c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_9BYTE	7:0	X	861B AVI_info packet Data byte 9

6.13.30 AVI INFO PACKET DATA BYTE 10 (PK_AVI_10BYTE) (0x871d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_10BYTE	7:0	X	861B AVI_info packet Data byte 10

6.13.31 AVI INFO PACKET DATA BYTE 11 (PK_AVI_11BYTE) (0x871e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_11BYTE	7:0	X	861B AVI_info packet Data byte 11

6.13.32 AVI INFO PACKET DATA BYTE 12 (PK_AVI_12BYTE) (0x871f)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
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Name	AVI_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_12BYTE	7:0	X	861B AVI_info packet Data byte 12

6.13.33 AVI INFO PACKET DATA BYTE 13 (PK_AVI_13BYTE) (0x8720)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_13BYTE	7:0	X	861B AVI_info packet Data byte 13

6.13.34 AVI INFO PACKET DATA BYTE 14 (PK_AVI_14BYTE) (0x8721)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_14BYTE	7:0	X	861B AVI_info packet Data byte 14 (Reserved for standards extension)

6.13.35 AVI INFO PACKET DATA BYTE 15 (PK_AVI_15BYTE) (0x8722)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_15BYTE							

Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_15BYTE	7:0	X	861B AVI_info packet Data byte 15 (Reserved for standards extension)

6.13.36 AVI INFO PACKET DATA BYTE 16 (PK_AVI_16BYTE) (0x8723)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_16BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_16BYTE	7:0	X	861B AVI_info packet Data byte 16 (Reserved for standards extension)

6.13.37 AUD INFO PACKET HEADER BYTE 0 (PK_AUD_0HEAD) (0x8730)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_0HEAD	7:0	X	861B AUD_info packet Header byte 0 (= type)

6.13.38 AUD INFO PACKET HEADER BYTE 1 (PK_AUD_1HEAD) (0x8731)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_1HEAD							

Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_1HEAD	7:0	X	861B AUD_info packet Header byte 1 (= version)

6.13.39 AUD INFO PACKET HEADER BYTE 2 (PK_AUD_2HEAD) (0x8732)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_2HEAD	7:0	X	861B AUD_info packet Header byte 2 (= data length)

6.13.40 AUD INFO PACKET DATA BYTE 0 (PK_AUD_0BYTE) (0x8733)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_0BYTE	7:0	X	861B AUD_info packet Data byte 0 (= checksum)

6.13.41 AUD INFO PACKET DATA BYTE 1 (PK_AUD_1BYTE) (0x8734)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_1BYTE	7:0	X	861B AUD_info packet Data byte 1

6.13.42 AUD INFO PACKET DATA BYTE 2 (PK_AUD_2BYTE) (0x8735)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_2BYTE	7:0	X	861B AUD_info packet Data byte 2

6.13.43 AUD INFO PACKET DATA BYTE 3 (PK_AUD_3BYTE) (0x8736)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_3BYTE	7:0	X	861B AUD_info packet Data byte 3

6.13.44 AUD INFO PACKET DATA BYTE 4 (PK_AUD_4BYTE) (0x8737)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_4BYTE	7:0	X	861B AUD_info packet Data byte 4

6.13.45 AUD INFO PACKET DATA BYTE 5 (PK_AUD_5BYTE) (0x8738)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_5BYTE	7:0	X	861B AUD_info packet Data byte 5

6.13.46 AUD INFO PACKET DATA BYTE 6 (PK_AUD_6BYTE) (0x8739)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_6BYTE	7:0	X	861B AUD_info packet Data byte 6 (Reserved for standards extension)

6.13.47 AUD INFO PACKET DATA BYTE 7 (PK_AUD_7BYTE) (0x873a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_7BYTE	7:0	X	861B AUD_info packet Data byte 7 (Reserved for standards extension)

6.13.48

AUD INFO PACKET DATA BYTE 8 (PK_AUD_8BYTE) (0x873b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_8BYTE	7:0	X	861B AUD_info packet Data byte 8 (Reserved for standards extension)

6.13.49

AUD INFO PACKET DATA BYTE 9 (PK_AUD_9BYTE) (0x873c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_9BYTE	7:0	X	861B AUD_info packet Data byte 9 (Reserved for standards extension)

6.13.50

AUD INFO PACKET DATA BYTE 10 (PK_AUD_10BYTE) (0x873d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description

AUD_10BYTE	7:0	X	861B AUD_info packet Data byte 10 (Reserved for standards extension)
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6.13.51 MS INFO PACKET HEADER BYTE 0 (PK_MS_0HEAD) (0x8740)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_0HEAD	7:0	X	861B MS_info packet Header byte 0 (= type)

6.13.52 MS INFO PACKET HEADER BYTE 1 (PK_MS_1HEAD) (0x8741)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_1HEAD	7:0	X	861B MS_info packet Header byte 1 (= version)

6.13.53 MS INFO PACKET HEADER BYTE 2 (PK_MS_2HEAD) (0x8742)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_2HEAD	7:0	X	861B MS_info packet Header byte 2 (= data length)

6.13.54

MS INFO PACKET DATA BYTE 0 (PK_MS_0BYTE) (0x8743)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_0BYTE	7:0	X	861B MS_info packet Data byte 0 (= checksum)

6.13.55

MS INFO PACKET DATA BYTE 1 (PK_MS_1BYTE) (0x8744)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_1BYTE	7:0	X	861B MS_info packet Data byte 1

6.13.56

MS INFO PACKET DATA BYTE 2 (PK_MS_2BYTE) (0x8745)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_2BYTE	7:0	X	861B MS_info packet Data byte 2

6.13.57 MS INFO PACKET DATA BYTE 3 (PK_MS_3BYTE) (0x8746)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_3BYTE	7:0	X	861B MS_info packet Data byte 3

6.13.58 MS INFO PACKET DATA BYTE 4 (PK_MS_4BYTE) (0x8747)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_4BYTE	7:0	X	861B MS_info packet Data byte 4

6.13.59 MS INFO PACKET DATA BYTE 5 (PK_MS_5BYTE) (0x8748)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_5BYTE	7:0	X	861B MS_info packet Data byte 5

6.13.60 MS INFO PACKET DATA BYTE 6 (PK_MS_6BYTE) (0x8749)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
-----	----	----	----	----	----	----	----	----

Name	MS_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
MS_6BYTE	7:0	X	861B MS_info packet Data byte 6 (Reserved for standards extension)					

6.13.61 MS INFO PACKET DATA BYTE 7 (PK_MS_7BYTE) (0x874a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
MS_7BYTE	7:0	X	861B MS_info packet Data byte 7 (Reserved for standards extension)					

6.13.62 MS INFO PACKET DATA BYTE 8 (PK_MS_8BYTE) (0x874b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
MS_8BYTE	7:0	X	861B MS_info packet Data byte 8 (Reserved for standards extension)					

6.13.63

MS INFO PACKET DATA BYTE 9 (PK_MS_9BYTE) (0x874c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field

Bit

Default

Description

MS_9BYTE

7:0

X

861B MS_info packet Data byte 9 (Reserved for standards extension)

6.13.64

MS INFO PACKET DATA BYTE 10 (PK_MS_10BYTE) (0x874d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field

Bit

Default

Description

MS_10BYTE

7:0

X

861B MS_info packet Data byte 10 (Reserved for standards extension)

6.13.65

SPD INFO PACKET HEADER BYTE 0 (PK_SPD_0HEAD) (0x8750)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field

Bit

Default

Description

SPD_0HEAD

7:0

X

861B SPD_info packet Header byte 0 (= type)

6.13.66 SPD INFO PACKET HEADER BYTE 1 (PK_SPD_1HEAD) (0x8751)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_1HEAD	7:0	X	861B SPD_info packet Header byte 1 (= version)

6.13.67 SPD INFO PACKET HEADER BYTE 2 (PK_SPD_2HEAD) (0x8752)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_2HEAD	7:0	X	861B SPD_info packet Header byte 2 (= data length)

6.13.68 SPD INFO PACKET DATA BYTE 0 (PK_SPD_0BYTE) (0x8753)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_0BYTE	7:0	X	861B SPD_info packet Data byte 0 (= checksum)

6.13.69 SPD INFO PACKET DATA BYTE 1 (PK_SPD_1BYTE) (0x8754)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
-----	----	----	----	----	----	----	----	----

Name	SPD_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_1BYTE	7:0	X	861B SPD_info packet Data byte 1

6.13.70 SPD INFO PACKET DATA BYTE 2 (PK_SPD_2BYTE) (0x8755)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_2BYTE	7:0	X	861B SPD_info packet Data byte 2

6.13.71 SPD INFO PACKET DATA BYTE 3 (PK_SPD_3BYTE) (0x8756)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_3BYTE	7:0	X	861B SPD_info packet Data byte 3

6.13.72 SPD INFO PACKET DATA BYTE 4 (PK_SPD_4BYTE) (0x8757)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_4BYTE	7:0	X	861B SPD_info packet Data byte 4

6.13.73 SPD INFO PACKET DATA BYTE 5 (PK_SPD_5BYTE) (0x8758)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_5BYTE	7:0	X	861B SPD_info packet Data byte 5

6.13.74 SPD INFO PACKET DATA BYTE 6 (PK_SPD_6BYTE) (0x8759)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_6BYTE	7:0	X	861B SPD_info packet Data byte 6

6.13.75 SPD INFO PACKET DATA BYTE 7 (PK_SPD_7BYTE) (0x875a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TC358840XBG/870XBG			Confidential

SPD_7BYTE	7:0	X	861B SPD_info packet Data byte 7
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6.13.76 SPD INFO PACKET DATA BYTE 8 (PK_SPD_8BYTE) (0x875b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_8BYTE	7:0	X	861B SPD_info packet Data byte 8

6.13.77 SPD INFO PACKET DATA BYTE 9 (PK_SPD_9BYTE) (0x875c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_9BYTE	7:0	X	861B SPD_info packet Data byte 9

6.13.78 SPD INFO PACKET DATA BYTE 10 (PK_SPD_10BYTE) (0x875d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_10BYTE	7:0	X	861B SPD_info packet Data byte 10

6.13.79

SPD INFO PACKET DATA BYTE 11 (PK_SPD_11BYTE) (0x875e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X
Register Field	Bit	Default	Description					
SPD_11BYTE	7:0	X	861B SPD_info packet Data byte 11					

6.13.80

SPD INFO PACKET DATA BYTE 12 (PK_SPD_12BYTE) (0x875f)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X
Register Field	Bit	Default	Description					
SPD_12BYTE	7:0	X	861B SPD_info packet Data byte 12					

6.13.81

SPD INFO PACKET DATA BYTE 13 (PK_SPD_13BYTE) (0x8760)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X
Register Field	Bit	Default	Description					
SPD_13BYTE	7:0	X	861B SPD_info packet Data byte 13					

6.13.82

SPD INFO PACKET DATA BYTE 14 (PK_SPD_14BYTE) (0x8761)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_14BYTE	7:0	X	861B SPD_info packet Data byte 14

6.13.83

SPD INFO PACKET DATA BYTE 15 (PK_SPD_15BYTE) (0x8762)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_15BYTE	7:0	X	861B SPD_info packet Data byte 15

6.13.84

SPD INFO PACKET DATA BYTE 16 (PK_SPD_16BYTE) (0x8763)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_16BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_16BYTE	7:0	X	861B SPD_info packet Data byte 16

6.13.85

SPD INFO PACKET DATA BYTE 17 (PK_SPD_17BYTE) (0x8764)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_17BYTE							

Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
SPD_17BYTE	7:0	X	861B SPD_info packet Data byte 17					

6.13.86 SPD INFO PACKET DATA BYTE 18 (PK_SPD_18BYTE) (0x8765)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_18BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
SPD_18BYTE	7:0	X	861B SPD_info packet Data byte 18					

6.13.87 SPD INFO PACKET DATA BYTE 19 (PK_SPD_19BYTE) (0x8766)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_19BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
SPD_19BYTE	7:0	X	861B SPD_info packet Data byte 19					

6.13.88 SPD INFO PACKET DATA BYTE 20 (PK_SPD_20BYTE) (0x8767)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_20BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_20BYTE	7:0	X	861B SPD_info packet Data byte 20

6.13.89 SPD INFO PACKET DATA BYTE 21 (PK_SPD_21BYTE) (0x8768)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_21BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_21BYTE	7:0	X	861B SPD_info packet Data byte 21

6.13.90 SPD INFO PACKET DATA BYTE 22 (PK_SPD_22BYTE) (0x8769)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_22BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_22BYTE	7:0	X	861B SPD_info packet Data byte 22

6.13.91 SPD INFO PACKET DATA BYTE 23 (PK_SPD_23BYTE) (0x876a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_23BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_23BYTE	7:0	X	861B SPD_info packet Data byte 23

6.13.92

SPD INFO PACKET DATA BYTE 24 (PK_SPD_24BYTE) (0x876b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_24BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_24BYTE	7:0	X	861B SPD_info packet Data byte 24

6.13.93

SPD INFO PACKET DATA BYTE 25 (PK_SPD_25BYTE) (0x876c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_25BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_25BYTE	7:0	X	861B SPD_info packet Data byte 25

6.13.94

SPD INFO PACKET DATA BYTE 26 (PK_SPD_26BYTE) (0x876d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_26BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_26BYTE	7:0	X	861B SPD_info packet Data byte 26 (Reserved for standards extension)

6.13.95

SPD INFO PACKET DATA BYTE 27 (PK_SPD_27BYTE) (0x876e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_27BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_27BYTE	7:0	X	861B SPD_info packet Data byte 27 (Reserved for standards extension)

6.13.96

VS INFO PACKET HEADER BYTE 0 (PK_VS_0HEAD) (0x8770)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_0HEAD	7:0	X	861B VS_info packet Header byte 0 (= type)

6.13.97

VS INFO PACKET HEADER BYTE 1 (PK_VS_1HEAD) (0x8771)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_1HEAD	7:0	X	861B VS_info packet Header byte 1 (= version)

6.13.98

VS INFO PACKET HEADER BYTE 2 (PK_VS_2HEAD) (0x8772)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_2HEAD	7:0	X	861B VS_info packet Header byte 2 (= data length)

6.13.99

VS INFO PACKET DATA BYTE 0 (PK_VS_0BYTE) (0x8773)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_0BYTE	7:0	X	861B VS_info packet Data byte 0 (= checksum)

6.13.100

VS INFO PACKET DATA BYTE 1 (PK_VS_1BYTE) (0x8774)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_1BYTE	7:0	X	861B VS_info packet Data byte 1

6.13.101 VS INFO PACKET DATA BYTE 2 (PK_VS_2BYTE) (0x8775)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_2BYTE							

Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
VS_2BYTE	7:0	X	861B VS_info packet Data byte 2					

6.13.102 VS INFO PACKET DATA BYTE 3 (PK_VS_3BYTE) (0x8776)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
VS_3BYTE	7:0	X	861B VS_info packet Data byte 3					

6.13.103 VS INFO PACKET DATA BYTE 4 (PK_VS_4BYTE) (0x8777)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
VS_4BYTE	7:0	X	861B VS_info packet Data byte 4					

6.13.104 VS INFO PACKET DATA BYTE 5 (PK_VS_5BYTE) (0x8778)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_5BYTE	7:0	X	861B VS_info packet Data byte 5

6.13.105 VS INFO PACKET DATA BYTE 6 (PK_VS_6BYTE) (0x8779)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_6BYTE	7:0	X	861B VS_info packet Data byte 6

6.13.106 VS INFO PACKET DATA BYTE 7 (PK_VS_7BYTE) (0x877a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_7BYTE	7:0	X	861B VS_info packet Data byte 7

6.13.107 VS INFO PACKET DATA BYTE 8 (PK_VS_8BYTE) (0x877b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TC358840XBG/870XBG			<i>Confidential</i>

VS_8BYTE	7:0	X	861B VS_info packet Data byte 8
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6.13.108

VS INFO PACKET DATA BYTE 9 (PK_VS_9BYTE) (0x877c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_9BYTE	7:0	X	861B VS_info packet Data byte 9

6.13.109

VS INFO PACKET DATA BYTE 10 (PK_VS_10BYTE) (0x877d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_10BYTE	7:0	X	861B VS_info packet Data byte 10

6.13.110

VS INFO PACKET DATA BYTE 11 (PK_VS_11BYTE) (0x877e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_11BYTE	7:0	X	861B VS_info packet Data byte 11

VS_11BYTE	7:0	X	861B VS_info packet Data byte 11
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6.13.111 VS INFO PACKET DATA BYTE 12 (PK_VS_12BYTE) (0x877f)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_12BYTE	7:0	X	861B VS_info packet Data byte 12

6.13.112 VS INFO PACKET DATA BYTE 13 (PK_VS_13BYTE) (0x8780)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_13BYTE	7:0	X	861B VS_info packet Data byte 13

6.13.113 VS INFO PACKET DATA BYTE 14 (PK_VS_14BYTE) (0x8781)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_14BYTE	7:0	X	861B VS_info packet Data byte 14

6.13.114

VS INFO PACKET DATA BYTE 15 (PK_VS_15BYTE) (0x8782)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_15BYTE	7:0	X	861B VS_info packet Data byte 15

6.13.115

VS INFO PACKET DATA BYTE 16 (PK_VS_16BYTE) (0x8783)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_16BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_16BYTE	7:0	X	861B VS_info packet Data byte 16

6.13.116

VS INFO PACKET DATA BYTE 17 (PK_VS_17BYTE) (0x8784)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_17BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_17BYTE	7:0	X	861B VS_info packet Data byte 17

6.13.117

VS INFO PACKET DATA BYTE 18 (PK_VS_18BYTE) (0x8785)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_18BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_18BYTE	7:0	X	861B VS_info packet Data byte 18

6.13.118

VS INFO PACKET DATA BYTE 19 (PK_VS_19BYTE) (0x8786)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_19BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_19BYTE	7:0	X	861B VS_info packet Data byte 19

6.13.119

VS INFO PACKET DATA BYTE 20 (PK_VS_20BYTE) (0x8787)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_20BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_20BYTE	7:0	X	861B VS_info packet Data byte 20

6.13.120 VS INFO PACKET DATA BYTE 21 (PK_VS_21BYTE) (0x8788)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_21BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_21BYTE	7:0	X	861B VS_info packet Data byte 21

6.13.121 VS INFO PACKET DATA BYTE 22 (PK_VS_22BYTE) (0x8789)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_22BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_22BYTE	7:0	X	861B VS_info packet Data byte 22

6.13.122 VS INFO PACKET DATA BYTE 23 (PK_VS_23BYTE) (0x878a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_23BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_23BYTE	7:0	X	861B VS_info packet Data byte 23

6.13.123 VS INFO PACKET DATA BYTE 24 (PK_VS_24BYTE) (0x878b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
-----	----	----	----	----	----	----	----	----

Name	VS_24BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_24BYTE	7:0	X	861B VS_info packet Data byte 24

6.13.124 VS INFO PACKET DATA BYTE 25 (PK_VS_25BYTE) (0x878c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_25BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_25BYTE	7:0	X	861B VS_info packet Data byte 25

6.13.125 VS INFO PACKET DATA BYTE 26 (PK_VS_26BYTE) (0x878d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_26BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_26BYTE	7:0	X	861B VS_info packet Data byte 26

6.13.126 VS INFO PACKET DATA BYTE 27 (PK_VS_27BYTE) (0x878e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_27BYTE							
Type	RO							

Default	X	X	X	X	X	X	X	X
---------	---	---	---	---	---	---	---	---

Register Field	Bit	Default	Description
VS_27BYTE	7:0	X	861B VS_info packet Data byte 27

6.13.127 ACP INFO PACKET HEADER BYTE 0 (PK_ACP_0HEAD) (0x8790)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_0HEAD	7:0	X	861B ACP_info packet Header byte 0 (= type)

6.13.128 ACP INFO PACKET HEADER BYTE 1 (PK_ACP_1HEAD) (0x8791)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_1HEAD	7:0	X	861B ACP_info packet Header byte 1 (= version)

6.13.129 ACP INFO PACKET HEADER BYTE 2 (PK_ACP_2HEAD) (0x8792)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_2HEAD	7:0	X	861B ACP_info packet Header byte 2 (= data length)

6.13.130 ACP INFO PACKET DATA BYTE 0 (PK_ACP_0BYTE) (0x8793)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_0BYTE	7:0	X	861B ACP_info packet Data byte 0 (= checksum)

6.13.131 ACP INFO PACKET DATA BYTE 1 (PK_ACP_1BYTE) (0x8794)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_1BYTE	7:0	X	861B ACP_info packet Data byte 1

6.13.132 ACP INFO PACKET DATA BYTE 2 (PK_ACP_2BYTE) (0x8795)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_2BYTE	7:0	X	861B ACP_info packet Data byte 2

6.13.133 ACP INFO PACKET DATA BYTE 3 (PK_ACP_3BYTE) (0x8796)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_3BYTE	7:0	X	861B ACP_info packet Data byte 3

6.13.134 ACP INFO PACKET DATA BYTE 4 (PK_ACP_4BYTE) (0x8797)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_4BYTE	7:0	X	861B ACP_info packet Data byte 4

6.13.135 ACP INFO PACKET DATA BYTE 5 (PK_ACP_5BYTE) (0x8798)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_5BYTE	7:0	X	861B ACP_info packet Data byte 5

6.13.136 ACP INFO PACKET DATA BYTE 6 (PK_ACP_6BYTE) (0x8799)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
-----	----	----	----	----	----	----	----	----

Name	ACP_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_6BYTE	7:0	X	861B ACP_info packet Data byte 6

6.13.137 ACP INFO PACKET DATA BYTE 7 (PK_ACP_7BYTE) (0x879a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_7BYTE	7:0	X	861B ACP_info packet Data byte 7

6.13.138 ACP INFO PACKET DATA BYTE 8 (PK_ACP_8BYTE) (0x879b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_8BYTE	7:0	X	861B ACP_info packet Data byte 8

6.13.139 ACP INFO PACKET DATA BYTE 9 (PK_ACP_9BYTE) (0x879c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
ACP_9BYTE	7:0	X	861B ACP_info packet Data byte 9					

6.13.140 ACP INFO PACKET DATA BYTE 10 (PK_ACP_10BYTE) (0x879d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
ACP_10BYTE	7:0	X	861B ACP_info packet Data byte 10					

6.13.141 ACP INFO PACKET DATA BYTE 11 (PK_ACP_11BYTE) (0x879e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
ACP_11BYTE	7:0	X	861B ACP_info packet Data byte 11					

6.13.142 ACP INFO PACKET DATA BYTE 12 (PK_ACP_12BYTE) (0x879f)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
ACP_12BYTE	7:0	X	861B ACP_info packet Data byte 12					

6.13.143 ACP INFO PACKET DATA BYTE 13 (PK_ACP_13BYTE) (0x87a0)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_13BYTE	7:0	X	861B ACP_info packet Data byte 13

6.13.144 ACP INFO PACKET DATA BYTE 14 (PK_ACP_14BYTE) (0x87a1)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_14BYTE	7:0	X	861B ACP_info packet Data byte 14

6.13.145 ACP INFO PACKET DATA BYTE 15 (PK_ACP_15BYTE) (0x87a2)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_15BYTE	7:0	X	861B ACP_info packet Data byte 15

6.13.146 ACP INFO PACKET DATA BYTE 16 (PK_ACP_16BYTE) (0x87a3)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_16BYTE							

Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
ACP_16BYTE	7:0	X	861B ACP_info packet Data byte 16					

6.13.147 ACP INFO PACKET DATA BYTE 17 (PK_ACP_17BYTE) (0x87a4)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_17BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
ACP_17BYTE	7:0	X	861B ACP_info packet Data byte 17					

6.13.148 ACP INFO PACKET DATA BYTE 18 (PK_ACP_18BYTE) (0x87a5)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_18BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
ACP_18BYTE	7:0	X	861B ACP_info packet Data byte 18					

6.13.149 ACP INFO PACKET DATA BYTE 19 (PK_ACP_19BYTE) (0x87a6)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_19BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
Confidential								

ACP_19BYTE	7:0	X	861B ACP_info packet Data byte 19
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6.13.150 ACP INFO PACKET DATA BYTE 20 (PK_ACP_20BYTE) (0x87a7)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_20BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_20BYTE	7:0	X	861B ACP_info packet Data byte 20

6.13.151 ACP INFO PACKET DATA BYTE 21 (PK_ACP_21BYTE) (0x87a8)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_21BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_21BYTE	7:0	X	861B ACP_info packet Data byte 21

6.13.152 ACP INFO PACKET DATA BYTE 22 (PK_ACP_22BYTE) (0x87a9)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_22BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_22BYTE	7:0	X	861B ACP_info packet Data byte 22

6.13.153

ACP INFO PACKET DATA BYTE 23 (PK_ACP_23BYTE) (0x87aa)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_23BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_23BYTE	7:0	X	861B ACP_info packet Data byte 23

6.13.154

ACP INFO PACKET DATA BYTE 24 (PK_ACP_24BYTE) (0x87ab)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_24BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_24BYTE	7:0	X	861B ACP_info packet Data byte 24

6.13.155

ACP INFO PACKET DATA BYTE 25 (PK_ACP_25BYTE) (0x87ac)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_25BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_25BYTE	7:0	X	861B ACP_info packet Data byte 25

6.13.156

ACP INFO PACKET DATA BYTE 26 (PK_ACP_26BYTE) (0x87ad)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
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Name	ACP_26BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_26BYTE	7:0	X	861B ACP_info packet Data byte 26

6.13.157 ACP INFO PACKET DATA BYTE 27 (PK_ACP_27BYTE) (0x87ae)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_27BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_27BYTE	7:0	X	861B ACP_info packet Data byte 27

6.13.158 ISRC1 INFO PACKET HEADER BYTE 0 (PK_ISRC1_0HEAD) (0x87b0)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_0HEAD	7:0	X	861B ISRC1_info packet Header byte 0 (= type)

6.13.159 ISRC1 INFO PACKET HEADER BYTE 1 (PK_ISRC1_1HEAD) (0x87b1)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
Confidential			

ISRC1_1HEAD	7:0	X	861B ISRC1_info packet Header byte 1 (= version)
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6.13.160 ISRC1 INFO PACKET HEADER BYTE 2 (PK_ISRC1_2HEAD) (0x87b2)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_2HEAD	7:0	X	861B ISRC1_info packet Header byte 2 (= data length)

6.13.161 ISRC1 INFO PACKET DATA BYTE 0 (PK_ISRC1_0BYTE) (0x87b3)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_0BYTE	7:0	X	861B ISRC1_info packet Data byte 0 (= checksum)

6.13.162 ISRC1 INFO PACKET DATA BYTE 1 (PK_ISRC1_1BYTE) (0x87b4)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_1BYTE	7:0	X	861B ISRC1_info packet Data byte 1

6.13.163 ISRC1 INFO PACKET DATA BYTE 2 (PK_ISRC1_2BYTE) (0x87b5)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_2BYTE							
Type	RO							

Default	X	X	X	X	X	X	X	X
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Register Field	Bit	Default	Description					
ISRC1_2BYTE	7:0	X	861B ISRC1_info packet Data byte 2					

6.13.164 ISRC1 INFO PACKET DATA BYTE 3 (PK_ISRC1_3BYTE) (0x87b6)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
ISRC1_3BYTE	7:0	X	861B ISRC1_info packet Data byte 3					

6.13.165 ISRC1 INFO PACKET DATA BYTE 4 (PK_ISRC1_4BYTE) (0x87b7)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description					
ISRC1_4BYTE	7:0	X	861B ISRC1_info packet Data byte 4					

6.13.166 ISRC1 INFO PACKET DATA BYTE 5 (PK_ISRC1_5BYTE) (0x87b8)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_5BYTE	7:0	X	861B ISRC1_info packet Data byte 5

6.13.167 ISRC1 INFO PACKET DATA BYTE 6 (PK_ISRC1_6BYTE) (0x87b9)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_6BYTE	7:0	X	861B ISRC1_info packet Data byte 6

6.13.168 ISRC1 INFO PACKET DATA BYTE 7 (PK_ISRC1_7BYTE) (0x87ba)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_7BYTE	7:0	X	861B ISRC1_info packet Data byte 7

6.13.169 ISRC1 INFO PACKET DATA BYTE 8 (PK_ISRC1_8BYTE) (0x87bb)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_8BYTE	7:0	X	861B ISRC1_info packet Data byte 8

6.13.170 ISRC1 INFO PACKET DATA BYTE 9 (PK_ISRC1_9BYTE) (0x87bc)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_9BYTE	7:0	X	861B ISRC1_info packet Data byte 9

6.13.171 ISRC1 INFO PACKET DATA BYTE 10 (PK_ISRC1_10BYTE) (0x87bd)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_10BYTE	7:0	X	861B ISRC1_info packet Data byte 10

6.13.172 ISRC1 INFO PACKET DATA BYTE 11 (PK_ISRC1_11BYTE) (0x87be)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_11BYTE	7:0	X	861B ISRC1_info packet Data byte 11

6.13.173 ISRC1 INFO PACKET DATA BYTE 12 (PK_ISRC1_12BYTE) (0x87bf)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_12BYTE	7:0	X	861B ISRC1_info packet Data byte 12

6.13.174 ISRC1 INFO PACKET DATA BYTE 13 (PK_ISRC1_13BYTE) (0x87c0)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_13BYTE	7:0	X	861B ISRC1_info packet Data byte 13

6.13.175 ISRC1 INFO PACKET DATA BYTE 14 (PK_ISRC1_14BYTE) (0x87c1)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_14BYTE	7:0	X	861B ISRC1_info packet Data byte 14

6.13.176 ISRC1 INFO PACKET DATA BYTE 15 (PK_ISRC1_15BYTE) (0x87c2)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_15BYTE	7:0	X	861B ISRC1_info packet Data byte 15

6.13.177 ISRC2 INFO PACKET HEADER BYTE 0 (PK_ISRC2_0HEAD) (0x87d0)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_0HEAD	7:0	X	861B ISRC2_info packet Header byte 0 (= type)

6.13.178 ISRC2 INFO PACKET HEADER BYTE 1 (PK_ISRC2_1HEAD) (0x87d1)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_1HEAD	7:0	X	861B ISRC2_info packet Header byte 1 (= version)

6.13.179 ISRC2 INFO PACKET HEADER BYTE 2 (PK_ISRC2_2HEAD) (0x87d2)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_2HEAD	7:0	X	861B ISRC2_info packet Header byte 2 (= data length)

6.13.180 ISRC2 INFO PACKET DATA BYTE 0 (PK_ISRC2_0BYTE) (0x87d3)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_0BYTE	7:0	X	861B ISRC2_info packet Data byte 0 (= checksum)

6.13.181 ISRC2 INFO PACKET DATA BYTE 1 (PK_ISRC2_1BYTE) (0x87d4)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_1BYTE	7:0	X	861B ISRC2_info packet Data byte 1

6.13.182 ISRC2 INFO PACKET DATA BYTE 2 (PK_ISRC2_2BYTE) (0x87d5)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_2BYTE	7:0	X	861B ISRC2_info packet Data byte 2

6.13.183 ISRC2 INFO PACKET DATA BYTE 3 (PK_ISRC2_3BYTE) (0x87d6)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_3BYTE	7:0	X	861B ISRC2_info packet Data byte 3

6.13.184 ISRC2 INFO PACKET DATA BYTE 4 (PK_ISRC2_4BYTE) (0x87d7)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_4BYTE	7:0	X	861B ISRC2_info packet Data byte 4

6.13.185 ISRC2 INFO PACKET DATA BYTE 5 (PK_ISRC2_5BYTE) (0x87d8)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_5BYTE	7:0	X	861B ISRC2_info packet Data byte 5

6.13.186 ISRC2 INFO PACKET DATA BYTE 6 (PK_ISRC2_6BYTE) (0x87d9)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_6BYTE	7:0	X	861B ISRC2_info packet Data byte 6

6.13.187 ISRC2 INFO PACKET DATA BYTE 7 (PK_ISRC2_7BYTE) (0x87da)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_7BYTE	7:0	X	861B ISRC2_info packet Data byte 7

6.13.188 ISRC2 INFO PACKET DATA BYTE 8 (PK_ISRC2_8BYTE) (0x87db)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_8BYTE	7:0	X	861B ISRC2_info packet Data byte 8

6.13.189 ISRC2 INFO PACKET DATA BYTE 9 (PK_ISRC2_9BYTE) (0x87dc)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_9BYTE	7:0	X	861B ISRC2_info packet Data byte 9

6.13.190 ISRC2 INFO PACKET DATA BYTE 10 (PK_ISRC2_10BYTE) (0x87dd)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_10BYTE	7:0	X	861B ISRC2_info packet Data byte 10

6.13.191 ISRC2 INFO PACKET DATA BYTE 11 (PK_ISRC2_11BYTE) (0x87de)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_11BYTE	7:0	X	861B ISRC2_info packet Data byte 11

6.13.192 ISRC2 INFO PACKET DATA BYTE 12 (PK_ISRC2_12BYTE) (0x87df)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_12BYTE	7:0	X	861B ISRC2_info packet Data byte 12

6.13.193 ISRC2 INFO PACKET DATA BYTE 13 (PK_ISRC2_13BYTE) (0x87e0)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_13BYTE	7:0	X	861B ISRC2_info packet Data byte 13

6.13.194 ISRC2 INFO PACKET DATA BYTE 14 (PK_ISRC2_14BYTE) (0x87e1)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_14BYTE	7:0	X	861B ISRC2_info packet Data byte 14

6.13.195 ISRC2 INFO PACKET DATA BYTE 15 (PK_ISRC2_15BYTE) (0x87e2)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_15BYTE	7:0	X	861B ISRC2_info packet Data byte 15

6.13.196 ISRC2 INFO PACKET DATA BYTE 16 (PK_ISRC2_16BYTE) (0x87e3)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_16BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_16BYTE	7:0	X	861B ISRC2_info packet Data byte 16

6.13.197 ISRC2 INFO PACKET DATA BYTE 17 (PK_ISRC2_17BYTE) (0x87e4)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_17BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_17BYTE	7:0	X	861B ISRC2_info packet Data byte 17

6.13.198 ISRC2 INFO PACKET DATA BYTE 18 (PK_ISRC2_18BYTE) (0x87e5)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_18BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_18BYTE	7:0	X	861B ISRC2_info packet Data byte 18

6.13.199 ISRC2 INFO PACKET DATA BYTE 19 (PK_ISRC2_19BYTE) (0x87e6)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_19BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_19BYTE	7:0	X	861B ISRC2_info packet Data byte 19

6.13.200 ISRC2 INFO PACKET DATA BYTE 20 (PK_ISRC2_20BYTE) (0x87e7)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_20BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_20BYTE	7:0	X	861B ISRC2_info packet Data byte 20

6.13.201 ISRC2 INFO PACKET DATA BYTE 21 (PK_ISRC2_21BYTE) (0x87e8)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_21BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_21BYTE	7:0	X	861B ISRC2_info packet Data byte 21

6.13.202 ISRC2 INFO PACKET DATA BYTE 22 (PK_ISRC2_22BYTE) (0x87e9)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_22BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_22BYTE	7:0	X	861B ISRC2_info packet Data byte 22

6.13.203 ISRC2 INFO PACKET DATA BYTE 23 (PK_ISRC2_23BYTE) (0x87ea)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_23BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_23BYTE	7:0	X	861B ISRC2_info packet Data byte 23

6.13.204 ISRC2 INFO PACKET DATA BYTE 24 (PK_ISRC2_24BYTE) (0x87eb)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_24BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_24BYTE	7:0	X	861B ISRC2_info packet Data byte 24

6.13.205 ISRC2 INFO PACKET DATA BYTE 25 (PK_ISRC2_25BYTE) (0x87ec)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_25BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_25BYTE	7:0	X	861B ISRC2_info packet Data byte 25

6.13.206 ISRC2 INFO PACKET DATA BYTE 26 (PK_ISRC2_26BYTE) (0x87ed)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_26BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_26BYTE	7:0	X	861B ISRC2_info packet Data byte 26

6.13.207 ISRC2 INFO PACKET DATA BYTE 27 (PK_ISRC2_27BYTE) (0x87ee)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_27BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_27BYTE	7:0	X	861B ISRC2_info packet Data byte 27

6.14 HDMI Rx HDCP Registers

Only a few are listed here. The others can be referred to HDCP spec. For register 0x88_XX, please refer to HDCP register 0xXX. For example: For register 0x88_08 → HDCP RI'0 Data.

6.14.1 HDCP BCAPS Register (BCAPS) (0x8840)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	HDMI_RSVD	Repeater	Ready	FastI2C	Reserved		1.1Fea	Fast_ReAu
Type	RW	RW	RW	RW	RO		RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
HDMI_RESERVED	7	0	0: automatic move to HDMI mode is not performed.
REPETER	6	0	1: HDCP Repeter
READY	5	0	KSVFiFo is Ready for 2 nd Authentication
FAST(DDC I2C speed)	4	0	1: 400 KHz Supported
Reserved	[3:2]	0	
1.1_FEATURES	1	0	Fixed at '0'
FAST_REAUTH	0	0	Fast re-authentication

6.14.2 HDCP Rx BSTATUS0 Register (BSTATUS0) (0x8841)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MAX_DEVS_EXCEEDED				DEVICE_COUNT			
Type	RW				RW			
Default	0				0x00			

Register Field	Bit	Description
MAX_DEVS_EXCEEDED	7	If later stage connection devices number is 17 or more, set to "1".
DEVICE_COUNT	[6:0]	Later stage connection device number (not including self)

6.14.3 HDCP Rx BSTATUS1 Register (BSTATUS1) (0x8842)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		HDMI_RSVD	HDMI_MODE	MAX_EXCED	DEPTH		

Type	RO	RW	RW	RW	RW
Default	0	0	0	0	0

Register Field	Bit	Default	Description
Reserved	[7:6]	0	
HDMI_RSVD	5	0	V' value calculation state machine reset 1: Reset (Auto clear)
HDMI_MODE	4	0	HDMI mode setting 0: DVI mode, 1: HDMI mode
MAX_EXCED	3	0	Topology error indicator. When set to one, more than seven levels of the repeater have been cascaded together.
DEPTH	[2:0]	0	Three-bit repeater cascade depth. This value gives the number of attached levels through the connection topology.

6.14.4 KSVFIFO Register (KSVFIFO) (0x8843)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	KSVFIFO							
Type	RW							
Default	0							

Register Field	Bit	Default	Description
KSVFIFO	[7:0]	0x00	Total 80Byte for 16Devices, DDC Address: 0x74, Offset 0x43

6.15 VIDEO Output Format Registers

6.15.1 VIDEO OUTPUT FORMAT REGISTER (VOUT_FMT) (0x8A00)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			422_SEL	Reserved		VOUT_SEL	
Type	RO			RW	RO		RW	
Default	0			0	0		2	

Register Field	Bit	Description
Reserved	[7:5]	
422_SEL	4	4:2:2 format setting 1'b0 : Normal Format Y[11:0] data are outputted from Y_o[15:4] ports.

		CB/CR[11:0] data are outputted from CB_o[15:4] ports. 1'b1 : HDMI through format Y[11:4] data are outputted from Y_o[15:8] ports. Y[3:0] data are outputted from CB_o[11:8] ports. CB/CR[11:4] data are outputted from CR_o[15:8] ports. CB/CR[3:0] data are outputted from CB_o[15:12] ports.
Reserved	[3:2]	
VOUT_SEL	[1:0]	VIDEO Output Format setting 2'b00 : 444/RGB video output mode 2'b01 : 422 video output mode 2'b1x : Through mode (Output Format = Input Format)

6.15.2 VIDEO 422/444 Conversion REGISTER (VOUT_444) (0x8A01)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			444FIL_SEL	Reserved	422FIL_SEL		
Type	RO			RW	RO	R/W		
Default	0			1	0	2		

Register Field	Bit	Description
Reserved	[7:5]	
444FIL_SEL	4	422to444 conversion characteristic setting. 1'b0 : Color pixel is repeated twice at the time of 422 input. 1'b1 : 2tap linear interpolation is used at the time of 422 input. Note) 422to444 conversion is bypassed at the time of 444 inputs.
Reserved	3	
422FIL_SEL	[2:0]	444to422 conversion characteristic setting. 3'b000 : 2tap filter is always used. 3'b001 : 3tap filter is always used. 3'b010 : filter is not used . 3'b011 : 2tap filter is used at the time of 444 input, and filter is not used at the time of 422 input. 3'b100 : 3tap filter is used at the time of 444 input, and filter is not used at the time of 422 input. 3'b101 : 2tap filter is used at the time of 444 input or CSC_on, and filter is not used at the time of 422 input and CSC_off. 3'b11x : 3tap filter is used at the time of 444 input or CSC_on, and filter is not used at the time of 422 input and CSC_off

6.15.3 VIDEO OUTPUT SYNC MODE REGISTER 0 (VOUT_SYNC0) (0x8A02)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M3_VSIZE		M3_HSIZE		Reserved		VOUT_MODE	
Type	RW		RW		RO		RW	
Default	1		0		0		2	

Register Field	Bit	Description
M3_VSIZE	7:6	The active period setup of VD_o in Mode3. Note) Invalid at the time of Mode2
M3_HSIZE	5:4	The active period setup of HD_o in Mode3. Note) Invalid at the time of Mode2
Reserved	3:2	
VOUT_MODE	1:0	Video Sync output mode setting. 2'b00 : Not use (for TEST) 2'b01 : Not use (for TEST) 2'b10 : Mode2 = VD_o and DE_o output timing is almost the same as the timing of inputted HD, VD and DE. 2'b11 : Mode3 = VD_o and DE_o are re-generated on the basis of active edge of inputted DE.

6.15.4 VIDEO OUTPUT SYNC MODE REGISTER 1 (VOUT_SYNC1) (0x8A03)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			VOut_Dly				
Type	RO			RW				
Default	0			0x0C				

Register Field	Bit	Description
Reserved	7:5	
VOut_Dly	4:0	DE_o, DV_o, Y_o, CB_o, CR_o and CBCR_o Output Delay setting in Mode3 5'b00000 : With no delay 5'b00001 : Delay time is 1 cycle of EN_o 5'b00010 : Delay time is 2 cycle of EN_o ~~~~~ 5'b01111 : Delay time is 15 cycle of EN_o 5'b1xxxx : Delay time is 16 cycle of EN_o Note) The maximum delay is 16 cycle of EN_o

		Note) When EN_o is constant H, they are delayed by the cycle of PXCLK. Note) Invalid at the time of Mode2
--	--	--

6.15.5 VIDEO COLOR SPACE CONVERSION REGISTER (VOUT_csc) (0x8A08)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	VOUT_COLOR_SEL			Reserved		CSC_Mode	
Type	RO	RW			RO		RW	
Default	0	3			0		0	

Register Field	Bit	Description
Reserved	7	
VOUT_COLOR_SEL	6:4	Video output color setting 000: RGB Full 001: RGB Limited 010: 601YCbCr Full 011: 601 YCbCr Limited 100: 709 YCbCr Full 101: 709 YCbCr Limited 110: Range conversion (Full→Limited) 111: Range conversion (Limited→Full) Note) This setup becomes effective only when CSC_MODE is set as 2 'b01 or 2' b10.
Reserved	3:2	
CSC_Mode	1:0	CSC setting 2'b00 : CSC is turned OFF 2'b01 : CSC is turned ON (Built-in coefficient used) 2'b10 : CSC ON/OFF auto select (for Toshiba DTV-SoC) When xvYCC or sYCC, or Adobe YCC601 input, CSC is turned off. When an input is except the above, CSC is turned ON (Built-in coefficient used) 2'b 11: CSC is turned ON (Host setting coefficient used)

6.15.6 SCLK FREQUENCY for CSC controller REGISTER 0 (SCLK_CSC0) (0x8A0C)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SYS_FREQ[7:0]							
Type	RW							
Default	1	0	0	0	1	0	0	0

6.15.7 SCLK FREQUENCY for CSC controller REGISTER 1 (SCLK_CSC1) (0x8A0D)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SYS_FREQ[15:8]							
Type	RW							
Default	1	0	0	0	1	0	0	0

Register Field	Bit	Description
SYS_FREQ	[15:0]	<p>System clock frequency setting Set System clock frequency setting ÷10000 integer Initial Value : system clock at 50MHz, 5000 =16'h1388 Ex.) When system clock at 42MHz, 4200 =16'h1068</p> <p>Note) Set up the same value as Address 0x8540 and 0x8541</p>

6.15.8 VIDEO CSC Packet Limit REGISTER (CSC_LIMIT) (0x8AB0)

Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	NO_VS_LIMIT2					NO_AVI_LIMIT2			
Type	RW					RW			
Default	0	0	1	1	1	1	0	0	

Register Field	Bit	Description
NO_VS_LIMIT2	7:4	<p>When no VS packet is received during setting value*80msec period, it is judged that VS packet transmission stopped. Note) At 4'b0000 setting, Judgment operation is OFF.</p> <p>Note) Set up the same value as Address 0x870E [7:4].</p>
NO_AVI_LIMIT2	3:0	<p>When no AVI packet is received during setting value*80msec period, it is judged that AVI packet transmission stopped. Note) At 4'b0000 setting, Judgment operation is OFF.</p> <p>Note) Set up the same value as Address 0x870B [3:0].</p>

7 Package

The 80-pin package for TC358840/70 is described in the figures below.

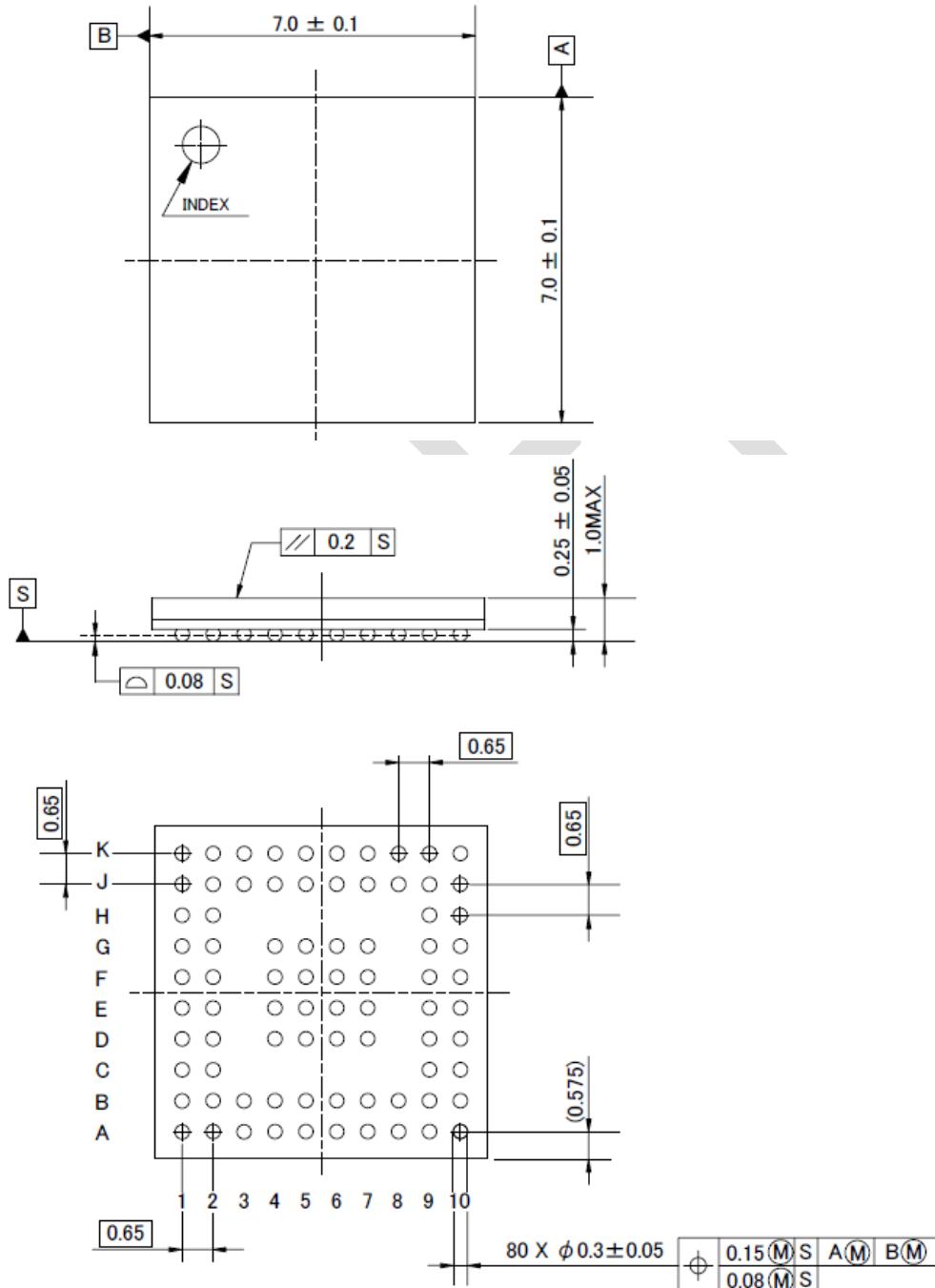


Figure 7-1 TC358840/70 package (80 pins)

The mechanical dimension of BGA80 package is listed below.

Table 7-1 Mechanical Dimension

Package	Solder Ball Pitch	Solder Ball Height	Package Dimension	Package Height
80-Pin	0.65 mm	0.25 mm	7.0 x 7.0 mm ²	1.0 mm

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

VSS= 0V reference

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V - Digital IO)	VDDIO18	-0.3 ~ +3.9	V
Supply voltage (3.3V - Digital IO)	VDDIO33	-0.3 ~ +3.9	V
Supply voltage (1.1V – Digital Core)	VDDC11	-0.3 ~ +1.8	V
Supply voltage (1.2V – MIPI CSI PHY)	VDD12_MIPI	-0.3 ~ +1.8	V
Supply voltage (3.3V – HDMIRX Phy)	VDD33_HDMI	-0.3 ~ +3.9	V
Supply voltage (1.1V – HDMIRX Phy)	VDD11_HDMI	-0.3 ~ +1.8	V
Input voltage (CSI IO)	V _{IN_CSI}	-0.3 ~ VDD12_MIPI+0.3	V
Output voltage (CSI IO)	V _{OUT_CSI}	-0.3 ~ VDD12_MIPI+0.3	V
Input voltage (Digital IO)	V _{IN_IO}	-0.3 ~ VDDIO18+0.3 -0.3 ~ VDDIO33+0.3	V
Output voltage (Digital IO)	V _{OUT_IO}	-0.3 ~ VDDIO18+0.3	V
Junction temperature	T _j (TBD)	125	°C
Storage temperature	T _{stg}	-40 ~ +125	°C

8.2 Recommended Operating Condition

VSS= 0V reference

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (1.8 – Digital IO)	VDDIO18	1.65	1.8	1.95	V
Supply voltage (3.3V – Digital IO)	VDDIO33	3.0	3.3	3.6	V
Supply voltage (1.1V – Digital Core)	VDDC11	1.0	1.1	1.2	V
Supply voltage (3.3V – HDMIRX PHY)	VDD33_HDMI	3.135	3.3	3.465	V
Supply voltage (1.1V – HDMIRX PHY)	VDD11_HDMI	1.0	1.1	1.2	V
Supply voltage (1.2V – MIPI CSI PHY)	VDD12_MIPIO VDD12_MIPI1	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	T _a (TBD)	-30	+25	+70	°C
Supply Noise Voltage	V _{SN}			100	mV _{pp}

8.3 DC Electrical Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage, High level input Note1	V_{IH}	0.7 VDDIO18 0.7 VDDIO33		VDDIO18 VDDIO33	V
Input voltage, Low level input Note1	V_{IL}	0		0.3 VDDIO18 0.3 VDDIO33	V
Input voltage High level CMOS Schmitt Trigger Note1,2	V_{IHS}	0.7 VDDIO18 0.7 VDDIO33		VDDIO18 VDDIO33	V
Input voltage Low level CMOS Schmitt Trigger Note1,2	V_{ILS}	0		0.3 VDDIO18 0.3 VDDIO33	V
Output voltage High level Note1, Note2	V_{OH}	0.8 VDDIO18 0.8 VDDIO33		VDDIO18 VDDIO33	V
Output voltage Low level Note1, Note2	V_{OL}	0		0.2 VDDIO18 0.2 VDDIO33	V
Input leak current, High level (Condition: $V_{IN} = +VDDIO$, $VDDIO = 3.6V$)	I_{ILH1} (Note4)	-10	-	10	uA
Input leak current, Low level (Condition: $V_{IN} = 0V$, $VDDIO = 3.6V$)	I_{ILL1} (Note5)	-10	-	10	uA

Note1 : Each power source is operating within recommended operation condition.

Note2 : Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note4 : Normal pin or Pull-up IO pin applied VDDIO18, VDDIO33 supply voltage to Vin (input voltage)

Note5 : Normal pin applied VSS (0V) to Vin (input voltage)

9 Timing Definitions

9.1 RefClk Input Requirement

Parameter	Min.	Typ.	Max.	Unit
Frequency		40 - 50		MHz
Duty Cycle	40	50	60	%
Jitter	-100	0	100	ppm

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9.2 MIPI CSI – 2 / DSI Timings

Timing specification below has been ported from Draft MIPI Alliance specification for D-PHY version 0.91.00 r0.01. Timing defined in Draft MIPI Alliance specification for D-PHY version 0.91.00 r0.01 has precedence over timing described in the sections below.

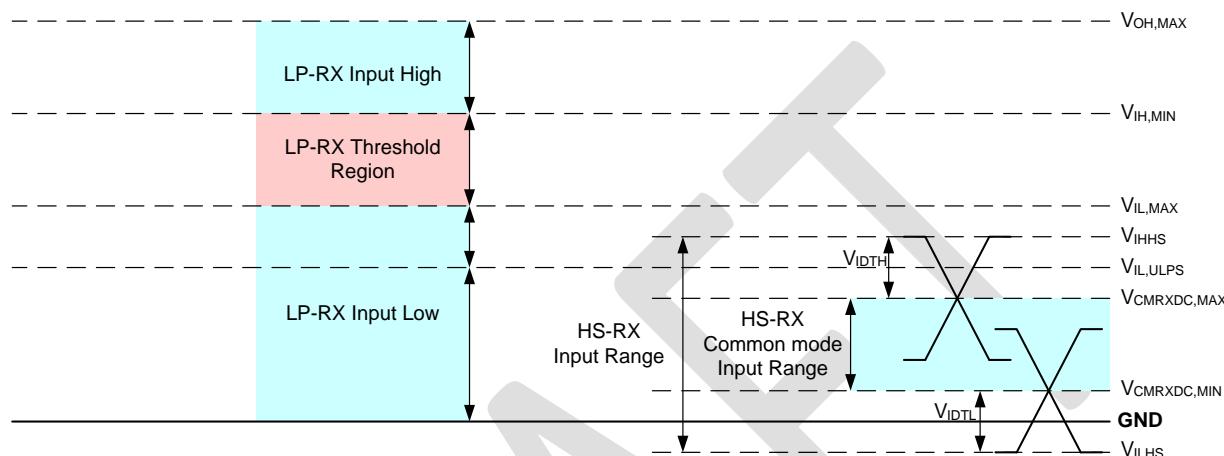


Figure 9-1 Signaling and voltage levels

Table 9-1 DC specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{PIN}	Pin signal voltage range	-50		1350	mV	
$V_{PIN(absmax)}$	Transient pin voltage	-0.15		1.45	V	
$T_{VPIN(absmax)}$	Maximum transient time above $V_{PIN(absmax)}$ or below $V_{PIN(absmax)}$.			20	ns	3
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	
V_{IH}	Logic 1 input voltage	880			mV	
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV	
$V_{CMRX(DC)}$	Common-mode voltage HS receiver mode	70		330	mV	1,2
V_{IDTH}	Differential input high threshold			70	mV	
V_{IDTL}	Differential input low threshold	-70			mV	
V_{IHS}	Single-ended input high voltage			460	mV	1

V_{ILHS}	Single-ended input low voltage	-40			mV	1
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Notes:

1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
2. This table value included a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz.
3. The voltage undershoot or overshoot beyond V_{PIN} is only allowed during a single 20 ns window after any LP-0 LP-1 transition or vice versa. For all other situations it must stay within the V_{PIN} range.

Table 9-2 High Speed AC specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz			100	mV	2
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz- 450MHz	-50		50	mV	1,3

Notes:

1. Excluding 'static' ground shift of 50mV
2. $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.
3. Voltage difference compared to the DC average common-mode potential.

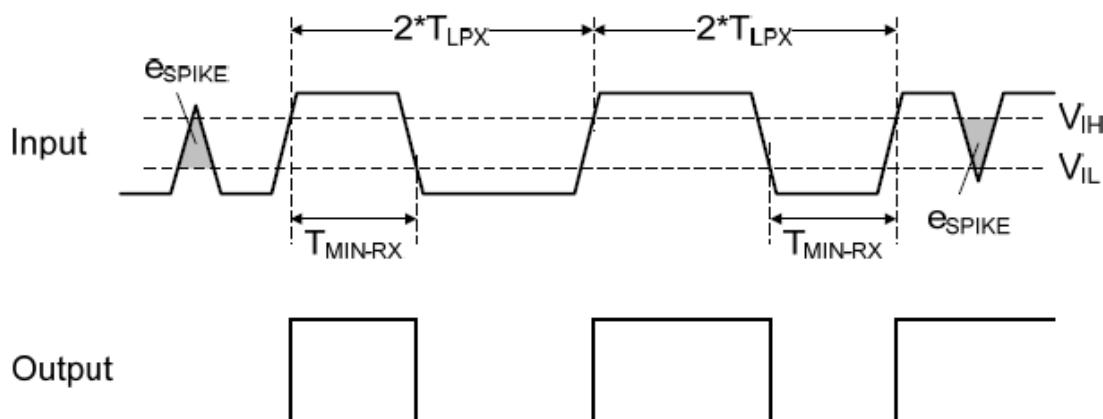


Figure 9-2 Input Glitch Rejection

Table 9-3 Low Power AC characteristics

Parameter	Description	Min	Nom	Max	Units	Notes
e_{SPIKE}	Input pulse rejection			300	V.ps	1,2,3
T_{MIN-RX}	Minimum pulse width response	20			ns	4

V_{INT}	Peak interference amplitude			200	mV	
F_{INT}	Interference frequency	450			MHz	
T_{LPX}	Length of any Low Power state period	50			ns	

Notes:

1. Time-voltage integration of a spike above V_{IL} when being in LP-0 or below V_{IH} when being in LP-1 state.
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
4. An input pulse greater than this shall toggle the output.

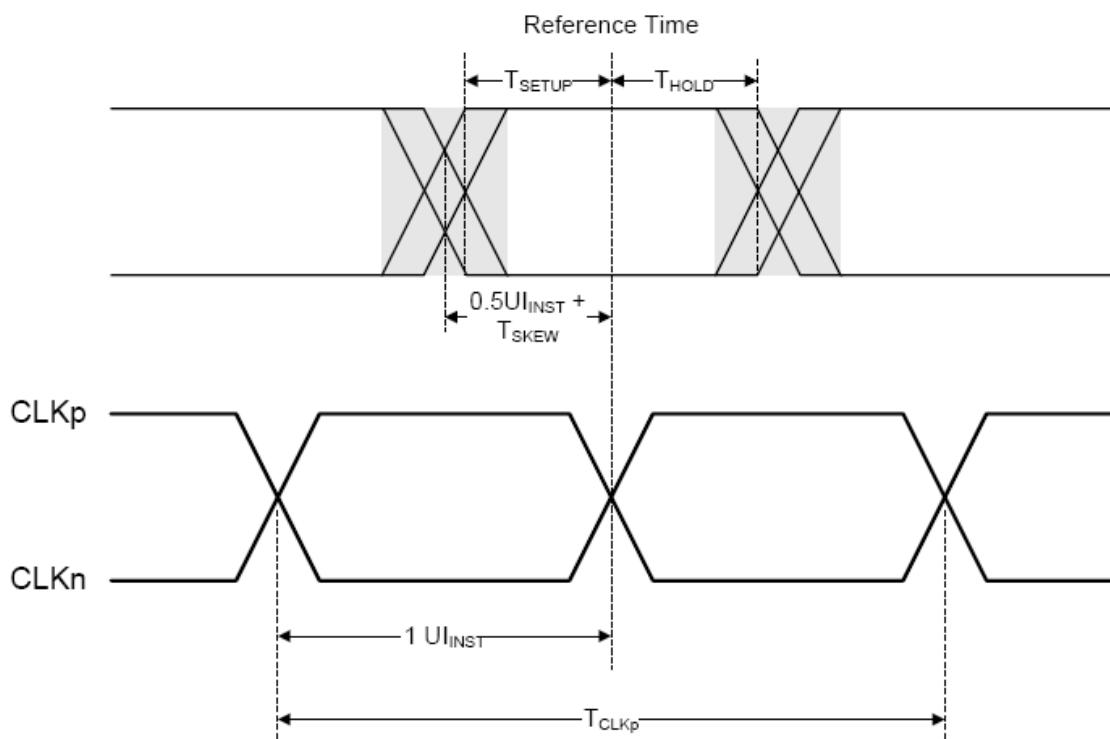


Figure 9-3 Data to clock timing reference

Table 9-4 Data-Clock timing specification

Parameter	Description	Min	Nom	Max	Units	Notes
T_{SKEW}	Data to clock skew measured at the transmitter	-0.15		0.15	UI_{INST}	
T_{SETUP}	Data to clock setup time at	0.15			UI_{INST}	

	receiver					
T _{HOLD}	clock to data hold time at receiver	0.15			UI _{INST}	
UI _{INST}	1 Data bit time (instantaneous)			12.5	ns	
T _{CLKp}	Period of dual data rate clock	2	2	2	UI _{INST}	

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9.3 I2C Timings

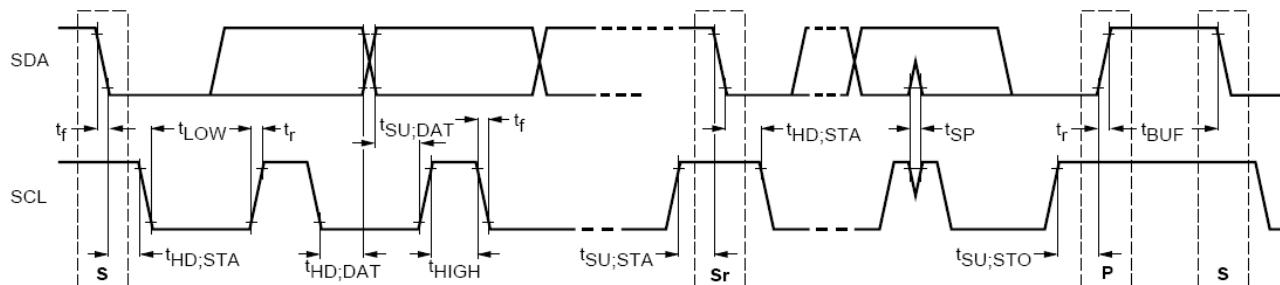


Figure 9-4 I2C Timing Diagram

Table 9-5 I2C timing specification

Item	Symbol	Min	Max	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	-	μs
LOW period of the SCL clock	t_{LOW}	1.3	-	μs
HIGH period of the SCL clock	t_{HIGH}	0.6	-	μs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	μs
Data hold time: for I2C-bus devices	$t_{HD;DAT}$	0	0.9	μs
Data set-up time	$t_{SU;DAT}$	100	-	ns
Rise time of both SDA and SCL signals	t_r	$20+0.1Cb$	300	ns
Fall time of both SDA and SCL signals	t_f	$20+0.1Cb$	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	μs
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	μs

Note: Cb = Capacitive load for each bus line (400pF max.)

9.4 HDMI-RX Input

(Ta=25°C, VDD11_HDMI =1.10V,
VDD33_HDMI)

Parameter	Symbol	min	typ	max	unit	Comment
DAC Output Impedance	Zy	160	200	240	Ω	
HDMI Clock Frequency	FIN	25	---	297	MHz	300 mVpp
HDMI minimum Amplitude	VMIN	159	---	---	mVp-p	225MHz at TP2 Compliance test (TestID 8-5)

9.5 I2S/TDM Timings

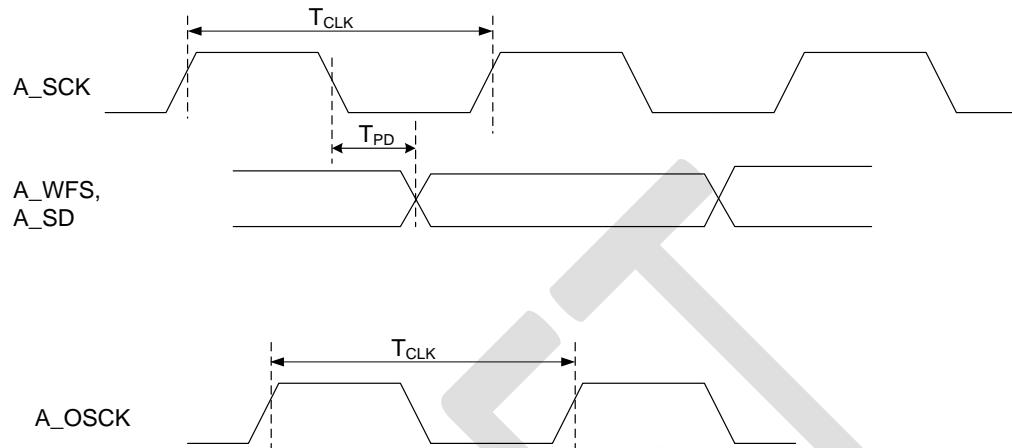


Figure 9-5 I2S/TDM Timing Diagram

Table 9-6 I2S/TDM timing specification

Item	Symbol	Min	TYP	Max	Unit
Propagation Output Delay	T_{PD}	0	--	6	ns
Clock Period	T_{CLK}	20	--	--	ns

Notes: Above timing are for 15pf load on all I2S/TDM signals

9.6 SLIMbus IO

9.6.1 Clock Output Timing

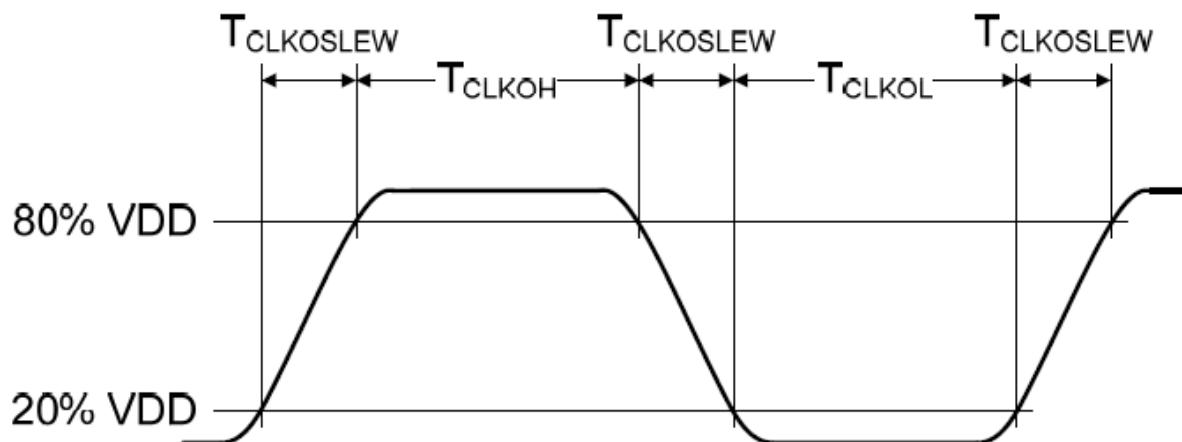


Figure 9-6 Clock Driver Output Waveform Constraints

Table 9-7 Clock Output Timing Characteristics

Item	Symbol	Condition	Min	TYP	Max	Unit
Clock Output High Time	T_{CLKOH}		12	--	--	ns
Clock Output Low Time	T_{CLKOL}		12	--	--	ns
Clock Output Slew Rate	SR_{CLK}	$20\% < VO < 80\%$	$0.02*VDD$	--	$0.2*VDD$	V/ns

9.6.2 Clock Input Timing

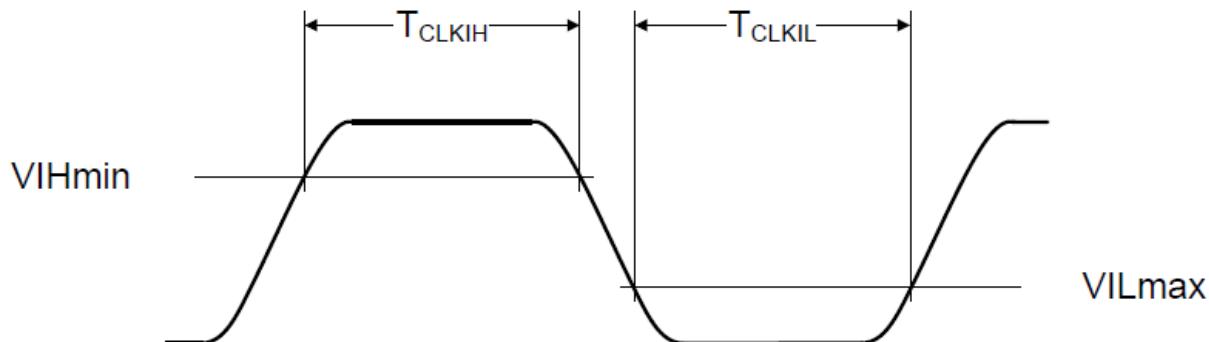


Figure 9-7 Received Clock Signal Constraints

Table 9-8 Clock Input Timing Characteristics

Item	Symbol	Condition	Min	TYP	Max	Unit
Clock Input High Time	T _{CLKIH}		12	--	--	ns
Clock Input Low Time	T _{CLKIL}		12	--	--	ns
Clock Input Slew Rate	SR _{CLKI}	20%<VI<80%	0.02*VDD	--	--	V/ns

Table 9-9 Clock Input Electrical Characteristics

Item	Symbol	Condition	Min	TYP	Max	Unit
Clock Input Hysteresis	H _{CLKI}		50	--	--	mV

9.6.3 Data Timing

Table 9-10 Data Output Timing Characteristics

Item	Symbol	Condition	Min	TYP	Max	Unit
Data Output Slew Rate	SR _{DATA}	20%<V _O <80%	--	--	0.5*VDD	V/ns
Time for Data Output Valid	T _{DV}		--	--	12	ns

Table 9-11 Data input Timing Requirements

Item	Symbol	Condition	Min	TYP	Max	Unit
Data Input Hold Time	T _H		2	--	--	mV
Data Input Setup Time	T _{SETUP}		3.5	--	--	mV

Table 9-12 Driver Disable Timing Specification

Item	Symbol	Condition	Min	TYP	Max	Unit
Driver Disable Time	T _{DD}		--	--	10	ns

Table 9-13 Bus Holder Electrical Specification

Item	Symbol	Condition	Min	TYP	Max	Unit
Bus Holder Output Impedance	R _{DATAS}	0.1*VDD<V<0.9*VDD	10K	--	50K	Ohm

9.7 SlimBus Timing

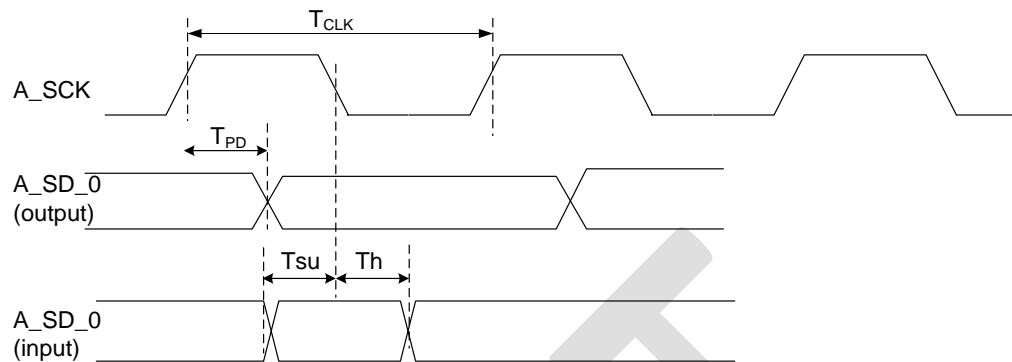


Figure 9-8 SlimBus Timing Diagram

Table 9-14 SlimBus timing specification

Item	Symbol	Min	TYP	Max	Unit
Data Output Propagation Delay	T_{PD}	0	--	7	ns
Data Input Setup Time	T_{SU}	3.5	--	--	ns
Data Input Hold Time	T_h	2	--	--	ns
Clock Period	T_{CLK}	33	--	--	ns

Notes: Above timing are for 75pf load on all signals

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