

## plan9-hardware

Synthesizing and building the plan9-hardware component requires the Convey PDK to be installed. The design is implemented in Chisel, with some VHDL blackboxes down the module hierarchy. All configuration and parameterization happens in `CarpParameters.scala`. The `ChiselParameters` trait is an interface specifying the parameters required for the design to synthesize. It also provides semi-sane defaults. Instead of changing the values in the trait directly, it is recommended to create a new object implementing the trait and change only the necessary values on a per-need basis, as shown below.

```
package plan9
```

```
object SpecificExperimentParams extends CarpParameters {  
  SNNTopology = Array(4,2,1)  
}
```

To have the new parameters be used during synthesis, `SpecificExperimentParams` has to be passed as a parameter when instantiating the `Carp`-module in `Plan9.scala`.

```
val carpParams = SpecificExperimentParams  
...  
val carp = Module(new Carp(carpParams))
```

### Make targets

**make gen\_verilog**

`make gen_verilog` invokes the Scala Build Tool and generates Verilog based on the Chisel code.

**make all**

Invokes the `gen_verilog` target before starting the Xilinx flow, incorporating the plan9-design into the Convey Application Engine wrapper and generating a bitfile. This takes a while.

**make release**

Moves the bitfile resulting from the previous run of `make all` to the `hardware.released` directory. Useful for archiving separate versions of the design.

**make install**

Deploys the most recently synthesized bitfile to the Convey personalities folder. This target requires the following variables to be set in `phys/Makefile`:

- **PERSONALITY**: Personality ID.
- **RELEASE\_DIR**: Path to the folder into which **make release** moves bitfiles.
- **CNY\_DIR**: Path to the root Convey directory, usually `/opt/convey`.

## Setup on NTNU servers

`moog.idi.ntnu.no` has been used for synthesis. The Convey cards are installed on `lobo.idi.ntnu.no`. This means that the bitfile resulting from **make all** will have to be manually moved between the two, instead of using the **make install** target. This can be done with the following commands:

```
$ scp moog.idi.ntnu.no:/home/<your_user>/<path_to_plan9>/\
    hardware.released/<release_tag>/ae_fpga.tgz ./
$ scp ae_fpga.tgz lobo.idi.ntnu.no:/opt/convey/\
    personalities/65002.0.0.4.0/
```