ORTA DOĞU TEKNİK ÜNİVERSİTESİ
MIDDLE EAST TECHNICAL UNIVERSITY

EE464 STATIC POWER CONVERSION II

Final Report

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Introduction

The isolated DC-DC converter design for the specifications indicated below requires several design and testing steps. Firstly, the topology had to be selected depending on the ratings and group member preferences. After that, the main power stage of the converter had to be designed followed by the controller selection and implementation into the circuit. The components were selected with the considerations explained below. The physical implementation came with several problems. The tests were made, and the demonstration has been conducted. This report explains all these steps and what we learned from this project.

Topology Selection Considerations

The topology selection was explained in detail in "Simulation and Magnetic Design Report". This report includes the summary of why we chose Flyback topology for the project.

- The general expectancy of the efficiency of the flyback converter is applicable to this project [1].
- Most of the other groups were choosing the flyback topology, meaning that a supportive network could be created.
- Flyback topology was also the most selected topology by the previous year's groups. They could also be good references (mostly for the magnetic design) for the project.
- The components were mostly available on the laboratory or quite cheap. Note that comparison with other topologies was not made.
- The component number is relatively small which will be mentioned again in the controller design section.

  Regarding the reasons mentioned above, the flyback topology was selected for this project.

Magnetic Design Considerations and Tests

Next, the transformer had to be designed. The necessary values for the flyback converter were selected/calculated as follows (the MATLAB file which includes all the calculations is included in the GitHub repo):

- N2/N1 = 3
- Minimum magnetizing inductance (primary referred) = 59.68 uH
- The maximum current = 8.318 A (without losses)
- N1 = 16 (five parallel of AWG21), N2 = 48 (two parallel of AWG21)
- B = 0.1205 T

The core selection was made considering the laboratory inventory. The cores available at the lab were investigated by reading each of their datasheets. The sizes, saturation limits, inductance per turn squared values, and window sizes were compared. The selected core was 00K4022E090 with its coil former.

The physical implementation of the transformer brought several challenges. First of all, the coils had to be stranded. The drill was used to strand to coils. Next, although the fill factor (around 0.3) stated otherwise, winding the coils were not possible with the selected values above. We needed to decrease the turn numbers to N1 = 10 and N2 = 30 to be able to wind the paralleled coils. After the turn number changes, the transformer was winded very strictly and the coils had nearly no empty space between them. The inductances were measured with the LCR meter available in the lab. The measurements are included in the following figures.

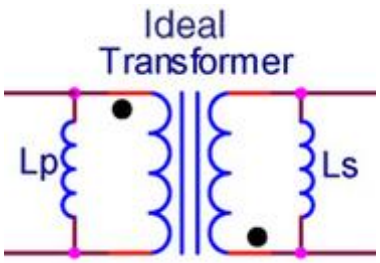


Fig. 1. Ideal transformer representation.

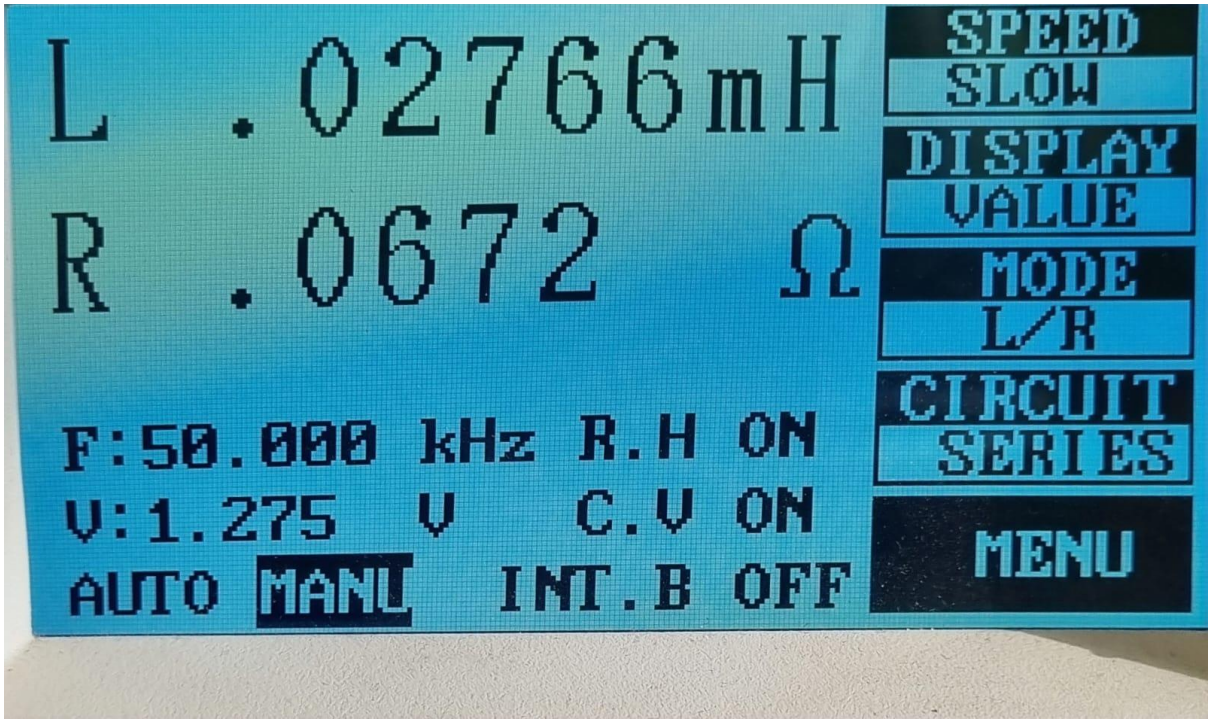


Fig. 2. Secondary side open circuited, primary side measurement.

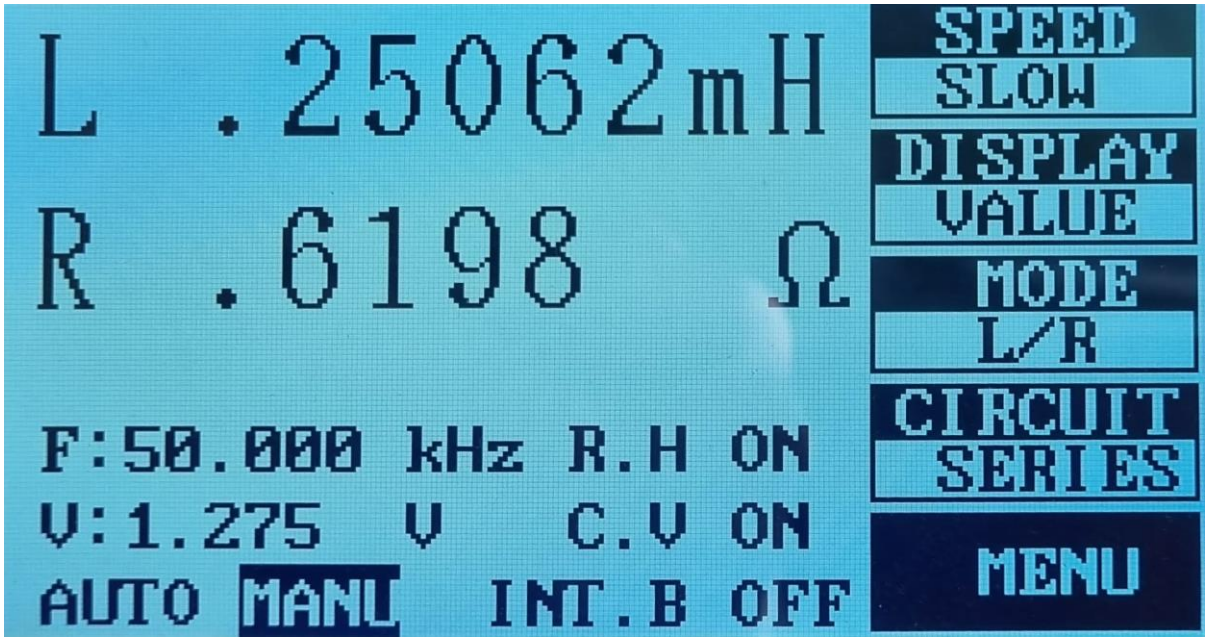


Fig. 3. Primary side open circuited, secondary side measurement.

From Fig. 2 and Fig. 3, the turn ratio is calculated as N2/N1 = Sqrt(0.25062 / 0.02766) = 3.01, which is what we wanted.

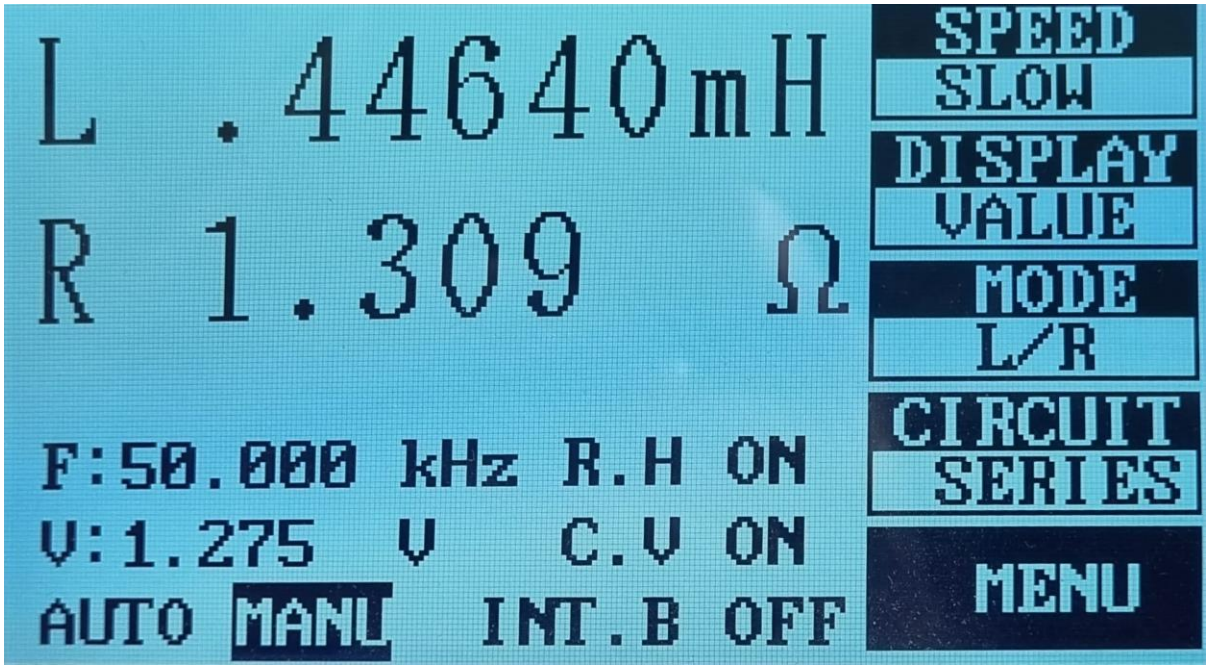


Fig. 4. Two dotted or two undotted terminals are shorted, measurement taken from the other available terminals (Lp + Ls + 2M).

Fig. 5. One dotted and one undotted different side terminals are shorted, measurement taken from the other available terminals (Lp + Ls - 2M).

The magnetizing inductance is calculated from Fig. 4 and Fig. 5 using the logic in Fig. 1 as:

Lm = (0.44640-0.11533)/4 = 82.77 uH, which is larger than what is calculated for the design. However, the result does not harm any other quantity such as B_max of the core or I_max. It only changes the CCM-DCM boundary which will be compensated by the controller. Also, the core losses are expected to be decreased as the current ripple is further reduced meaning that the used region in the B-H curve is reduced.

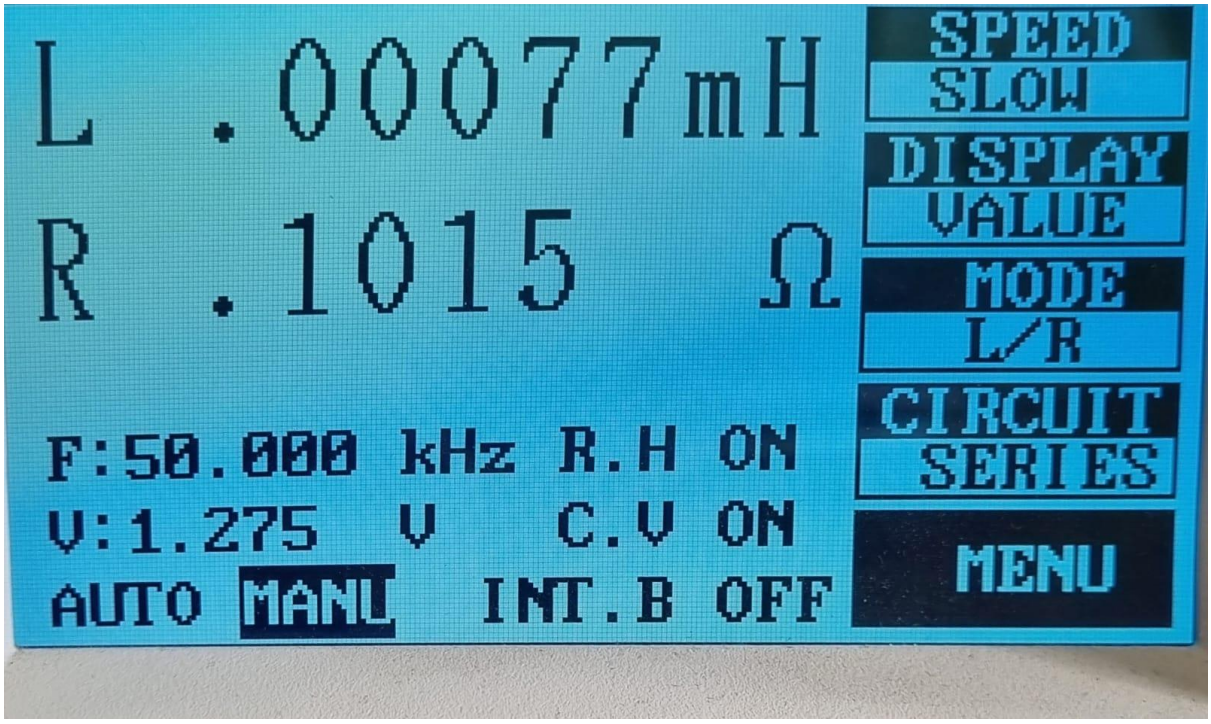


Fig. 6. Secondary side short circuited, primary side measurement (leakage inductance referred to primary).

Since the winding part of the implementation was quite difficult by itself, we didn't wind the primary and secondary side windings in a changing manner order to decrease the proximity effect as the leakage came out to be 77/2766 = 2.7%, which less than 5%.

Next, to see if the transformer worked as desired (1:3 ratio) and determine the polarity of the terminals, a signal generator is connected to the primary side of the transformer and oscilloscope measurements are taken from both sides. The expected behavior was to get 90 degrees phase shifted waveforms and voltage ratios to be around 3 which is shown in Fig. 7.

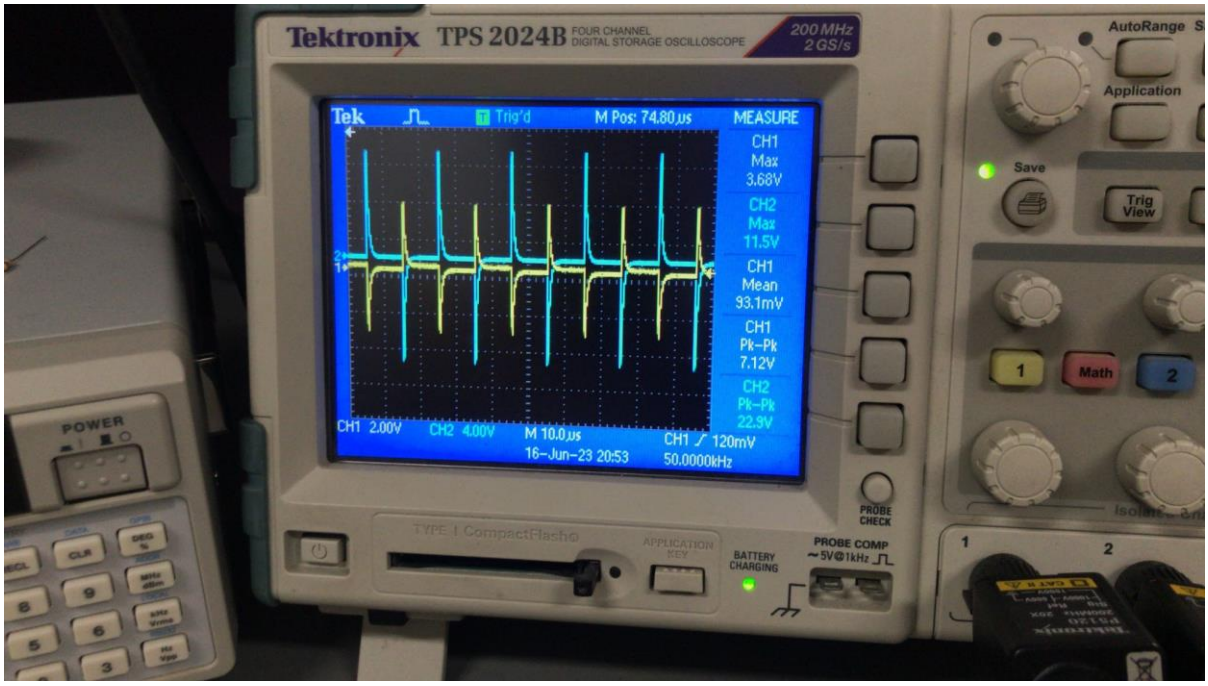


Fig. 7. Transformer test. CH1 is primary and CH2 is secondary.

Here, the ratio came up to be around N2/N1=3.13 unlike LCR meter findings. We though that one of the measurement devices was used wrongly. In any case, this result is unimportant as the controller will compensate for the discrepancies related with the transformer.

Controller and Isolation Optocoupler Design

For the controller selection, UC3843 is selected as a controller. It is one of the most used controllers for DC-DC Converters. There are several advantages of UC3843 for our design as follow:

- It has a flexible frequency range up to 500 kHz
- It has a current-mode control property that it has a simplified phase compensation circuit design.
- It has a pulse by pulse current limit property.
- It was available in Özdisan such that we can buy and obtain in a short time.
- It meets the line regulation and load regulation requirements.

Texas Insturments has a property of providing an example circuit structure when the design requirements are given. According to our design requirements, TI gave us the following example circuit schematic;

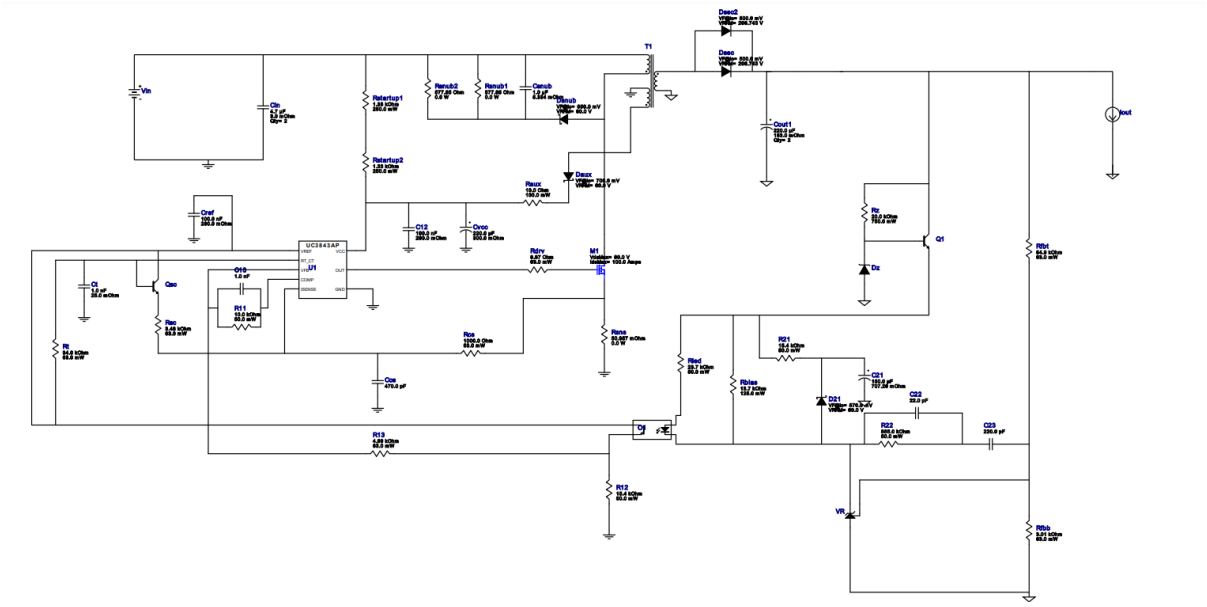


Fig. 8. Flyback design for given requirements.

According to TI design, LT Spice model of the circuit design is constructed. While adjusting the LTSPice model, some components are subtracted whether they are not necessary or their functioning is not understood. Moreover, LT1243 is used as a equivalent of UC3843 since LT Spice does not include UC3843. The resulting LTSpice Model is as follows;

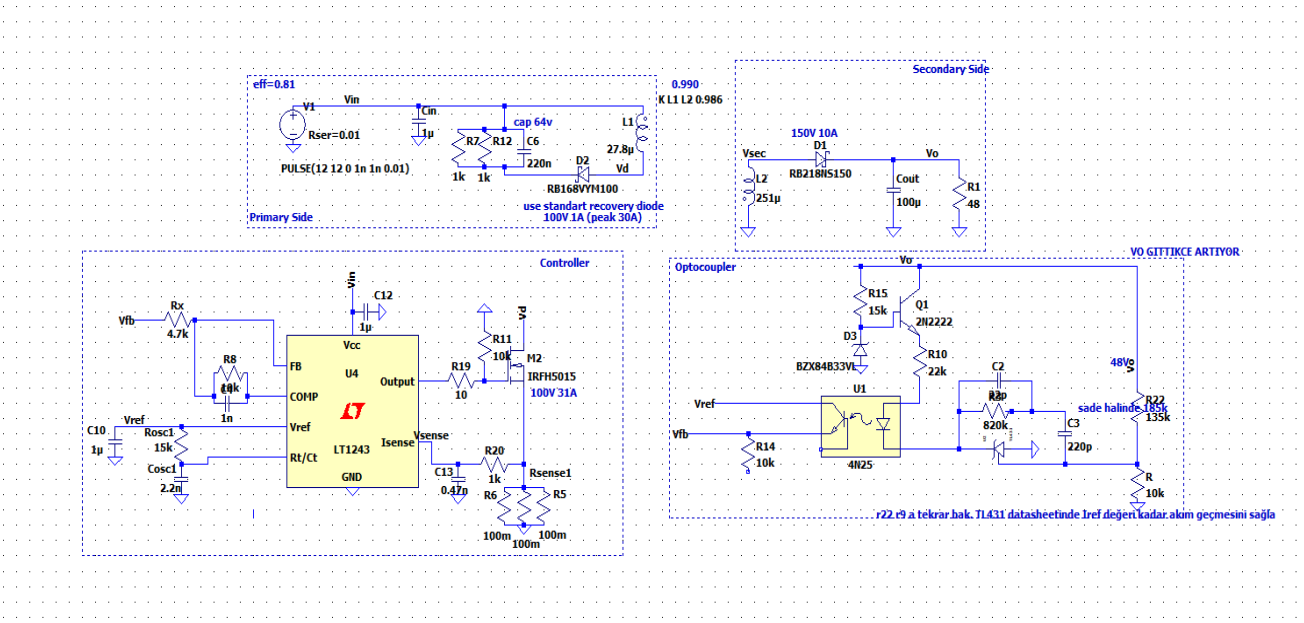


Fig. 9. LTspice model fo flyback converter.

Let’s introduce the configuration;

Power Part:

The primary side and secondary side constructs the power part of the design. Primary side includes RCD snubber circuit to reduce inductance leakage ringing and prevent di/problems. If the snubber is not used, the mosfet would have to handle with large magnitude oscillations. The input and output capacitance are also chosen to keep constant voltage both on the input and output side.

Controller Part:

For the controller part, let’s define each pin for better understanding.

COMP: Error amplifier compensation pin. The parallel configuration of resistance and capacitance are connected to this pin to modify the error amplifier output.

FB: Inverting input to the internal error amplifier. It is used to control the voltage-feedback loop for stability. Rx and R14 resistances are connected in series to this pin from the optocoupler output.

Isense: It is primary-side current sense pin. R6, Rsense1 and R5 resistances are connected in parallel to sense the mosfet current. The mosfet is opened or closed according to desired current limit. Low pass filter with R20 and C13 is also used to reduce noise and harmonics.

Rt/Ct: This pin decides the frequency of the oscillator according to following formula;

$$fosc = \frac{1.72}{Rrt * Cct}$$

Rosc1 and Cosc1 resistances are chosen to adjust 50 kHz frequency.

GND: It is connected to ground of primary side.

Output: It drives the gate of the mosfet. It is the output of the on-chip driver stage. It is low when Vcc is below the threshold value.

Vcc: It is input to the controller for supplying power to the it. The parallel capacitance is added to this pin keep required voltage on the pin.

Vref: It is the reference voltage for error amplifer. It is supplied by the optocoupler and the parallel capacitor C10 is connected to keep reference stability and to prevent noise problems with high-speed switching transients.

Optocoupler Part:

LTV-814S: The optocoupler is providing isolated feedback from secondary side to primary side. As an optocoupler, LTV-814S is used. When the current flows through the LED diode on the optocoupler, it activates the transistor on the other side optically. The isolation is done in this way. The resistance R10 protects LED diode from the short circuit.

TL431: It is a shunt regulator such that provides programmable reference for output voltage. It maintains the continuous output voltage with R22 and R resistances by suppliyin constant 2.5 V at it’s reference pin. The parallel resistance and capacitor provides a path for parasitic currents around TL431. The maximum cathode to anode voltage of TL431 is 37V. However, if the upper part of the optocoupler part (D3 diode, 2N2222 BJT,R15 resistor) is not used, then cathode to anode voltage of

TL431 becomes 40V. D3 zener diode clamps this voltage to 24V through the 2N2222 BJT. In this way, TL431 is protected.

Computer Simulations

18V Input Voltage Cases:

No Load:

Since this is a no load case, the general plots(including both transient and steady state responses) are represented instead of steady state responses.

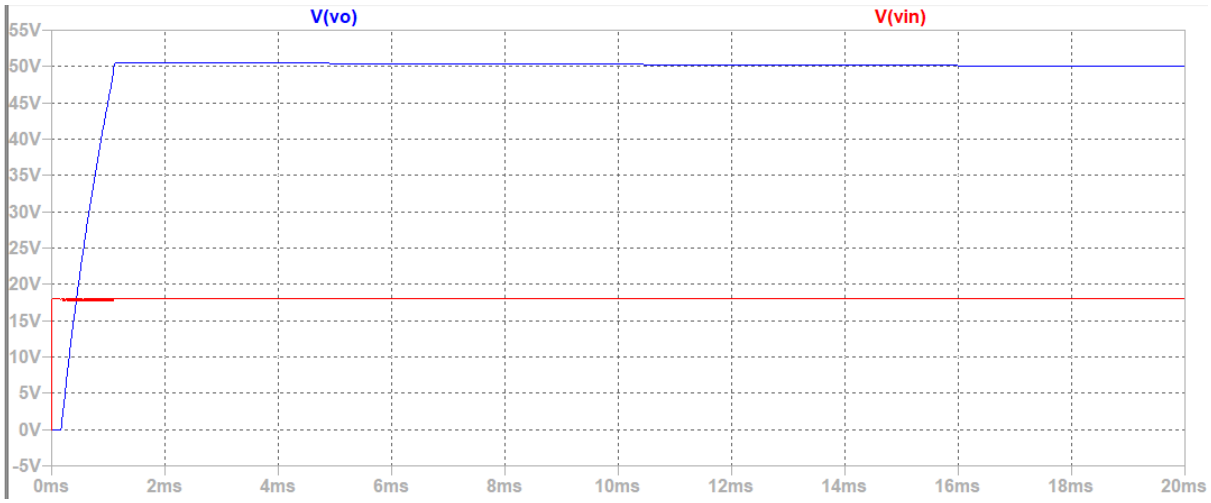


Fig. 10. The input and output voltage for 8V input, no-load case.

Vout(avg) = 50.346 V

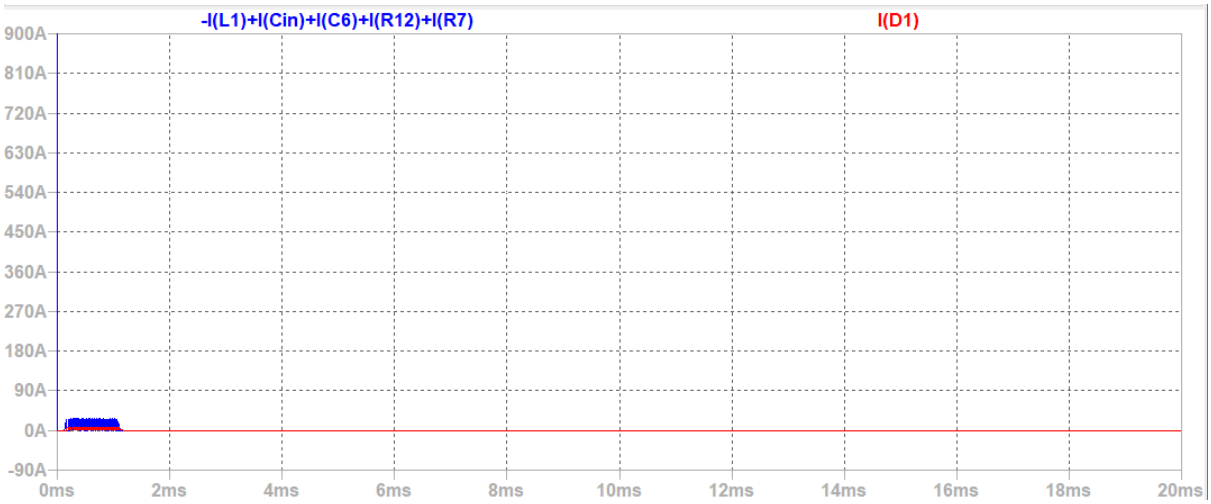


Fig. 11. The Input and Output Current For 18V Input - No Load Case.

Iin(avg) = 456 Ma

Iout(avg) = 252.75 mA

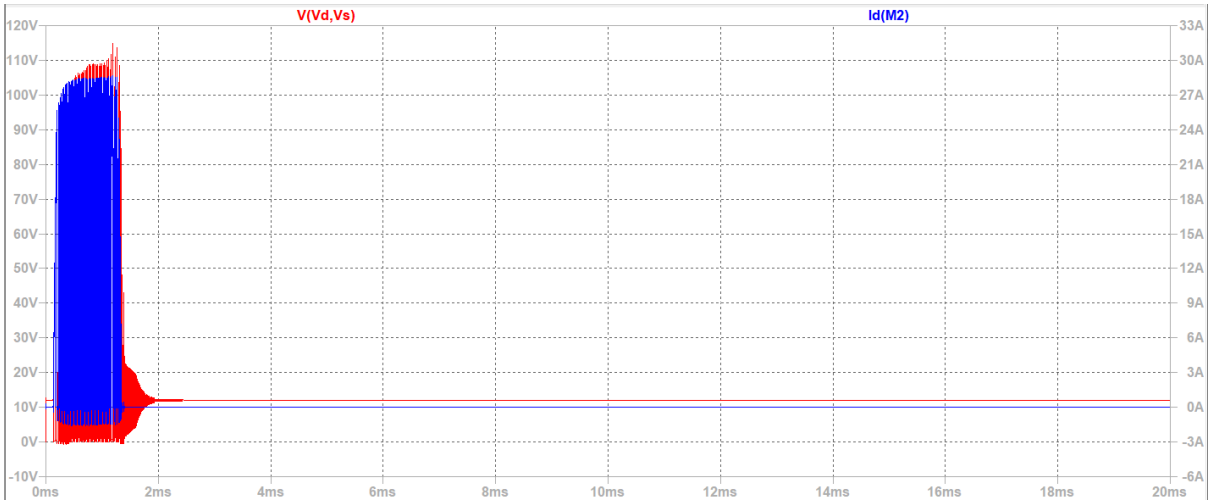


Fig. 12. The Mosfet Current and Voltage For 18V Input - No Load Case.

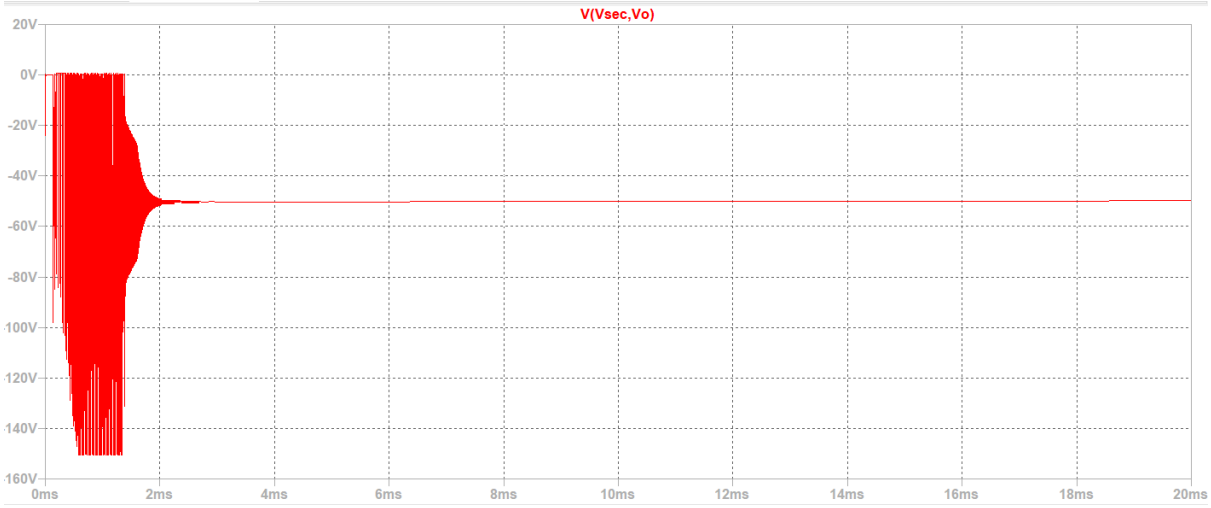


Fig. 13. The Output Diode Voltage For 18V Input - No Load Case.

After dynamics elements are charged and transient response is over, both the mosfet and output diode are off since this is a no load case. The system reaches steady state.

50% Load:

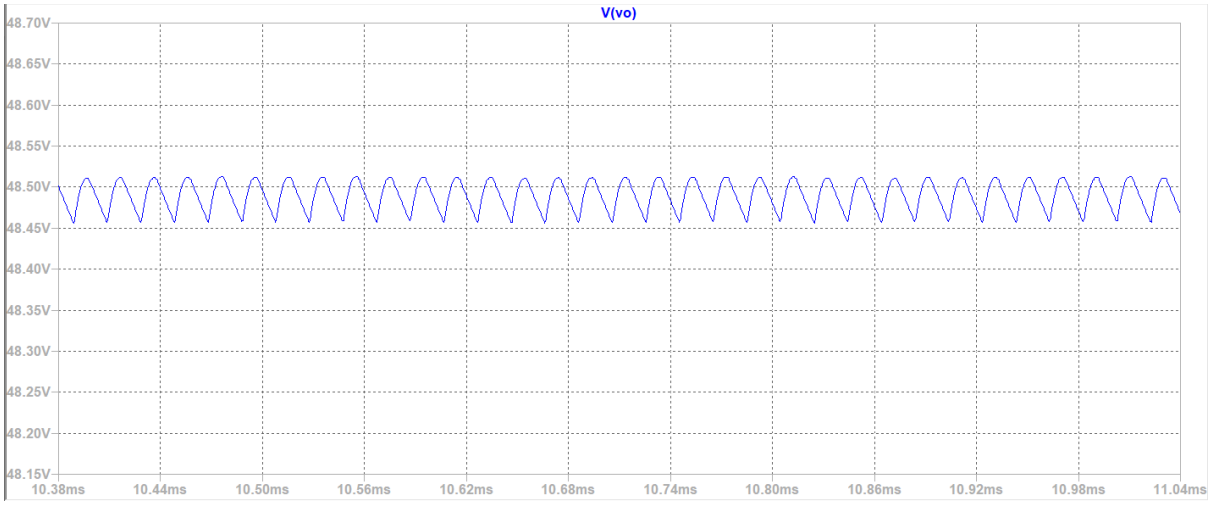


Fig. 14. The Output Voltage For 18V Input – 50% Load Case.

Vout(avg) = 48.49 V

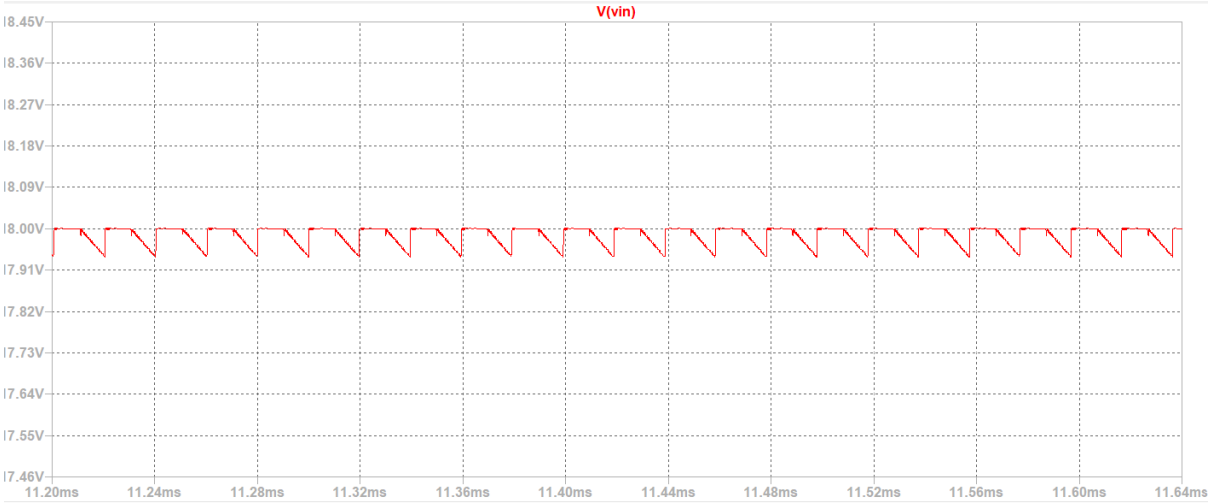


Fig. 15. The Input Voltage For 18V Input – 50% Load Case.

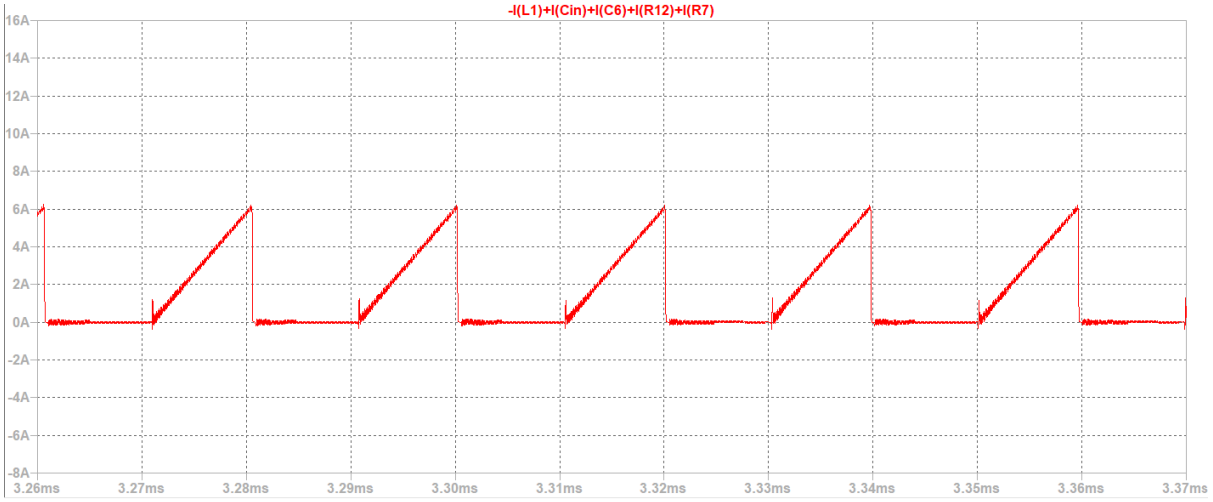


Fig. 16. The Input Current For 18V Input – 50% Load Case.

Iin(avg) = 1.38 A

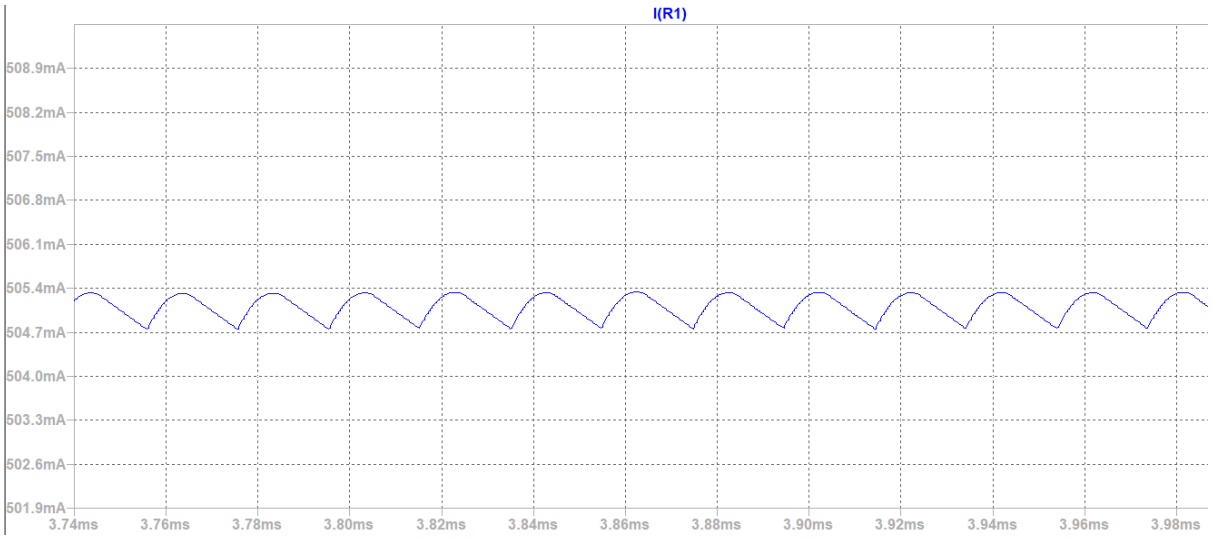


Fig. 17. The Output Current For 18V Input – 50% Load Case.

Iout(avg) = 505.1 Ma

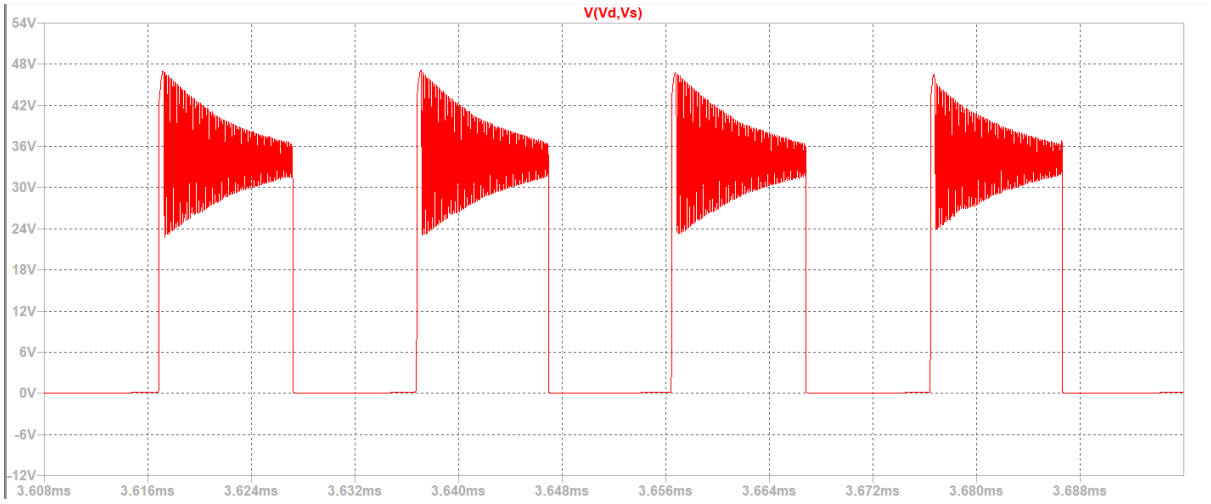


Fig. 18. The Mosfet Voltage For 18V Input – 50% Load Case.

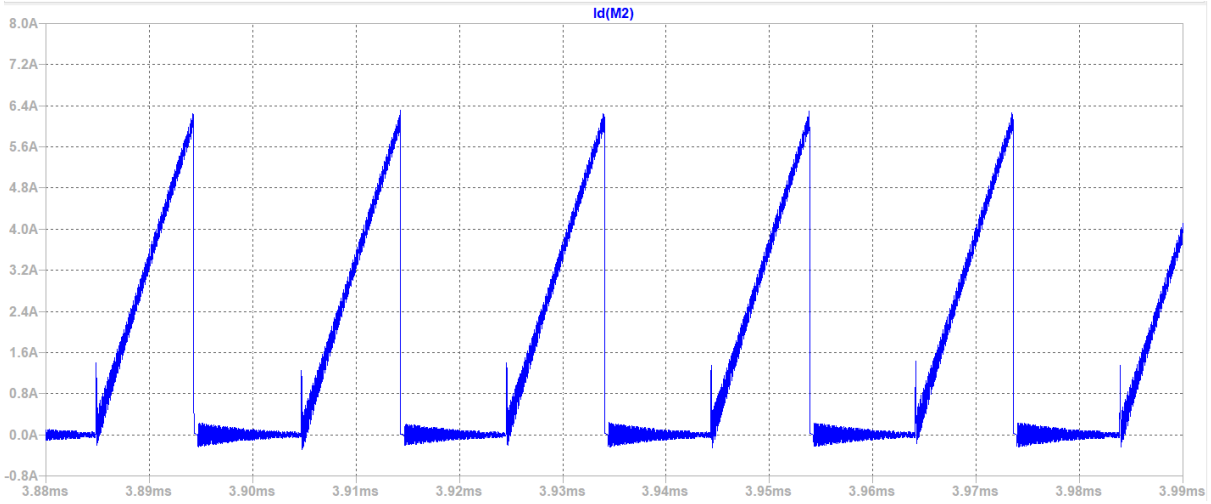


Fig. 19. The Mosfet Current For 18V Input – 50% Load Case.

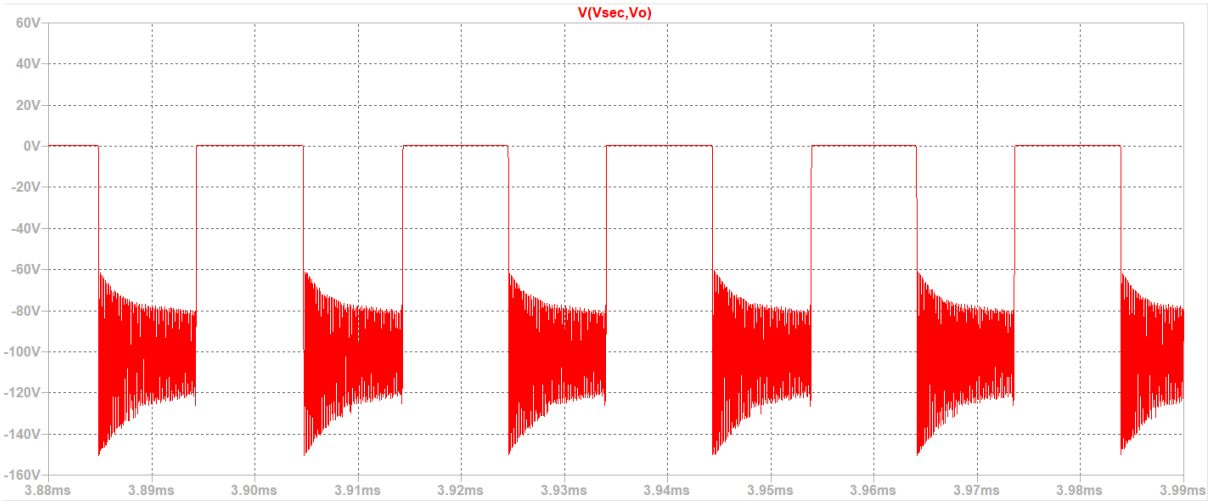


Fig. 20. The Output Diode Voltage For 18V Input – 50% Load Case.

It is obvious from the mosfet current that, converter operates at DCM at 50% load.

100% Load:

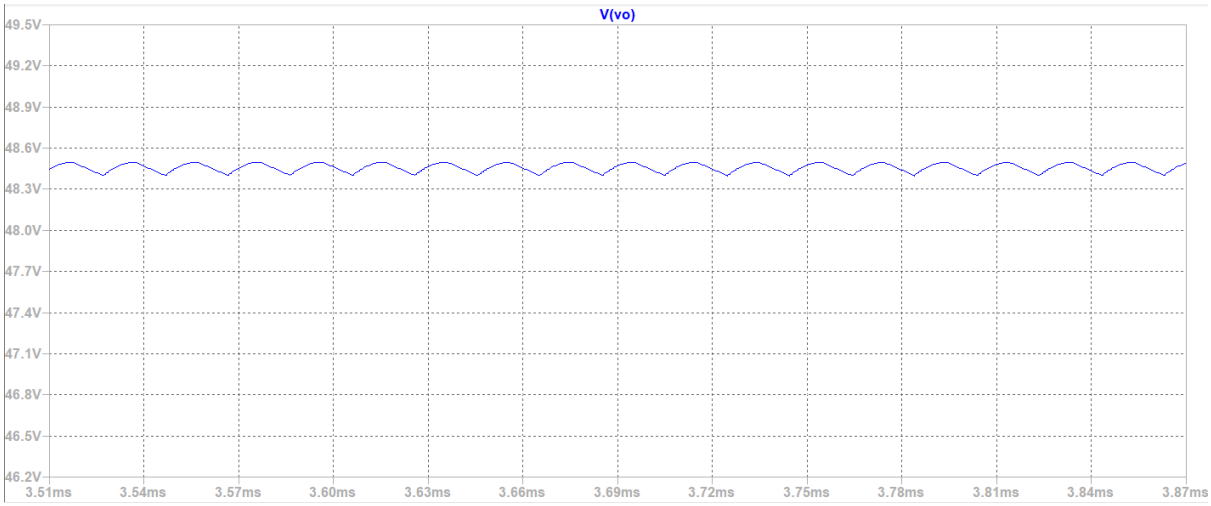


Fig. 21. The Output Voltage For 18V Input – 100% Load Case.

Vout(avg) = 48.45 V

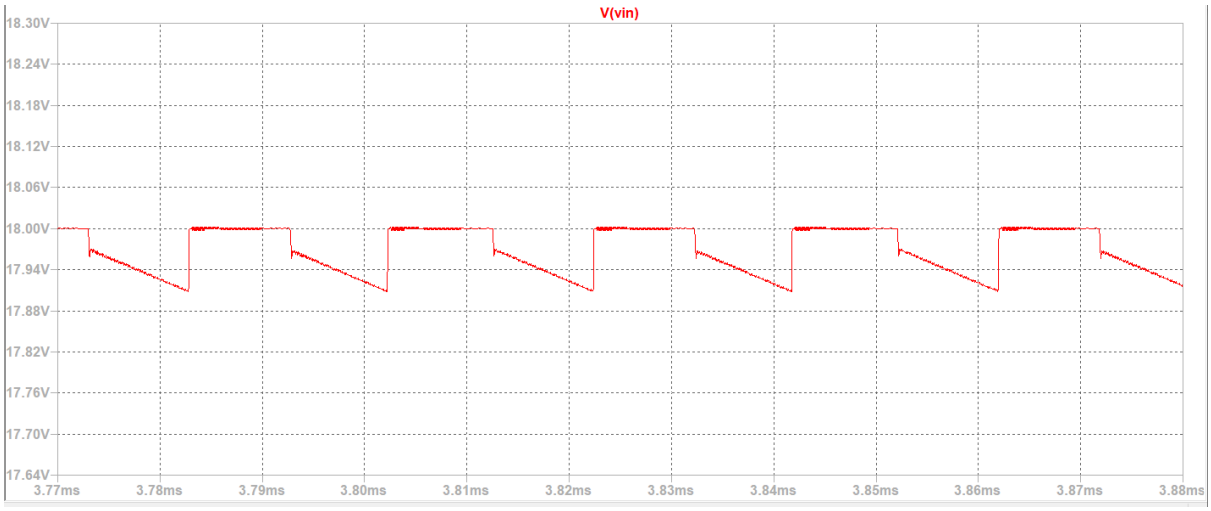


Fig. 22. The Input Voltage For 18V Input – 100% Load Case.

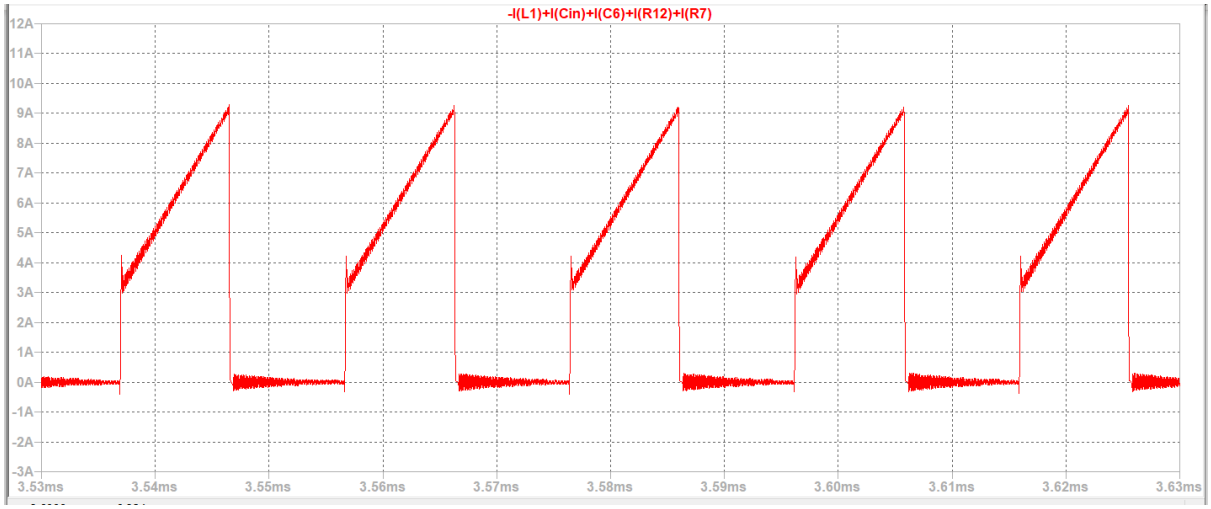


Fig. 23. The Input Current For 18V Input – 100% Load Case.

Iin(avg) = 2.949 A

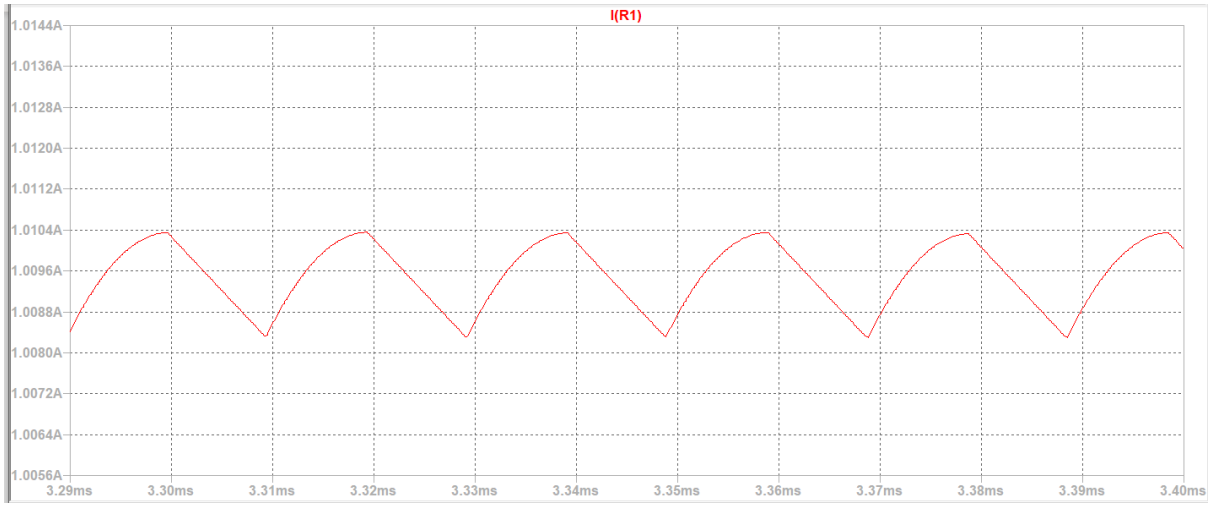


Fig. 24. The Output Current For 18V Input – 100% Load Case.

Iout(avg) = 1.0095 A

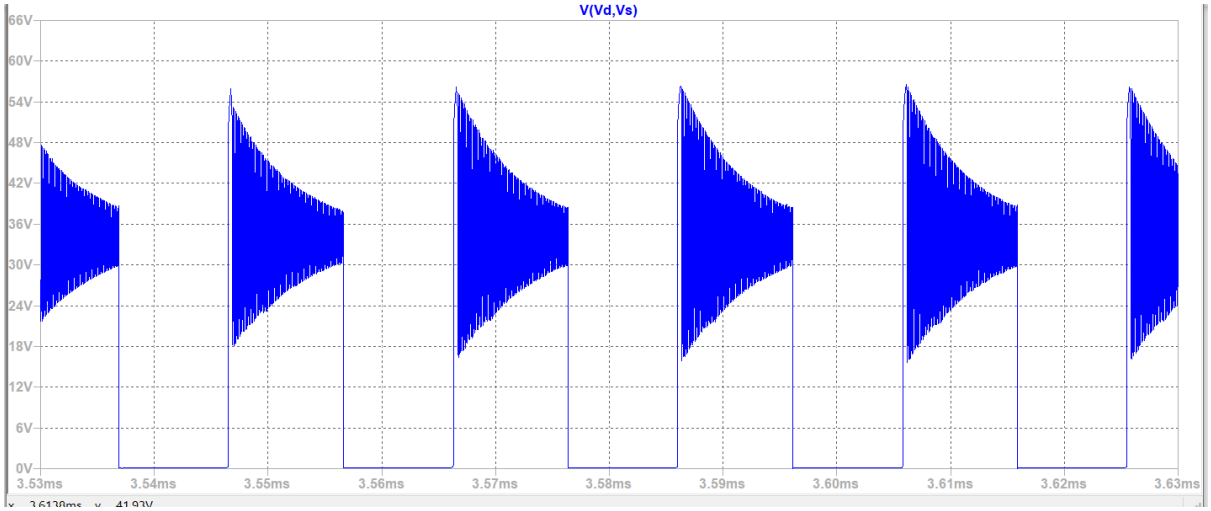


Fig. 25. The Mosfet Voltage For 18V Input – 100% Load Case.

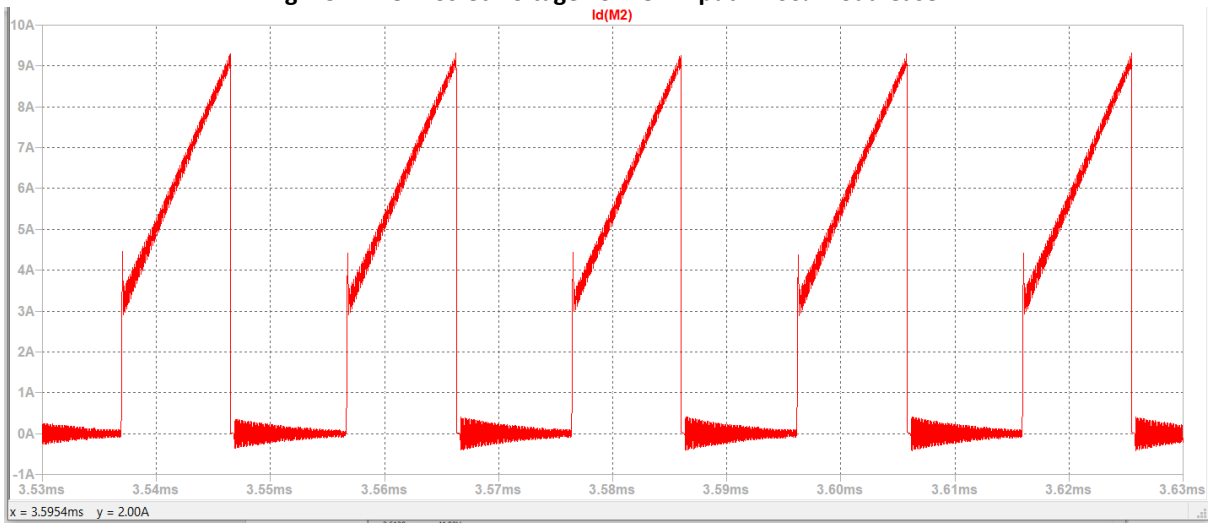


Fig. 26. The Mosfet Current For 18V Input – 100% Load Case.

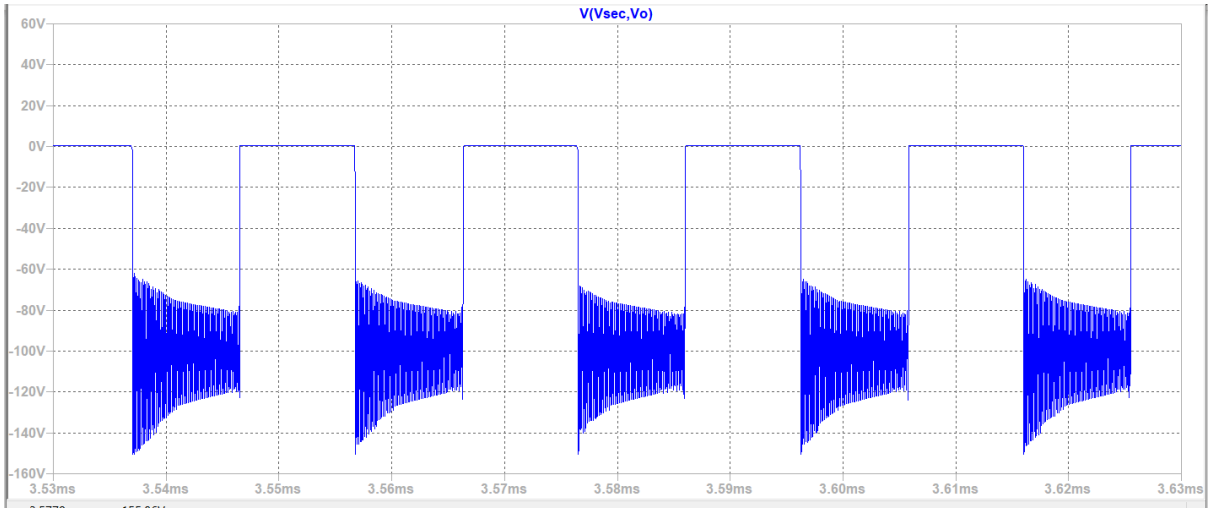


Fig. 27. The Output Diode Voltage For 18V Input – 100% Load Case.

It is obvious from the MOSFET current that the converter operates at CCM for full load case.

Component Selection

Mosfet:

The maximum mosfet voltage is

$$Vsw(\max) = Vd + \frac{N1}{N2} * Vo = 18 + \frac{1}{3} * 48 = 34\ V$$

On the other hand, the maximum switch current is

$$Isw(\max) = \frac{1}{1-D} * \frac{N2}{N1} * Io + \frac{N1}{N2} * \frac{(1-D) * Ts}{2 * Lm} * Vo = 2.38 * 3 * 1 + \frac{1}{3} * \frac{0.42 * \frac{1}{50000}}{2 * 59.68 * 10^{-6}} * 48$$

$$= 8.266\ A$$

We have chosen IRF 540 N Mosfet because it has a current rating of 28 A and voltage rating of 100 V. This values guarantees proper operation. Moreover, it has a drain to source resistance of 44 mohm which is quite low.

Output Diode:

The maximum reverse voltage of the diode is equal to output voltage when the switch is on case and it is 48 V . + 18*3 = 102 V. Moreover, maximum current on the diode is

$$\frac{8 + \frac{2.835}{2}}{3} = 3.14\ A$$

For the diode selection, we have chosen DSA10C150PB Schottky diode which has a current rating of 2x5 A and voltage rating of 150V. Moreover, it has a forward voltage drop 0.71 V.

Output Capacitor:

The output capacitor is selected as:

$$\frac{\Delta Vo}{Vo} = \frac{D}{R * C * f}$$

$$C = \frac{D}{R * \frac{\Delta Vo}{Vo} * f} = 8\ uF$$

To guarantee proper operation, C was chosen as 100 uF, and the voltage rating is chosen as 63 V. However, during the test, the voltage deviation was more than the value on specification. Hence, the capacitor value increased to 500 uF.

Input Capacitor:

In the project, we assumed the power supply gives the DC voltage with small deviation. Therefore, by putting a small capacitor, the deviation at voltage can be minimized. As a result, 3 uF capacitor was chosen, and the voltage rating was 50V. However, when we test the controller, too much voltage drop is detected. Hence, the capacitor must be higher (3 times as high as output capacitor).

Transformer:

The selection criteria of the transformer are stated at *Magnetic Design Considerations and Tests* section.

Controller:

UC3845 is one of the most used DC-DC switching controller on the market. The line and load regulation values are suitable for the design requirements. Also, since the input voltage of the controller can be between 12V and 28V, extra converter or third winding of the transformer is not required. In general, UCxxxx series are looking applicable for the project.

Current Control mode resistor:

Rms current of the primary side is equal to 8.3 A. Hence, the power loss at the Current Control mode resistor is equal to $I_{pri,rms}^2 * R_{current\ control} = 8.3^2 * 50 * 10^{-3} = 3.44W$. Therefore, sandstone resistors are preferred.

Snubber Diode:

Because of the current control with UC3843, max current that can be flow through primary side is 20 A. In addition, maximum reverse voltage of the snubber diode is 102 V according to simulation. Hence, DSA60C150PB Schottky diode was chosen which has a current rating of 2x30 A and voltage rating of 150V. Moreover, it has a forward voltage drop 0.8 V.

All the resistors and capacitors for controller is chosen through-hole package.

Test Results

The flyback converter that is designed by Dragonfly is shown in figure 28. After simulation and component selection the PCB is designed. However, due to limited time and the order issues, Pertinax is used to test the converter. Since we anticipate that we may encounter such problems, instead of ordering surface mounted packages, through-hole packages are ordered. As a result, we built are design on Pertinax without wasting the time.

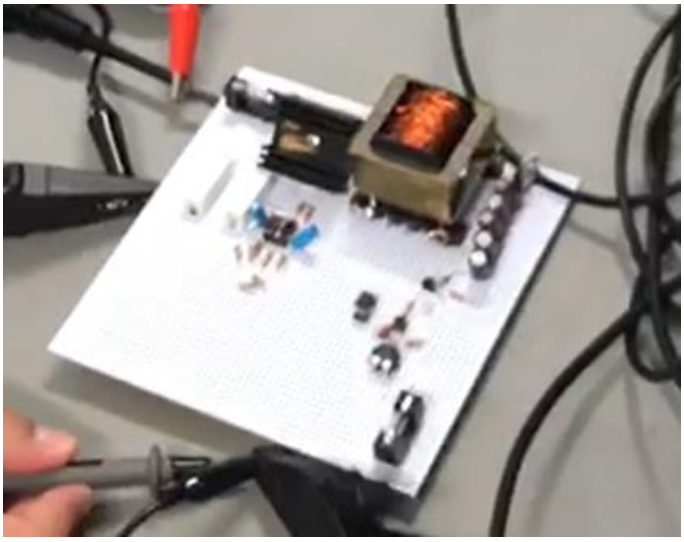


Fig. 28. Flyback Converter designed by Dragonfly.

In order to test the flyback converter, the following units are used:

- DC Power Supply
- Multimeter
- Resistive Load Bank

To observe the output voltage deviation when the load and the input voltage changes, this basic setup was built. The load is changed by paralleling the resistor via switches and by connecting multimeter at the output the voltage can be observed. As can be seen in figures 29,30,31,32 and 33, the converter can fix the output voltage around 48V with small deflection which is acceptable because of the design specifications which states that 3% voltage deviation is acceptable while load regulation and line regulation.

Fig. 29. The test setup for 25% Load, V=18V.

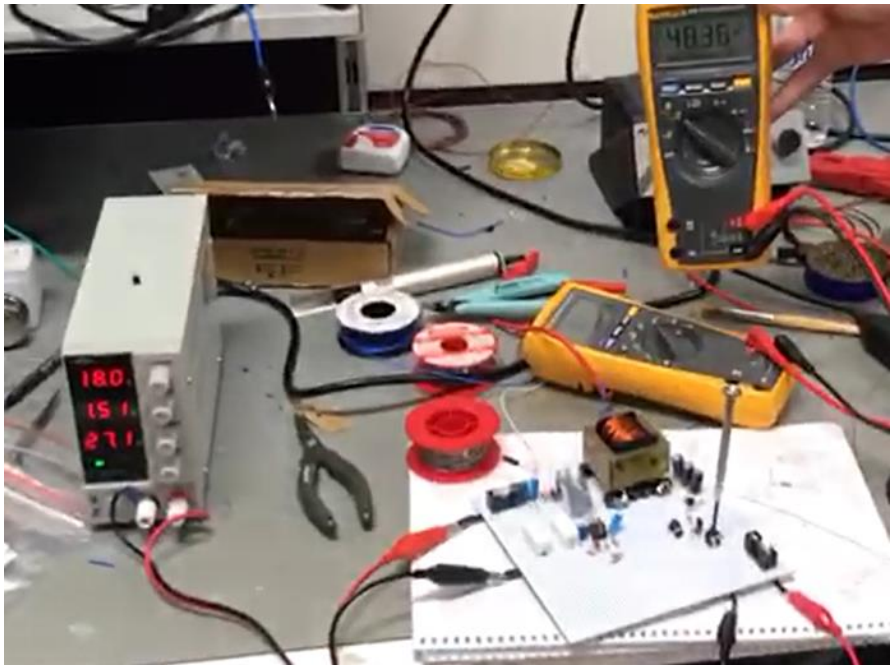


Fig. 30. The test setup for 50% Load, V=18V.

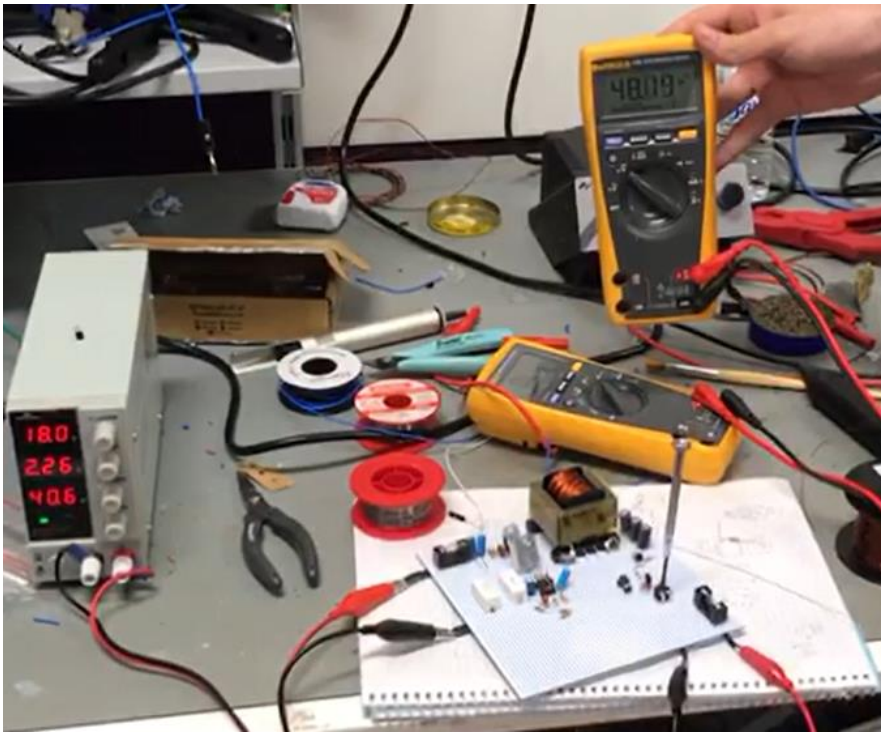


Fig. 31. The test setup for 75% Load, V=18V.

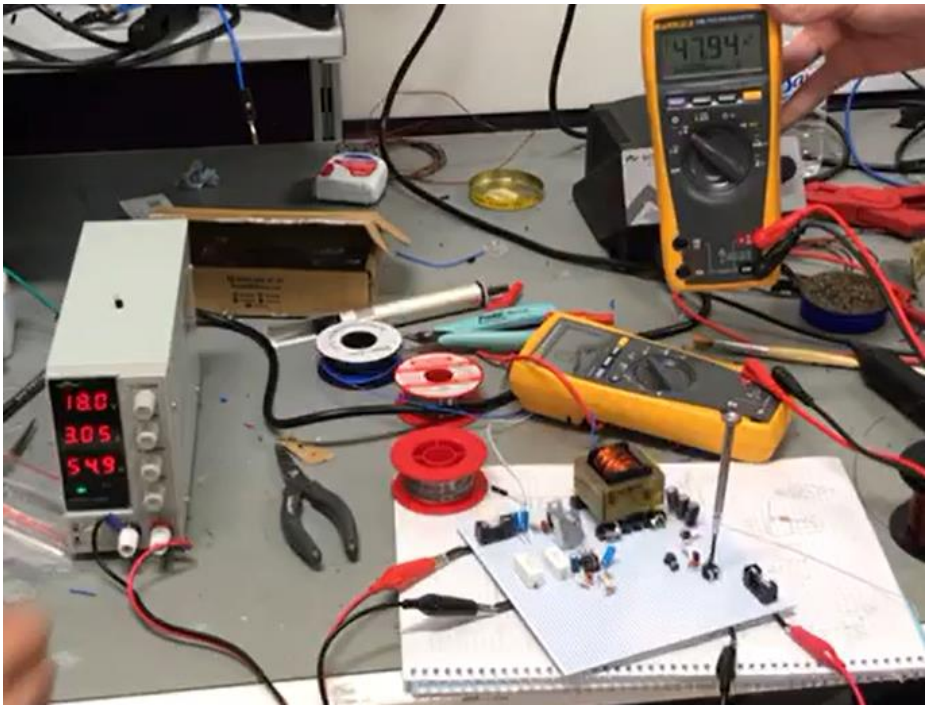


Fig. 32. The test setup for 100% Load, V=18V.

Fig. 33. The test setup for 100% Load, V=12V.

Table 1 Test Results with different loads.

Load (Ω)	$Output\ Voltage$ (V)	
	V_{in} =18V	V_{in} =12V
430	48.51	48.09
210	48.46	48.02
106	48.36	47.78
72	48.19	47.33
53	47.94	47.02

From the specification:

- Line Regulation(Deviation of percent output voltage when input voltage is changed from its minimum to maximum or vice versa): 3%
- Load Regulation(Deviation of percent output voltage when load current is changed from 10% to 100% or vice versa): 3%

$$48 * \frac{3}{100} = 1.44V$$

Load Regulation

- 430 Ω(11.16% Load) and 53 Ω(90.57% Load) for Vin=18V;

  |48.51-47.94|=0.57V<1.44V

- 430 Ω(11.16% Load) and 53 Ω(90.57% Load) for Vin=12V;

  |48.09-47.02|=1.07 V<1.44V

Line Regulation

- Vin = 18V and Vin = 12V for R=53Ω (90.57% Load)

  |47.94-47.02|=0.92 V<1.44V

- Vin = 18V and Vin = 12V for R=72Ω (66.67% Load)

  |48.19-47.33|=0.86 V<1.44V

- Vin = 18V and Vin = 12V for R=106Ω (45.228% Load)

  |48.36-47.78|=0.58 V<1.44V

- Vin = 18V and Vin = 12V for R=210Ω (22.86% Load)

  |48.46-48.02|=0.44 V<1.44V

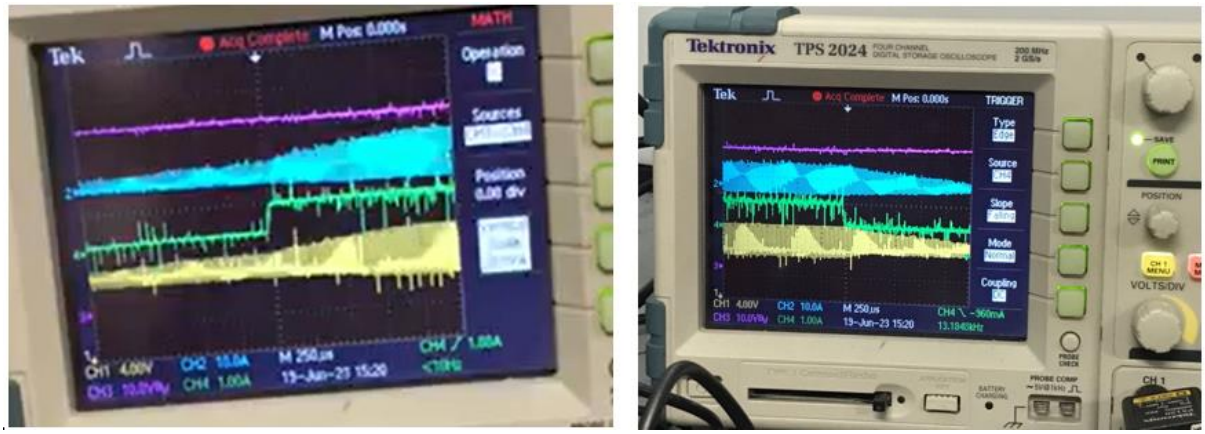
- Vin = 18V and Vin = 12V for R=430Ω (11.16% Load)

  |48.51-48.09|=0.42 V<1.44V

Although the results satisfy the specification, for Load regulation it is not enough to decide whether the converter operates within the load regulation or not. Therefore, another test setup is built. This test setup contains:

- DC Power Supply
- Oscilloscope
- Resistive Load Bank
- Digital Load

With this test setup instead of using multimeter to observe the output voltage, the oscilloscope is used. Oscilloscope probs are connected such that input voltage (CH1), input current (CH2), output voltage (CH3) and output current (CH4) can be measured simultaneously. The Resistive load bank and digital load are connected parallel so that the load can be adjusted from 10% to 100% instantly. The results are shown in figure 34. Input voltage (yellow), input current (blue), output voltage (purple) and output current (green) can be observed. Although, the output current changes from 0.1 A to 1 A instantly, the output voltage maintains its value with small deflection as shown in figure 34a. Additionally, the circuit tested when the load changes from 100% to 10% as shown in figure 34b.



(a) *(b)*

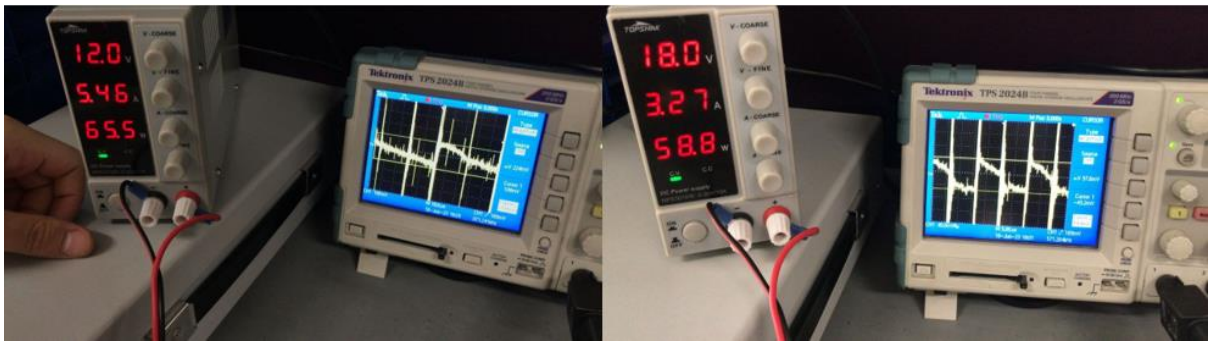
Fig. 34. Test results for load regulation (a) 10% load to 100% load, (b) 100% load to 10% load.

After the design control whether the converter operates within the specification, the efficiency of the converter is calculated. In figure 35, the input data can be seen when the load = 53 Ω. Hence;

$$\eta(\%) = \frac{48^2/_{53}}{65.5} * 100 = 66.37\% \; for \; V_{in} = 12 \; V$$

$$\eta(\%) = \frac{48^2/_{53}}{58.8} * 100 = 73.93\% \; for \; V_{in} = 18 \; V$$

Since, the efficiency of the flyback converter is low, the converter heated during the test especially the MOSFET as it can be seen in figure 36. Even though, heatsink is used to radiate the heat better, the temperature of the MOSFET increased to $129^o C$ during the test.



(a) *(b)*

Fig. 35. Test results of the converter's input data at Load = 53 Ω.

Fig. 36. The thermal results of the converter when Vin=12V.

Conclusion

In conclusion, the isolated DC-DC converter design using the flyback topology has been successfully implemented and tested. The selection of the flyback topology was based on several factors, including its efficiency, availability of components, and previous group references. The transformer design was carefully executed, although there were challenges in winding the coils. The measurements confirmed the desired turn ratio and magnetizing inductance, with minor deviations that can be compensated by the controller. The UC3843 controller was selected for its flexible frequency range, current-mode control, and availability. The LTSpice model of the circuit design was constructed, and computer simulations were performed for different input voltage cases and load conditions. The simulation results demonstrated satisfactory performance in terms of input and output voltage, current, and MOSFET behavior. Although there was an efficiency problem for 12V and high load cases in the real experimental procedure, the project provided valuable insights into the design, implementation, and testing of an isolated DC-DC converter.

References

[1] Improving the Performance of Traditional Flyback-Topology With Two-Switch –Approach