EE 464
Static Power Conversion II
Simulation Project II

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March 2019

Introduction

In this simulation project, we are assigned to simulate hardware project topology. At the first part, we simulated the topology with ideal components. Then, we designed our transformer. After calculations, we added parasitic components and re-simulated the topology. For desired output characteristics, we determined related duty cycle values. At the last part of the project, we made preliminary component selection according to simulation findings .

Part a.

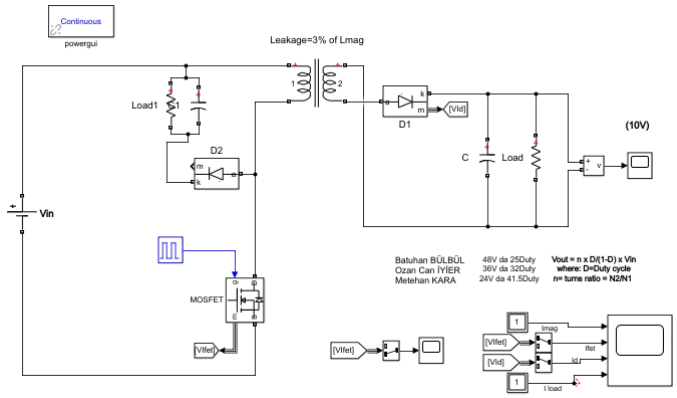

Figure 1: The Schematic of Flyback Converter with Ideal Converters

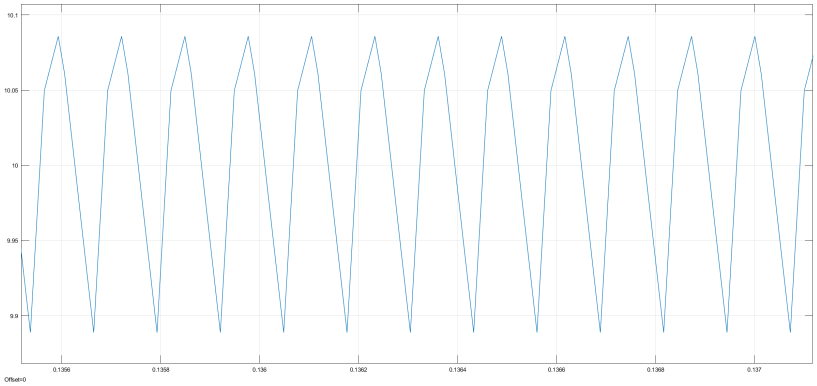

Figure 2: The Output Voltage Graph for 24V Input (Duty=0.44)

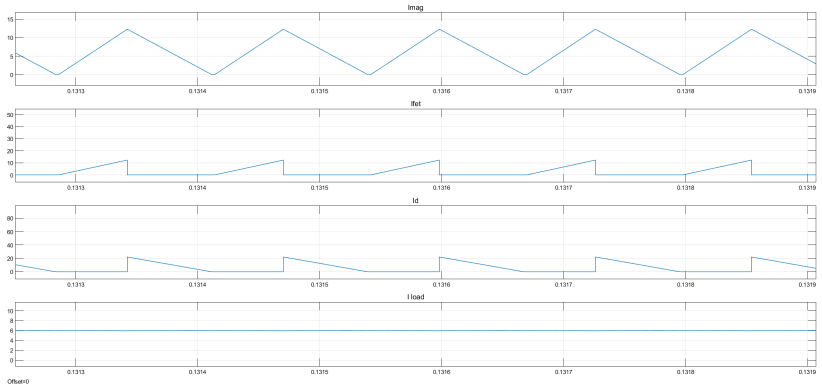

Figure 3: The Currents for 24V Input

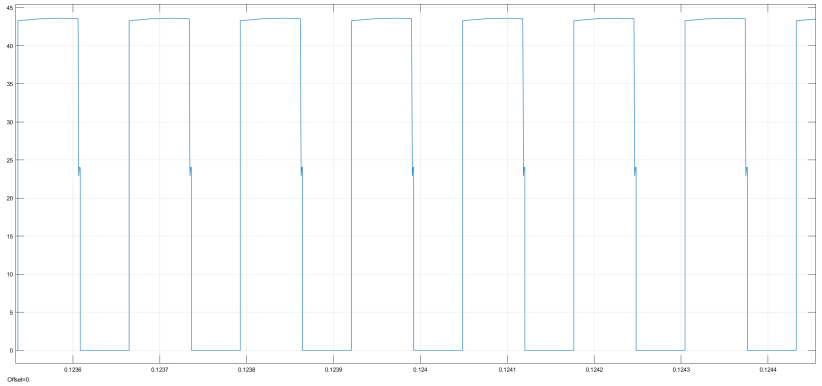

Figure 4: The Mosfet Voltage for 24V Input

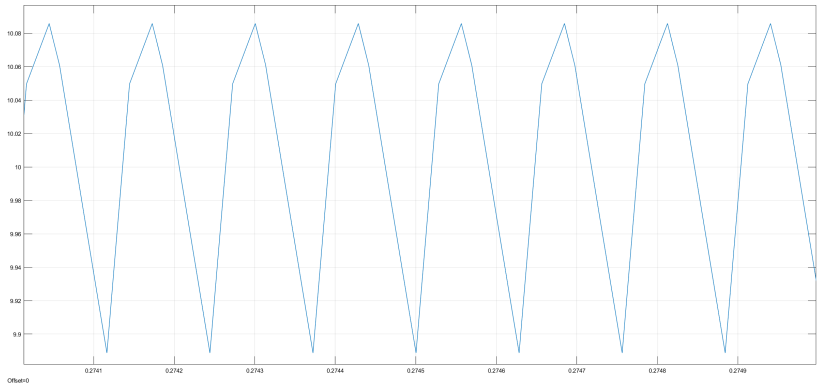

Figure 5: Output Voltage Graph for 48V input(Duty=0.22)

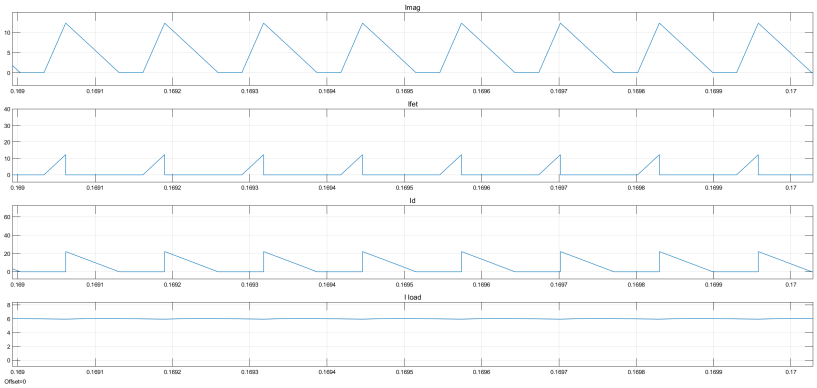

Figure 6: The Currents for 48V Input

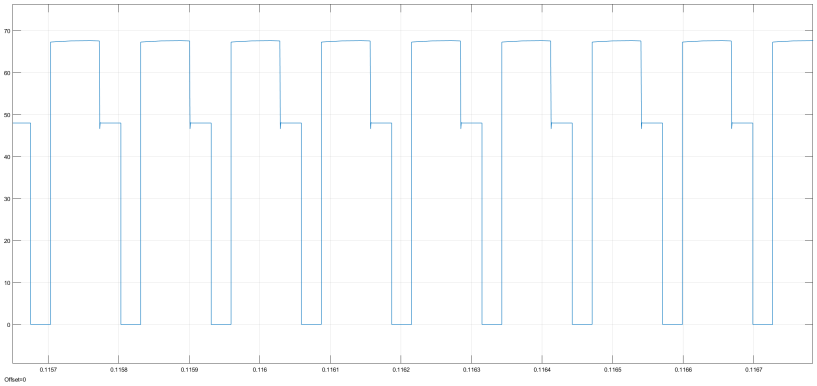

Figure 7: The Mosfet Voltage for 48V Input

Part b.

MATLAB CODE:

```
Vo=10; % desired output voltage
Vin_min=24; % Minimum input voltage
Vin_max=48; % Maximum input voltage
Eff=0.9; % efficiency
fs=7815; % frequency
Po_max=65; % Maximum output power
Pin_max=Po_max/Eff; % Maximum input power

Io_max=6; % Load Current
D=0.45; % Maximum duty cycle


Lmax= (Vin_min^2*D^2*Eff)/(2*fs*Po_max); % calculation of L-mag

Ipeak= sqrt((2*Po_max)/(0.85*Lmax*fs*Eff)); % Peak primary current

Turns= (Vin_min*D)/((1-D)*(Vo+0.8)); % Turn ratio of transformer
```

```
%% Output capacitor selection

Vo_ripple=0.04*10;
C_out=Io_max*D/(fs*Vo_ripple);
```

The following calculations explains transformer design procedure;

$$L_M = 0.1mH$$

$$A_L = 300nH/T^2$$

*Where T is number of turns.

$$\frac{L_M}{A_L} = T^2$$

*Where T is found as 18.25.
$n_{secondary} = 10$ is chosen to have 1.8 turns ratio.
Total Number of Turns= 28
Window Area of Selected Core= $530mm^2$
Maximum Cable Size= $\frac{530}{28} = 18.92mm^2$
Considering the fact that current carrying capacity of AWG type wires AWG12 is chosen.
Path length of selected core is 147mm.
Total length of cable required for wiring is 147*28=4.11 meter.
Total resistance of the wire is 21.44mΩ.
For simulation leakage inductance is assumed as % 3 of Lm.

Part c.

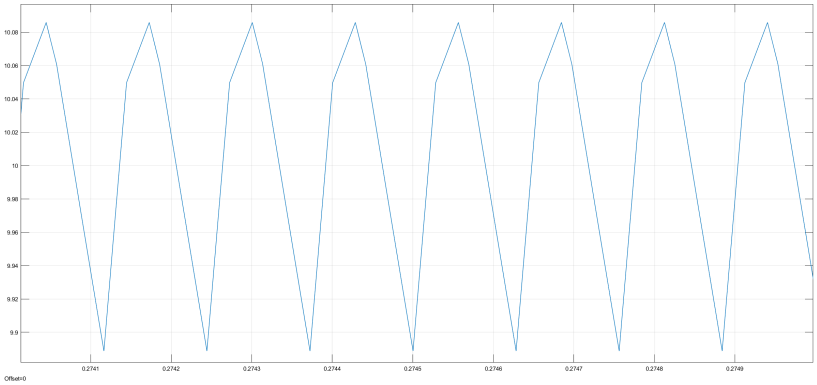

Figure 8: Output Voltage Graph for 48V input(Duty=0.22)

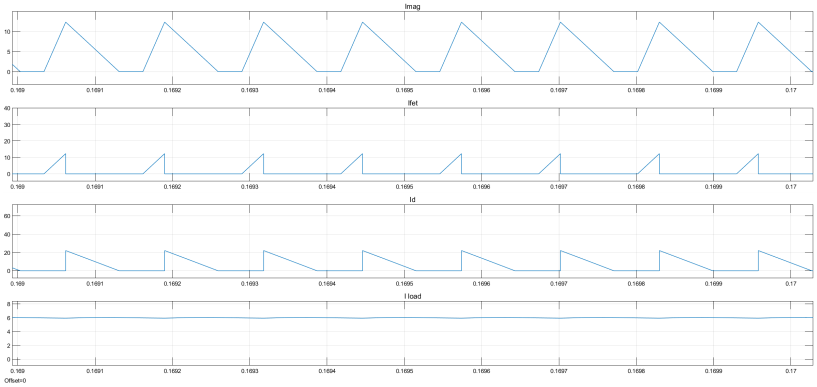

Figure 9: The Currents for 48V Input

Part d.

We designed our converter to work under DCM mode. For any load condition designed converter works under DCM.

Part e.

Part f.

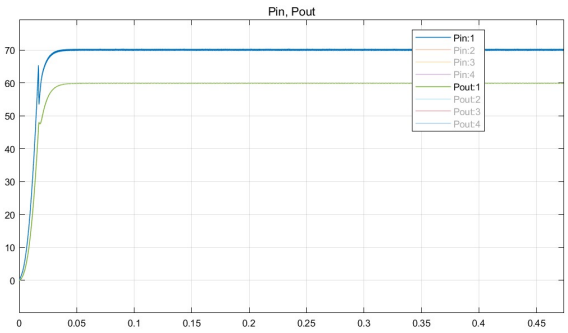

Figure 10: The Pin(=70W) and Pout(=60W) for 100% Loading(Efficiency= 85.71%)

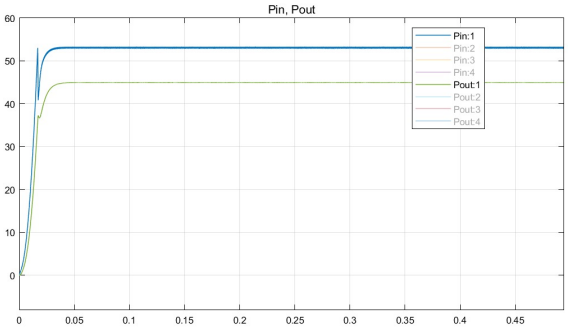

Figure 11: The Pin(=53W) and Pout(=45W) for 75% Loading(Efficiency= 84.91%)

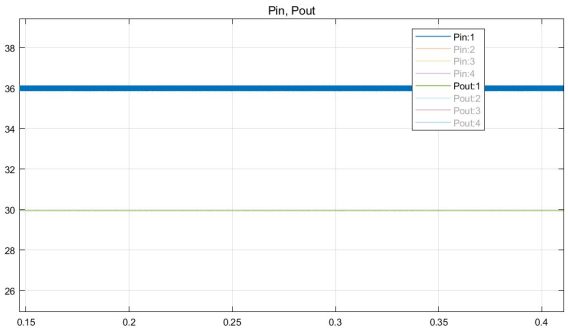

Figure 12: The Pin(=36W) and Pout(=30W) for 50% Loading(Efficiency= 83.33%)

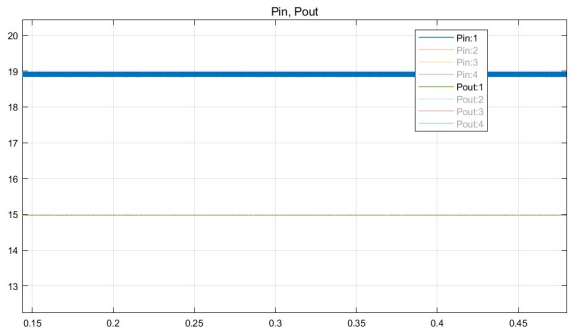

Figure 13: The Pin(=19W) and Pout(=15W) for 25% Loading(Efficiency= 78.95%)

Part g.

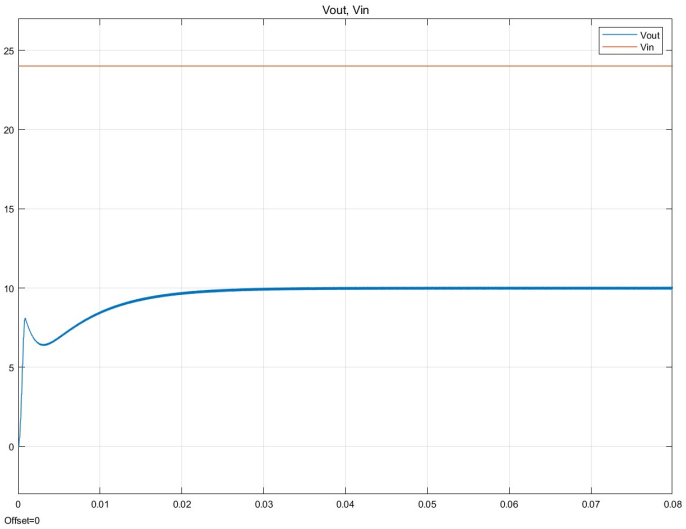

Figure 14: The Input-Output Voltage Graph for 24V input

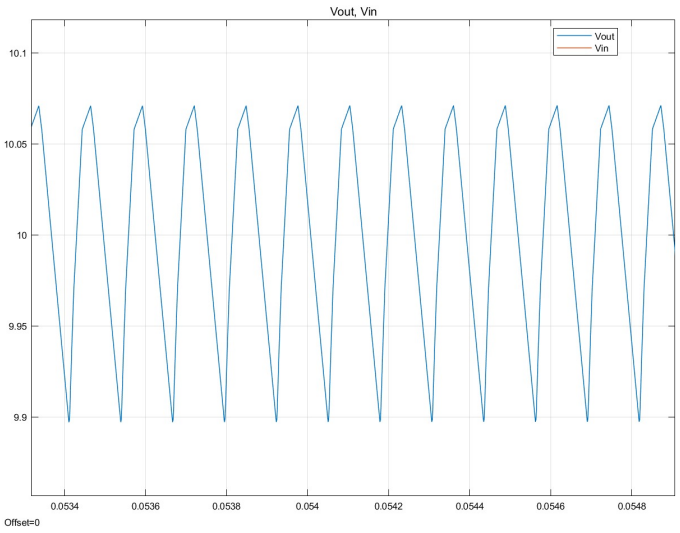

Figure 15: The Output Voltage Ripple(=184mV) When Vin=24V

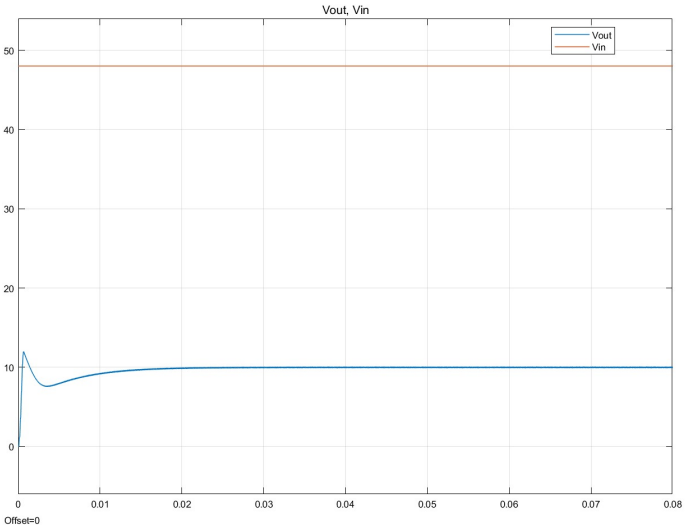

Figure 16: The Input-Output Voltage Graph for 48V input

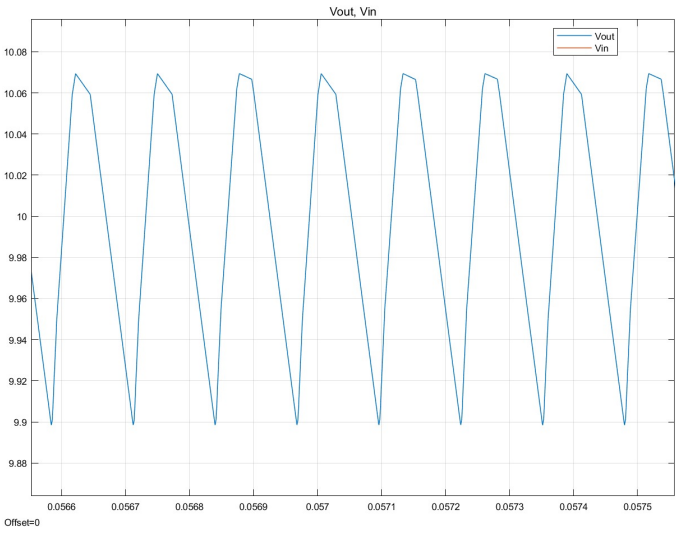

Figure 17: The Output Voltage Ripple(=182mV) When Vin=48V

Part h.

Table 1: Component List

Component	**Value**	**Brand**
Inductor 1	4.7 mH	sd
Inductor 2	4.7 mH	sd
Capacitor 1	100μF	sd
Capacitor 2	1 mF	sd
Load	4Ω	sd

Conclusion

This project was a preliminary for hardware project. At first part of the project, we worked with ideal components. Hence, although the output values are at desired levels. The parasitic elements are affected the output values inevitably. For realistic case, we calculated transformer parameters, snubbers and other components' values. At the last part of the project, we selected possible components according to simulation results. Although these components fit for simulations, there can be some unexpected situations at real life implementations. This project was a good exerxice for next stages of hardware project.