EE 464
Static Power Conversion II
Simulation Project II
Flyback Converter#3

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Introduction

In this simulation project, we are assigned to simulate hardware project topology which is Flyback converter with following specifications.

- Minimum input Voltage: 24V
- Maximum input Voltage: 48V
- Output Voltage: 12V
- Output Power: 60V
- Output Ripple: %4

At the first part, we simulated the topology with ideal components. Then, we designed our transformer. After calculations, we added parasitic components and re-simulated the topology. For desired output characteristics, we determined related duty cycle values. At the last part of the project, we made preliminary component selection according to simulation findings .

Part a.

For the first part of the project, we have simulated our system without any modification and obtained steady state response of our system.The schematic of our system can be seen from figure 1.

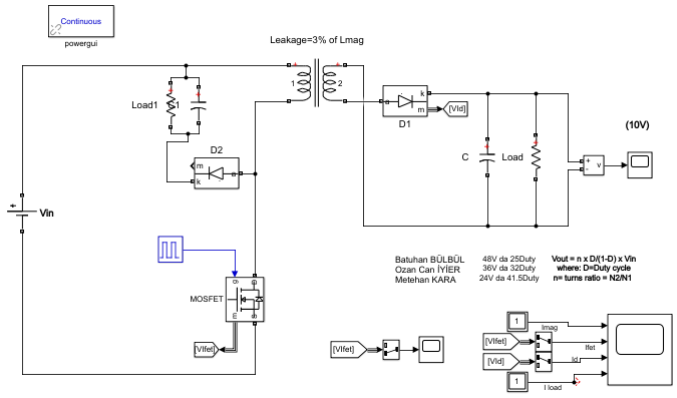

Figure 1: The Schematic of Flyback Converter with Ideal Components

For maximum and minimum input voltages, we determined the duty cycles as 0.44 for 24 V and 0.22 for 48V Case. According to these values, we obtained V_{Out}, currents and mosfet voltages for both cases. From simulation results which are indicated figure 2,3,4,5,6 and 7 we can observe that the output ripple values is convenient for %4 limitation. Current graphs shows us that our system is in the border of DCM. Although this graph observations are convenient for our system, the parasitic elements will be very crucial for the design. These effects will be discussed in the next parts of the reports.

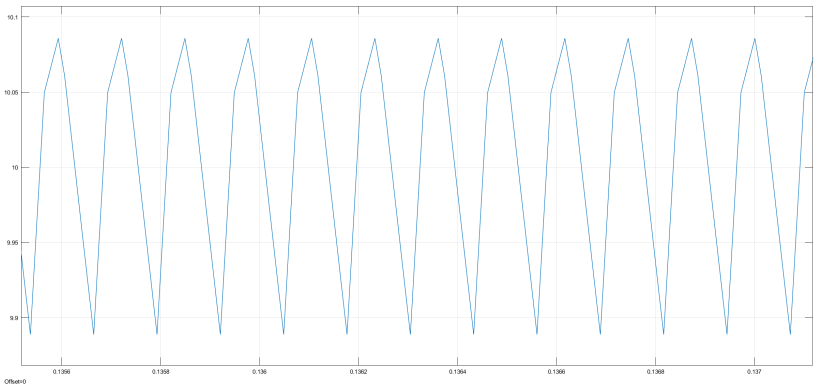

Figure 2: The Output Voltage Graph for 24V Input (Duty=0.44)

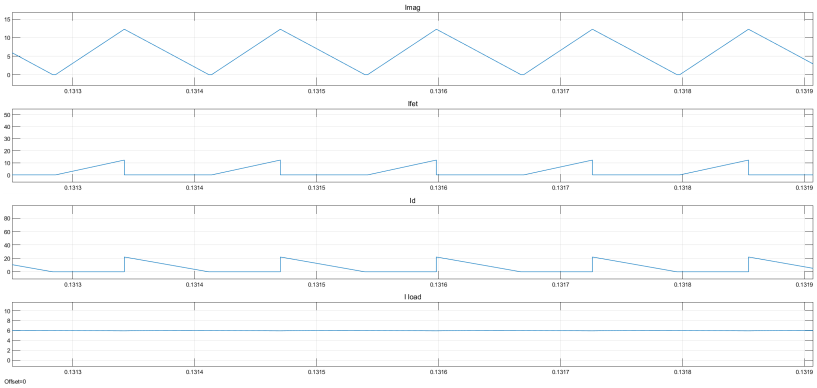

Figure 3: The Currents for 24V Input

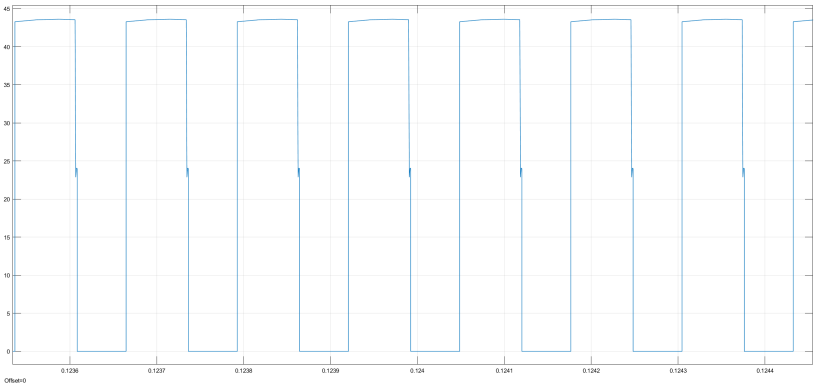

Figure 4: The Mosfet Voltage for 24V Input

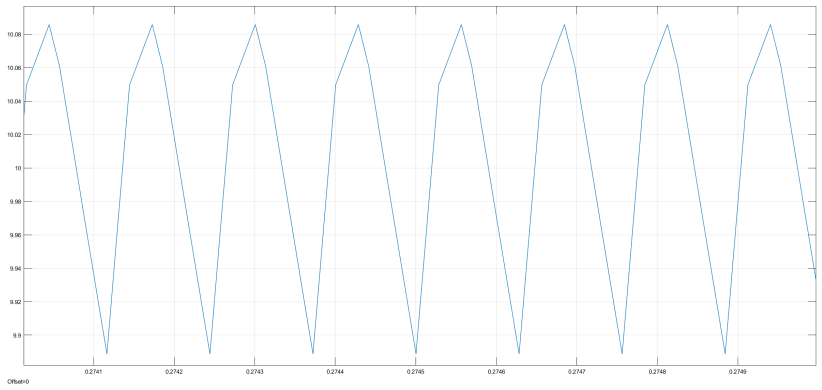

Figure 5: Output Voltage Graph for 48V input(Duty=0.22)

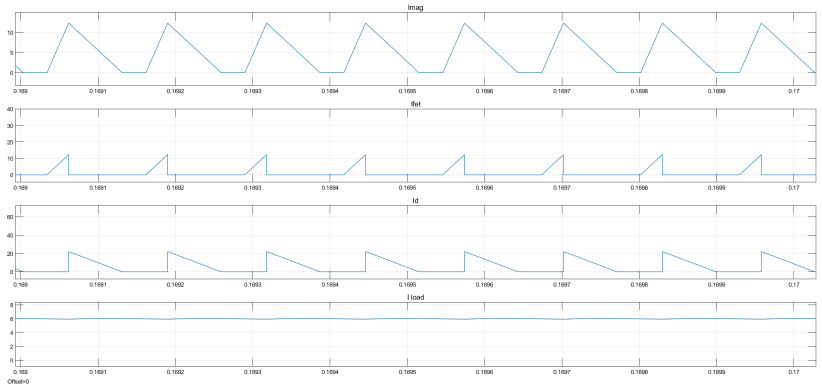

Figure 6: The Currents for 48V Input

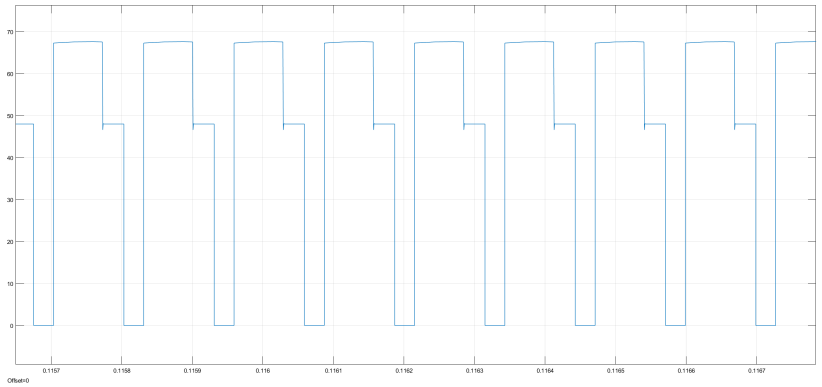

Figure 7: The Mosfet Voltage for 48V Input

Part b.

For transformer design, we created a MATLAB code to facilitate our work. The code calculates $I_{primary}, L_m$and turns ratio of the transformer. While creating this code Würth Cook Book Transformer Design Guideline is used. The MATLAB code and outputs can be seen from following figures.

```
Vo=10; % desired output voltage
Vin_min=24; % Minimum input voltage
Vin_max=48; % Maximum input voltage
Eff=0.9; % efficiency
fs=7815; % frequency
Po_max=65; % Maximum output power
Pin_max=Po_max/Eff; % Maximum input power

Io_max=6; % Load Current
D=0.45; % Maximum duty cycle


Lmax= (Vin_min^2*D^2*Eff)/(2*fs*Po_max); % calculation of L-mag

Ipeak= sqrt((2*Po_max)/(0.85*Lmax*fs*Eff)); % Peak primary current

Turns= (Vin_min*D)/((1-D)*(Vo+0.8)); % Turn ratio of transformer
```

```
%% Output capacitor selection

Vo_ripple=0.04*10;
C_out=Io_max*D/(fs*Vo_ripple);
```

Workspace

Name	Value
C_out	8.6372e-04
D	0.4500
Eff	0.9000
fs	7815
Io_max	6
Ipeak	14.5067
Lmax	1.0333e-04
Pin_max	72.2222
Po_max	65
Turns	1.8182
Vin_max	48
Vin_min	24
Vo	10
Vo_ripple	0.4000

Figure 8: Code Results

After obtaining the $I_{primary}, L_m$and turns ratio values we made some calculation in order to finalize

procedure. The following calculations explains transformer design procedure;

$$L_M = 0.1mH$$

$$A_L = 300nH/T^2$$

*Where T is number of turns.

$$\frac{L_M}{A_L} = T^2$$

*Where T is found as 18.25.
$n_{secondary} = 10$ is chosen to have 1.8 turns ratio.
Total Number of Turns= 28
Window Area of Selected Core= $530mm^2$
Maximum Cable Size= $\frac{530}{28} = 18.92mm^2$
Considering the fact that current carrying capacity of AWG type wires AWG12 is chosen.
Path length of selected core is 147mm.
Total length of cable required for wiring is 147*28=4.11 meter.
Total resistance of the wire is 21.44mΩ.
For simulation leakage inductance is assumed as % 3 of Lm.

Part c.

As explained in Part A, we tried to idealize our components as much as possible. In addition to that we made our snubbers too big to carry current and made our swtiches as ideal as possible. The some of calculations of this part is explained previous part. The simulation results are indicated at following figures.

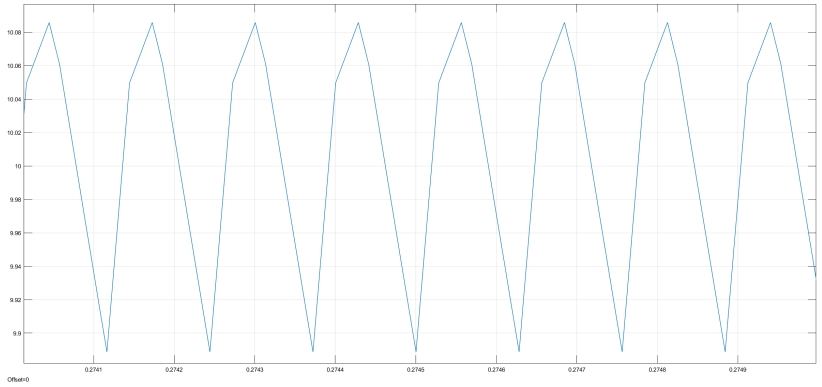

Figure 9: Output Voltage Graph for 48V input(Duty=0.22)

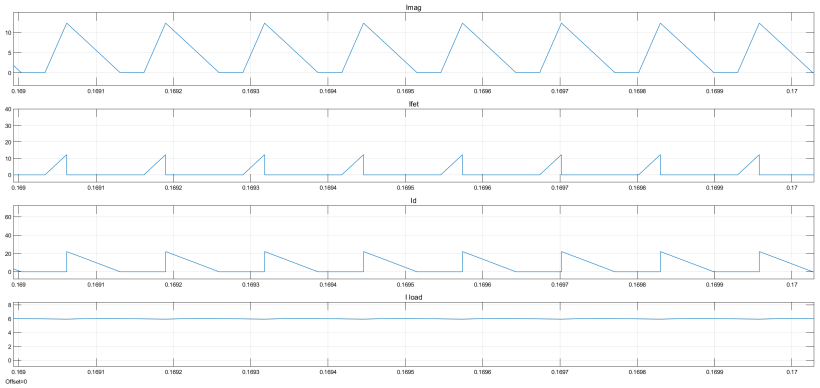

Figure 10: The Currents for 48V Input

Part d.

We designed our converter to work under DCM mode which is a possible result of using Würth Cook Book. The following two figures are supporting this idea. Hence, for any load condition designed converter works under DCM.

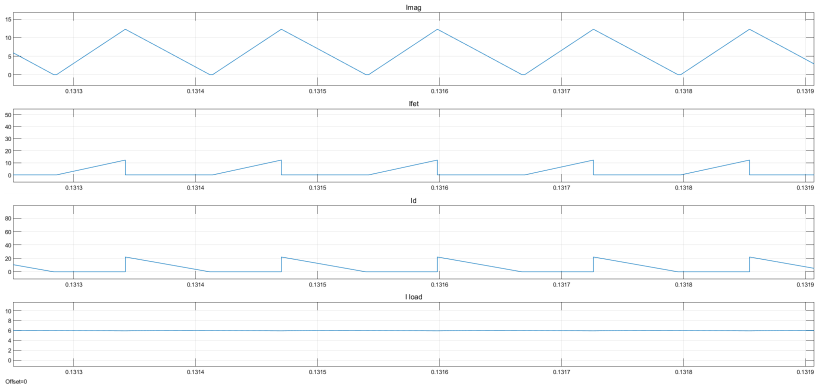

Figure 11: The Currents for 24V Input

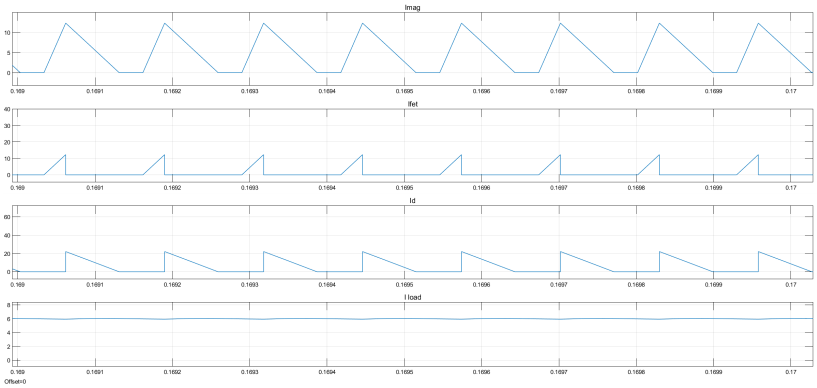

Figure 12: The Currents for 24V Input

Part e.

In this part, we investigated effects of parasitic components in diode and mosfet. The internal resistance and reactance leads some losses. Hence system efficiency decreases because of voltage drop on this components.

In this part, the effect of parasitic components inside the switches are observed. The resistances (i.e. snubber and FET resistances) cause a power loss to the system. Moreover, they cause a voltage drop across the switches. In addition to that, the default voltage drop across the switches has the same effect, too.

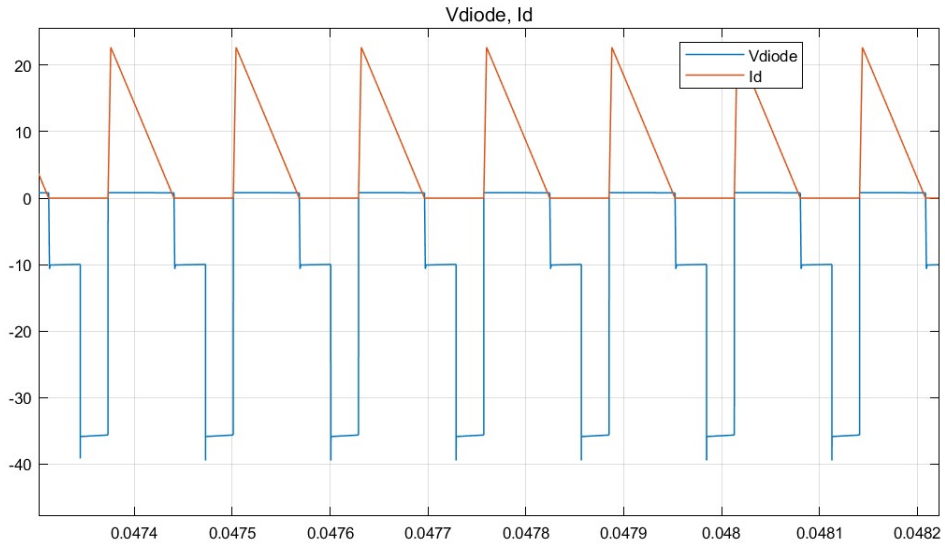

Figure 13: Diode Mosfet and Current

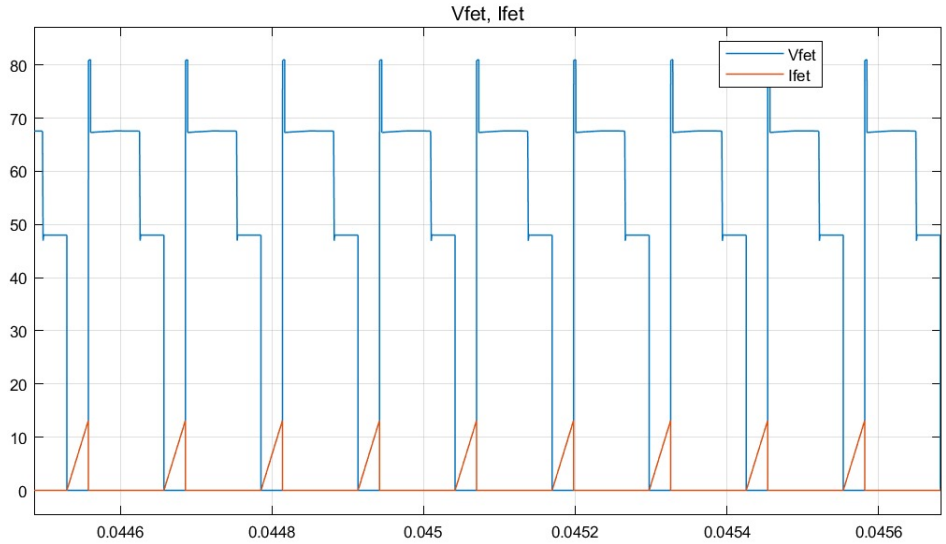

Figure 14: Mosfet Voltage and Current

Part f.

In this part, we simulated our topology under different load conditions. For each case we obtained input, output powers. The input, output power and efficiency values which are obtained from simulation blocks are indicated at captions of the figures for each case.

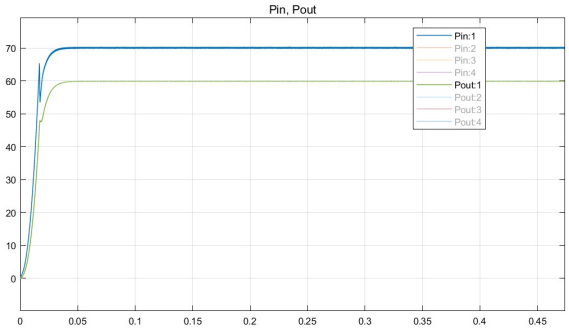

Figure 15: The Pin(=70W) and Pout(=60W) for 100% Loading(Efficiency= 85.71%)

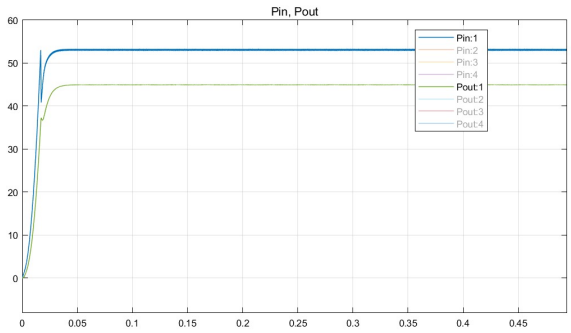

Figure 16: The Pin(=53W) and Pout(=45W) for 75% Loading(Efficiency= 84.91%)

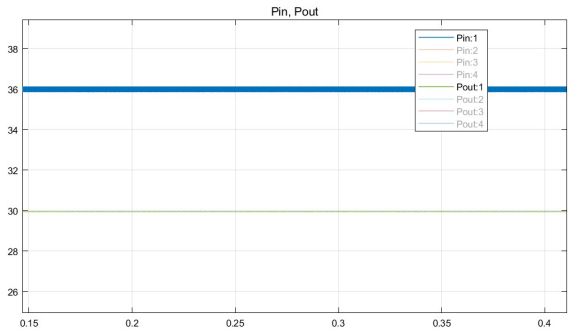

Figure 17: The Pin(=36W) and Pout(=30W) for 50% Loading(Efficiency= 83.33%)

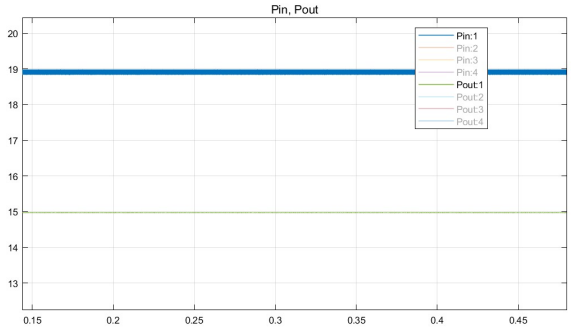

Figure 18: The Pin(=19W) and Pout(=15W) for 25% Loading(Efficiency= 78.95%)

Part g.

For 24 Volts and 48 Volts inputs we simulated our topology and obtained the following figures which shows our system works properly for each case. If we face a ripple problem during real life testing part, we can handle this problem by using a larger capacitor at output. Hence we can set the ripple as desired values.

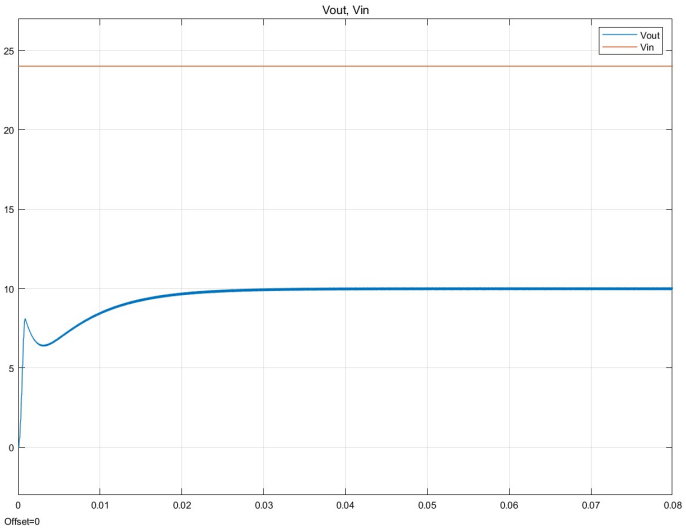

Figure 19: The Input-Output Voltage Graph for 24V input

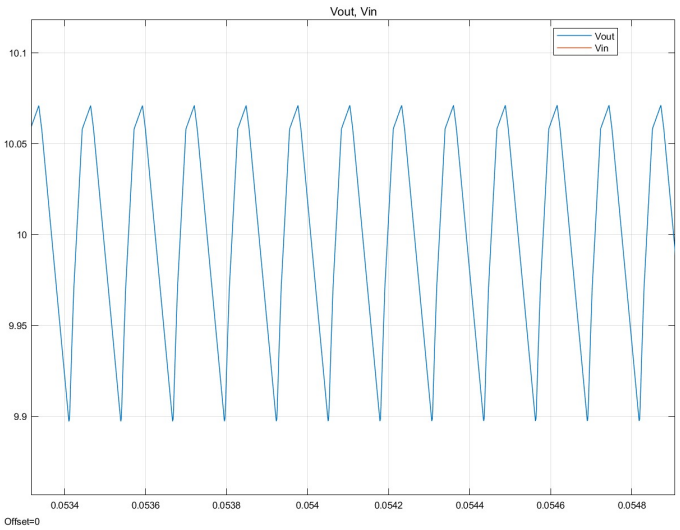

Figure 20: The Output Voltage Ripple(=184mV) When Vin=24V

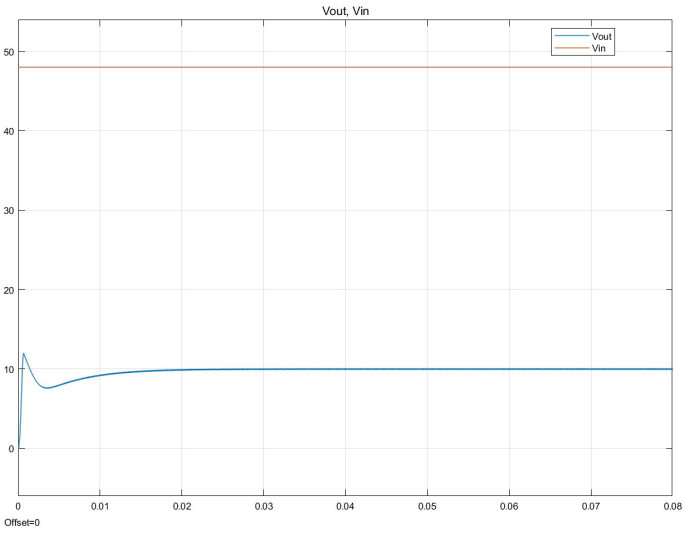

Figure 21: The Input-Output Voltage Graph for 48V input

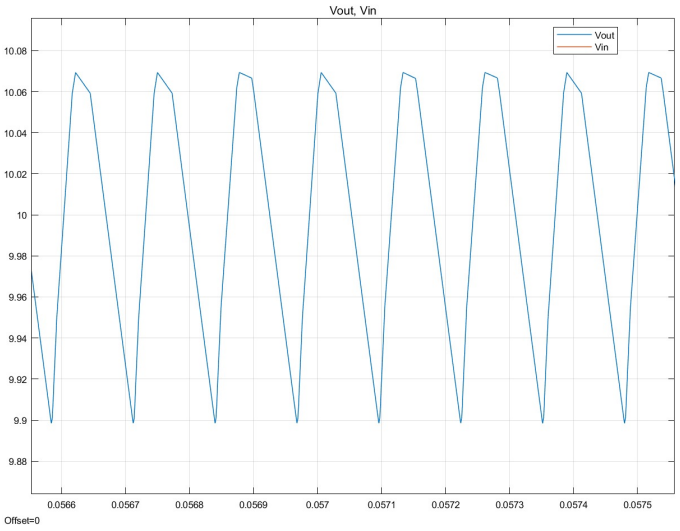

Figure 22: The Output Voltage Ripple(=182mV) When Vin=48V

Part h.

Mosfet Selection

In order to select proper mosfet we looked at drain to source voltage rating and continuous current ratings. As seen Figure 7 at 48 volt imput mosfet voltage has 67 V peak value. Continuous current rating of mosfet is 13 A. From this calculations selected mosfet ratings are shown in Table 1.

Product Code	MTP20N15E
Drain–Source Voltage	150 V (dc)
Drain – Continuous	20 A (dc) / 12 A @ 100°C
Operating and Storage Temperature Range	−55 to 150 °C
Gate–Source Voltage	± 20 V (dc)
Pruduct link	https://www.onsemi.com/pub/Collateral/MTP20N15E-D.PDF

Diode Selection

For the diode selection important parameters are peak inverse voltage and current capability.

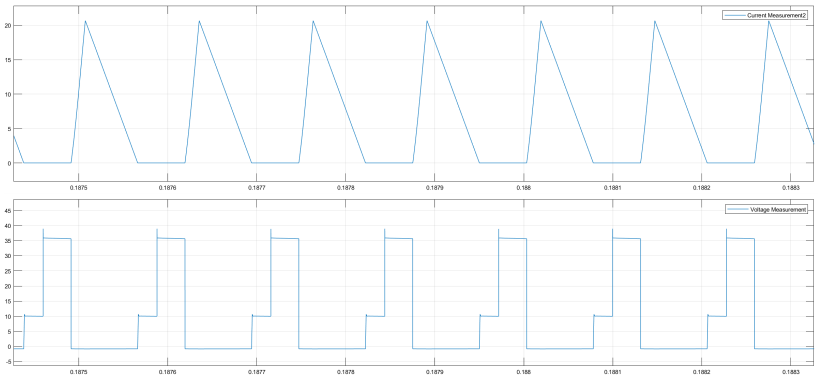

Figure 23: Diode voltage and current ratings

From Figure 23. We found peak inverse voltage as 40 V and continuous current as 22 A. Using these parameters a diode is selected and it's parameters shown in table 2.

Product Code	STPS30M100S
IF(AV)	30 A
VRRM	100 V
Tj (max.)	150 °C
VF (typ.	0.605 V
Product Link	https://www.st.com/content/ccc/resource/technical/document/datasheet/e4/43/ab/35/b9/4b/41/c9/CD00228906.pdf/files/CD00228906.pdf/jcr:content/translations/en.CD00228906.pdf

Filter Capacitor Selection

At the outpu capacitor wer calculated that we need 3 680 uF capacitor. It is also known that our output voltage rating is 10 V. After finding these parameters we selected our capacitor whose parameters is seen at Table 3.

Product code	PEG124MG368AQL1
Capacitance	680 µF
Voltage - Rated	63 V
Ripple Current @ High Frequency	7.5A @ 5kHz
Product Link	https://content.kemet.com/datasheets/KEM_A4011_PEG124.pdf

Snubber Elements

Snubber Capacitor selection

In the simulation we found capacitor voltage and current ratings which are indicated in Figure 24.

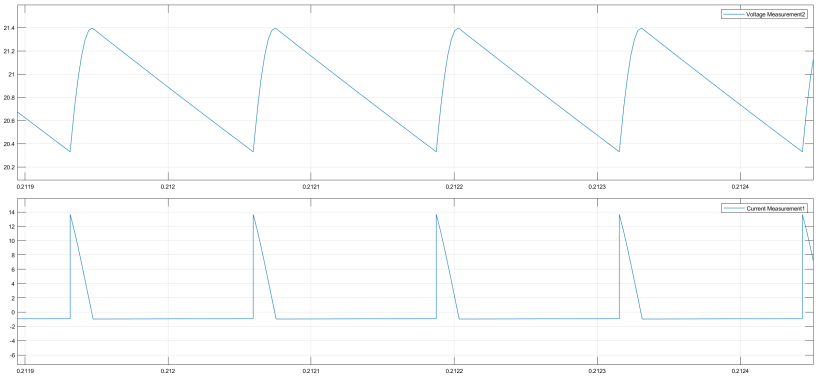

Figure 24: Snubber capacitor voltage and current ratings

After determining these values an aluminum electrolytic capacitor is selected as seen in table 4.

Product code	B41890A7107M
Capacitance	100µF
Voltage - Rated	35V
Product Link	https://www.tdk-electronics.tdk.com/inf/20/30/db/aec/B41890.pdf

Snubber Diode

Similar to snubber capacitor selection by looking at its voltage and current rating a diode is selected. Simulation results are shown in Figure 25.

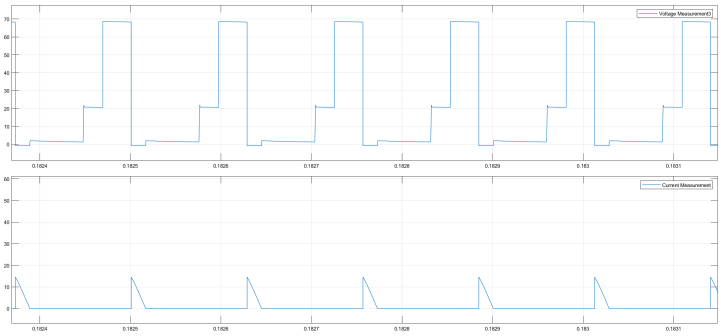

Figure 25: Snubber diode voltage and current ratings

Selected diode and its parameters indicated in Table 5.

Product code	TST40L 150CW
IF(AV)	20 A
VRRM	150 V
Tj (max.)	150 °C
VF (typ.	0.86 V
Product Link	https://www.taiwansemi.com/products/datasheet/TST40L100CW%20SERIES_B14.pdf

Conclusion

This project was a preliminary for hardware project. At first part of the project, we worked with ideal components. Hence, although the output values are at desired levels. The parasitic elements are affected the output values inevitably. For realistic case, we calculated transformer parameters, snubbers and other components' values. At the last part of the project, we selected possible components according to simulation results. Although these components fit for simulations, there can be some unexpected situations at real life implementations. This project was a good exerxice for next stages of hardware project.