CSE 436/536

Digital Integrated Circuits

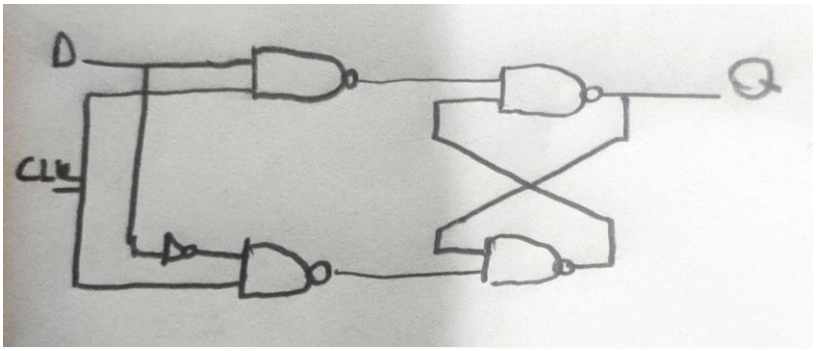
Final Project -VLSI Design of Sequential Square Root

1801042103

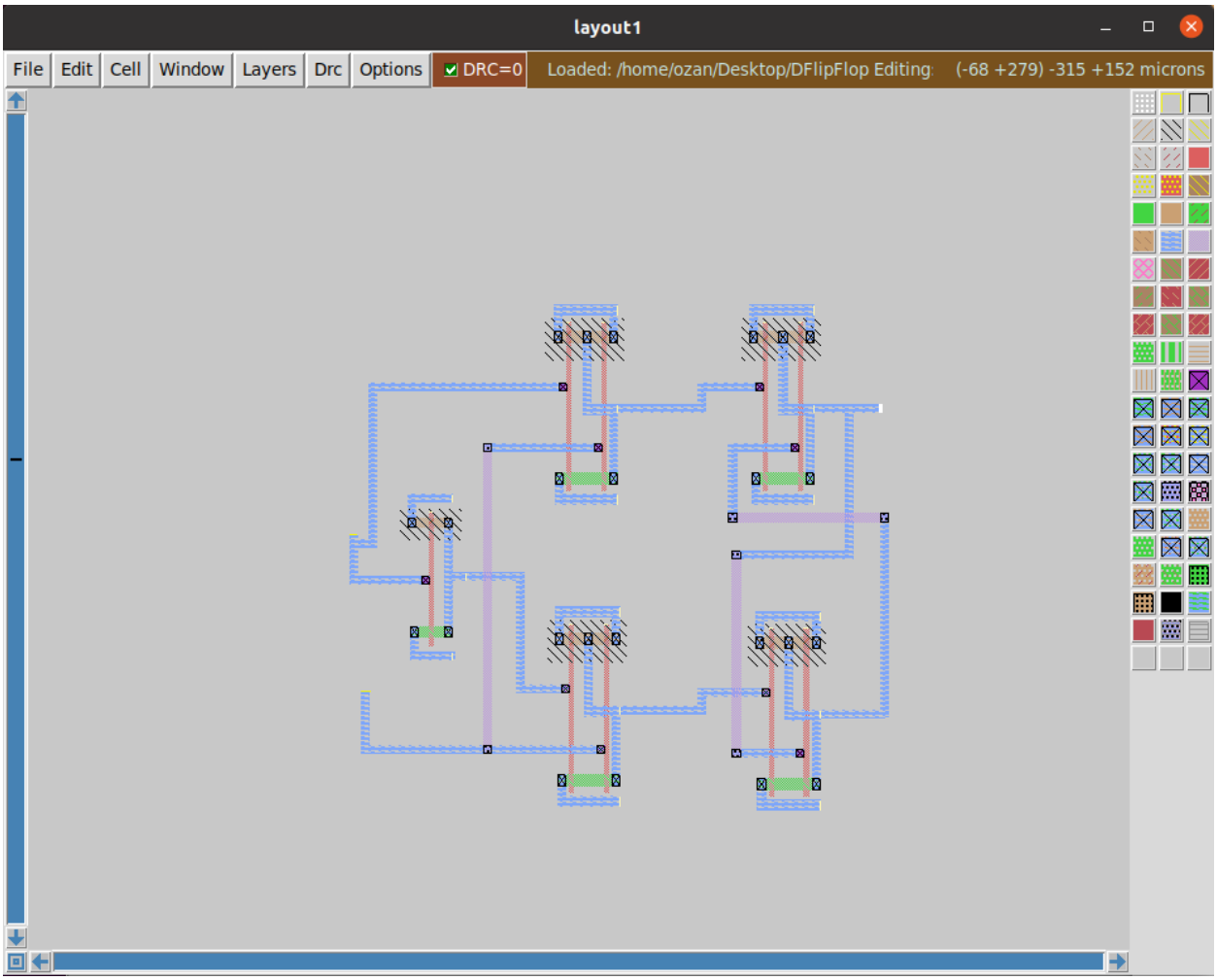
Ozan GEÇKİN

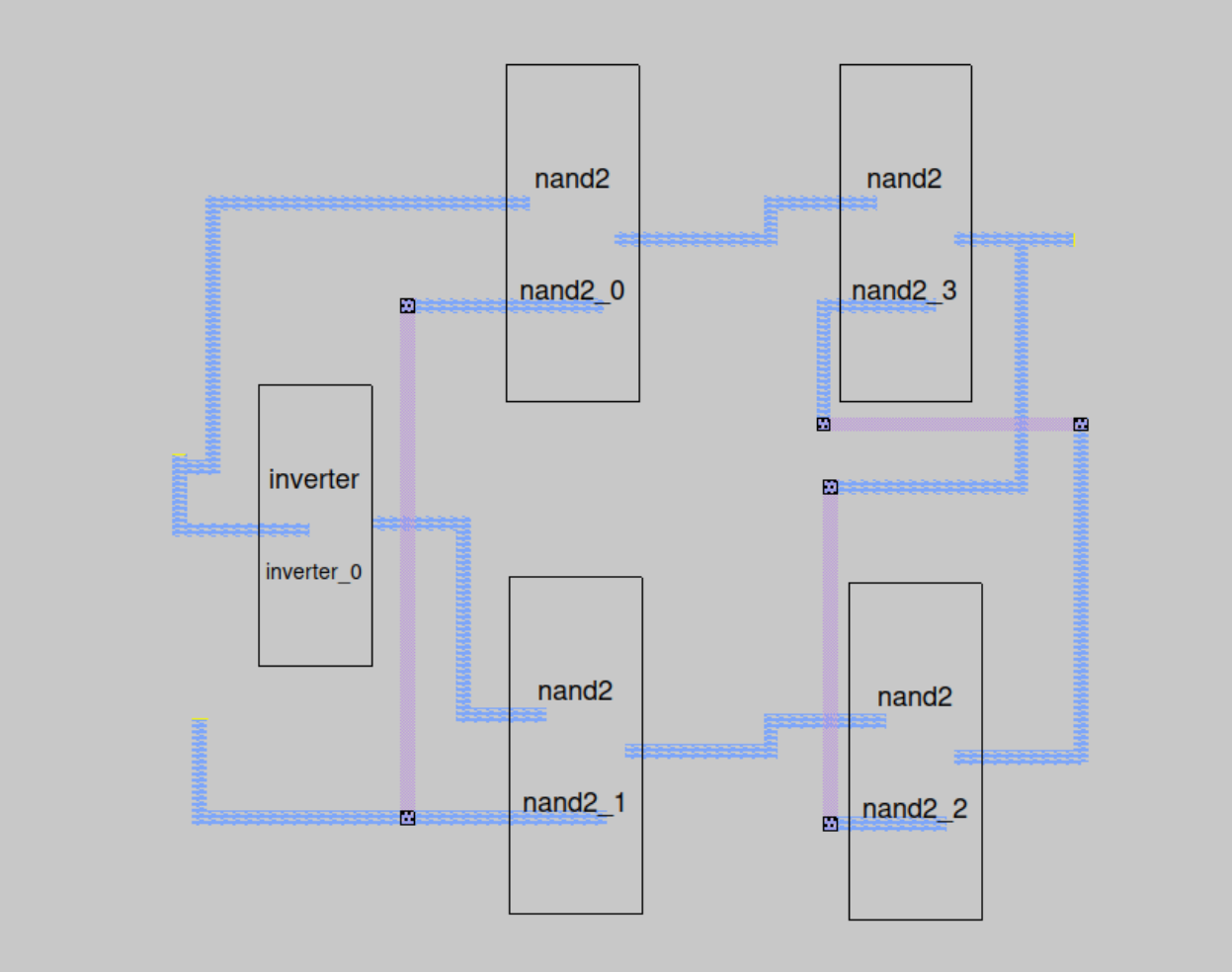
1.In this assignment, using Magic Layout Tool you will design a 0.25um TSMC process standard cell for D flip flop.

First, I made the drawing with the gates.



Then I completed my drawing in magic with 4 NAND2 and 1 inverter by making hierarchy with Magic cell.




nand2
nand2_0
nand2
nand2_3
inverter
inverter_0
nand2
nand2_1
nand2
nand2_2

For Question 2, I could only draw a state diagram.