



Course Name: DIGITL LOGIC DES LAB

Course Number and Section: 14:332:233:01

Experiment: Lab 5 Report

Lab Instructor: ZAHRA AREF

Date Performed: 11/15/24

Date Submitted: 11/15/24

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Course Name: _____

Course Number and Section: 14:332:xxx:xx

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GRADE: _____

COMMENTS:

Lab 5 Prelab:

2.1 SR Latch:

```
always @(s, r)
begin
    if (s == 1'b0 && r == 1'b0)
    begin
        q <= q;
        qbar <= qbar;
    end
    else if (s == 1'b0 && r == 1'b1)
    begin
        q <= 1'b0;
        qbar <= 1'b1;
    end
    else if (s == 1'b1 && r == 1'b0)
    begin
        q <= 1'b1;
        qbar <= 1'b0;
    end
    else if (s == 1'b1 && r == 1'b1)
    begin
        q <= 1'bx;
        qbar <= 1'bx;
    end
end
```

```
end
```

```
end
```

2.1 Testbench:

```
module SR_latch_tb();
```

```
    reg s, r;
```

```
    wire q, qbar;
```

```
    SR_latch uut (.s(s), .r(r), .q(q), .qbar(qbar));
```

```
    initial begin
```

```
        s = 0; r = 0; #10;
```

```
        s = 0; r = 1; #10;
```

```
        s = 1; r = 0; #10;
```

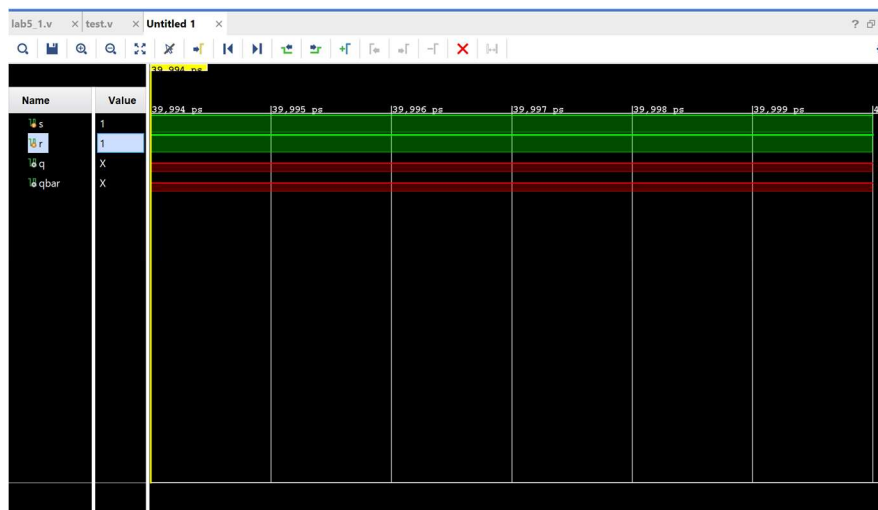
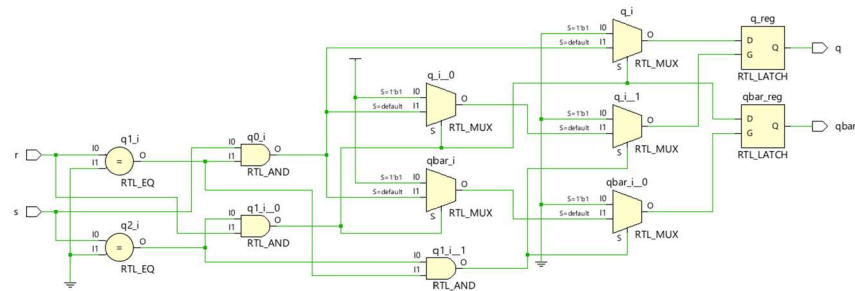
```
        s = 1; r = 1; #10;
```

```
        $finish;
```

```
    end
```

```
endmodule
```

2.1 Schematic & Simulation:



2.2 D Latch:

```
module D_latch(
```

```
    input d,
```

```
    input c,
```

```
    output reg q,
```

```
    output reg qbar
```

```
);
```

```

always @(d or c) begin
    if (c) begin
        q <= d;
        qbar <= ~d;
    end
end
endmodule

```

2.2 Testbench:

```

module lab5_2tb(
);
    reg d;
    reg c;
    wire q;
    wire qbar;

    D_latch D_latch(d,c,q,qbar);

    initial begin
        c = 0; d = 0; #10;
        c = 1; d = 0; #10;
    end
endmodule

```

```
c = 1; d = 1; #10;
```

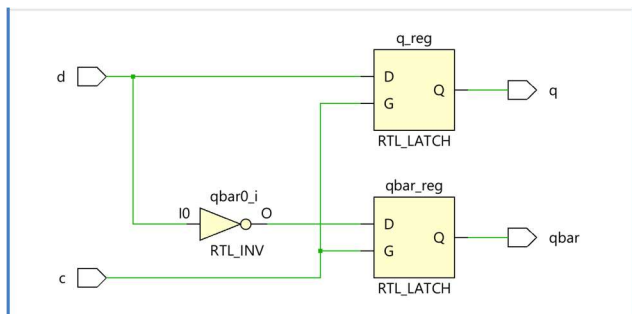
```
c = 0; d = 1; #10;
```

```
$finish;
```

```
end
```

```
endmodule
```

2.2 Schematic & Simulation:



Name	Value	39,596 ps	39,998 ps	40,000 ps
d	1			
c	0			
q	1			
qbar	0			

Lab 5 Report:

