Course Name: DIGITL LOGIC DES LAB

Course Number and Section: **14:332:233:01**

Experiment: Laboratory 3: Combinational MSI Circuits Pre-Lab

Lab Instructor: ZAHRA AREF

Date Performed: 10/18/2024

Date Submitted: 10/18/2024

Submitted by: Chance Reyes 225006531

Course Name: _____

Course Number and Section: **14:332:xxx:xx**

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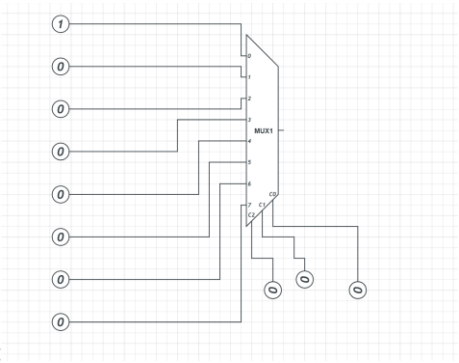
----------For Lab Instructor Use ONLY----------

GRADE: _____

COMMENTS:

1.1 Synthesis and Simulation of a 3-bit Gray Encoder



1.1.1 8-1 Mux Logic diagram:

1.1.2 8-1 Mux Verilog Code:

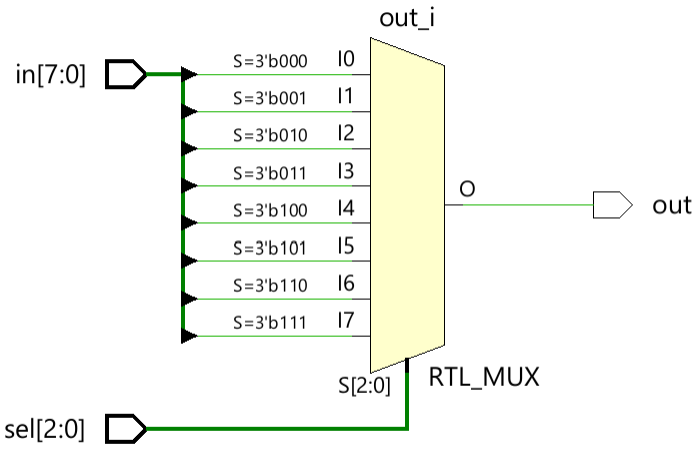
```
`timescale 1ns / 1ps
module mux (
   input [7:0] in,
   input [2:0] sel,
   output reg out
);

always @(*) begin
   case(sel)
      3'b000: out = in[0];
      3'b001: out = in[1];
      3'b010: out = in[2];
      3'b011: out = in[3];
      3'b100: out = in[4];
      3'b101: out = in[5];
      3'b110: out = in[6];
      3'b111: out = in[7];
   endcase
end

endmodule
```

1.1.3 3-bit Gray code encoder:

```
module gray_encoder (
   input [2:0] binary_in,
   output g2,
   output g1,
   output g0
);

   assign g2 = binary_in[2];
```

```
mux mux_g1(
   .in(8'b00001111),
   .sel(binary_in[2:0]),
   .out(g1)
);

mux mux_g0(
   .in(8'b00110110),
   .sel(binary_in[2:0]),
   .out(g0)
);

Endmodule
```

1.1.4 Elaborated Design Schematic:



1.1.5 Timing diagram: