Course Name: DIGITL LOGIC DES LAB

Course Number and Section: **14:332:233:01**

Experiment: Lab 6 Lab Report

Lab Instructor: ZAHRA AREF

Date Performed: 11/26/2024

Date Submitted: 12/6/2024

Submitted by: Chance Reyes 225006531

Course Name: _________________

Course Number and Section: **14:332:xxx:xx**

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GRADE: _______________

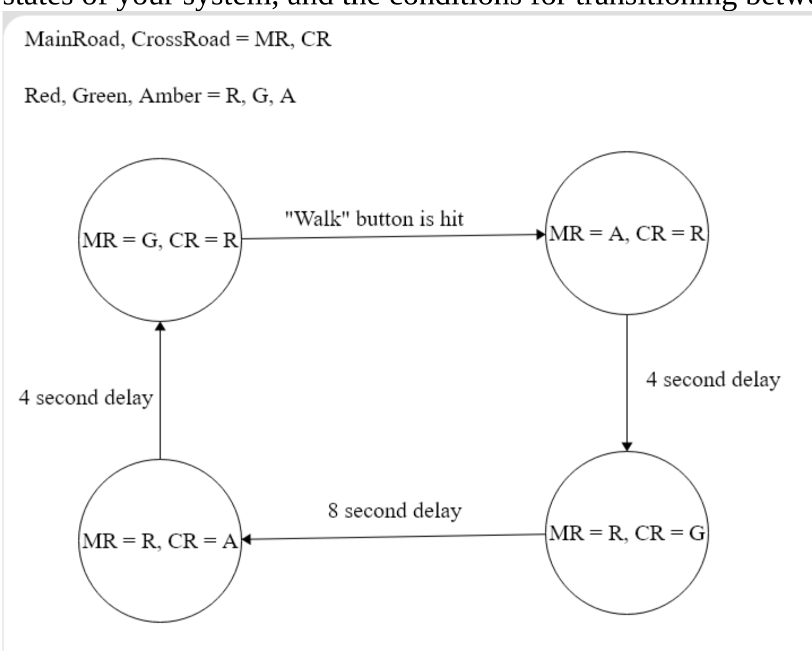
COMMENTS:

Prelab

1- Explain your understanding of the design problem and describe the goal of the experiment in your own words.
The design task is to create a traffic light that prioritizes the main road but switches the lights to allow pedestrians to walk across the crossroad when a button is hit. This system will keep the main road green until the walk button is triggered by a pedestrian. When the button is hit, the main light goes to amber (4 seconds), then the main light and cross light go to red and green, respectively for 8 seconds. Finally, the main light and cross light go back to green and red, respectively. The goal is to let both cars and pedestrians pass in a safe manner by following a specific time sequence of the lights.

2- Describe your own understanding of what a state diagram is, how it is being constructed, and how it generally can help in designing finite state machines.
A state diagram represents a finite state machine. Each element on a diagram represents a unique state of the system and has paths to show how one state transitions to the next. These diagrams are useful for visualizing how a state machine functions and makes designing and debugging them easier.

3- Draw a state diagram for the described traffic signal controller, showing all the discrete states of your system, and the conditions for transitioning between states.



4- Propose a design solution. Provide a preliminary schematic of your proposed circuit. Identify the logic gates needed.

Logic gates needed: 2 Latch IC, 555 Timers, NOT gates

Preliminary Schematic:

https://www.tinkercad.com/things/8feAgVmj9aP-dazzling-uusam-vihelmo/editel?returnTo=https%3A%2F%2Fwww.tinkercad.com%2Fdashboard&sharecode=a887sI95oSM0r5Z8SE4kOujHZWZIISL__Wzcha9CVPY

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Final Schematic:
https://www.tinkercad.com/things/8feAgVmj9aP-dazzling-uusam-vihelmo/editel?returnTo=https%3A%2F%2Fwww.tinkercad.com%2Fdashboard&sharecode=a887sI95oSM0r5Z8SE4kOujHZWZIISL__Wzcha9CVPY

Pictures and videos:
https://drive.google.com/drive/folders/1lusO_MP2NsqWMx20eAYbyxgzdUABeWd0?usp=sharing

Lab Report:
3. We started by drafting a state diagram to map all possible states and transitions based on the given input conditions. This state diagram became the blueprint for designing our traffic signal controller. Next, we selected key components: 555 timers to generate clock pulses, logic gates for state transitions, and flip-flops for state storage. Afterward, we created a basic circuit schematic and simulated it in TinkerCad to ensure functionality.

4. Significant changes were made to our initial design. A major problem was that the 555-timer sent out pulses too quickly. We resolved this by adjusting resistor and capacitor values. Another challenge involved unexpected state transitions, which we traced to an incorrectly placed wire. The most difficult aspect was achieving the desired timing for the yellow light, as it initially turned off too quickly.

5. Various resources were utilized throughout this lab. We referred to datasheets and example circuits for understanding the 555 timer's operation and watched instructional videos to clarify concepts related to state machines and how to implement them using flip-flops.

6. Key lessons included generating precise clock pulses with the 555 timer and constructing state diagrams that clearly illustrated state transitions.

7. The knowledge of 555 timers enabled us to produce a stable clock signal essential for the state machine's operation. Additionally, the state diagram provided a clear framework for implementing the controller's logic.

8. We encountered several wiring issues, including an incorrect connection to one of the flip-flops, which was identified and corrected. Timing inconsistencies between light transitions were resolved by modifying capacitor and resistor values. Loose wires also caused problems, which we addressed by using better-fitting connectors.

9. Despite our fixes, there were still some imperfections. For instance, the yellow light timing remained uneven, with the main road's signal being noticeably shorter. Additionally, overlapping wires in the circuit risked accidental shorts.

10. To mitigate potential power failures, incorporating non-volatile memory could allow the system to store its current state. After power is given to the light, the system could resume from the last known state, ensuring accurate signal displays.

11. I felt inadequately prepared to solve some of the challenges in this lab. The difficulty level was around 9/10, and some helpful hints guiding the process of designing the circuit would have made the process significantly easier. Including hints or guidance in the lab manual would be helpful, as the transition from heavily assisted previous labs to this one felt abrupt and overwhelming.