Course Name: Principles of Electrical Engineering 1 Lab

Course Number and Section: **14:332:223:01**

Experiment: Lab #4

Lab Instructor: Anastasios Kleniatis

Date Performed: 11/11/24

Date Submitted: 12/1/24

Submitted by: Ishaan Mhatre - irm33 Chance Reyes - cr977

Part D

C.3.5 For a binary input 100, what will be the associated output voltage v_o =?

C.3.6 For a binary input 110, what will be the associated output voltage v_o =?

PART D: In Lab Experiments

14:332:223 Principles of Electrical Engineering I Laboratory – Fall 2024

Lab Experiment #4

Date of lab experiment: 11/18/24

Lab section: 01 GROUP (A/B): B

Team members: Ishaan Mhatre

Laboratory instruments:

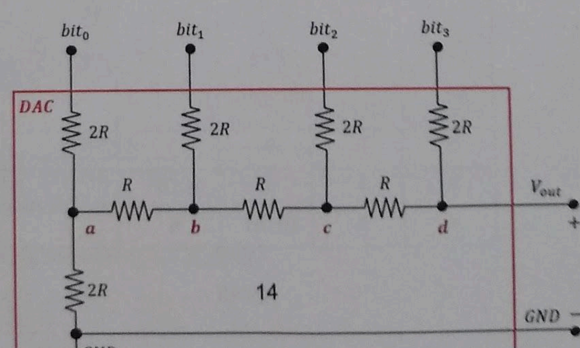
- Power supply: Keithley 2231-30-3
- Digital Multimeter (DMM): Keysight (Agilent) 34461A
- Mixed Domain Oscilloscope: Tektronix MDO3024
- Breadboard/Arduino set
- 1kΩ and higher resistors by design
- 0.01µF and 15µF capacitors
- LM741 op-amp

Experiment # 4.1: Basic DAC Design

Experiment # 4.1: PART A

Wiring Part 1a:

a. Use the circuit in Figure 1 for this experiment:



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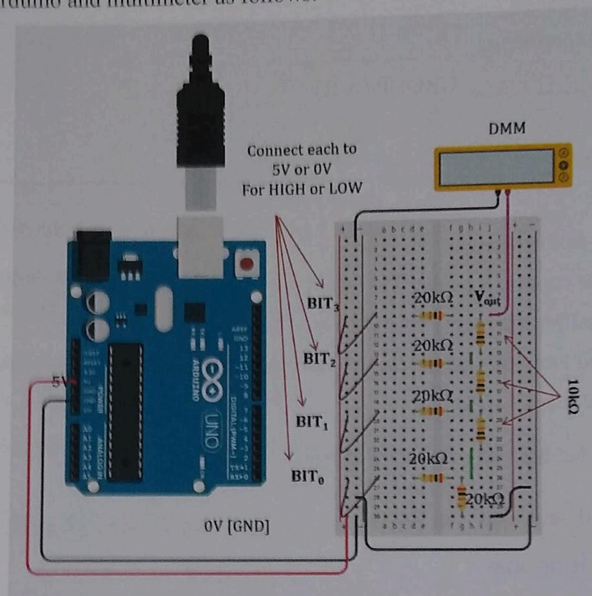
Note: in both experiment we will be using this basic R-2R resistor ladder-based DAC! In the next steps we will only add to this basic circuit

b. Choose for all resistors a value **of R=10kΩ**

c. Connect the Arduino and multimeter as follows:



d. Connect BIT_0 through BIT_3 to either '+' (5V) for HIGH or '-' (0V) for LOW to measure the output voltage for Table 2.

e. **Measurement recording:**

Table 2: implemented 4-bit DAC output voltage measurements

SET Binary Level to:				Decimal Level	Measured Output Voltage v_{out} (volts)
MSB 2^3=8 bit_3		2^1=2 bit_1	LSB $2^0 = 1$ bit_0		
0	0	0	0	0	0
0	0	0	HIGH	1	0.452
0	0	HIGH	0	2	0.689

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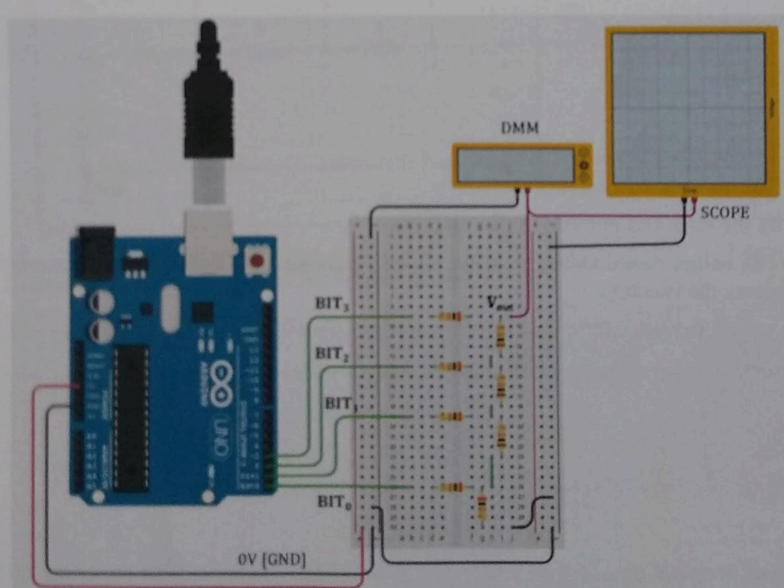
0	HIGH	0	0	4	1.27
0	HIGH	HIGH	0	6	1.96
HIGH	0	0	0	8	2.46
HIGH	0	HIGH	0	10	3.14
HIGH	HIGH	0	0	12	3.72
HIGH	HIGH	HIGH	0	14	4.41
HIGH	HIGH	HIGH	HIGH	15	4.85

Experiment # 4.1: PART B

Wiring Part 1b:

- With the R-2R resistor ladder connected as before, connect the four inputs ($bit_3, bit_2, bit_1, bit_0$) to the Arduino digital IOs as follows:

Arduino	DAC
D0	bit_0
D1	bit_1
D2	bit_2
D3	bit_3



- Connect the DMM and the scope to the DAC output v_{out}.
- Upload the following software to the Arduino.

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Software for Part 1b: you may use the Arduino sketch 'BareMinimum' under File>Examples>01.Basics' as a starting point or upload the file from a memory stick.

```
------------------
void setup(){
// RUNs once: LAB 4-part 1a
// we first need to define D0 to D3 as digital outputs
// DDRD: command that sets Port D Data Direction Register-read/write
// its sets Arduino pins 0 to 7 as outputs
// equivalent to: pinMode(0,OUTPUT);pinMode(1,OUTPUT); …;pinMode(7,OUTPUT);

DDRD = B11111111;
}

void loop() {
// RUNs repeatedly:
// PORTD is the register for the state of the outputs
// ++ increments the value of a variable by 1

PORTD ++;
// Wait for 1000 millisecond(s)

delay(1000);
}
------------------
```

- Verify the code and upload it to the Arduino
- **NOTE:** before downloading the code, please **disconnect D0 and D1**. Once successful, reconnect the two IOs.
- The output voltage will be a sawtooth waveform with values similar to the ones in Table 1.
- **SCOPE**: choose an appropriate time and voltage scales to display the sawtooth waveform.

TA Verification: __________

- Save an image of the scope to be added later to the post lab report (use either the USB port with a memory stick or take a picture of the screen).

  9.04 − (−7.96) = 16 s
- What is the period T of the sawtooth waveform?
  - T = 16 Seconds

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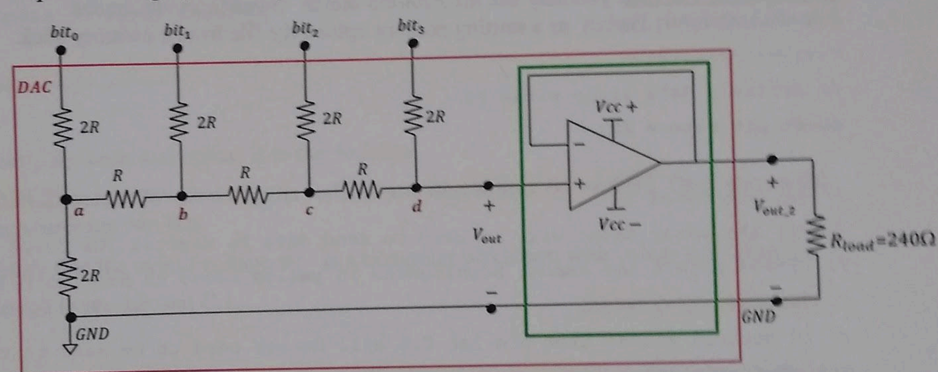
Sawtooth Waveform:

Experiment # 4.2: DAC with a buffer stage and more

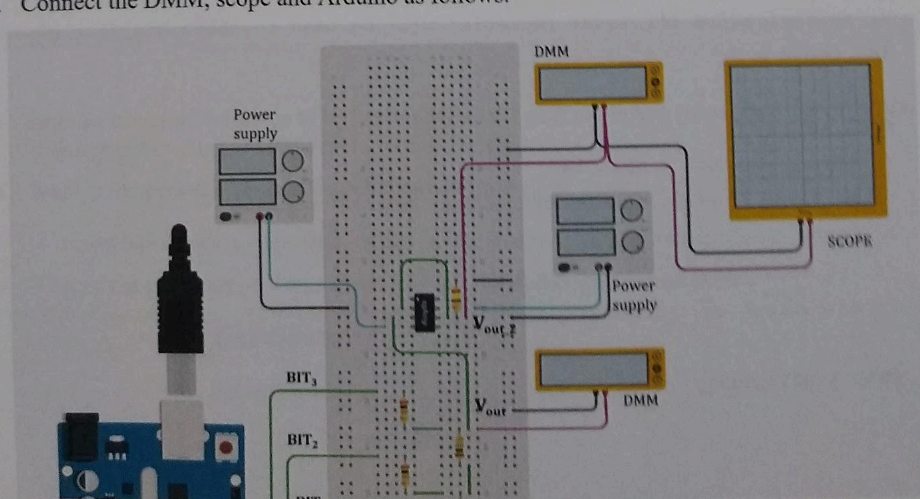
Experiment # 4.2: PART A

Wiring Part 2a:

a. Building on experiment 4.1b, disconnect the Arduino digital IOs D0 and D1 and add the op-amp buffer stage (marked by the green box) as shown in the schematic below:



b. Connect the DMM, scope and Arduino as follows:



- Connect the DMM and the scope to the op-amp output v_{out} and the buffer output v_{out_2}.
- **Use $\pm 15V$ for the op-amp references. Make sure to connect ALL ground points on the breadboard.**
- Based on the pre-lab, use the values you found for the triangular waveform to set the DAC output using the following sketch:

Software for Part 2a: you may use the Arduino sketch 'BareMinimum' under File>Examples>01.Basics' as a starting point or upload the file from a memory stick.

```
-------------------
// Define a data array size= 20
const int size = 20;

// Declare types &
// set the array data: will be used to send data to digital IOs D3-D0
// PLEASE UPDATE the number highlighted in yellow based on pre-lab C.1
// Triangular waveform
// 20 decimal values from pre-lab C.1 will be set here to be sent to the DAC
int mBuffer[size] = { , , , , , , , , , ,
                      , , , , , , , , , };
// initial value for index variable: will be used to read info from mBuffer
int index = 0;

void setup(){
// RUNs once: LAB 4-part 1a
// we first need to define D0 to D3 as digital outputs
// DDRD: command that sets Port D Data Direction Register-read/write
// its sets Arduino pins 0 to 7 as outputs
// equivalent to: pinMode(0,OUTPUT);pinMode(1,OUTPUT); …;pinMode(7,OUTPUT);

DDRD = B11111111;
```

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```
}

void loop() {
// RUNs repeatedly:
// increment index variable: read next value from mBuffer
index = index+1;
// read next value from mBuffer
unsigned char dvolt = mBuffer[index];

// send value (digital data) to PORT D
PORTD = dvolt;

// Wait for 1 millisecond(s)
delay(1);

// Once done going through mBuffer, start again
if (index == size) index=0;
}
------------------
```

- Verify the code and upload it to the Arduino
- **NOTE:** before downloading the code, please **disconnect D0 and D1**. Once successful, reconnect the two IOs.
- Verify that the output voltage v_{out} is a triangular waveform with values similar to the design in pre-lab part C.1.

TA Verification: ________

- Save an image of the scope to be later added to the post lab report (use either the USB port with a memory stick or take a picture of the screen).
- What is the period T of the triangular waveform v_{out_2}?
  - o T = 20 ms

T: 25-5=20

- What is the minimum and maximum voltage of the triangular waveform v_{out_2}?
  - o $v_{out}(maximum)$ = 426 V
  - o $v_{out}(minimum)$ = 0 V

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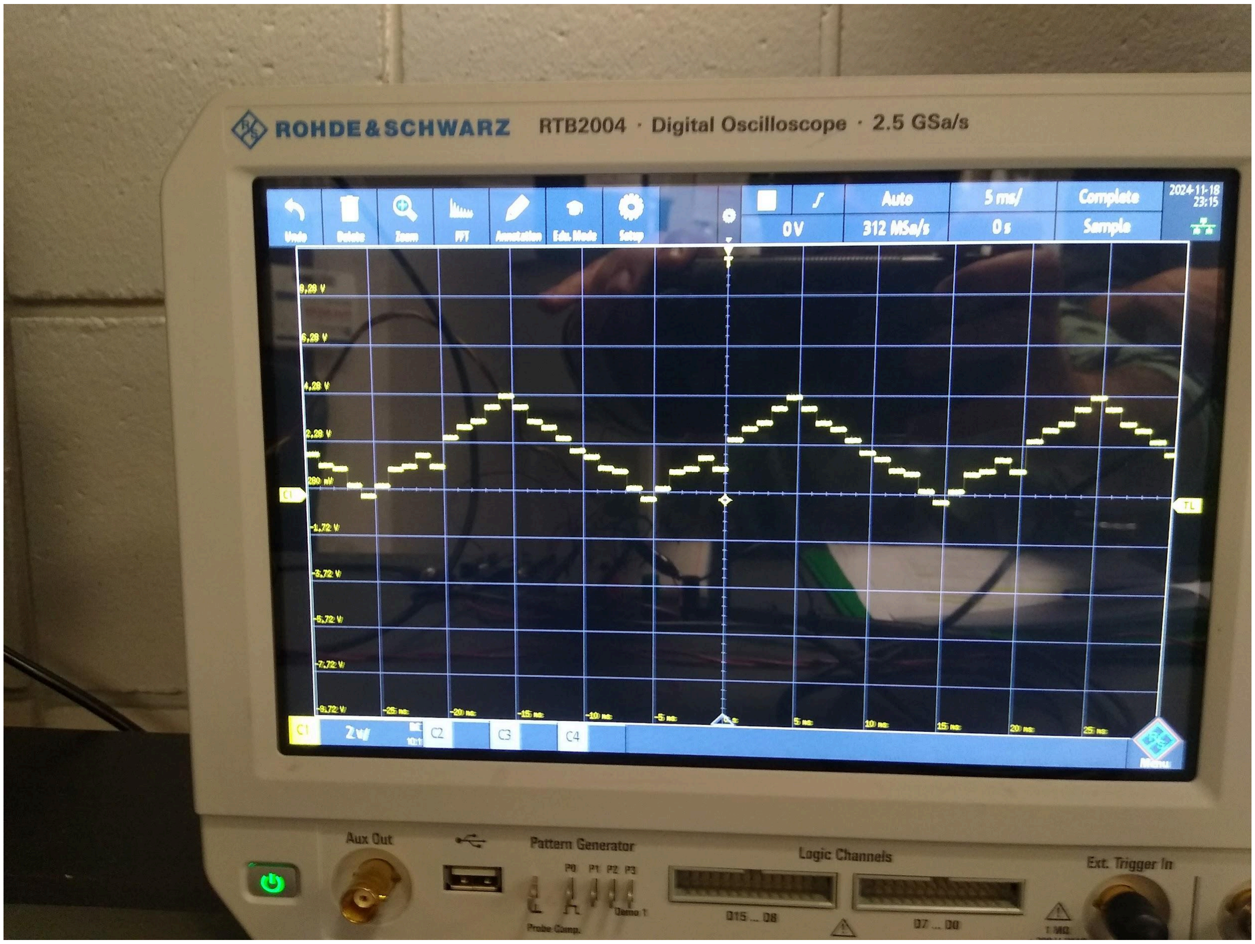
Triangle Waveform:



- Is it also a triangular waveform? Yes

Experiment # 4.2: PART B

Software for Part 2b: update the code in part 2a as follows

```
-----------------
// PLEASE UPDATE the number highlighted in yellow based on pre-lab C.2
// Sinusoidal waveform
// 20 decimal values from pre-lab C.2 will be set here to be sent to the DAC
int mBuffer[size] = { , , , , , , , , , ,
                      , , , , , , , , , };

------------------
```

- Verify the code and upload it to the Arduino
- **NOTE:** before downloading the code, please **disconnect D0 and D1**. Once successful, reconnect the two IOs.
- Verify that the output voltage v_{out} is a sinusoidal waveform with values similar to the design in pre-lab part C.2.
- Save an image of the scope to be added later to the post lab report (use either the USB port with a memory stick or take a picture of the screen).
- What is the period T of the sinusoidal waveform v_{out_2}?
    - $T =$ 20 ms   5 + (15) = 20 ms
- What is the minimum and maximum voltage of the sinusoidal waveform v_{out_2}?
    - $v_{out}(maximum) =$ 3.76
    - $v_{out}(minimum) =$ 0
    - Is it also a sinusoidal waveform? Yes

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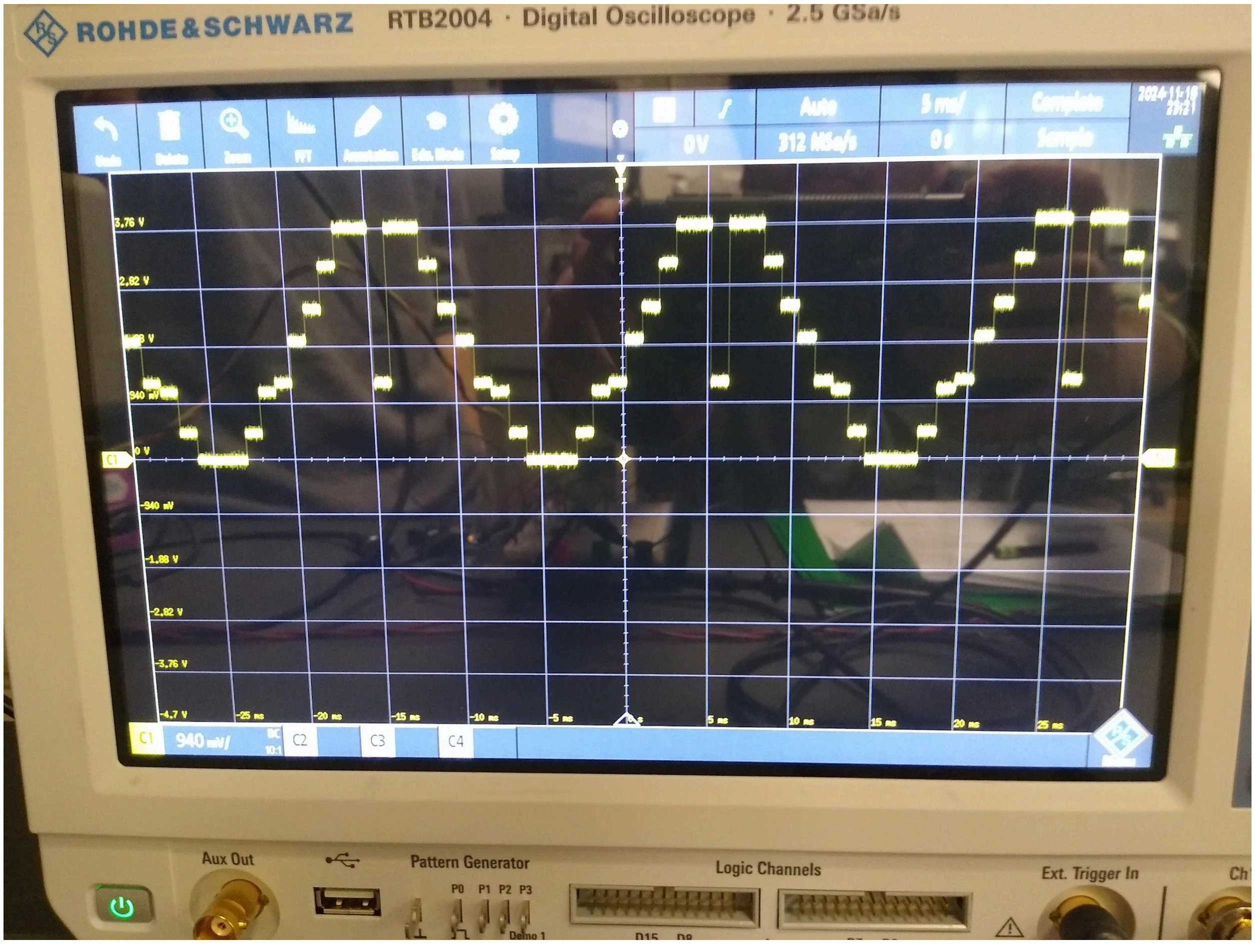
Sinusoidal Waveform

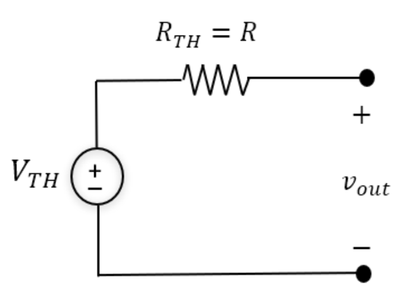


PART E: Post-Lab Report

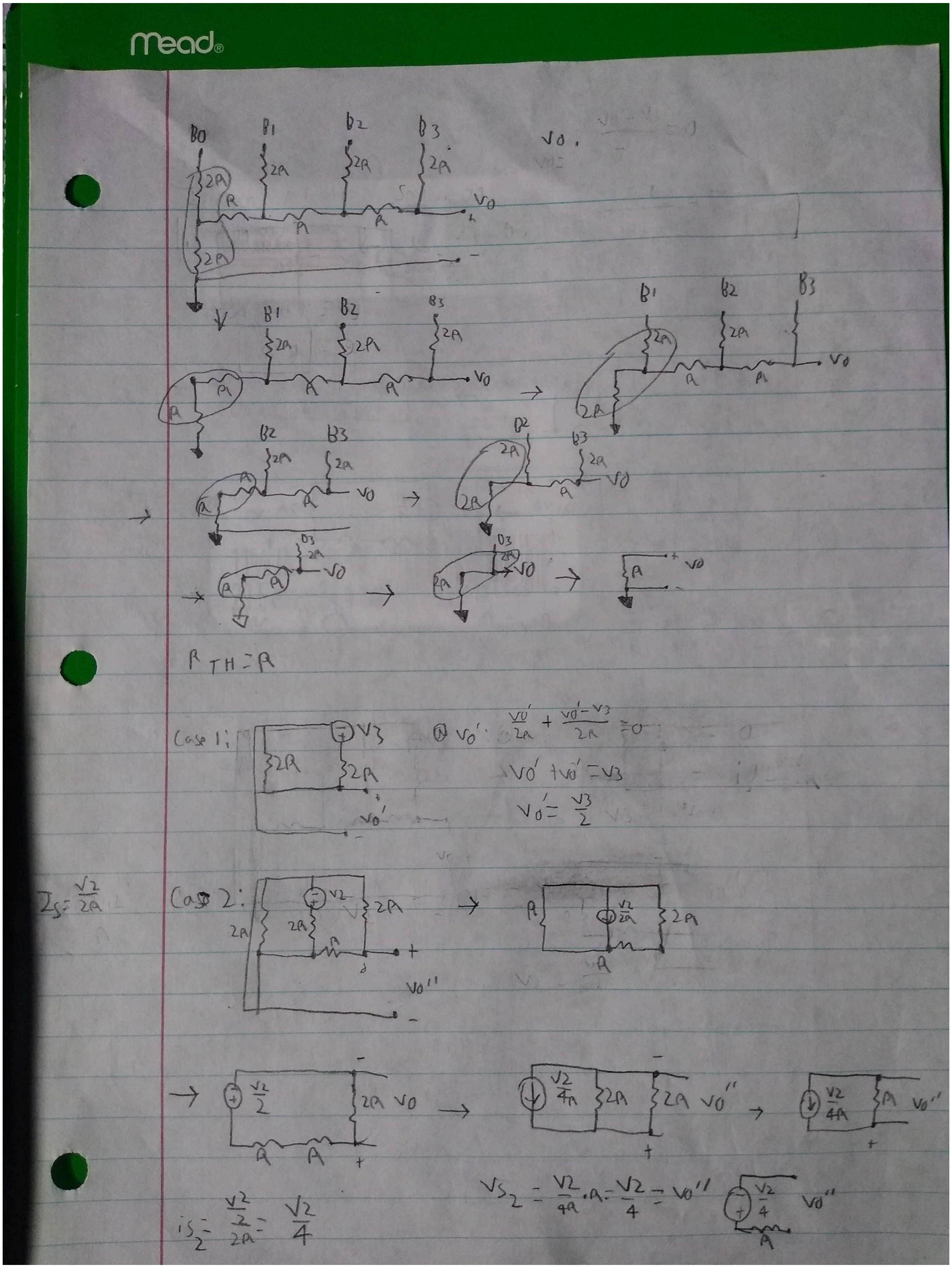
The lab report should include a filled and signed copy of part D and analysis of the data based on the following questions and required simulation.

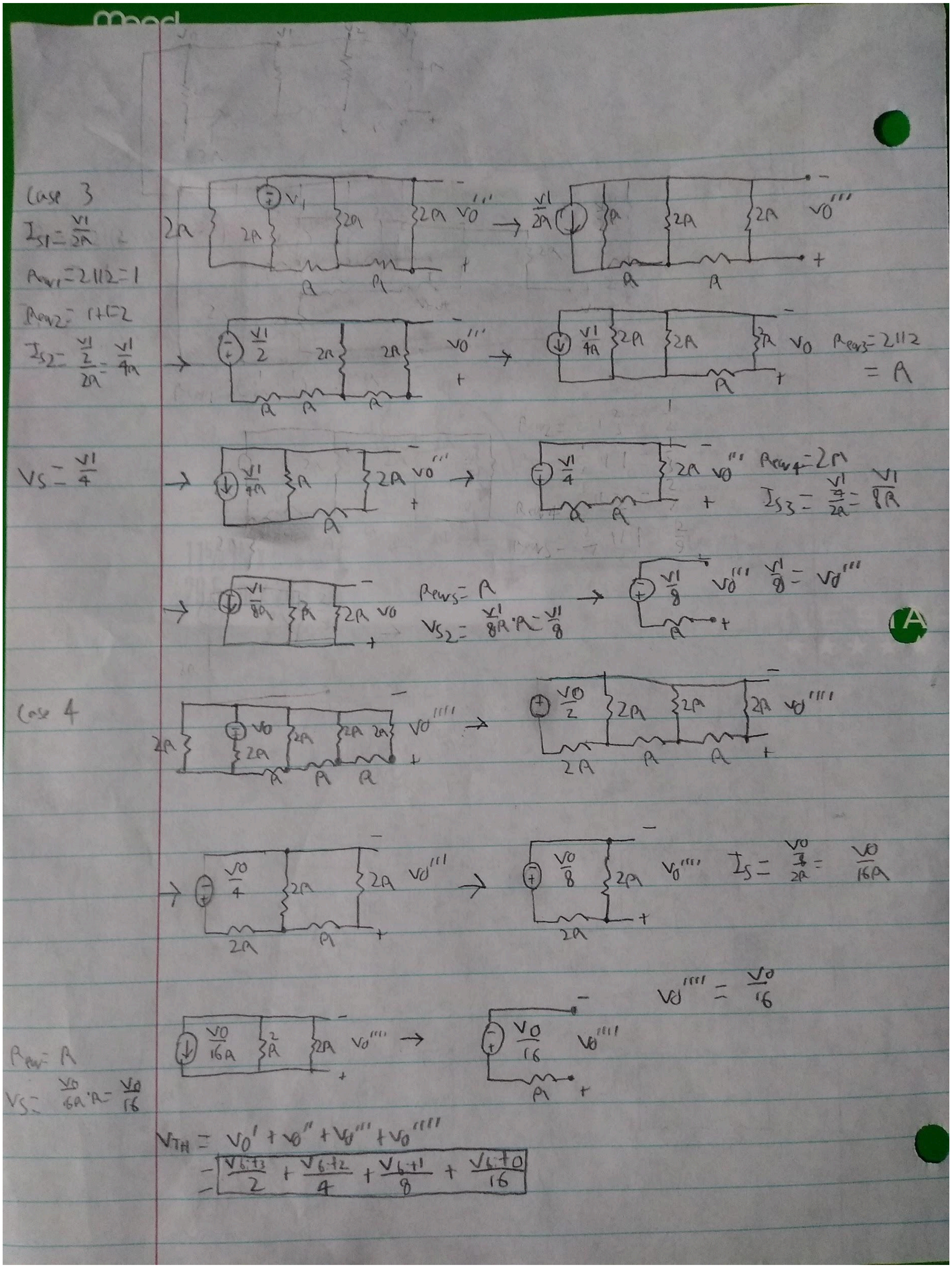
1. Verifying theory:

a. Use superposition and source transformation to show that the Thevenin equivalent for the DAC in Figure 1 is:

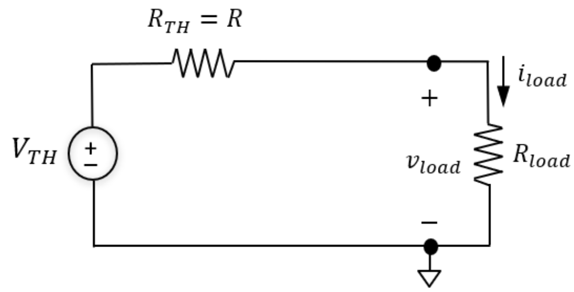


$$V_{TH} = \frac{v_{bit3}}{2} + \frac{v_{bit2}}{4} + \frac{v_{bit1}}{8} + \frac{v_{bit0}}{16}$$


Mead
B0
B1
B2
B3
2R
R
Vo
R TH = R
Case 1:
V3
2R
Vo'
@ Vo': Vo'/2R + (Vo' − V3)/2R = 0
Vo' + Vo' = V3
Vo' = V3/2
Is = V2/2R
Case 2:
V2
Vo''
V2/2
V2/4R
V2/4R
Vs2 = V2/4R · R = V2/4 = Vo''
is2 = (V2/2)/2R = V2/4


Case 3
Is1 = V1/2R
Reqv1 = 2R‖2R = R
Reqv2 = R+R = 2R
Is2 = (V1/2)/2R = V1/4R
Reqv3 = 2R‖2R = R
Vs = V1/4
Reqv4 = 2R
Is3 = (V1/4)/2R = V1/8R
Reqv5 = R
Vs2 = V1/8R · R = V1/8
V1/8 = Vo'''
Case 4
Is = (Vo/8)/2R = Vo/16R
Vo'''' = Vo/16
Req = R
Vs = Vo/16R · R = Vo/16
VTH = Vo' + Vo'' + Vo''' + Vo''''
= V6:t3/2 + V6:t2/4 + V6:t1/8 + V6:t0/16

b. Using the Thevenin equivalent for the DAC in Figure 1, find the voltage drop across the load connected to the DAC output, v_{load} as a function of the D0-D3 voltage levels, R and the load resistance

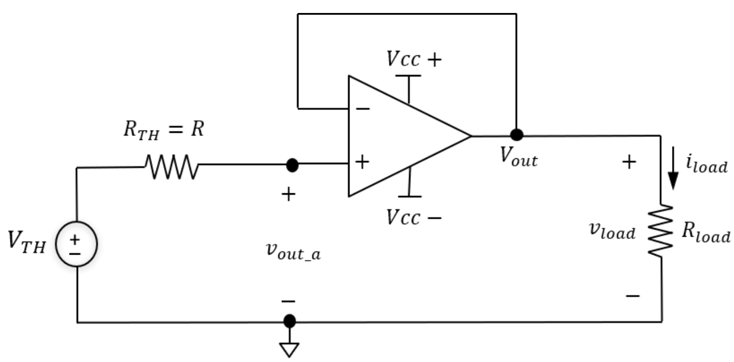


$$V_{TH} = \frac{v_{bit3}}{2} + \frac{v_{bit2}}{4} + \frac{v_{bit1}}{8} + \frac{v_{bit0}}{16}$$

$$\mathbf{v_{load}} = \frac{V_{TH} R_{load}}{R + R_{load}}$$

$$\mathbf{v_{load}} = \left[\frac{v_{bit3}}{2} + \frac{v_{bit2}}{4} + \frac{v_{bit1}}{8} + \frac{v_{bit0}}{16}\right] * \left(\frac{R_{load}}{R + R_{load}}\right)$$

c. Using the Thevenin equivalent for the DAC with a buffer in Figure 2, find the voltage drop across the load connected to the DAC output, v_{load} as a function of the D0-D3 voltage levels, R and the load resistance



$$V_{TH} = \frac{v_{bit3}}{2} + \frac{v_{bit2}}{4} + \frac{v_{bit1}}{8} + \frac{v_{bit0}}{16}$$

Due to the characteristics of an ideal op-amp, $V_p = V_{Th} = V_n$. Since there is no feedback resistor, $V_{out} = V_n$, and since the load resistor is connected directly to V_{out} and ground $v_{load} = V_{out} = V_{TH}$

Thus: $\mathbf{v_{load}} = \frac{v_{bit3}}{2} + \frac{v_{bit2}}{4} + \frac{v_{bit1}}{8} + \frac{v_{bit0}}{16}$

2 **Analysis for experiment 4.1** (*show all work for calculations and explain the experimental results versus calculated ones in each of the relevant sections*):

2.1 Compare the values measured for v_{out} in Table 2 with the expected values in Table 1. How do they compare? explain.

Decimal level	$V_{expected}$	$V_{measured}$
0	0	0
1	0.3125	0.452
2	0.625	0.689
4	1.25	1.27
6	1.875	1.96
8	2.5	2.46
10	3.125	3.14
12	3.75	3.72
14	4.375	4.41
15	4.6875	4.85

Most of the values are close to the expected results except for decimal 1, which has a much higher voltage than the expected value. All other measured values are within a tolerance range of ± 5%. The measured values with bit 3 (like decimal levels 8 and 12) appear to be generally lower than the expected voltage, so the resistor used for bit 3 likely has a higher resistance than the listed value. In contrast, measured values for decimals using all other bits are generally higher than expected, so these resistors likely have a lower resistance than the listed value. Decimal levels that use bit 1 especially have a large difference in the expected voltage versus the measured value, with the maximum difference being 0.1395 V for decimal value 1, so the resistor used in bit 1 might have a resistance even lower than the listed 5% tolerance, since the maximum value for the voltage of decimal 1 should be about 0.328 V.

2.2 The digital IOs of an Arduino have an output current of 40mA. How much power can it deliver at an output voltage of 5V?

P = I*V = 0.04 * 5 = **0.2 W**

2.3 For the DAC, connected to 4 IOs, what is the maximum power that the Arduino can deliver to the DAC?

4 IOs * 40 mA = 160 mA

P = I*V = 0.160*5 = **0.8 W**

2.4 What will determine how much power the DAC **without a buffer** can deliver to the load (Hint: use the Thevenin equivalent)?

V = IR

I = $\frac{V}{R}$

P = IV = $\frac{Vth^2}{Rth}$

2.5 What will be the maximum current the DAC **without a buffer** can deliver at the output (Hint: use the Thevenin equivalent) and how does it relate to the short circuit current for the DAC?

V = IR

$$\mathbf{I} = \frac{Vth}{Rth} = \frac{\frac{5}{2}+\frac{5}{4}+\frac{5}{8}+\frac{5}{16}}{10000} = \mathbf{0.47mA}$$

The maximum current is also the short circuit current, since the maximum current is reached with the smallest load.

3 **Analysis for experiment 4.2** (*show all work for calculations and explain the experimental results versus calculated ones in each of the relevant sections*):

3.1 Output short circuit current information for the LM 741 op-amp determines the maximum current the op-amp can source or sink at the output pin (typically 25mA).

6.5 Electrical Characteristics, LM741 (1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage	$R_S \le 10$ kΩ	T_A = 25°C		1	5	mV
		$T_{AMIN} \le T_A \le T_{AMAX}$			6	mV
Input offset voltage adjustment range	T_A = 25°C, V_S = ±20 V			±15		mV
Input offset current	T_A = 25°C			20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			85	500	
Input bias current	T_A = 25°C			80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$				1.5	µA
Input resistance	T_A = 25°C, V_S = ±20 V		0.3	2		MΩ
Input voltage range	$T_{AMIN} \le T_A \le T_{AMAX}$		±12	±13		V
Large signal voltage gain	V_S = ±15 V, V_O = ±10 V, $R_L \ge 2$ kΩ	T_A = 25°C	50	200		V/mV
		$T_{AMIN} \le T_A \le T_{AMAX}$	25			
Output voltage swing	V_S = ±15 V	$R_L \ge 10$ kΩ	±12	±14		V
		$R_L \ge 2$ kΩ	±10	±13		
Output short circuit current	T_A = 25°C			25		mA
Common-mode rejection ratio	$R_S \le 10$ Ω, V_{CM} = ±12 V, $T_{AMIN} \le T_A \le T_{AMAX}$		80	95		dB
Supply voltage rejection ratio	V_S = ±20 V to V_S = ±5 V, $R_S \le 10$ Ω, $T_{AMIN} \le T_A \le T_{AMAX}$		86	96		dB
Transient response: Rise time	T_A = 25°C, unity gain			0.3		µs
Transient response: Overshoot				5%		
Slew rate	T_A = 25°C, unity gain			0.5		V/µs
Supply current	T_A = 25°C			1.7	2.8	mA
Power consumption	V_S = ±15 V	T_A = 25°C		50	85	mW
		$T_A = T_{AMIN}$		60	100	
		$T_A = T_{AMAX}$		45	75	

A

a. What will determine how much power the DAC **with** a buffer can deliver to the load?

The short circuit current of the op-Amp and the resistance of the load itself will determine how much power the DAC with buffer can deliver to the load, since the speaker is connected in series with the load resistor.

b. What is the maximum power that will be delivered to the speaker?

$P_{max} = I_{sc}^2 * R_{speaker}$

$P_{max} = (25\ mA)^2 * 8\ \Omega$

$\mathbf{P_{max} = 0.005\ W = 5\ mW}$

Assuming we use the **DAC without the buffer** to feed the speaker:

c. What would be the maximum power delivered to the speaker (assuming an equivalent resistance of 8Ω)?

The maximum power delivered without the buffer can be found by using a voltage divider to find the maximum voltage across the speaker, then using the power formula in terms of voltage and resistance.

$V_{speaker} = V_{THmax} \frac{R_{speaker}}{R_{EQ}}$

$V_{speaker} = 4.6785\left(\frac{8\Omega}{8\Omega + 20{,}000\Omega}\right) = 0.00187\ V = 1.87\ mV$

$P_{max} = \frac{(V_{speaker})^2}{R_{speaker}}$

$\mathbf{P_{max}} = \frac{1.87\ mV^2}{8\Omega} = 4.37 * 10^{-7} W = \mathbf{4.37 * 10^{-4}\ mW}$

d. What will you need to change in the DAC design in order to deliver more power to the speaker?

In order to deliver more power to the speaker, resistors of smaller values should be used in the DAC so that more power is dissipated by the speaker rather than the resistors of the DAC itself.

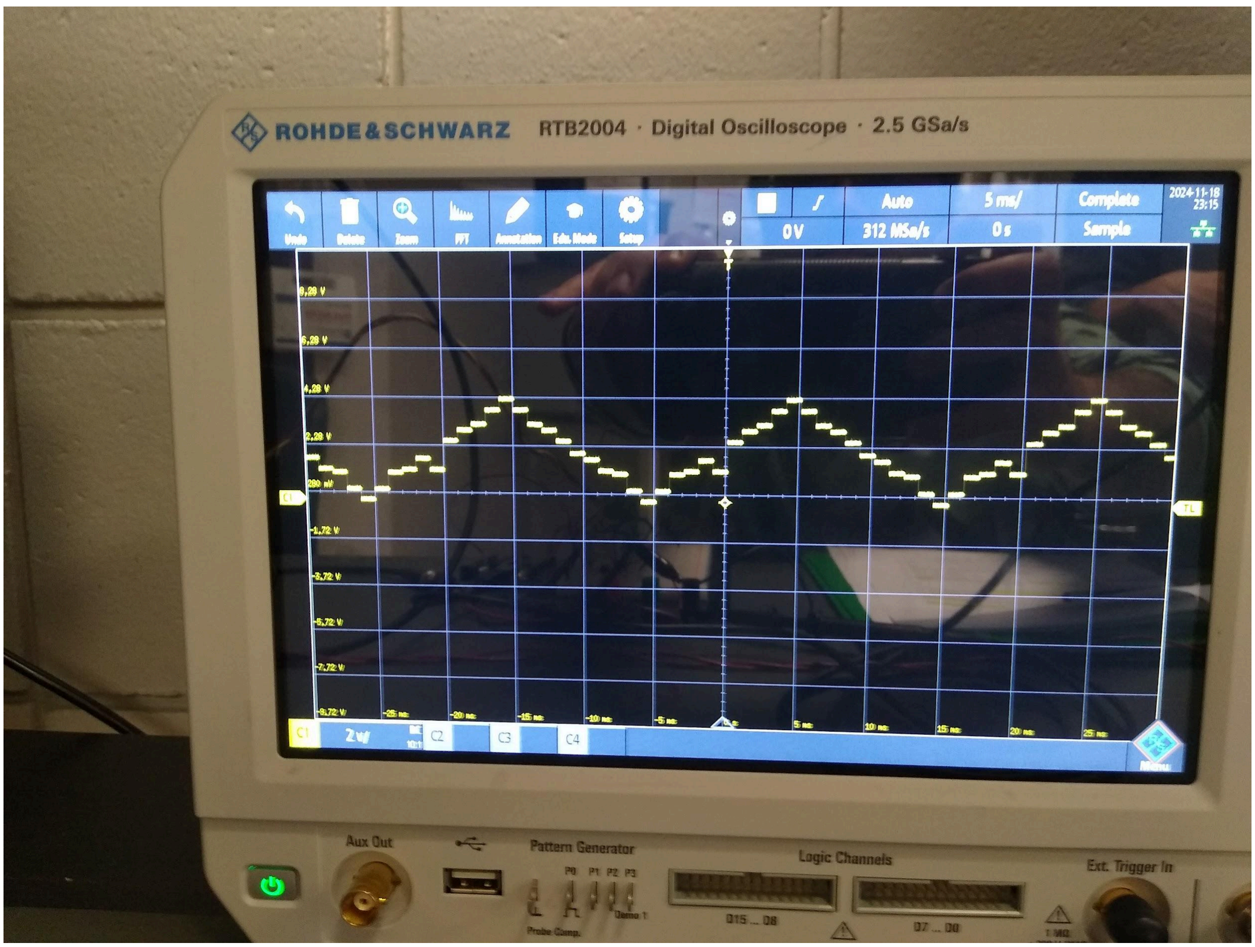
e. How will the digital IOs output current limit this design?

Since the resistors will have a much greater value than the input voltage, the output current of a digital IO will likely be very small, meaning that there would likely be few, if any, combinations that could provide enough power to drive the speaker in the first place.

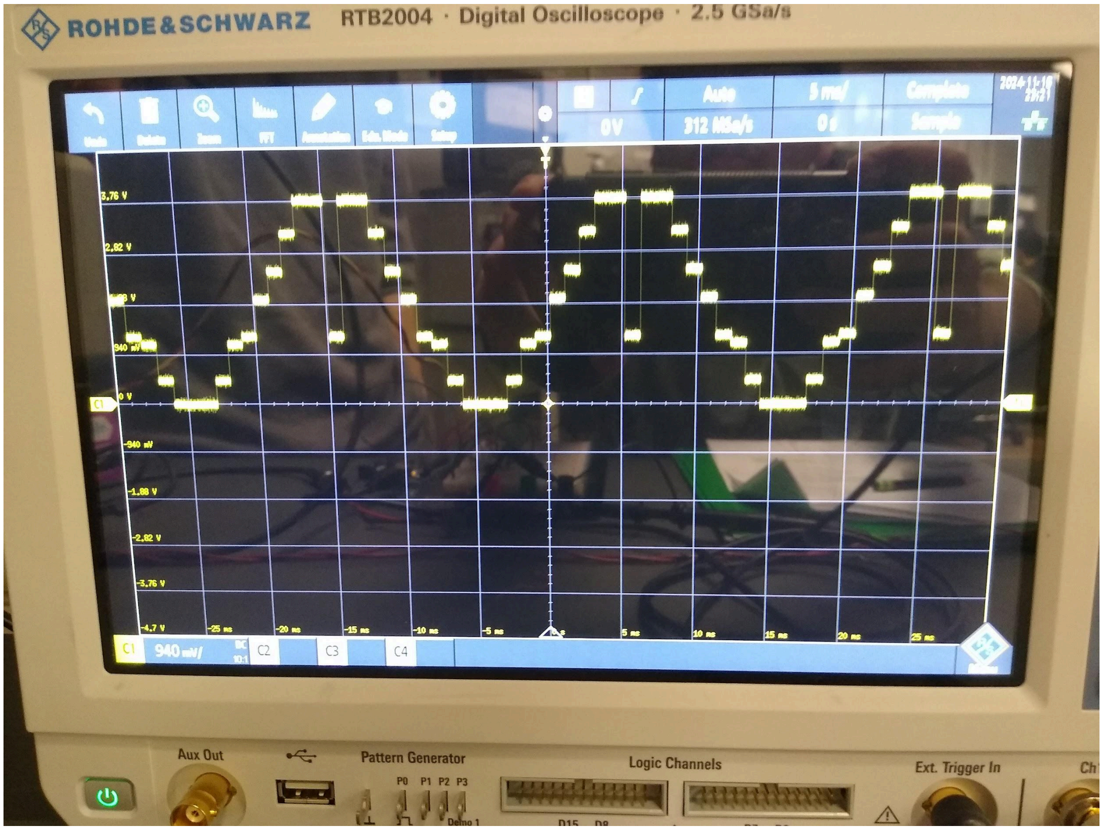
3.2 Evaluate the output of the DAC with the op-amp (buffer) for the triangular and sinusoidal signals. Include images of the actual waveforms

The output of the DAC with the buffer was very close to the expected results from the prelab materials for both the triangular and sinusoidal signals. While our waveforms created a triangular and sinusoidal signal for parts a and b respectively, the waveform for the triangular signal appeared cleaner as the sinusoidal signal went down to 0 instead of reaching the maximum value. While the values for the minimum were equal to the prelab, our maximum values slightly deviated from what was expected. For the triangular waveform that max voltage was expected to be around 4.0625, but ours was 4.26 V. However, this is still within the maximum voltage when accounting for the 5% tolerance of the resistors, which is 4.265 V. The sinusoidal waveform was expected to have the same maximum voltage, but the max voltage we measured was 3.76 V, which is outside of the minimum voltage even accounting for resistor tolerance, as that was found to be 3.859 V. Due to the irregularity in the measured sinusoidal waveform near each crest, this error was likely due to an error in the code inputted to the arduino.

Waveform for 2a:



Waveform for 2b:



3.3 What is the period (T) and the frequency (f) for the periodic function in part 2a and 2b when the delay command in the software was set to1ms?

2a: T = 20 ms; f = $\frac{1}{T} = \frac{1}{20\ ms} = 50\ Hz$

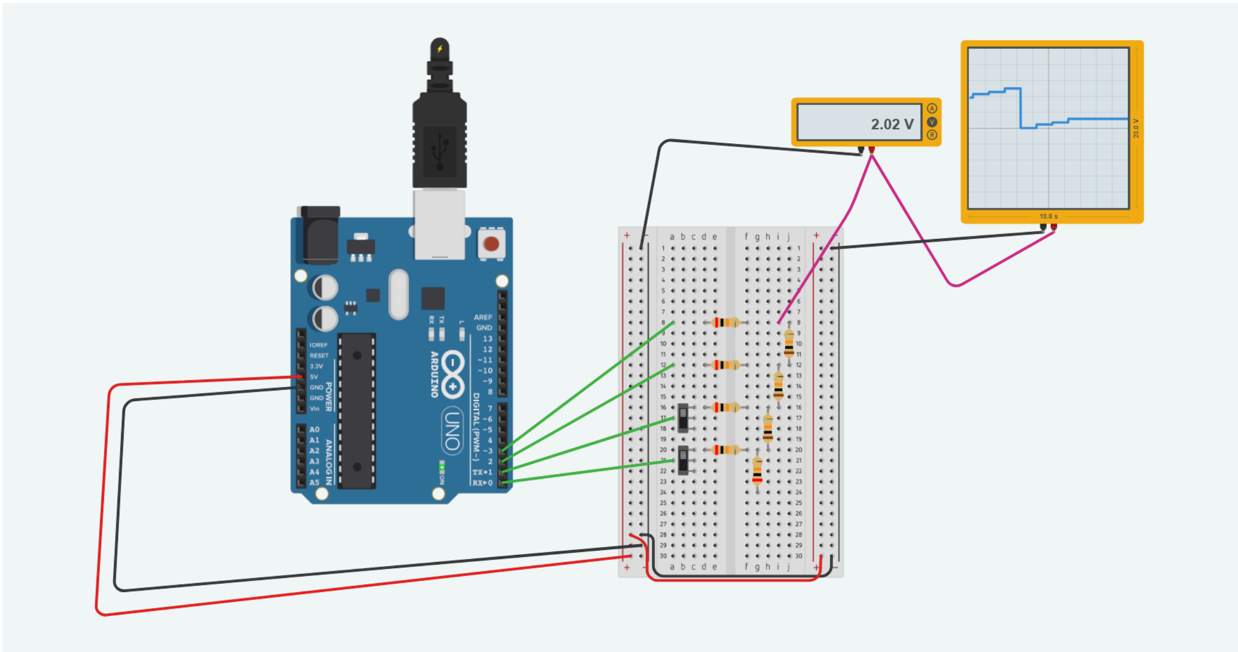
2b: T = 20 ms; f = $\frac{1}{T} = \frac{1}{20\ ms} = 50\ Hz$

Both of these values are identical to the period and frequency that were assumed in the prelab.

4 Simulation:

4.1 Simulate the networks used for experiment 4.1 and experiment 4.2 using TinkerCAD.

4.1 Circuit: Uses code from 1b (sawtooth wave) for the arduino, shows correct waveform if pin 0 and 1 are disconnected



4.2 Circuit: Uses code from 2a (triangle wave) for the arduino, shows correct waveform if pin 0 and 1 are disconnected