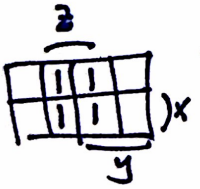
Name: ID#:

Question 1:[20pts] Design a combinational circuit with an input of a 3-bit binary number: $(xyz)_2$. The output is also a binary number that should be equal to 3 times the input. Design the circuit using NAND gates only. Completed (primed) variables are available.

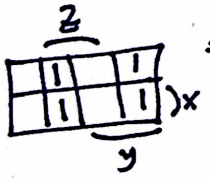
x y z	a_4 a_3 a_2 a_1 a_0
0 0 0	0 0 0 0 0
0 0 1	0 0 0 1 1
0 1 0	0 0 1 1 0
0 1 1	0 1 0 0 1
1 0 0	0 1 1 0 0
1 0 1	0 1 1 1 1
1 1 0	1 0 0 1 0
1 1 1	1 0 1 0 1

a_0:

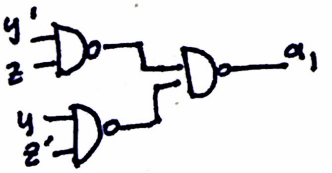


$\Rightarrow a_0 = z$

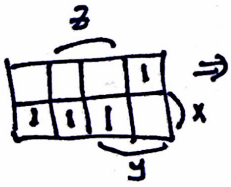
a_1:



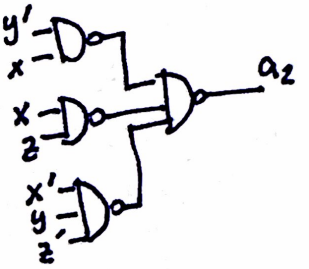
$\Rightarrow a_1 = y'z + yz'$ →



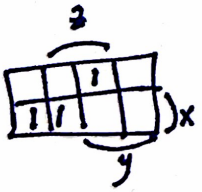
a_2:



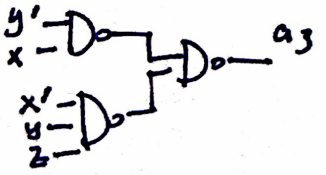
$\Rightarrow a_2 = xy' + xz + x'yz'$



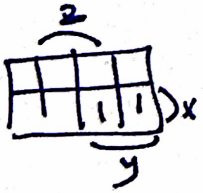
a_3:



$\Rightarrow a_3 = xy' + x'yz$



a_4:



$\Rightarrow a_4 = xy$ →

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Question 2:[30pts] Given a new flip flop (called XY-FF), with the following operational characteristics,

X	Y	Q(t+1)
0	0	0
0	1	0
1	0	Q'(t)
1	1	1

Using one XY-FF, design a RS-FF, using a minimum number of logic gates, complements of variables are available.

Char. table of RS-FF:

R	S	Q(t+1)
0	0	Q(t)
0	1	1
1	0	0
1	1	–

Excitation table of XY-FF

Q(t)	Q(t+1)	X	Y
0	0	0	X
0	1	1	X
1	0	*	*
1	1	1	1

→ {10, 00, 01} or {X0, 0X}

Circuit excitation table:

R	S	Q(t)	Q(t+1)	X	Y
0	0	0	0	0	X
0	0	1	1	1	1
0	1	0	1	1	X
0	1	1	1	1	1
1	0	0	0	0	X
1	0	1	0	*	*
1	1	0	–	X	X
1	1	1	–	X	X

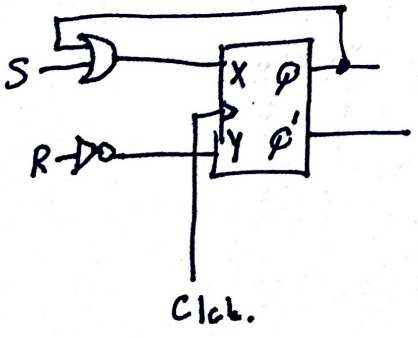
→ Choose X0 for (**)

X: Q(t) | 1 | 1 | 1 |
S | X | X | X | R

$\Rightarrow X = Q(t) + S$

Y: Q(t) | X | 1 | 1 | X |
S | X | X | X | X | R

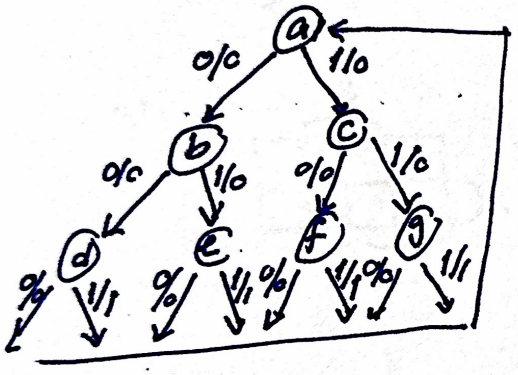
$\Rightarrow Y = R'$



Name: ID#:

Question 3:[30pts] Design a synchronous sequential circuit using a minimum number of JK flip-flops and logic gates. The circuit has single input and single output. The output is 1 if any of the following bit sequences are encountered in the input: {101, 110, 111, 100} and 0, otherwise. The least significant bit appears first in time. After a 3-bit sequence is processed, the circuit should proceed with the next 3-bits (i.e. nonoverlapping operation). *Hint: The characteristic equation of a JK-FF is: Q(t+1) =Q'(t)J + K'Q(t).*

State transition graph:



State transition table

PS	NS x=0	NS x=1	out x=0	out x=1
a	b	c	0	0
b	d	e	0	0
c	f	g	0	0
d	a	a	0	0
e	a	a	0	1
f	a	a	0	1
g	a	a	0	1

$S_1 = \{a, b, c\}$ $S_2 = \{d, e, f, g\}$

Reduced table

$S_1 = \{a\}$ $S_2 = \{b, c\}$ $S_3 = \{d, e, f, g\}$

A B C

PS	NS x=0	NS x=1	out x=0	out x=1
A	B	B	0	0
B	C	C	0	0
C	A	A	0	1

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

PS	NS x=0	NS x=1	out x=0	out x=1
00	01	01	0	0
01	10	10	0	0
10	00	00	0	1
11	XX	XX	X	X

x	PS $y_1 y_2$	NS $y_1^+ y_2^+$	$J_1 K_1$	$J_2 K_2$	out
0	0 0	0 1	0 X	1 X	0
0	0 1	1 0	1 X	X 1	0
0	1 0	0 0	0 X	0 X	0
0	1 1	X X	X X	X X	X
1	0 0	0 1	0 X	1 X	0
1	0 1	1 0	1 X	X 1	0
1	1 0	0 0	X 1	0 X	1
1	1 1	X X	X X	X X	X

$J_1 = y_2(t)$

$K_1 = 1$

$J_2 = y_1'(t)$

$K_2 = 1$

$out = x y_1(t)$

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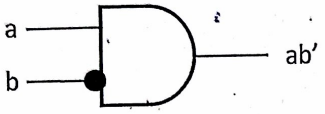
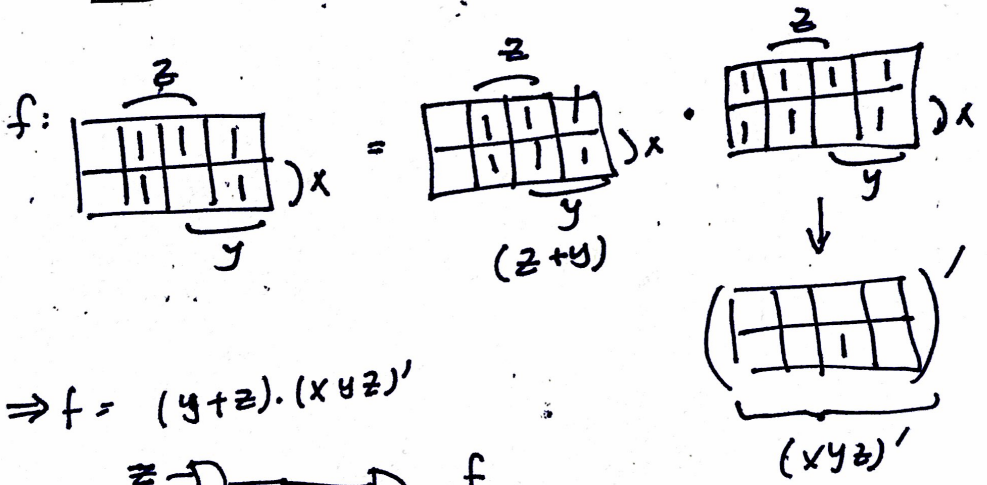
Question 4:[20pts] Given a function $f(x,y,z) = \Sigma(m_1,m_2,m_3,m_5,m_6)$

a) Implement f using two AND, one OR and one NOT gates only. Complemented (primed) variables are **not** available, logic constants 0/1 are **not** available.

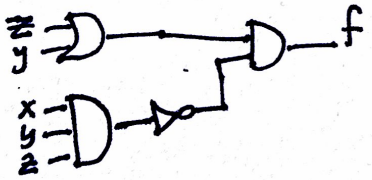
b) Implement f using one OR and three INHIBIT gates only. Complemented (primed) variables are **not** available, logic constants 0/1 are **not** available. INHIBIT gate is defined as follows:



a)

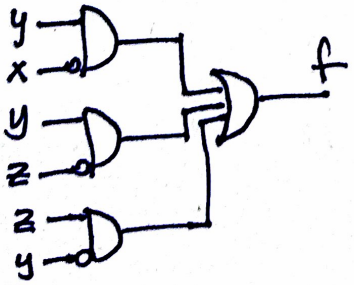


$\Rightarrow f = (y+z).(xyz)'$



b)

$f = y'z + x'y + z'y$



x1