

MIDDLE EAST TECHNICAL UNIVERSITY ELECTRICAL & ELECTRONICS ENGINEERING DEPARTMENT

EE464 HOMEWORK 1 – Magnetic Design of the Hardware Project

Members: Onat Şimşek - 2375772

Selen Özge Özgür – 2375566

Onur Emirhan Çon -

Date: 24.03.2024

Introduction

In this assignment, we will simulate the topology we had previously chosen for our hardware project. During the simulation, we will observe the characteristics of the ideal case and investigate how non-idealities affect our system. Additionally, we will identify the edge of DCM operation point of our topology and consider this in our design. Finally, by calculating the efficiency of our design, we will determine how lossy of a system we have designed.

Question 1)

As Team "The Isolated Ones", we plan to design a Flyback converter as an isolated DC/DC converter, or in other words as an SMPS.

a) While checking the analog controllers of the Flyback converter, we found out that UC3845 will be more than enough for this project. UC3845 can supply a duty cycle of 0.5 maximum, which gives us an upper boundary to choose our duty cycle. Hence, we have chosen a duty cycle range of 0.2 to 0.4. In order to ensure that the controller gives a duty cycle in this range, our turns ratio should be 1:1. This can be calculated as follows:

Due to the diode between the secondary side and the load, assume secondary voltage as 12.75V ($V_{secondary} = 12.75V$) so that our output voltage is around 12V. Moreover, it is known that the voltage equation of a Flyback converter is as follows:

$$\frac{V_2}{V_1} = \frac{D}{1 - D} * \frac{N_2}{N_1}$$

where V_2 = 12.75 V, V_1 = 20-40 V. When V_1 = 20 and $\frac{N_2}{N_1}$ ratio is taken as 1, D_{max} is found as around 0.39. Furthermore, when V_1 = 40 and $\frac{N_2}{N_1}$ ratio is taken as 1, D_{min} is found as around 0.24. The found duty cycles determine the boundaries of the operating region of the Flyback converter.

b) For the transformer of the Flyback converter, we have selected an E-core with a gap of 1mm. The datasheet of the core can be found in the appendix section. An E-core is selected since the leakage flux in E cores is smaller than toroid cores due to their shape. Moreover, due to the existence of coil formers for each and every E-core, it is much easier to wind the coils to the core. Also, since we are to design a Flyback converter, the energy should be stored in the core first to transfer the energy to the secondary side. Hence, an E-core with a gap is required for us to implement a better solution to store the energy in the core when the switch is ON. Another reason for us to select this core is that it has a high permeability, even with the air gap, and it does not have a high volume, with a volume of 11.5 cm³, so that the core will not take up so much space in our final design.

In order to find the required number of turns for both the primary and the secondary, which are the same for our design, we need to determine the magnetizing inductance value first. By using the magnetizing inductance formula in the Application Note, AN4137, Design Guidelines for Off-line Flyback Converters Using FPS [1], the magnetizing inductance L_m can be calculated as follows:

$$L_{m} = \frac{(V_{s,min} * D_{max})^{2}}{2 * P_{in} * f_{s} * K_{RF}}$$

where P_{in} is the input power, which is selected as 72W to ensure an efficiency more that 80%, K_{RF} is the ripple factor, which is defined as in the Figure 1 and selected as 0.35, f_s is the switching frequency, which is selected as 100kHz.

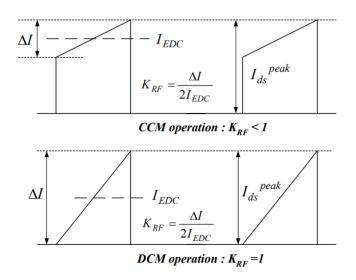


Figure 1. MOSFET drain current and ripple factor K_{RF}

After putting the values into the equation, L_m is found to be 18.55 μ H. Then, to find the required number of turns of the primary, the A_L value of the core is used and the required number of turns is found by using the following formula:

$$N^2 = \frac{L_m}{A_I}$$

where A_L value of the core we have selected having a 1mm of air gap is 196 nH/T². Hence, after making the calculation, the required number of turns are found as 10, approximately. Moreover, by limiting the B_{max} value, the minimum required number of turns can also be calculated to check whether the previously calculated number of turns is valid or not by using the formula present in [2] as follows:

$$N_{min} > \frac{V_{s,max} * D_{max}}{B_{sat} * A_{effective,core} * f_s}$$

where B_{sat} is selected as 0.2T, and effective area of the core we have selected is 125 mm². When putting all the numbers to the equation above, it is found that minimum required number of turns should be larger than 6.22 turns ($N_{min} > 6.22$ turns). This concludes that 10 turns in the primary and the secondary meet the requirement of minimum turns and can be used further in this design.

In order to determine the cable size in AWG system, the switching frequency and the current capability of the cable should be considered. Since our switching frequency is 100kHz and the RMS value of the current in the primary is around 6A, a wire that can carry a current having these features should be selected. Also, when the skin depth is calculated using the equation $\delta = \frac{75}{\sqrt{f_s}}$ where the unit of the skin depth is mm, and skin depth is found as 0.237 mm. Thus, the selected cable should also have a radius smaller than 0.237mm and have a power

transmission capability up to 100kHz, minimum. Hence, we selected a cable with a size of AWG 26.

In order to carry the current in the primary and the secondary side of the transformer, more than 16 AWG26 size cables should be paralleled. This number of required cables is calculated as follows:

$$n > \frac{I_{in,RMS}}{0.361} = 16.3$$

where 0.361A is the maximum current limit of the AWG26 size cable for power transmission and $I_{in,RMS}$ is calculated as follows:

$$I_{in,RMS} = \sqrt{\frac{\left(I_{peak}^2 + I_{min}^2 + I_{peak} * I_{min}\right) * D_{max}}{3}}$$

where I_{peak} = 12.48A, I_{min} = 6.01A, and D = 0.389. also, I_{peak} and I_{min} are calculated as follows:

$$I_{peak} = I_{EDC} + \frac{\Delta I}{2} = 12.48A$$
 $I_{min} = I_{EDC} - \frac{\Delta I}{2} = 6.01A$

and, IEDC is calculated as:

$$I_{EDC} = \frac{P_{in}}{V_{Smin} * D_{max}} = \frac{72}{20 * 0.389} = 9.247A$$

and, ΔI is calculated as:

$$\Delta I = 2 * I_{EDC} * K_{RF} = 6.473A$$

Thus, we decided to parallel 20 pieces of AWG26 size cable for both primary and the secondary windings of the transformer. Then, in order to calculate the fill factor of our core, the following equation is used:

$$fill\ factor = \frac{20*10*2*0.14mm^2}{178mm^2} = 0.31$$

where 0.14mm² is the cross section area of the selected cable and 178mm² is the window area of the core. And, the DC resistance of the cable is calculated as:

$$R_{DC} = \frac{1.68 * 10^{-5} * 69 * 10}{0.14 * 20} = 0.004\Omega$$

where 69mm is the mean length of one turn according to the datasheet of the selected core, $1.68*10^{-5}$ is the resistivity of the copper (Ω .mm), 14mm² is the cross section area of the selected cable, and 20 is the number of cables to be used in parallel.

The AC resistance of the cable in 100kHz is calculated using the following formula:

$$\delta = \sqrt{\frac{\rho}{\pi * f_s * \mu}}$$

$$A_{eff} = \delta * \pi * d$$

$$R_{AC} = \frac{\rho * l}{A_{eff} * 20} = \frac{0.09213}{20} = 4.606 * 10^{-3}$$

where d is the diameter of the conductor. Then, the copper losses in the conductor becomes:

$$P_{CU} = I_{RMS}^2 * R_{AC} = 2 * 5.88^2 * 4.606 * 10^{-3} = 0.32W$$

 $P_{cu}=I_{RMS}^2*R_{AC}=2*5.88^2*4.606*10^{-3}=0.32W$ The above equation is multiplied with 2 since RMS values in the primary and in the secondary are the same since the turns ratio of the transformer is 1.

The core loss of the transformer can be calculated using the datasheet of the core material given in the Appendix section. According to the datasheet, the relative core loss of the core is given as 375kW/m³, which is equal to 0.375W/cm³ Then, the core loss can be calculated as:

$$P_{core} = \ 0.375*11.5 = 4.3125W$$

The core loss of our transformer is higher than copper loss of our transformer, which concludes that our design does not require any new iterations. Also, since both loss values are reasonable values, there is no need for further iterations.

c) The simulation design with 20 V and 40V input voltage is given in the Figure 2. For this part of the homework, simulation is done by using ideal switches. Forward voltage drop of the diode and RDS, and Ron resistance of the MOSFET does not considered for this part.

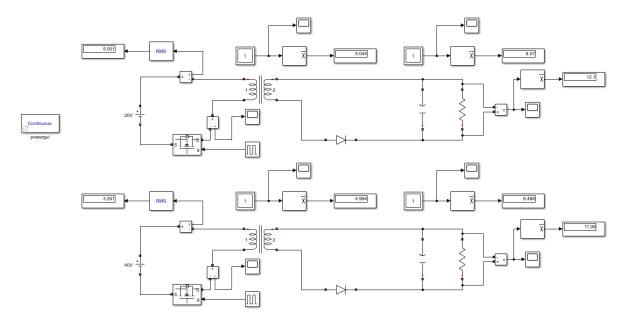


Figure 2: Ideal flyback converter simulation with 20-40V input.

Output voltage with 20V and 40 V inputs are given in Figure 3 and Figure 4. As we can see, output voltage reaches 12V within 0.005 second.

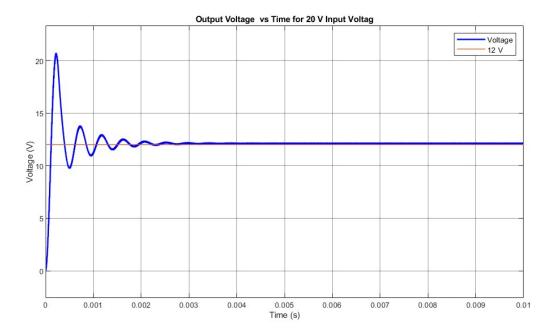


Figure 3.Output Voltage vs Time for 20 V Input Voltage for Ideal Case

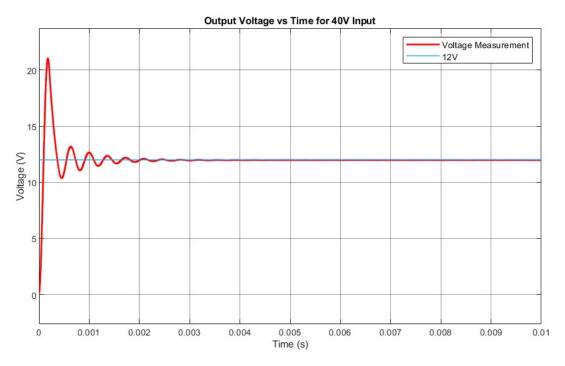


Figure 4.Output Voltage vs Time for 40 V Input Voltage for Ideal Case

MOSFET drain current characteristic for 20 V input is given in Figure 5. As you can see, current characteristic is same as in the Part b.



Figure 5.MOSFET Current vs Time at Steady State for 20V Input.

Since we want to operate in CCM, magnetizing ucrrent must not reach zero. As you can see from the Figure 6, minimum current in the steady state is 6.25 A and current ripple is 3.75 A for 40 V input. Similarly, from the Figure 7, minimum current in the steady state is 4.25 A and current ripple is 4 A for 20 V input.

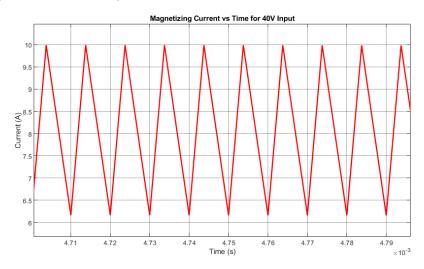


Figure 6.Magnetizing Current vs Time at Steady State for 20V Input.

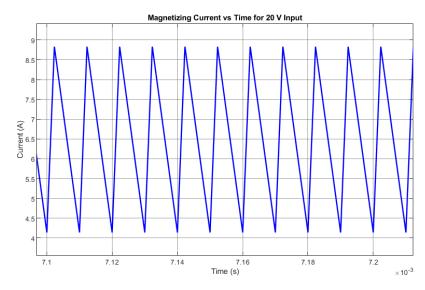


Figure 7. Magnetizing Current vs Time at Steady State for 40V Input.

d)

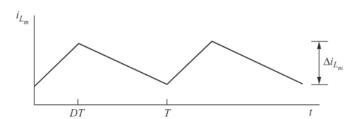


Figure 8. Magnetizing Current in CCM Operation

Figure 8 shows the magnetizing current in CCM operation. To get into the DCM mode, Δi_{L_m} must be smaller than $2*I_{L_m\,avg}$. This means edge of DCM mode is when $\Delta i_{L_m}=2*I_{L_m\,avg}$.

$$I_{L_{m \, avg}} = \frac{I_o}{(1-D)} * \frac{N_2}{N_1}$$

$$\Delta i_{L_m} = \frac{V_s}{L_m} DT_s$$

Then,

$$\frac{V_s}{L_m} DT_s = 2 * \frac{I_o}{(1-D)} * \frac{N_2}{N_1}$$

$$I_o = \frac{V_s}{2L_m} DT_s \frac{N_1}{N_2} (1 - D)$$

From the above equation, $I_{o_{40\,V}}=1.807\,A\,\&\,I_{o_{20\,V}}=1.1947\,A.$ By using this I_o values, we calculate $I_{L_{m\,avg}}$. By using the $I_{L_{m\,avg}}$, corresponding transformer current would be:

$$I_{L_{m\,ava}}*(1-D).$$

Since we are at the boundary of DCM, the minimum current will be 0. Consequently, the maximum current will be twice the value given by the formula above.

$$I_{max_{40 \, V \, input}} = 4.7 \, \text{A} \, \& \, I_{max_{20 \, V \, input}} = 3.824 \, \text{A}.$$

e) To simulate the system with non-ideal switches, we used IRF540NSPbF parameters for the MOSFET and MBR1545CT for the diode. The reason why we choose these components for the simulation purpose is they exist in the laboratory that we are going to use for the hardware project. The datasheets of the components are given in the appendix. Since we use MATLAB for simulation purposes, switches are simulated with snubber circuits as default, and we did not change the snubber circuit parameters.

Output voltage with 20V and 40 V inputs are given in Figure 9 and Figure 10. As we can see, output voltage can not reach 12V. The reason for this is the voltage drops on the MOSFET and the Diode. To get 12V output with non-ideal switches and transformer, we need to change duty cycleaccordingly. Since we can not estimate/calculate all non-idealities, adding closed loop control to design is currical.

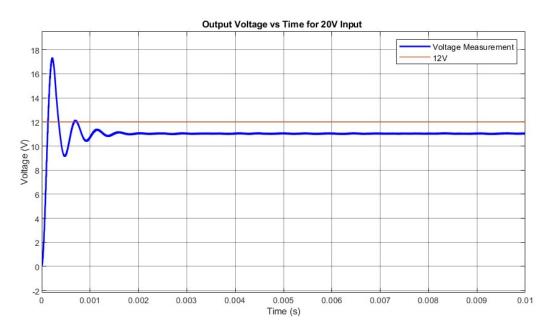


Figure 9. Output Voltage vs Time for 20 V Input (Non-ideal Case)

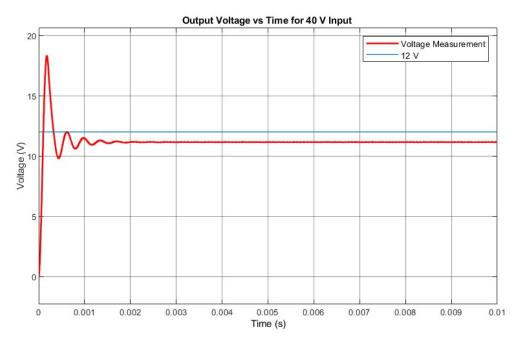


Figure 10. Output Voltage vs Time for 40 V Input (Non-ideal Case)

Measurements taken from the MOSFET, and the diode are given in the Figure 11 and Figure 12. These graphs are like ideal case with negligible oscillations.

If we look at the magnetizing current graphs in Figures 13 and 14, we can still see that we are operating in CCM (Continuous Conduction Mode). However, when compared to the ideal case, we observe a current drop caused by non-idealities.

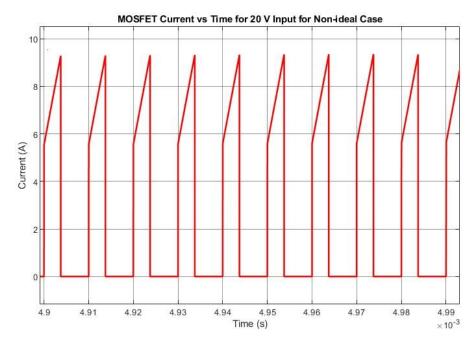


Figure 11. MOSFET Current vs Time for 20 V Input for Non-ideal Case

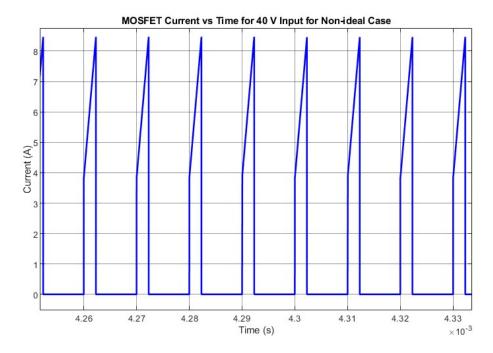


Figure 12. MOSFET Current vs Time for 40 V Input for Non-ideal Case

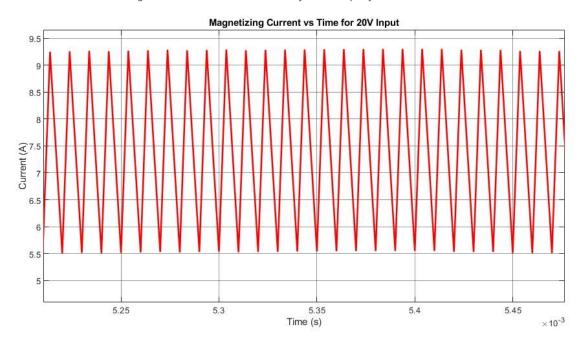


Figure 13. Magnetizing Current vs Time for 20V Input for Non-ideal Case

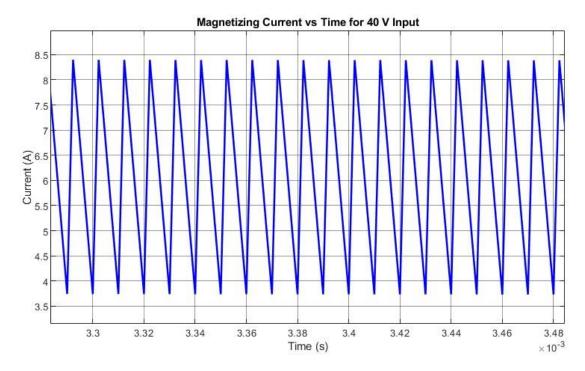


Figure 14. Magnetizing Current vs Time for 40V Input for Non-ideal Case

f)

$$\eta = \frac{\textit{P}_{out}}{\textit{P}_{out} + \textit{P}_{losses}} \, \text{or} \, \eta = \frac{\textit{P}_{out}}{\textit{P}_{in} \, + \, \textit{P}_{excessive \, losses}}$$

Efficiency calculation for 100% load condition for both voltage limits:

20V input:
$$\eta = \frac{11.05*4.603}{20*4.603+4.3125} = 52.8\%$$

40V input: $\eta = \frac{11.17*4.65}{40*3.029+4.3125} = 41.9\%$

Efficiency calculation for 50% load condition for both voltage limits:

20V input:
$$\eta = \frac{11.18 * 2.331}{20 * 2.427 + 4.3125} = 47.2\%$$

40V input: $\eta = \frac{11.23 * 2.338}{40 * 1.673 + 4.3125} = 36.9\%$

Efficiency calculation for 25% load condition for both voltage limits:

20V input:
$$\eta = \frac{11.3*1.18}{20*1.386+4.3125} = 41.6\%$$

40V input: $\eta = \frac{13.95*1.457}{40*1.361+4.3125} = 34.6\%$

In the simulation, R_c is taken a relatively high value and in the end, the core loss in the transformation is added to the calculated P_{in} value using the simulation data. This is only done for core losses in the transformer, copper losses in the transformer, conduction losses of the MOSFET, etc. are included in the calculated P_{in} value. It can be concluded that efficiency calculation using a simulation tool may be misleading.

Conclusion

In summary, when implementing our design in open loop, we need to consider non-idealities and adjust our duty cycle accordingly. We observed the output voltage deviation when we did

not update the duty cycle in the "Part E" section. Since we cannot always calculate non-idealities perfectly, closed-loop control is important in this regard. Additionally, due to operating at low powers, careful component selection and proper winding of the transformer are crucial. When these processes are not carried out carefully, we encounter low efficiency.

References

[1]: AN-4137 Design Guidelines for Off-line Flyback Converters using FPS. Available at:

https://u.dianyuan.com/bbs/u/0/1071889497.pdf

[2]: Single Transistor Forward Converter Design. Available at:

https://ocw.metu.edu.tr/pluginfile.php/152997/mod_resource/content/0/forward_magnetic_design_recitation.pdf

Appendix

Link to core datasheet:

https://www.tdk-electronics.tdk.com/inf/80/db/fer/etd 39 20 13.pdf

Link to core material datasheet:

https://www.tdk-

<u>electronics.tdk.com/download/528882/990c299b916e9f3eb7e44ad563b7f0b9/pdf-n87.pdf</u>

MOSFET Datasheet:

IRF540NS LPbF.pmd (direnc.net)

Diode Datasheet:

mbr1545ct.pdf (vishay.com)