

See discussions, stats, and author profiles for this publication at: <https://www.researchgate.net/publication/321903540>

# Practical Design of Buck Converter By Taufik

Presentation · December 2017

---

CITATIONS

2

READS

10,018

1 author:



Taufik Taufik

California Polytechnic State University, San Luis Obispo

233 PUBLICATIONS 1,599 CITATIONS

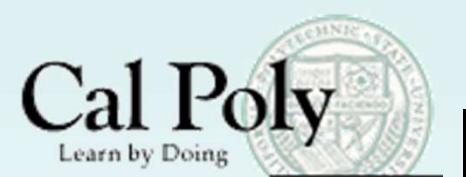
SEE PROFILE

# Practical Design of Buck Converter

**Dr. TAUFIK**

Professor of Electrical Engineering  
Director of Electric Power Institute  
California Polytechnic State University, San Luis Obispo, USA

[taufik@calpoly.edu](mailto:taufik@calpoly.edu)  
<http://www.ee.calpoly.edu/faculty/taufik>



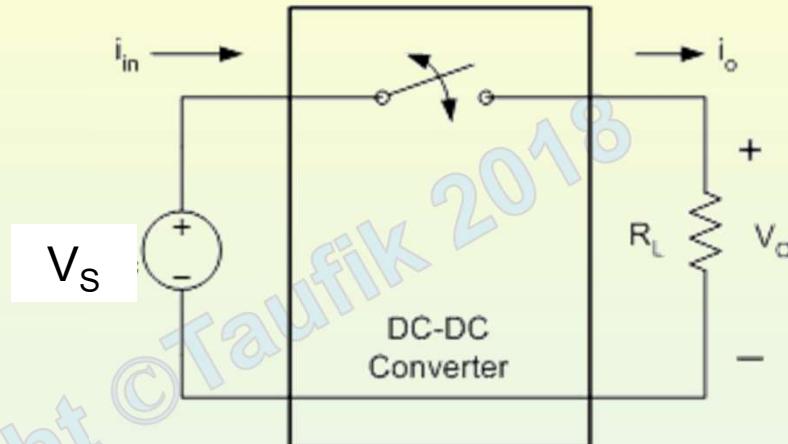
# Outline

- DC-DC Converter Basics
- Design Equations
- Loss Considerations
- Layout Considerations
- Efficiency Improvements
- Controller

# DC-DC Converter Basics

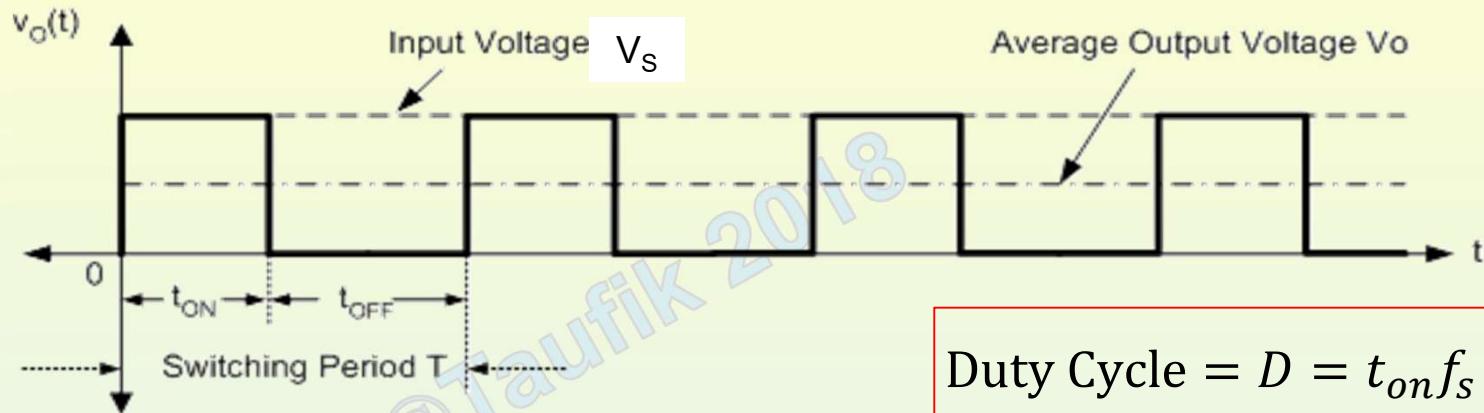
- A circuit employing switching network that converts a DC voltage at one level to another DC voltage
- Two basic topologies:
  - Non-Isolated
    - Buck, Boost, Buck-Boost, Cuk, SEPIC, Zeta
  - Isolated
    - Push-pull, Forward, Flyback, Half-Bridge, Full-Bridge

# DC-DC Converter Basics



- When ON: The output voltage is the same as the input voltage and the voltage across the switch is 0 V.
- When OFF: The output voltage is zero and there is no current through the switch.
- Ideally, the Power Loss is zero since output power = input power
- Periodic opening and closing of the switch results in pulse output

# DC-DC Converter Basics



$$\text{Duty Cycle} = D = t_{on}f_s = \frac{t_{on}}{T}$$

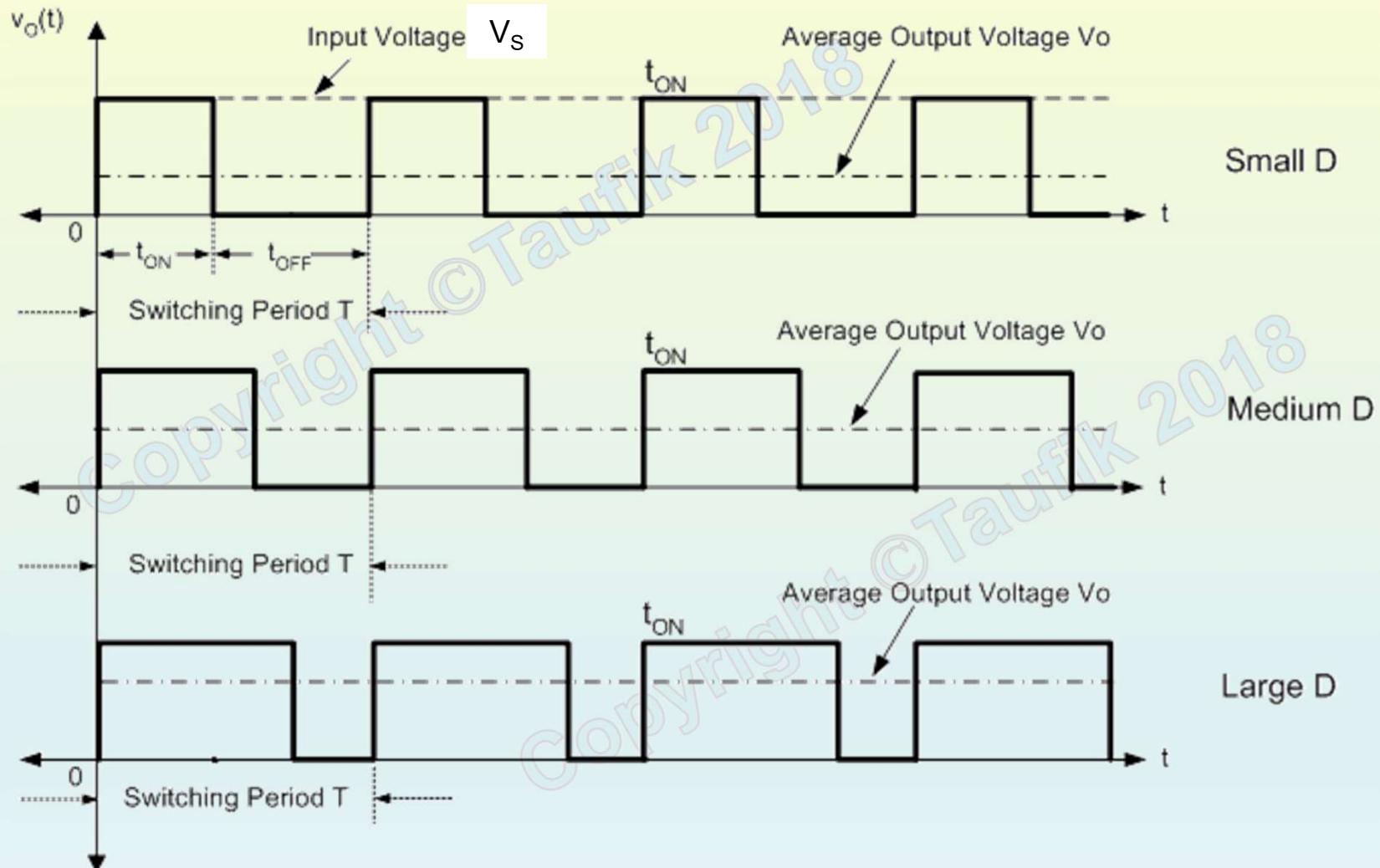
$$t_{on} = DT$$

$$t_{off} = T - t_{on} = T - DT = (1 - D)T$$

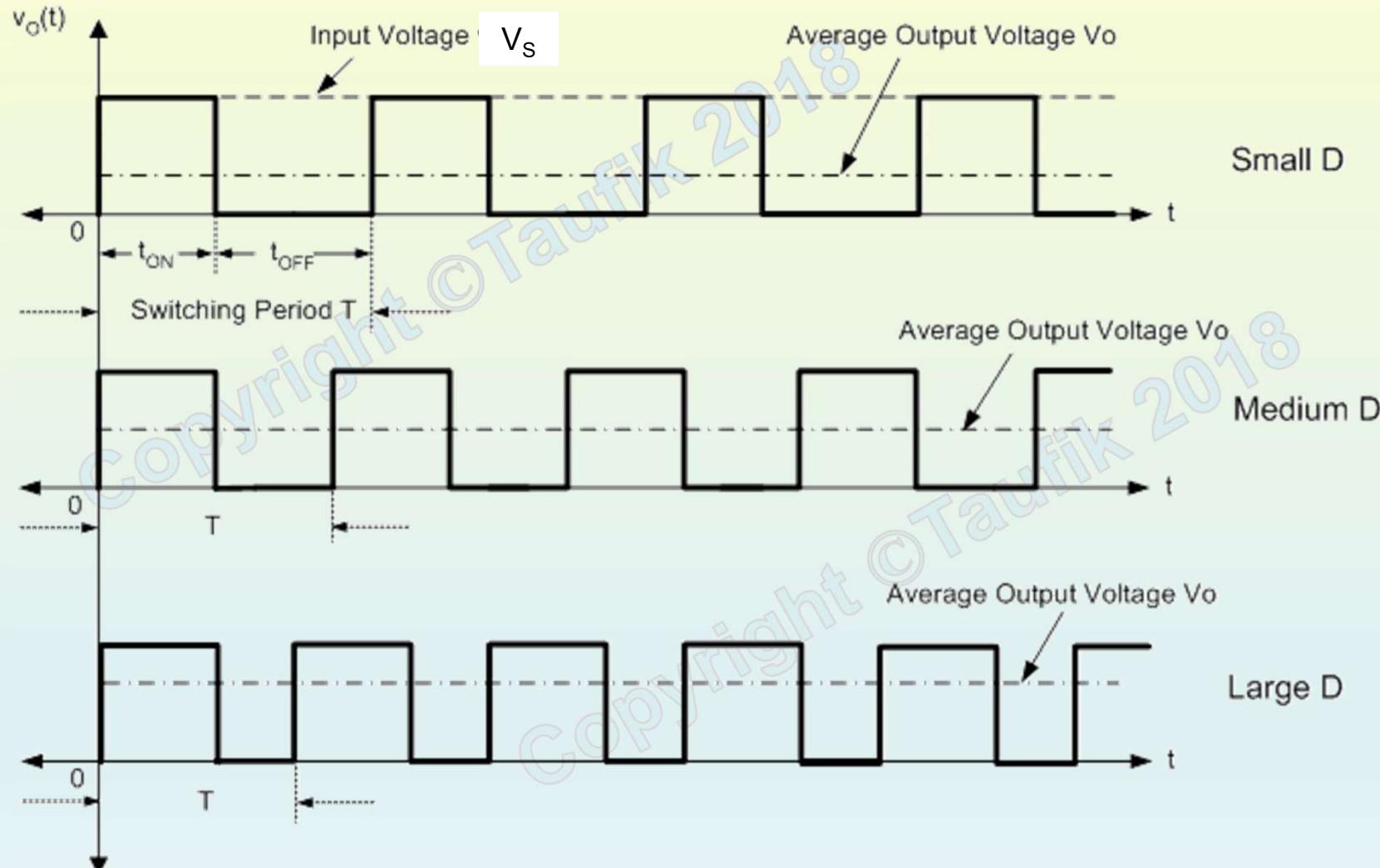
$$\bar{V}_o = \frac{1}{T} \int_0^T v_o(t) dt = \frac{1}{T} \int_0^{DT} V_s dt = V_s D$$

- Duty Cycle range:  $0 < D < 1$
- Two ways to vary the average output voltage:
  - Pulse Width Modulation (PWM), where  $t_{on}$  is varied while the overall switching period  $T$  is kept constant
  - Pulse Frequency Modulation (PFM), where  $t_{on}$  is kept constant while the switching period  $T$  is varied

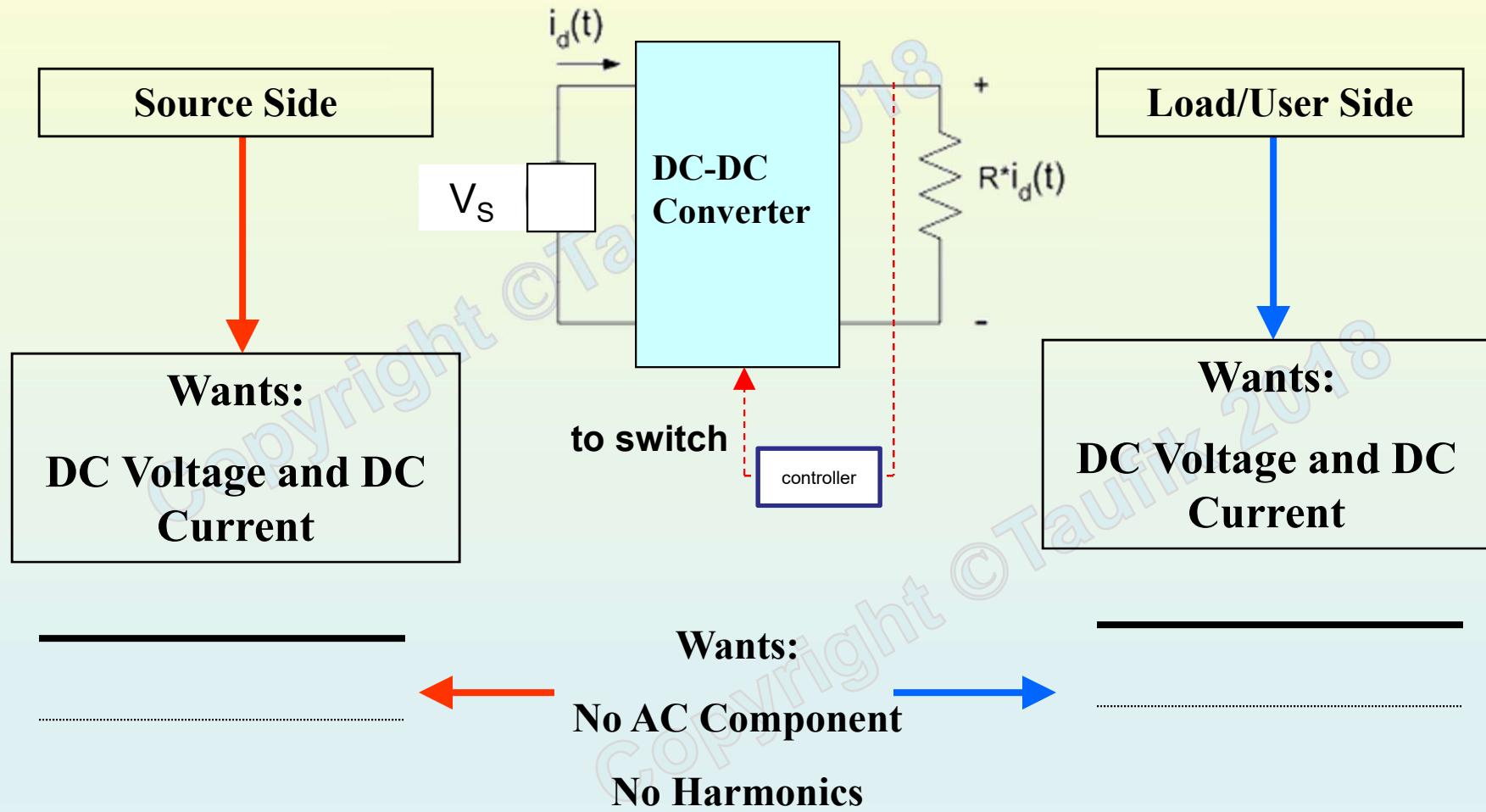
# DC-DC Converter Basics



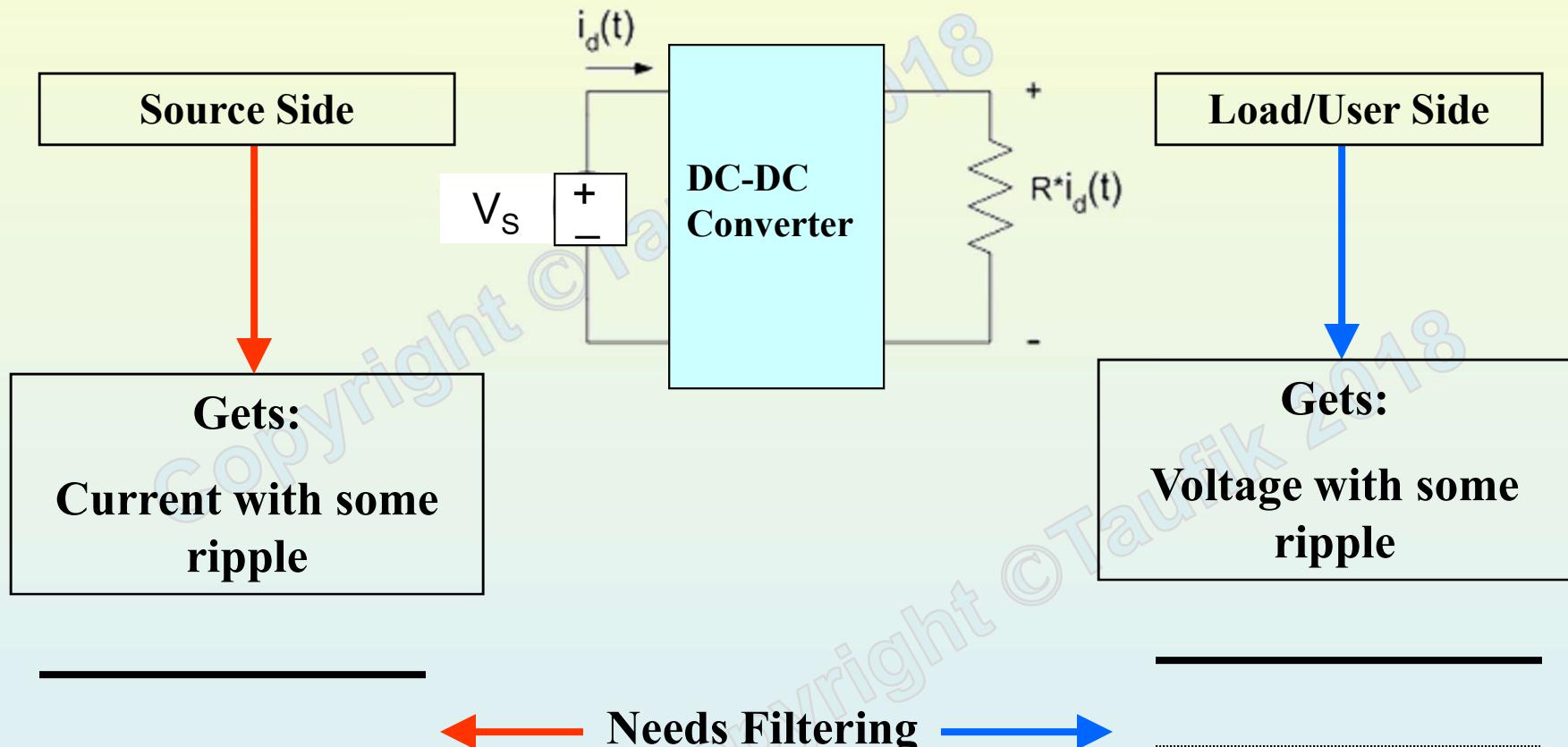
# DC-DC Converter Basics



# Review: DC-DC Converter Basics



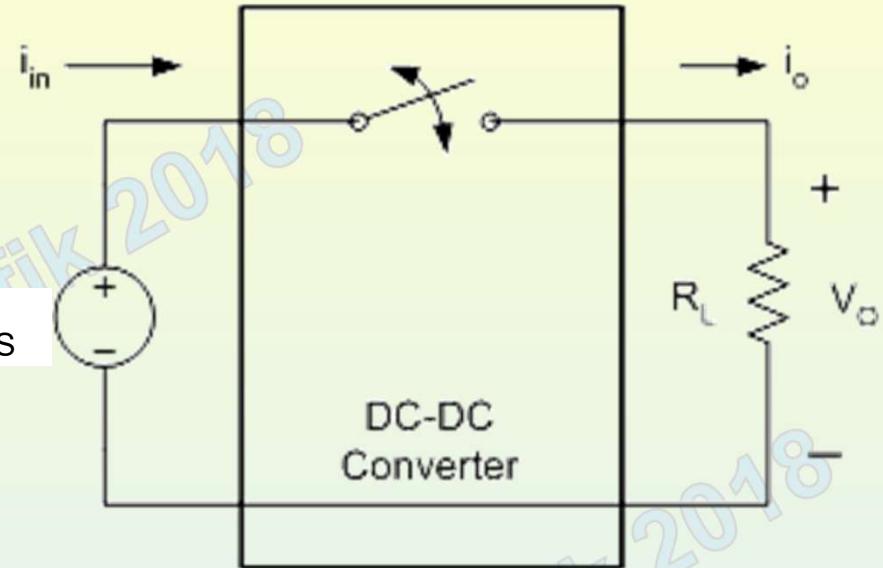
# DC-DC Converter Basics



# What is Buck Converter?

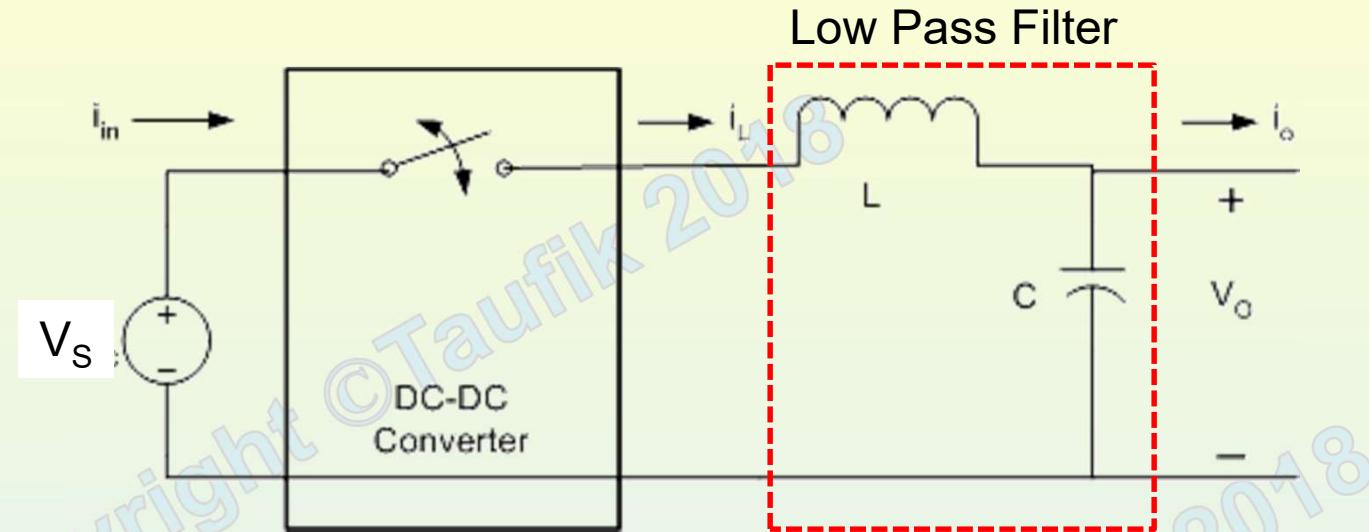
- A dc-dc converter circuit that steps down a dc voltage at its input
- Non-isolated, hence ideal for board-level circuitry where local conversion is needed
  - Cell-phones, PDAs, fax machines, copiers, scanners, computers, anywhere when there is the need to convert DC from one level (battery) to other levels
- Widely used in low voltage low power applications (though it may be used for KW applications as well)

# Basic Topology



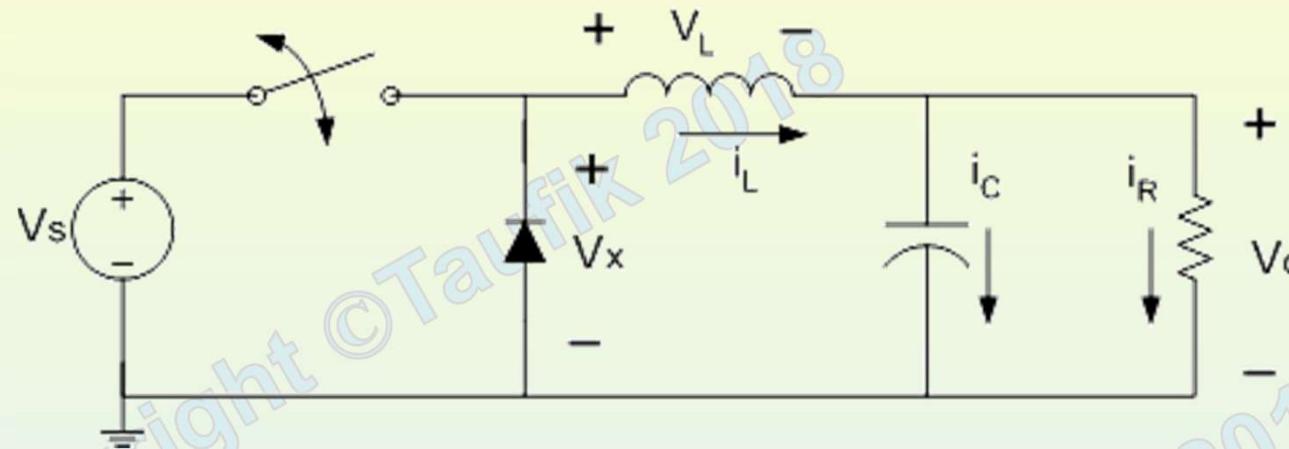
- Recall the basic switching circuit above produces square-wave output
- The square-wave output voltage contains significant ripple at switching frequency
- Switching frequency is typically high (10's to 100's of kHz), so why not add a low pass LC filter

# Basic Topology



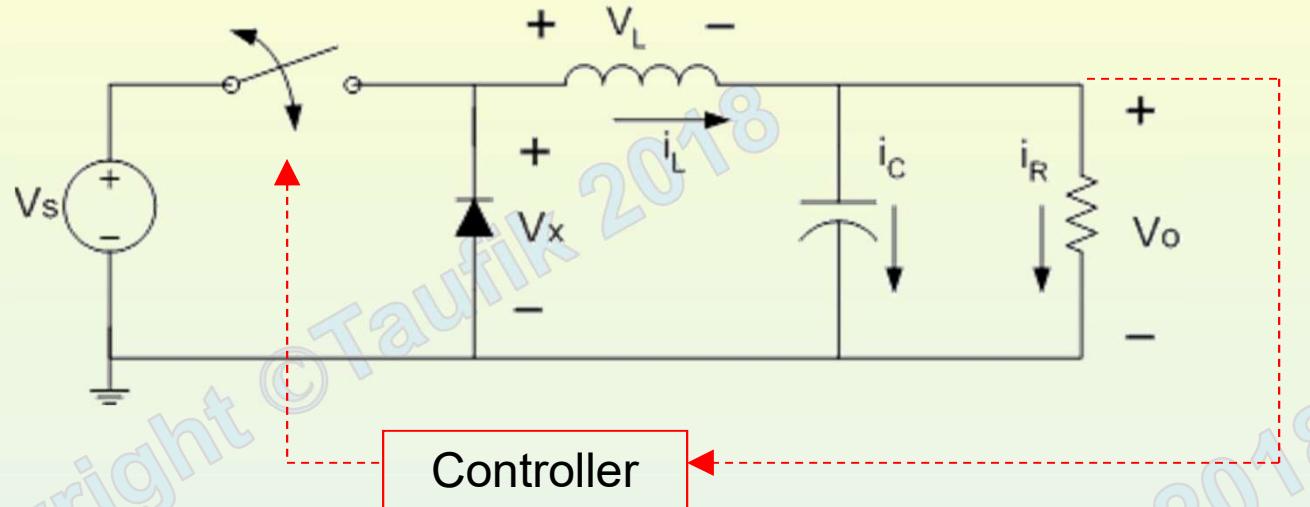
- Above circuit has a serious problem!
  - Switch is on, current flows through inductor
  - Switch is off, inductor current refuses to stop creating a high voltage across the switch, destroying the switch
    - Add a freewheeling diode to provide the continuity of inductor current when the switch is off

# Basic Topology

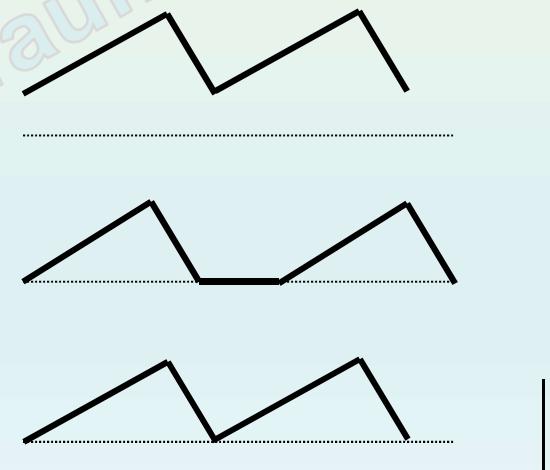


- After adding the diode, the circuit is the power stage of a BUCK converter!
- What is still missing is a mechanism to regulate the output voltage
  - The need to have a feedback control to close the loop

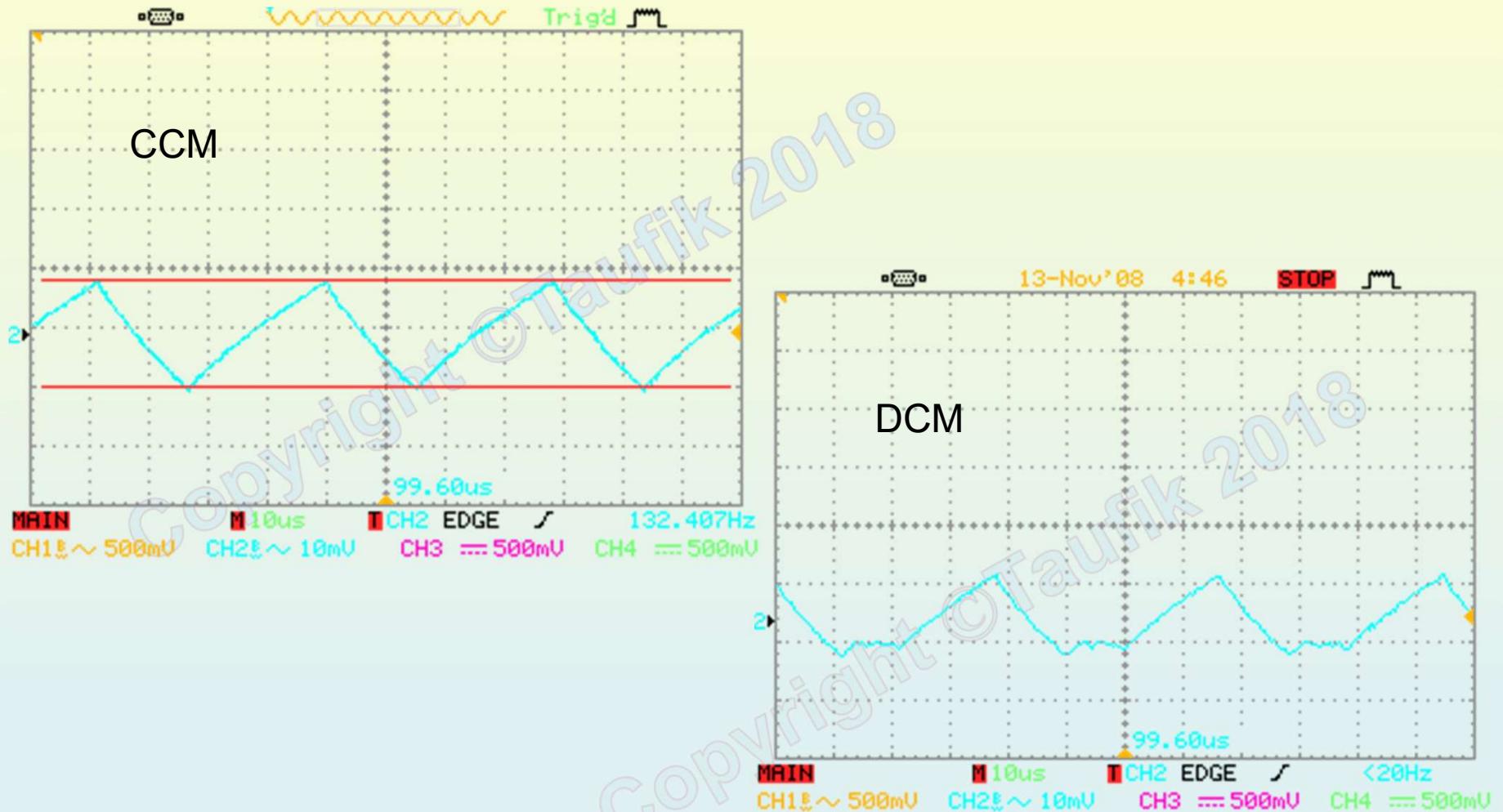
# The Basic Topology



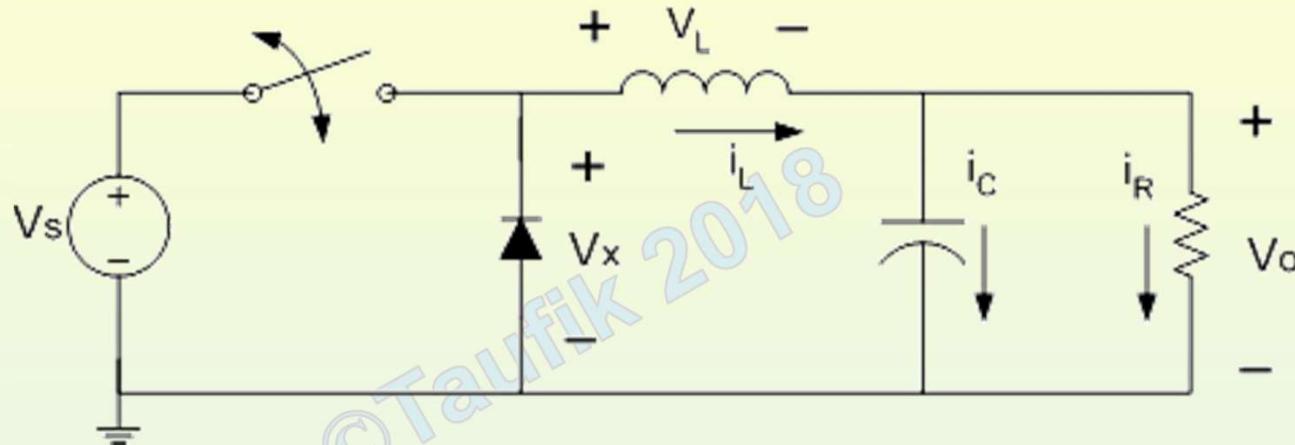
- Two types of Conduction Modes
  - Continuous Conduction Mode (CCM) where Inductor current remains positive throughout the switching period
  - Discontinuous Conduction Mode (DCM) where Inductor current remains zero for some time in the switching period
  - Boundary Conduction Mode (BCM)



# The Basic Topology



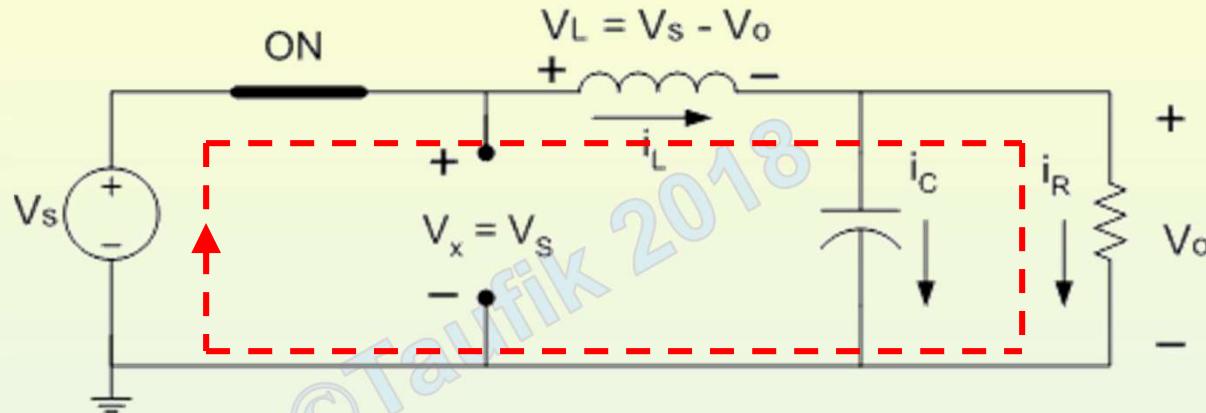
## Steady State Analysis of CCM Buck: Transfer Function



- Inductor is the main storage element
- Transfer function may be derived from Volt Second Balance (VSB):
  - Average Voltage across Inductor is Zero in steady state
  - Inductor looks like a short to a DC

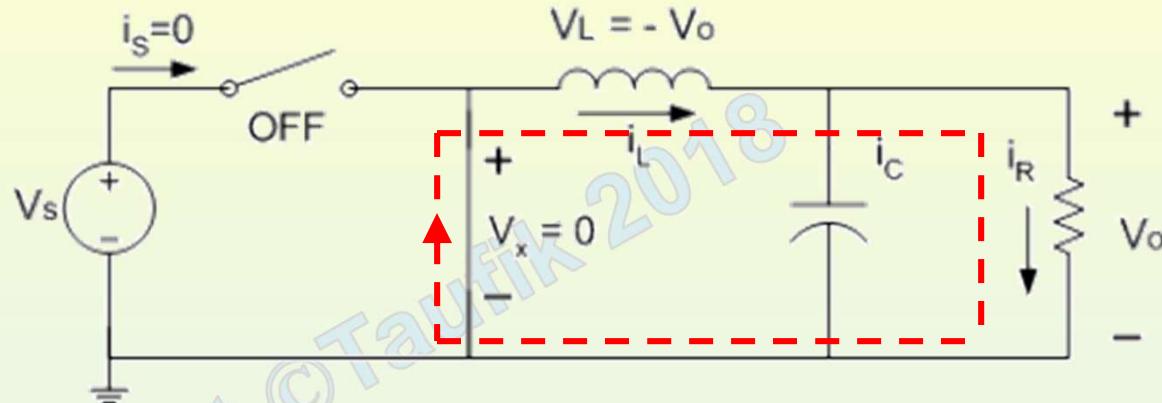
$$\bar{V}_L = v_{Lon} t_{on} + v_{Loff} t_{off} = 0$$

# CCM Buck: Transfer Function



- When the switch is **closed** or **ON**
  - Diode is reverse biased since
    - Cathode (at Positive of Input) is more positive than Anode (at 0 V)
  - Voltage across inductor:  $v_{Lon} = V_s - \bar{V}_o$
  - Recall that:  $D = t_{on}/T$
  - Then, duration of *on time*,  $t_{on}$ :  $t_{on} = DT$

# CCM Buck: Transfer Function



- When the switch is **OPEN** or **OFF**
  - Source is disconnected while load still demands energy
  - Forces inductor discharges causing its voltage to reverse polarity
  - In turn, makes the diode to be forward biased and conduct current since
    - Anode (0 V) is more positive than the Cathode (at some negative voltage)
  - Voltage across inductor:
  - Recall that:  $t_{off} = T - t_{on} = T - DT \Rightarrow t_{off} = (1 - D)T$

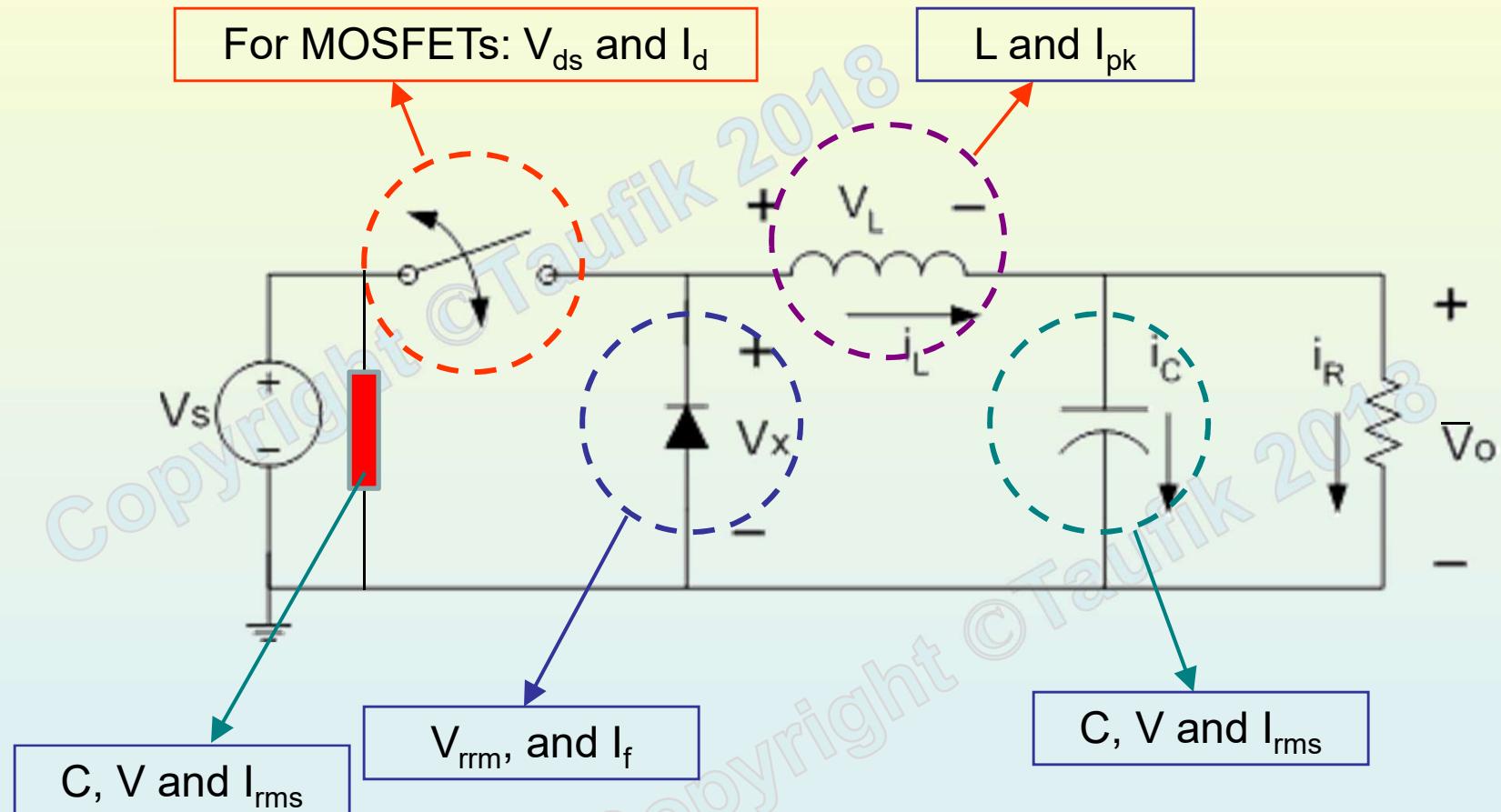
$$v_{Loff} = -\bar{V}_o$$

# CCM Buck: Transfer Function

$$v_{L_{on}} t_{on} + v_{L_{off}} t_{off} = 0$$
$$(V_s - \bar{V}_o)DT + (-\bar{V}_o)(1-D)T = 0$$
$$V_s D - \bar{V}_o D - \bar{V}_o + \bar{V}_o D = 0$$
$$\boxed{\bar{V}_o = DV_s}$$

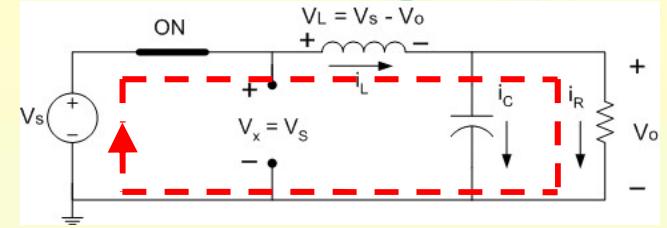
- Average output voltage is LESS than Input Voltage since  $0 < D < 1$

# CCM Buck: Sizing Components



A MUST HAVE!!!

# CCM Buck: Inductor Current



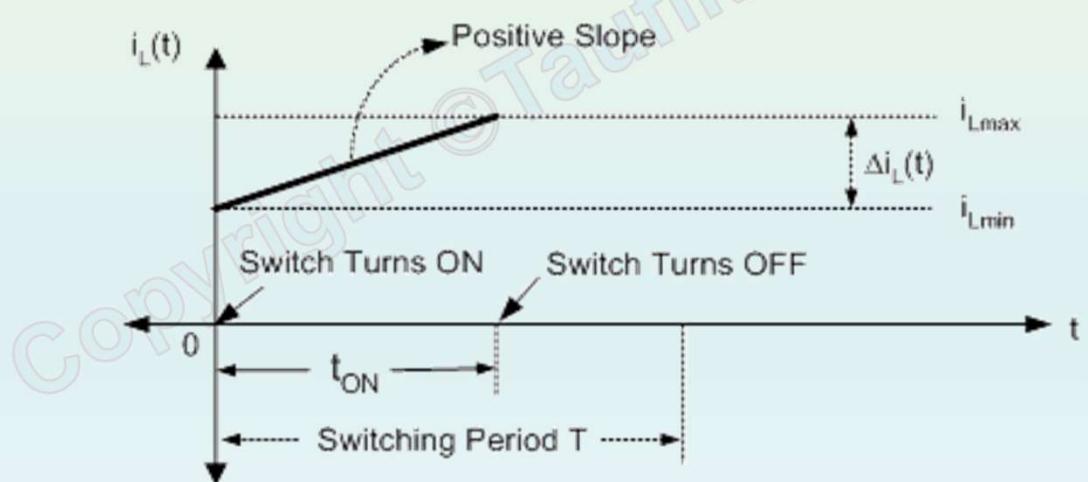
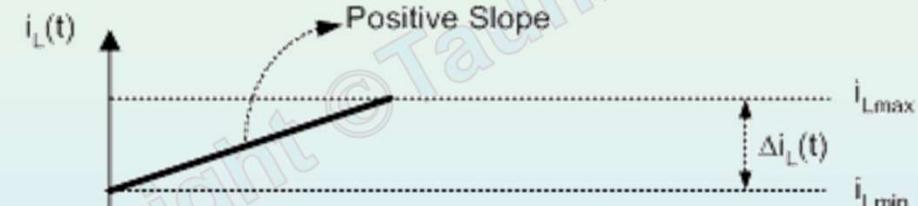
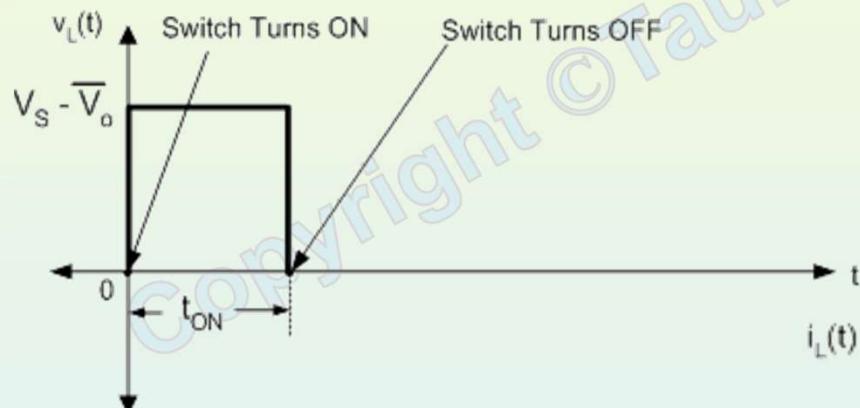
- When switch is ON, Inductor is *charging*:

$$v_L = V_S - \bar{V}_O = L \frac{di_L}{dt} \longrightarrow$$

$$\frac{di_L}{dt} = \frac{V_S - \bar{V}_O}{L} = \oplus$$

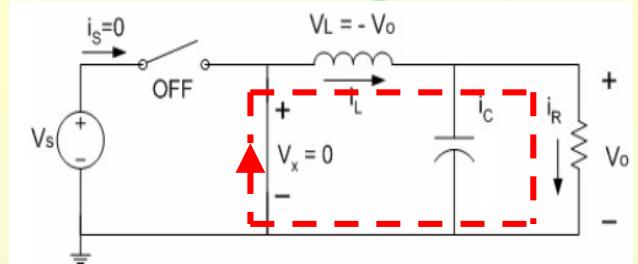
$$\Delta i_{Lon} = \frac{V_S - \bar{V}_O}{L} \Delta t_{on}$$

$$\Delta i_{Lon} = \frac{V_S - \bar{V}_O}{L} DT$$



# CCM Buck: Inductor Current

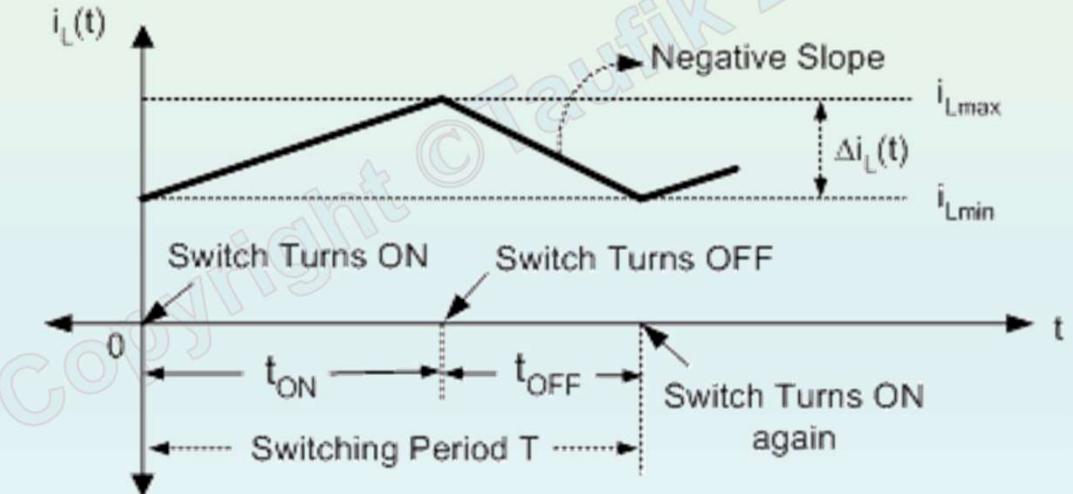
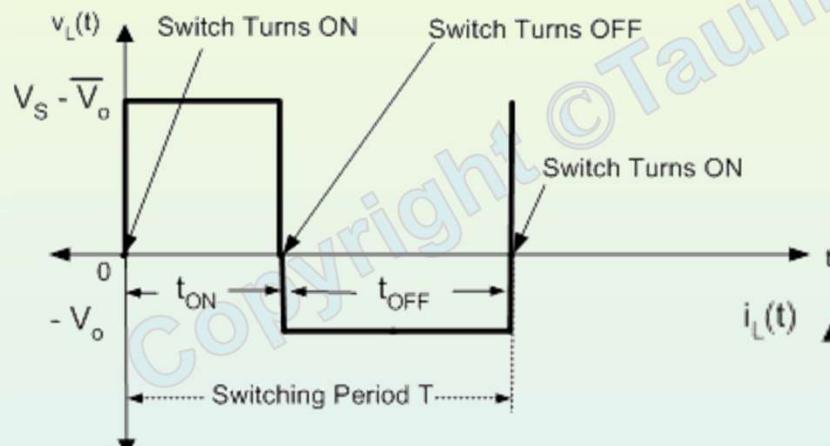
- When switch is OFF, Inductor is *discharging*:



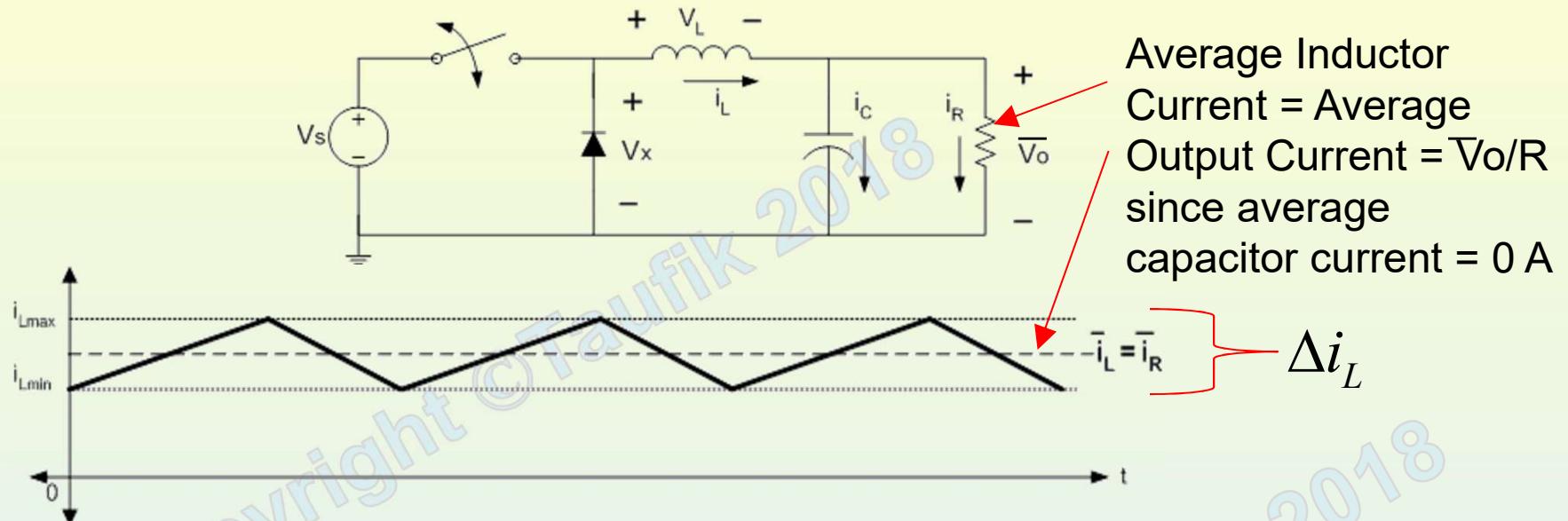
$$v_L = -\bar{V}_o = L \frac{di_L}{dt} \rightarrow \frac{di_L}{dt} = \frac{-\bar{V}_o}{L} = \boxed{\quad}$$

$$\Delta i_{Loff} = \frac{-\bar{V}_o}{L} \Delta t_{off}$$

$$\Delta i_{Loff} = \frac{-\bar{V}_o}{L} (1-D)T$$



# CCM Buck: Inductor Current



- We can then determine  $i_{L\min}$  and  $i_{L\max}$

$$I_{L\min} = \bar{I}_L - \frac{|\Delta i_L|}{2} = \frac{\bar{V}_o}{R} - \frac{1}{2} \left[ \frac{\bar{V}_o}{L} (1-D)T \right] = \bar{V}_o \left[ \frac{1}{R} - \frac{(1-D)}{2Lf} \right]$$

$$I_{L\max} = \bar{I}_L + \frac{|\Delta i_L|}{2} = \frac{\bar{V}_o}{R} + \frac{1}{2} \left[ \frac{\bar{V}_o}{L} (1-D)T \right] = \bar{V}_o \left[ \frac{1}{R} + \frac{(1-D)}{2Lf} \right]$$

# Sizing Inductor: Critical Inductance



- $I_{L\min}$  is used to determine the Critical Inductance (Minimum Inductance value at which the inductor current reaches Boundary Conduction Mode)
- Any inductance lower than critical inductance will cause the buck to operate in Discontinuous Conduction Mode
- Requirement is set either by means of **maximum  $\Delta i_L$**  or by specifying the minimum percentage load where converter still maintains CCM
- Set  $I_{L\min} = 0$ , then solve for  $L = L_C$ , then choose  $L > L_C$

$$I_{L\min} = 0 = \bar{I}_L - \frac{|\Delta i_L|}{2} = \bar{V}_0 \left[ \frac{1}{R_{\max}} - \frac{(1-D)}{2L_C f} \right] \rightarrow L_C = \frac{(1-D_{\max})R_{\max}}{2f}$$

# Sizing Inductor: Critical Inductance

$$L_C = \frac{(1 - D_{\max}) R_{\max}}{2f}$$

Calculated at Minimum Input Voltage

- Switching frequency typically chosen by the designer
- The higher the switching frequency, the smaller the required critical inductance, i.e. beneficial for reducing size of Buck

- Calculated at Minimum Output Current =  $R_{\max} = V_o/I_{\text{omin}}$
- $I_{\text{omin}}$  is either given as percentage of load to maintain CCM, e.g. 10% load with CCM
- Or,  $I_{\text{omin}}$  is calculated as specified by maximum  $\Delta i_L$ , such that  $I_{\text{omin}} = \Delta i_L/2$

# Sizing Inductor: Critical Inductance

- A more practical approach is to size the critical inductance by using percent peak to peak inductor current ripple  $\Delta i_L$  based on the maximum load current (calculated at maximum output power)
- $\Delta i_L$  is typically chosen between 30% to 40% of  $I_{o\max}$  (considering physical size, cost, losses, stability)

$$v_L = L \frac{di_L}{dt} \Rightarrow L = v_L \frac{dt}{di_L} = v_L \frac{\Delta t}{\Delta i_L}$$

## Sizing Inductor: Critical Inductance

- The equation may be calculated from ON time or OFF time of the switch
- Using the ON time:

$$L_c = |v_{L_{ON}}| \frac{\Delta t_{ON}}{\Delta i_L} = (V_s - \bar{V}_o) \frac{DT}{\Delta i_L} = (V_s - \bar{V}_o) \frac{D}{\Delta i_L f}$$

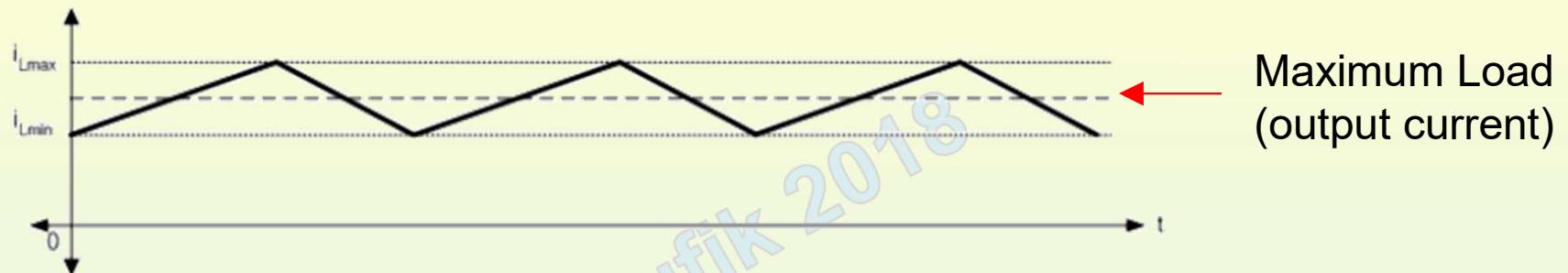
- Using the OFF time:

$$L_c = |v_{L_{OFF}}| \frac{\Delta t_{OFF}}{\Delta i_L} = (\bar{V}_o) \frac{(1 - D)T}{\Delta i_L} = (\bar{V}_o) \frac{1 - D}{\Delta i_L f}$$

- Thus:

$$L_c = (V_s - \bar{V}_o) \frac{D}{\Delta i_L f} = (\bar{V}_o) \frac{1 - D}{\Delta i_L f}$$

# Sizing Inductor: Peak Current



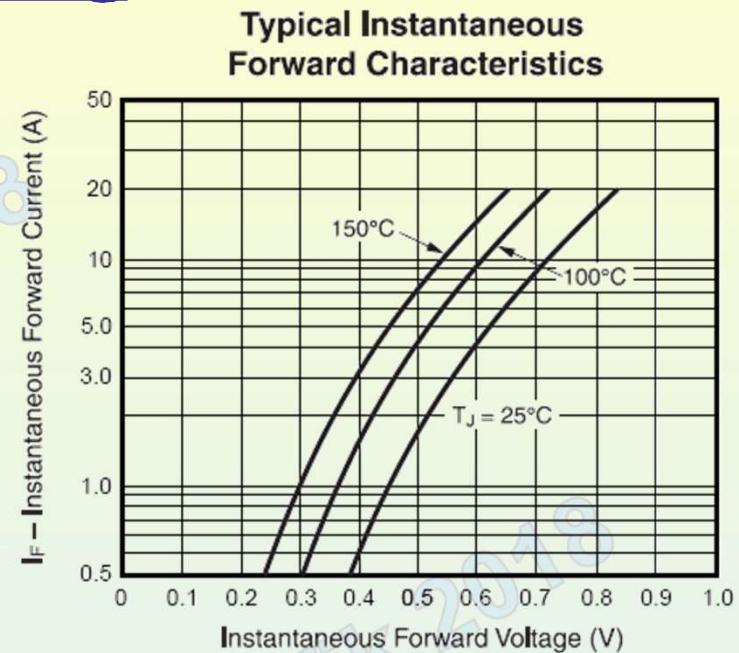
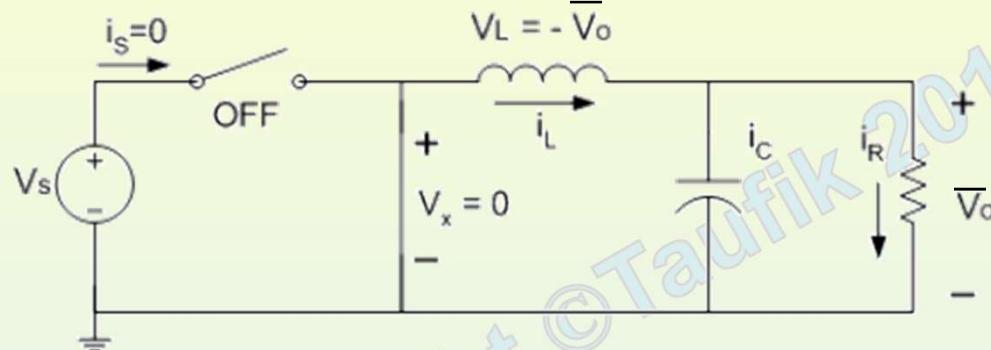
- $I_{L\max}$  is used to determine peak current rating of Inductor
- Worst case maximum inductor current occurs at maximum load → Maximum output power rating per specified required output voltage

$$I_{L\max} = \bar{I}_L + \frac{|\Delta i_L|}{2} = \bar{V}_0 \left[ \frac{1}{R_{\min}} + \frac{(1 - D_{\min})}{2Lf} \right]$$

Calculated from Highest Input Voltage

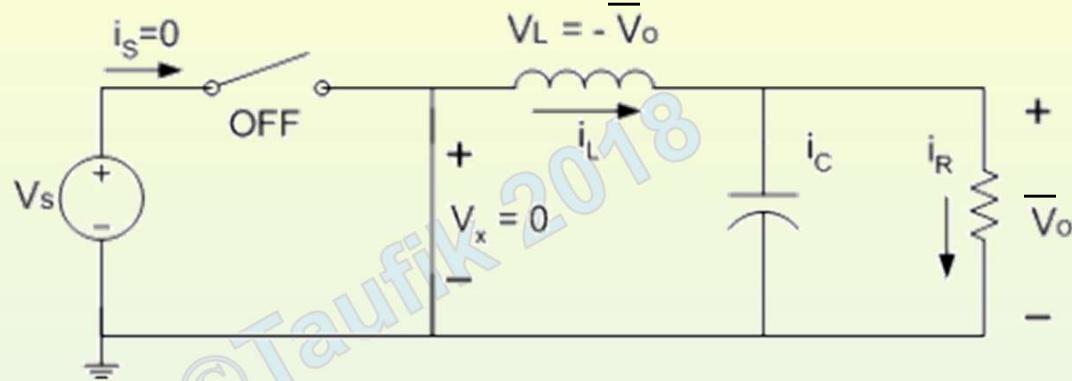
Chosen inductance value as discussed previously

# Sizing Switch: Voltage Rating



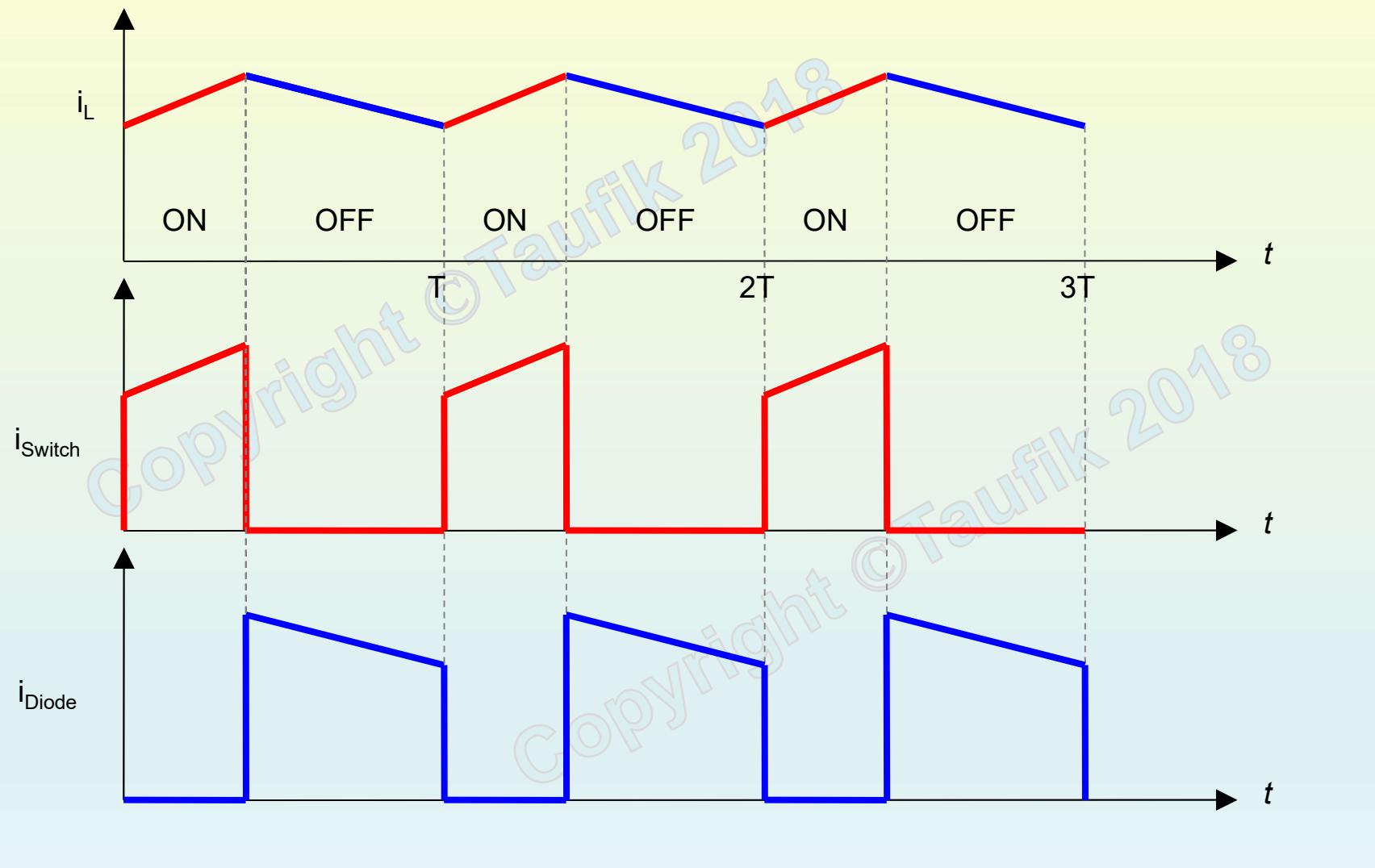
- With ideal diode and ideal buck, the  $V_{\text{switch-max}} = V_{\text{inmax}}$
- For non-ideal diode,  $V_{\text{switch-max}} = V_{\text{inmax}} + V_F$  where  $V_F$  is the maximum forward drop across the diode (calculated at maximum load current)
- Use safety factor of at least 20%
- For synchronous MOSFET, the rating would be  $V_{DS\text{max}}$

# Sizing Switch: Current Rating

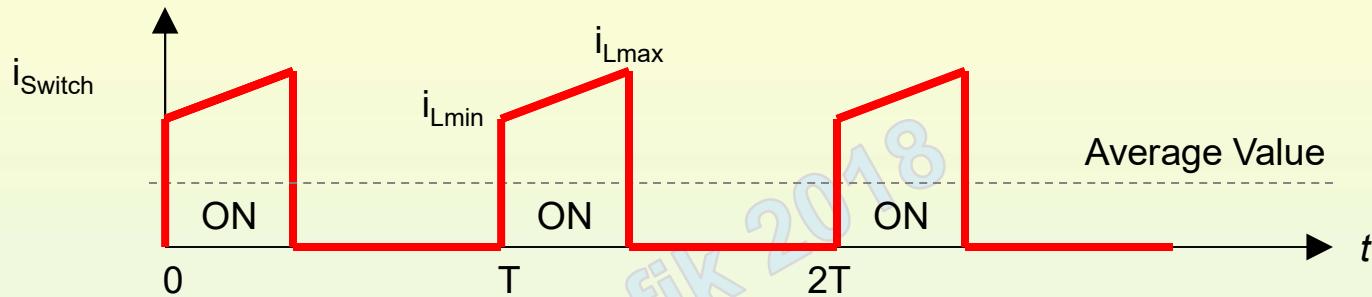


- Switch current rating is calculated based on average value
- Draw switch current waveform and then compute the average value
- By KCL, Inductor Current = Switch Current + Diode Current
- During  $t_{ON}$ , Inductor current equals switch current
- During  $t_{OFF}$ , Inductor current equals diode current

# Switch Current Waveform



# Switch Current Waveform for Current Rating



Average Switch Current is calculated from the area of the trapezoid

$$\bar{I}_{switch} = \frac{(i_{Lmin} + i_{Lmax})t_{on}}{2T}$$

$$\bar{I}_{switch} = \frac{([i_{Lmax} - \Delta i_L] + i_{Lmax})DT}{2T} = \frac{(2i_{Lmax} - \Delta i_L)D}{2}$$

$$\bar{I}_{switch} = \left( i_{Lmax} - \frac{\Delta i_L}{2} \right) D = \bar{I}_L D = \bar{I}_o D$$

$$\bar{I}_{switchmax} > \bar{I}_{omax} D$$

# MOSFET Rating Example

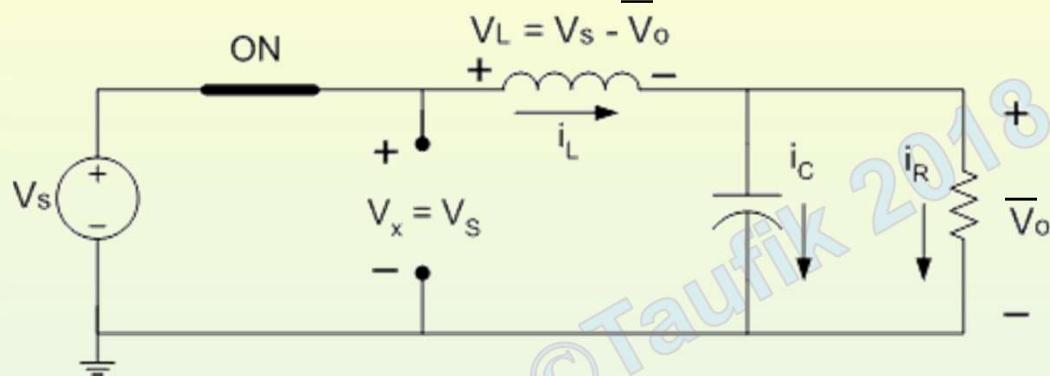
## **14A, 500V, 0.400 Ohm, N-Channel Power MOSFET**

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

### **Features**

- 14A, 500V
- $r_{DS(ON)} = 0.400\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature

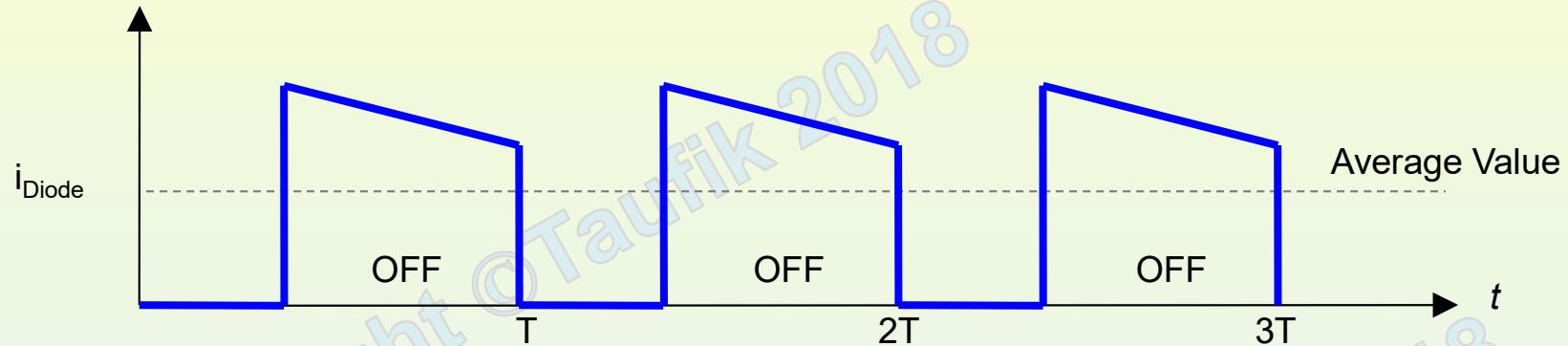
# Sizing Diode (Schottky): Voltage Rating



- Known as  $V_{RRM}$  is the maximum reverse voltage across the diode
- With ideal switch, the  $V_{RRM} = V_{inmax}$
- For non-ideal diode,  $V_{RRM} = V_{inmax} + V_{SW}$  where  $V_{SW}$  is the maximum forward drop across the switch (calculated at maximum load current)
- Allow at least > 20% safety factor

# Sizing Diode (Schottky): Current Rating

- Same approach as that for the switch current



$$\overline{I}_F = \frac{(i_{L_{\min}} + i_{L_{\max}}) \cdot t_{off}}{2 \cdot T}$$

$$\overline{I}_F = \frac{([i_{L_{\max}} - \Delta i_L] + i_{L_{\max}}) \cdot (1 - D) T}{2 \cdot T} = \frac{(2i_{L_{\max}} - \Delta i_L) \cdot (1 - D)}{2}$$

$$\overline{I}_F = \overline{I}_L \cdot (1 - D) = \overline{I}_o \cdot (1 - D)$$

$$\boxed{\overline{I}_F > \overline{I}_{o\max} \cdot (1 - D_{\min})}$$

# Schottky Diode Rating Example

SCHOTTKY RECTIFIER

2 Amp



## Major Ratings and Characteristics

Characteristics		Units
$I_{F(AV)}$ Rectangular waveform	2.0	A
$V_{RRM}$	45	V
$I_{FSM}$ @ $t_p = 5 \mu s$ sine	390	A
$V_F$ @ $1 A_{pk}, T_J = 125^\circ C$ (per leg)	0.50	V
$T_J$ range	-55 to 150	°C

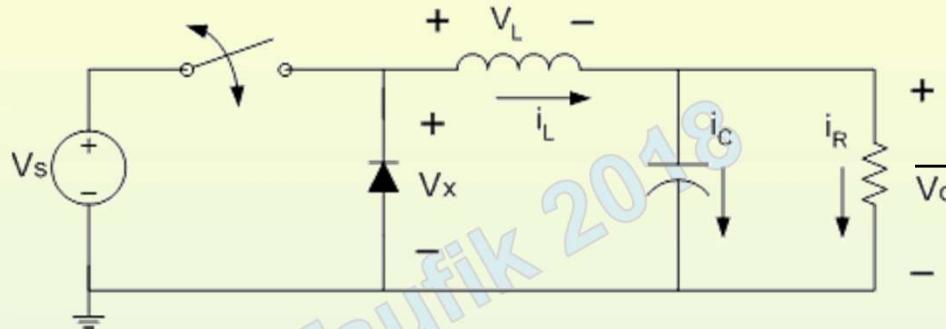
## Description/Features

The surface mount Schottky rectifier series has been designed for applications requiring very low forward drop and very small foot prints. Typical applications are in portables, switching power supplies, converters, automotive system, free-wheeling diodes, battery charging, and reverse battery protection.

- Small footprint, surface mountable
- Low profile
- Very low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- Common cathode

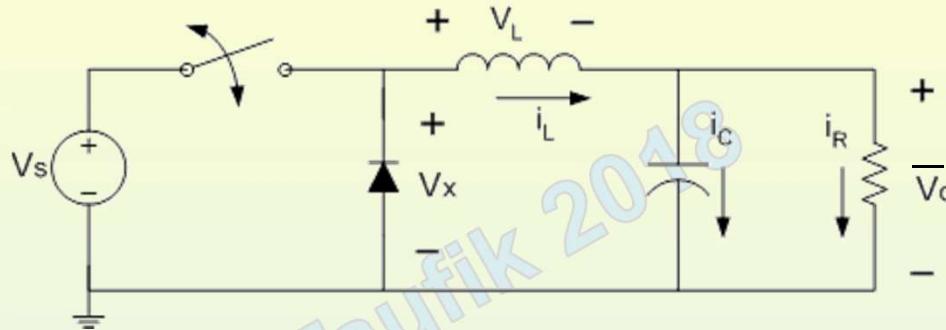
Courtesy of Infineon

# Sizing Output Capacitor: Voltage Rating

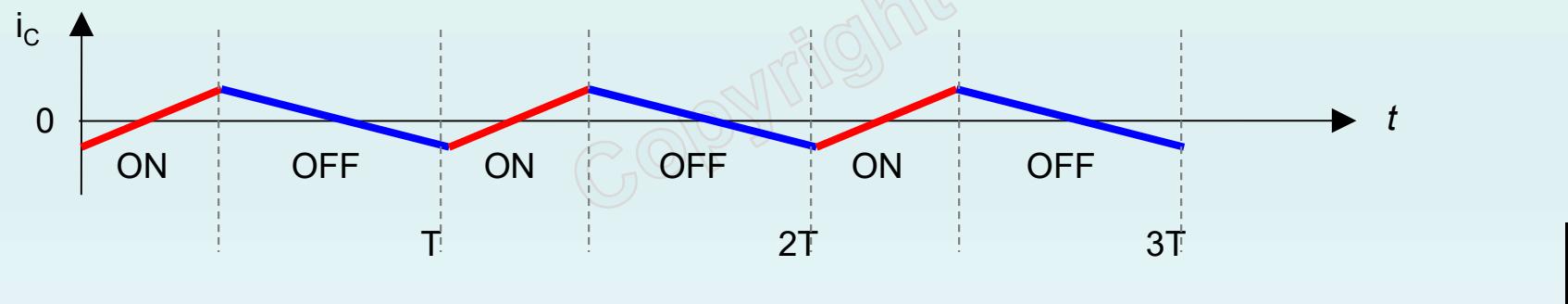


- Capacitor Voltage should withstand the maximum output voltage
  - Ideally:  $V_{cmax} = \bar{V}_o + \Delta V_o / 2$
  - More realistic: Capacitor has ESR (Equivalent Series Resistance) which worsens  $\Delta \bar{V}_o$
  - Output voltage ripple contributed by ESR is  $(\text{ESR} * \Delta i_L)$
  - Suppressing ripple contribution from ESR
    - Reduce ESR (Paralleling Caps, Low ESR Caps)
    - Reduce  $\Delta i_L$  by increasing L or increasing switching frequency

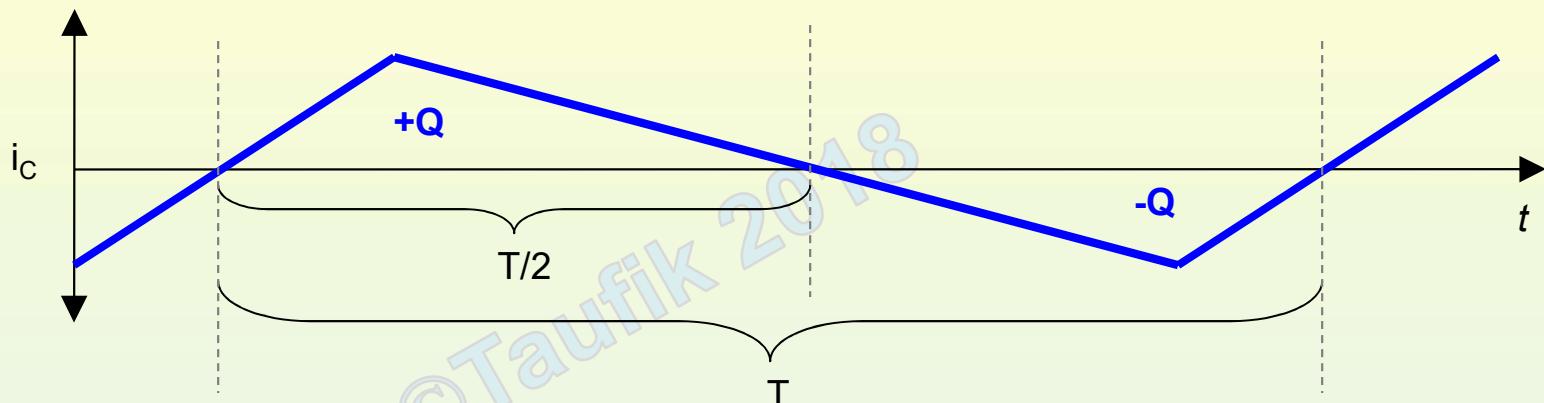
## Sizing Output Capacitor: Minimum Capacitance



- The AC component (ripple) of inductor current flows through the capacitor, leaving the average flowing through the load
- Capacitor current waveform will look like:



# Sizing Output Capacitor: Minimum Capacitance



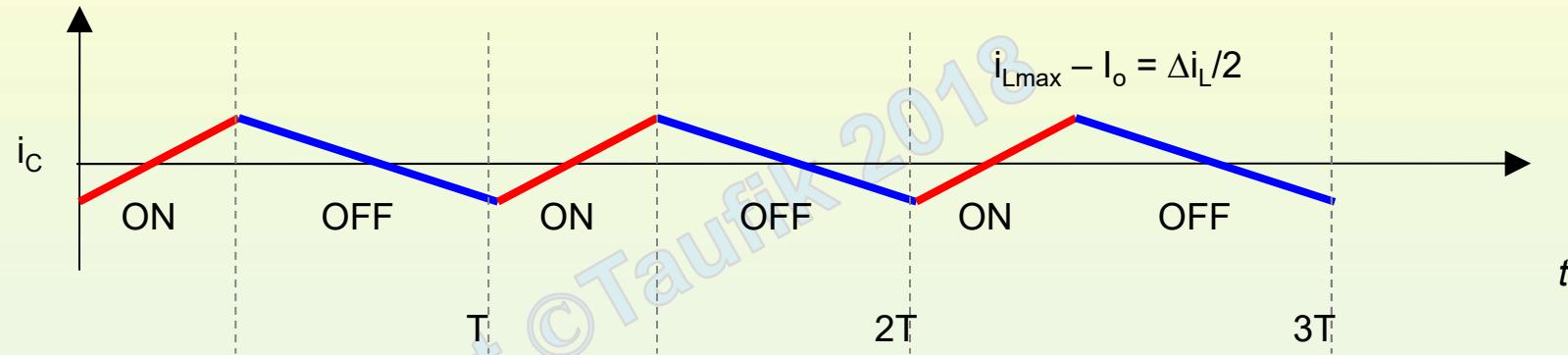
$$q = \text{Area} \cdot \Delta = \frac{1}{2} \left( \frac{T}{2} \right) \left( \frac{\Delta i_L}{2} \right) = \frac{\Delta i_L}{8f} = \frac{\bar{V}_o (1-D)T}{8f} = \frac{(1-D)\bar{V}_o}{8Lf^2}$$

$$q = C \cdot \Delta \bar{V}_o \Rightarrow C = \frac{q}{\Delta \bar{V}_o} = \frac{(1-D)\bar{V}_o}{8Lf^2 \Delta \bar{V}_o} = \frac{(1-D)}{8Lf^2 (\Delta \bar{V}_o / \bar{V}_o)}$$

$$C = \frac{(1 - D_{\min})}{8Lf^2 (\Delta \bar{V}_o / \bar{V}_o)}$$

→ Percent  $V_{\text{opp}}$

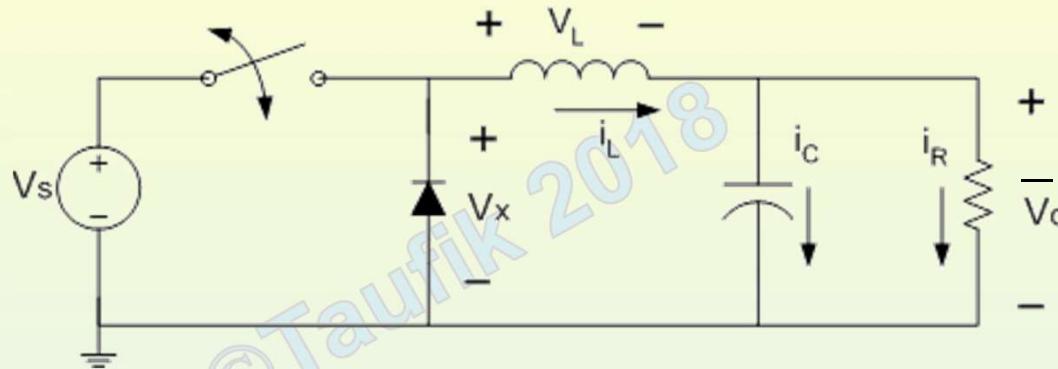
## Sizing Output Capacitor: RMS Current Rating



$$i_{Crms} = \frac{i_{Cpk}}{\sqrt{3}} = \frac{\Delta i_L/2}{\sqrt{3}} = \frac{(1 - D)\bar{V}_o}{2\sqrt{3}Lf}$$

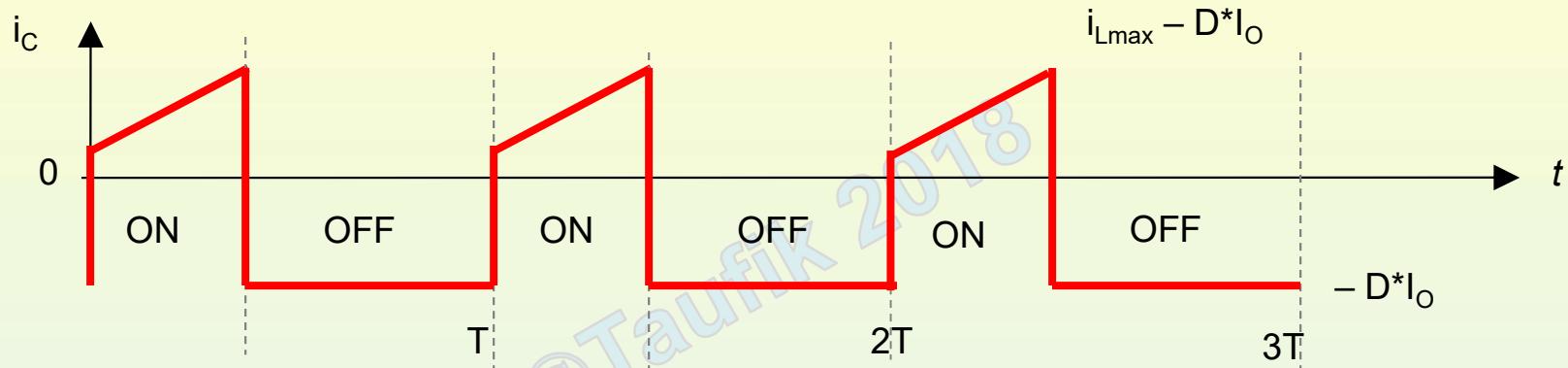
$$i_{Crms} = \frac{(1 - D_{min})\bar{V}_o}{2\sqrt{3}Lf}$$

# Sizing Input Capacitor: Voltage Rating



- Capacitor Voltage should withstand the max input voltage
  - Ideally:  $V_{cmax} = V_{inmax}$
  - More realistic: Capacitor has ESR (Equivalent Series Resistance) contributes to capacitor loss
  - Use of Electrolytic for energy storage in parallel with ceramic for high frequency transient energy requirement
  - Minimizing loss contribution from ESR
    - Reduce ESR (Paralleling Caps, Low ESR Caps)

## Sizing Input Capacitor: Minimum Capacitance

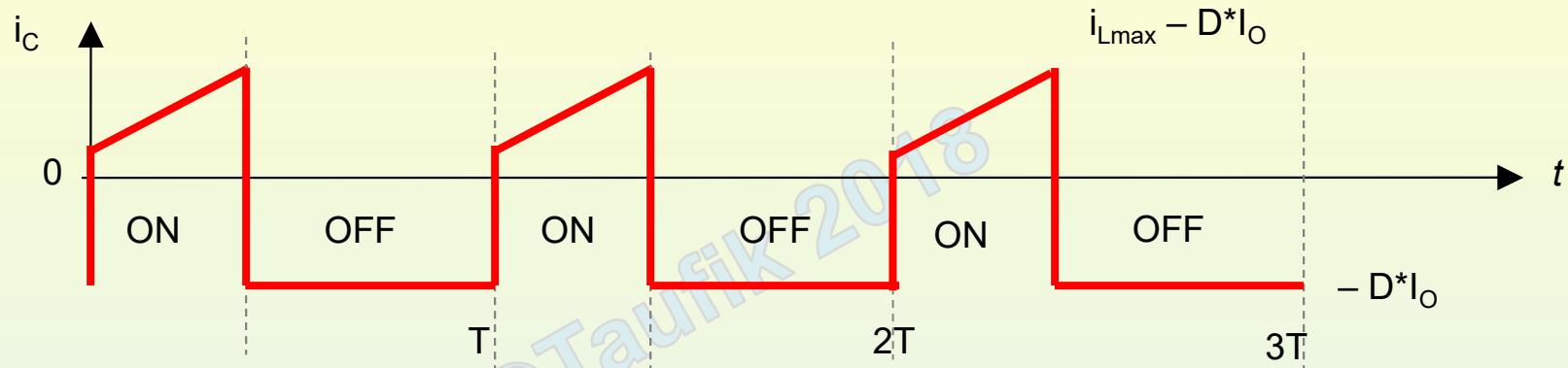


$$q = \text{Area} \cdot \square = t_{off} \cdot D \cdot I_O = (1 - D)T \cdot D \cdot I_O = \frac{(1 - D) \cdot D \cdot I_O}{f}$$

$$q = C \cdot \Delta V_{in} \Rightarrow C = \frac{q}{\Delta V_{in}} = \frac{(1 - D) \cdot D \cdot I_O}{f \Delta V_{in}} = \frac{(1 - D) \cdot D \cdot I_O}{f \Delta V_{in}}$$

$$C = \frac{(1 - D) \cdot D \cdot I_{O\max}}{f \Delta V_{in}}$$

# Sizing Input Capacitor: RMS Current Rating



Recall

$$I_{totrms}^2 = I_{acrms}^2 + I_{dc}^2 \Rightarrow I_{acrms} = \sqrt{I_{totrms}^2 - I_{dc}^2}$$

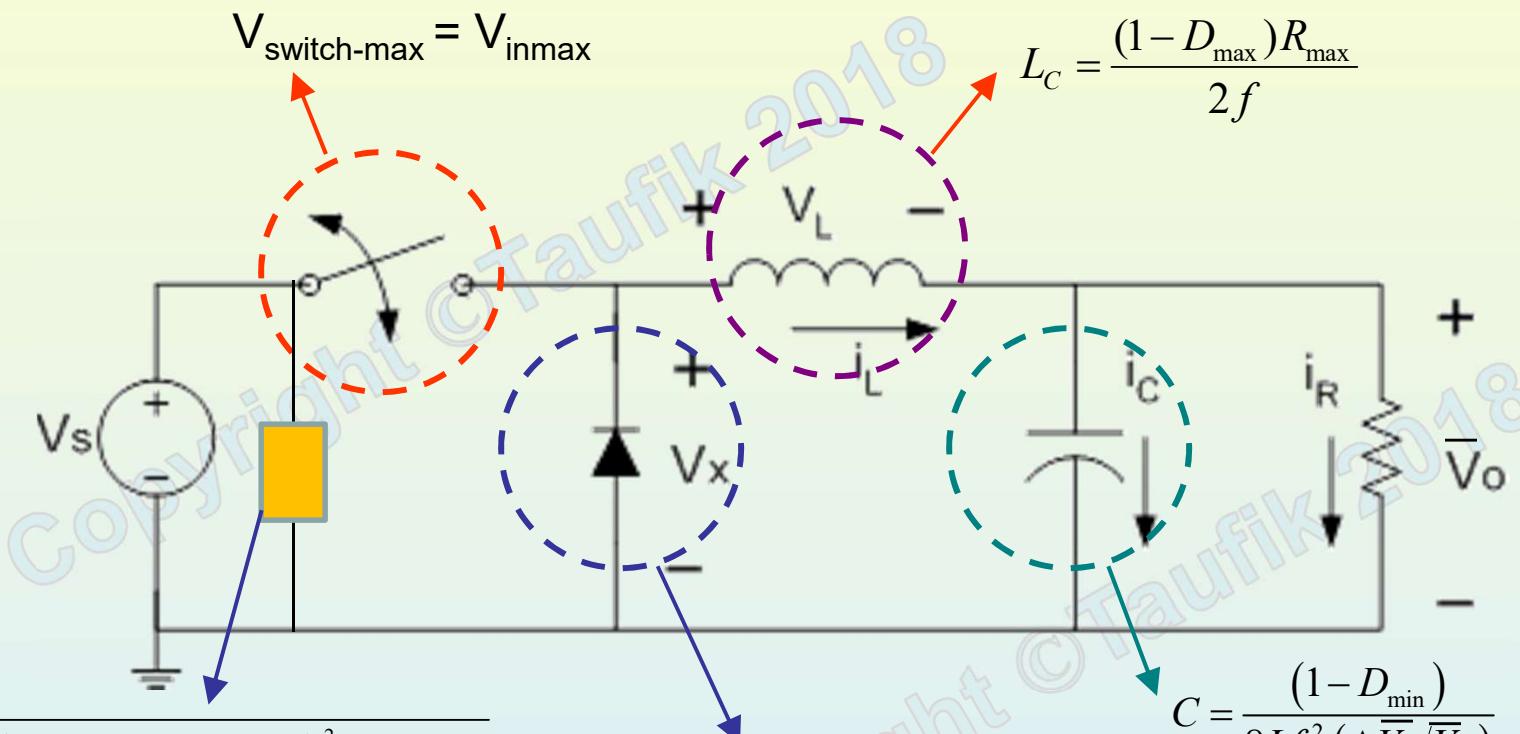
$$I_{Crms} = \sqrt{(I_{Switch-rms})^2 - (I_{switch-avg})^2}$$

$$I_{Crms} = \sqrt{\left( I_o \sqrt{D} \sqrt{\left( 1 + \left[ \frac{\Delta i_L}{2 \cdot I_o} \right] \right)^2} \right) - (D \cdot I_o)^2}$$

# To Summarize

$$\overline{I}_{\text{Switch-max}} > \overline{I}_{o\max} \cdot D_{\max}$$

$$V_{\text{switch-max}} = V_{\text{inmax}}$$



$$I_{L\max} = \bar{V}_0 \left[ \frac{1}{R_{\min}} + \frac{(1-D_{\min})}{2Lf} \right]$$

$$L_C = \frac{(1-D_{\max})R_{\max}}{2f}$$

$$I_{Crms} = \sqrt{\left( I_o \sqrt{D} \sqrt{\left( 1 + \left[ \frac{\Delta i_L}{2 \cdot I_o} \right] \right)^2} - (D \cdot I_o)^2 \right)}$$

$$C = \frac{(1-D) \cdot D \cdot I_{O\max}}{f \Delta V_{in}}$$

$$\overline{I}_F > \overline{I}_{o\max} \cdot (1-D_{\min})$$

$$V_{RRM} = V_{\text{inmax}}$$

$$C = \frac{(1-D_{\min})}{8Lf^2 (\Delta \bar{V}_o / \bar{V}_o)}$$

$$V_{c\max} = \bar{V}_o + \Delta \bar{V}_o / 2$$

$$i_{Crms} = \frac{(1-D_{\min}) \bar{V}_o}{2\sqrt{3}L}$$

# Simple Buck Design: 12V to 2.5V 1A

**Given:**  $V_s := 12V$        $V_o := 2.5V$        $I_{omax} := 1A$

$I_{occm} := 0.1A$        $\%V_o := 1\%$        $f := 50kHz$

**Solution:**

$$D := \frac{V_o}{V_s} \quad D = 0.208$$

**Inductor:**

$$L_{crit} := \frac{(1 - D)}{2 \cdot f} \cdot \frac{V_o}{I_{occm}} \quad L_{crit} = 1.979 \times 10^{-4} H$$

Choose:  $L := 200 \cdot 10^{-6} H$

$$I_{Lmax} := I_{omax} + \frac{(1 - D) \cdot V_o}{2 \cdot L \cdot f} \quad I_{Lmax} = 1.099 A$$

$$\Delta I_L := \frac{(1 - D) \cdot V_o}{L \cdot f} \quad \Delta I_L = 0.198 A$$

# Simple Buck Design: 12V to 2.5V 1A

## MOSFET:

$$V_{ds} := V_s$$

$$V_{ds} = 12 \text{ V}$$

$$I_d := D \cdot I_{omax}$$

$$I_d = 0.208 \text{ A}$$

## Diode:

$$V_{rrm} := V_s$$

$$V_{rrm} = 12 \text{ V}$$

$$I_f := (1 - D) \cdot I_{omax}$$

$$I_f = 0.792 \text{ A}$$

## Capacitor:

$$V_{cmax} := V_o + \frac{\%V_o \cdot V_o}{2}$$

$$V_{cmax} = 2.513 \text{ V}$$

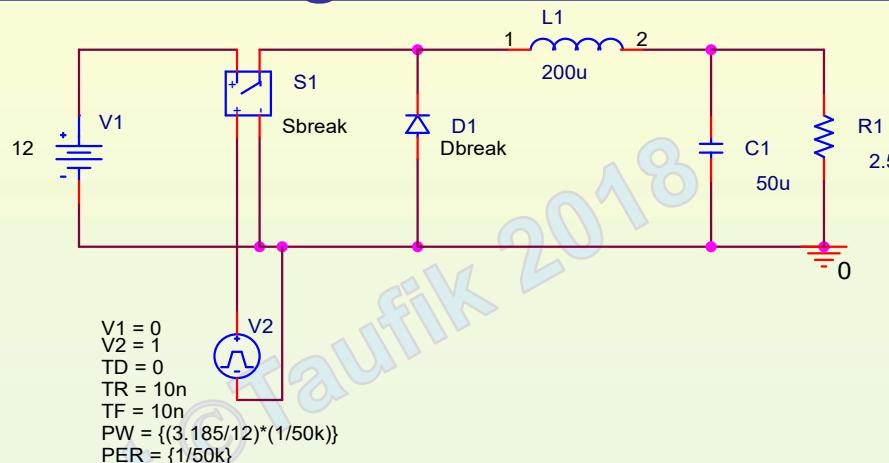
$$C := \frac{(1 - D)}{8 \cdot L \cdot f^2} \cdot \frac{1}{\%V_o}$$

$$C = 1.979 \times 10^{-5} \text{ F}$$

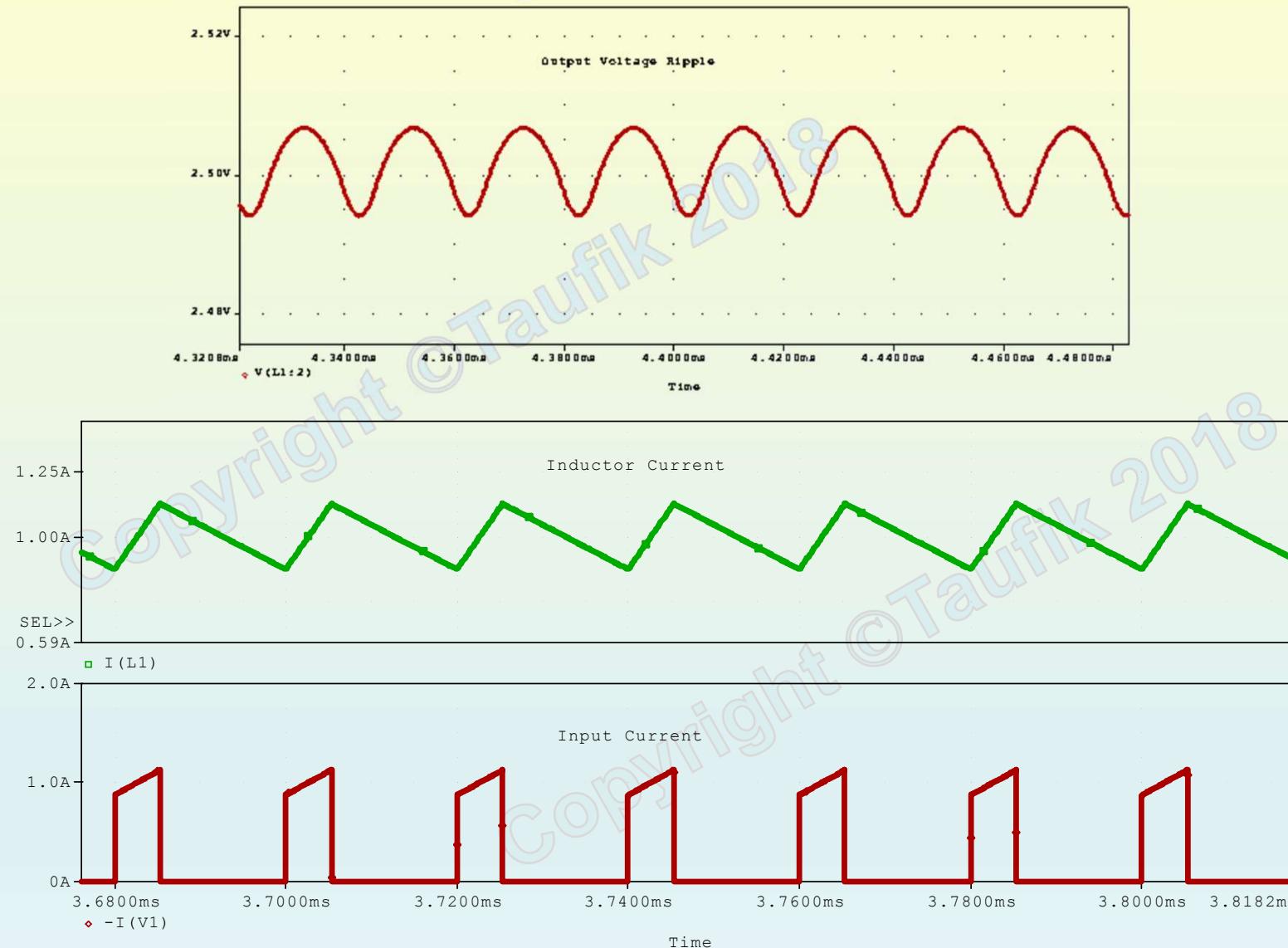
$$\text{Choose } C_o := 50 \cdot 10^{-6} \text{ F}$$

$$\%V_o := \frac{(1 - D)}{8 \cdot L \cdot f^2 \cdot C_o} \quad \%V_o = 0.396 \%$$

# Simple Buck Design: 12V to 2.5V 1A



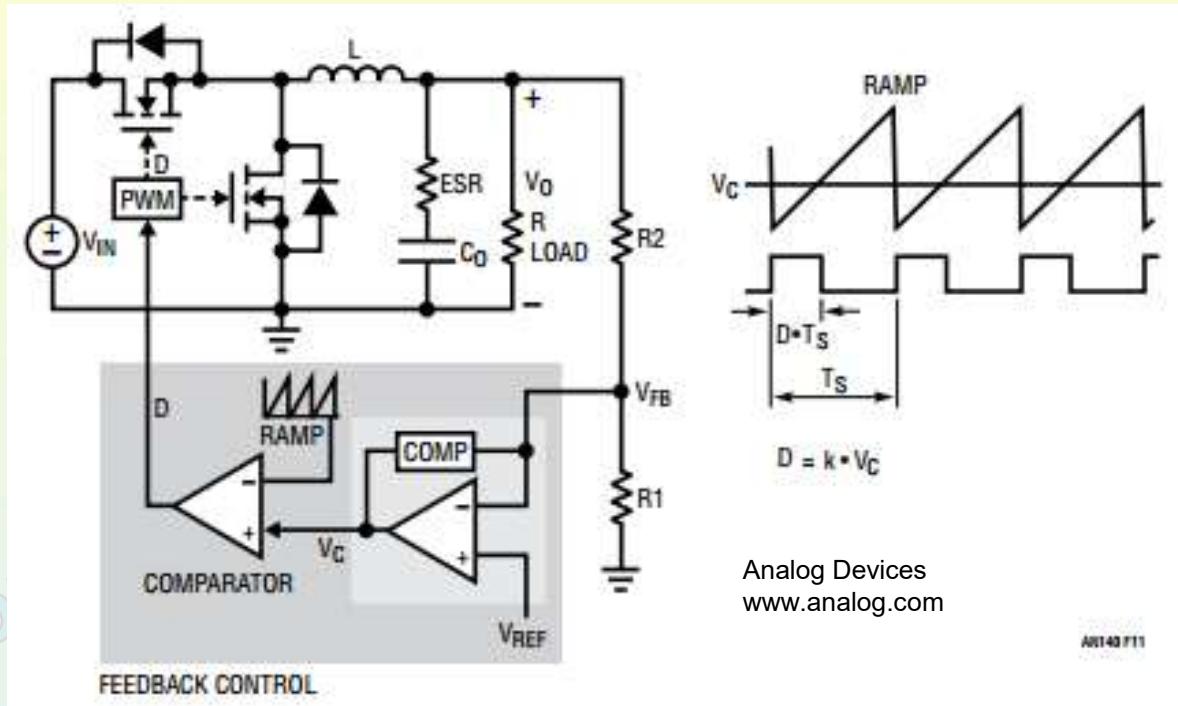
# Simple Buck Design: 12V to 2.5V 1A



# Closing the Loop

- As a minimum requirement, a practical buck converter must employ a voltage feedback by sensing its output voltage to maintain a constant output voltage
  - This method is called the Voltage Mode Control
  - The more popular method is the Current Mode Control where another feedback mechanism is provided (explained later)
- With Voltage Mode, the output voltage is sensed by a voltage divider whose mid-output voltage is compared with a reference voltage provided inside a controller → Error Signal
- The controller then processes the error signal to generate a pulse signal outputted into the switch (gate of the MOSFET used in the Buck as an example)

# Closing the Loop

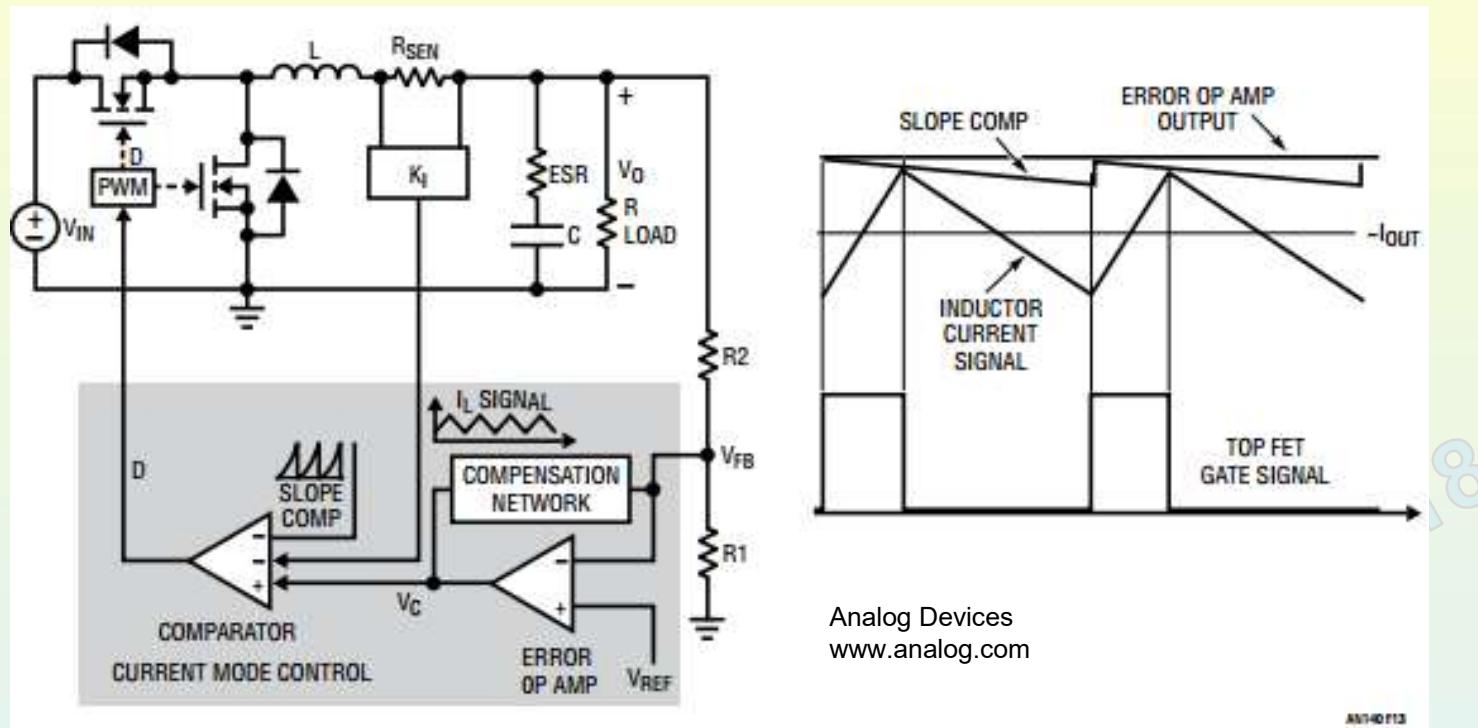


Analog Devices  
[www.analog.com](http://www.analog.com)

AN140-9T1

- Circuit diagram of Voltage Mode Control is shown above (courtesy of Analog Devices, Application Note 140-9)
- In practice, resistors  $R_1$  and  $R_2$  must be large enough to prevent loading
- Often, potentiometer is used for  $R_1$  for fine adjustment of output voltage
  - $R_2$  is part of feedback path and sometimes a series RC network is connected in parallel with  $R_2$  for compensation purpose

# Closing the Loop

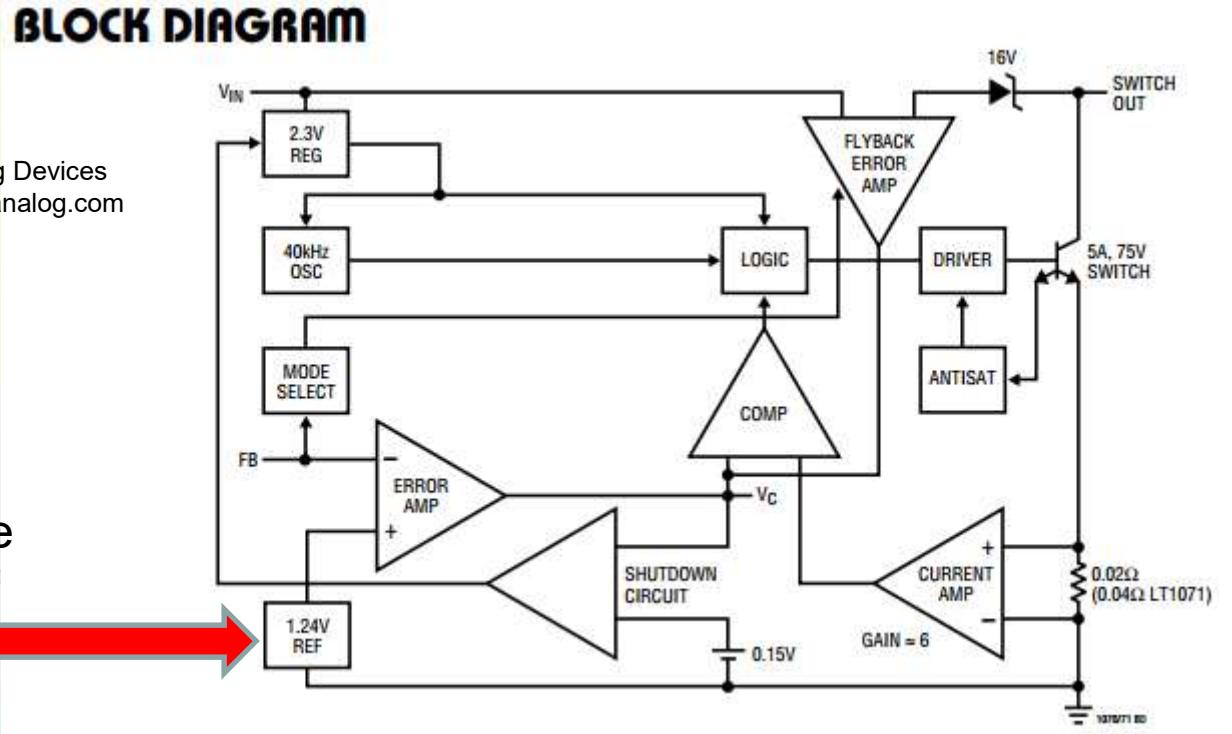


- Circuit diagram of Current Mode Control is shown above (courtesy of Analog Devices, Application Note 140-9)
- In practice, the additional sensor is for current through the TOP MOSFET since it carries the same peak current information as the inductor current, plus it is for the more efficient sensing method

# Closing the Loop

Analog Devices  
[www.analog.com](http://www.analog.com)

1.24 Voltage  
Reference



- Output of voltage divider must be set to equal to the reference voltage (1.24V in above example) per desired output voltage

# Closing the Loop

- Referring to previous two figures, if say a 5V output is desired then R1 and R2 are set following voltage divider equation

$$V_{reference} = \bar{V}_o \cdot \frac{R1}{R1 + R2}$$

- Note that Vreference and Vout are known, R1 and R2 are not
- Select R2 then solve for R1 (since R1 may use potentiometer)

$$R1 - \left( \frac{V_{reference}}{\bar{V}_o} \right) R1 = \left( \frac{V_{reference}}{\bar{V}_o} \right) R2 \Rightarrow R1 = \frac{\left( \frac{V_{reference}}{\bar{V}_o} \right) R2}{1 - \left( \frac{V_{reference}}{\bar{V}_o} \right)}$$

- If say R2 is chosen to be 100 kΩ, then for a 5V output with 1.24V reference the R1 value will be

$$R1 = \frac{\left( \frac{V_{reference}}{\bar{V}_o} \right) R2}{1 - \left( \frac{V_{reference}}{\bar{V}_o} \right)} = \frac{\left( \frac{1.24}{5} \right) 100}{1 - \left( \frac{1.24}{5} \right)} = \frac{24.8}{0.752} = 32.98 \text{ k}\Omega$$

# Buck with Feedback Example

## DESIGN EXAMPLE: BUCK REGULATOR

The following example illustrates the design of an ideal Buck Regulator in Continuous Conduction Mode which is maintained down to 10% of the full load current of 5A

### Given Parameters

Input Voltage                       $V_{in} := 48V$

Output Voltage                       $V_o := 12V$

Switching Frequency               $f_s := 100kHz$                       Hence

$$T_s := \frac{1}{f_s}$$

Full Load Current                 $I_{omax} := 10A$

Percent minload-CCM             $ccm := 10\%$

Output Vpp-ripple                 $\Delta V_o := 10 \cdot 10^{-3}V$

### Parameter dan Design Calculations

The ideal ON-time of the switch

$$t_{on} := \frac{V_o}{V_{in}} \cdot T_s$$

$$t_{on} = 2.5 \times 10^{-6} s$$

### Minimum Output Current while still maintaining CCM

$$I_{omin} := ccm \cdot I_{omax} \quad I_{omin} = 1 \text{ A}$$

Determine the Critical Inductance

$$L_c := \frac{V_{in} - V_o}{2 \cdot I_{omin}} \cdot t_{on} \quad L_c = 4.5 \times 10^{-5} \text{ H}$$

Choose a bigger inductor (say 10% bigger)  $L := 1.1 \cdot L_c$

$$L = 4.95 \times 10^{-5} \text{ H}$$

With the chosen inductor, the minimum output current can now be recomputed

$$I_{omin} := \frac{V_{in} - V_o}{2 \cdot L} \cdot t_{on} \quad I_{omin} = 0.909 \text{ A}$$

Next we will determine  $I_{Lmin}$  and  $I_{Lmax}$  at Full load

Initial Guesses for  $I_{Lmin}$  and  $I_{Lmax}$

$$I_{Lmin} := 1 \text{ A} \quad I_{Lmax} := 1 \text{ A}$$

Given TWO equations in terms of  $I_{Lmin}$  and  $I_{Lmax}$

Given

$$\frac{I_{Lmax} + I_{Lmin}}{2} = I_{omax}$$

$$I_{Lmax} - I_{Lmin} = \frac{V_{in} - V_o}{L} \cdot t_{on}$$

$$\begin{pmatrix} IL_{min} \\ IL_{max} \end{pmatrix} := \text{find}(IL_{min}, IL_{max})$$

Hence, at **FULL** load

$$IL_{min} = 9.091A \quad IL_{max} = 10.909A$$

$$\Delta IL := IL_{max} - IL_{min} \quad \Delta IL = 1.818A$$

Next we will determine  $IL_{min}$  and  $IL_{max}$  at Minimum load

Initial Guesses for  $IL_{min}$  and  $IL_{max}$        $IL_{min1} := 1A$

$IL_{max1} := 1A$

Given TWO equations in terms of  $IL_{min}$  and  $IL_{max}$

Given

$$\frac{IL_{max1} + IL_{min1}}{2} = I_{omin}$$

$$IL_{max1} - IL_{min1} = \frac{V_{in} - V_o}{L} \cdot t_{on}$$

$$\begin{pmatrix} IL_{min1} \\ IL_{max1} \end{pmatrix} := \text{Find}(IL_{min1}, IL_{max1})$$

Hence, at MINIMUM load

$$IL_{min1} = 0 \text{ A}$$

$$IL_{max1} = 1.818 \text{ A}$$

$$\Delta IL1 := IL_{max1} - IL_{min1}$$

$$\Delta IL1 = 1.818 \text{ A}$$

#### Finding Output Capacitor Value

Compute approximate value of ESR       $ESR := \frac{\Delta V_o}{\Delta IL}$        $ESR = 5.5 \times 10^{-3} \Omega$

Assume we will be using Electrolytic Capacitor whose  $ESR \cdot C = 65 \mu\text{s}$

$$C_o := \frac{65 \cdot 10^{-6} \text{ s}}{ESR} \quad C_o = 0.012 \text{ F}$$

Choose next standard value of the capacitor       $C_o := 15 \cdot 10^{-3} \text{ F}$

Recalculate ESR with the chosen capacitor

$$ESR := \frac{65 \cdot 10^{-6} \text{ s}}{C_o}$$
$$ESR = 4.333 \times 10^{-3} \Omega$$

Ripple due to Capacitor charge and discharge

$$\Delta V_c := \frac{\Delta I_L \cdot T_s}{8C_o}$$
$$\Delta V_c = 1.515 \times 10^{-4} \text{ V}$$

Ripple due to Capacitor's ESR

$$\Delta V_{esr} := \Delta I_L \cdot ESR$$
$$\Delta V_{esr} = 7.879 \times 10^{-3} \text{ V}$$

Total Ripple

$$\Delta V_{tot} := \Delta V_c + \Delta V_{esr}$$
$$\Delta V_{tot} = 8.03 \times 10^{-3} \text{ V}$$

**STOP! Check to see if  $\Delta V_{tot}$  meets the RIPPLE requirement!**

Next we compute RMS capacitor current

Equation of IL during ON time

$$IL1(t) := IL_{min} + \frac{\Delta IL}{ton} \cdot t$$

Equation of IL during OFF time

$$IL2(t) := IL_{max} + \frac{-\Delta IL}{Ts - ton} \cdot t$$

$$I_{crms} := \sqrt{\frac{1}{Ts} \left[ \int_{0s}^{ton} (IL1(t) - I_{max})^2 dt + \int_{ton}^{Ts} (IL2(t) - I_{max})^2 dt \right]}$$

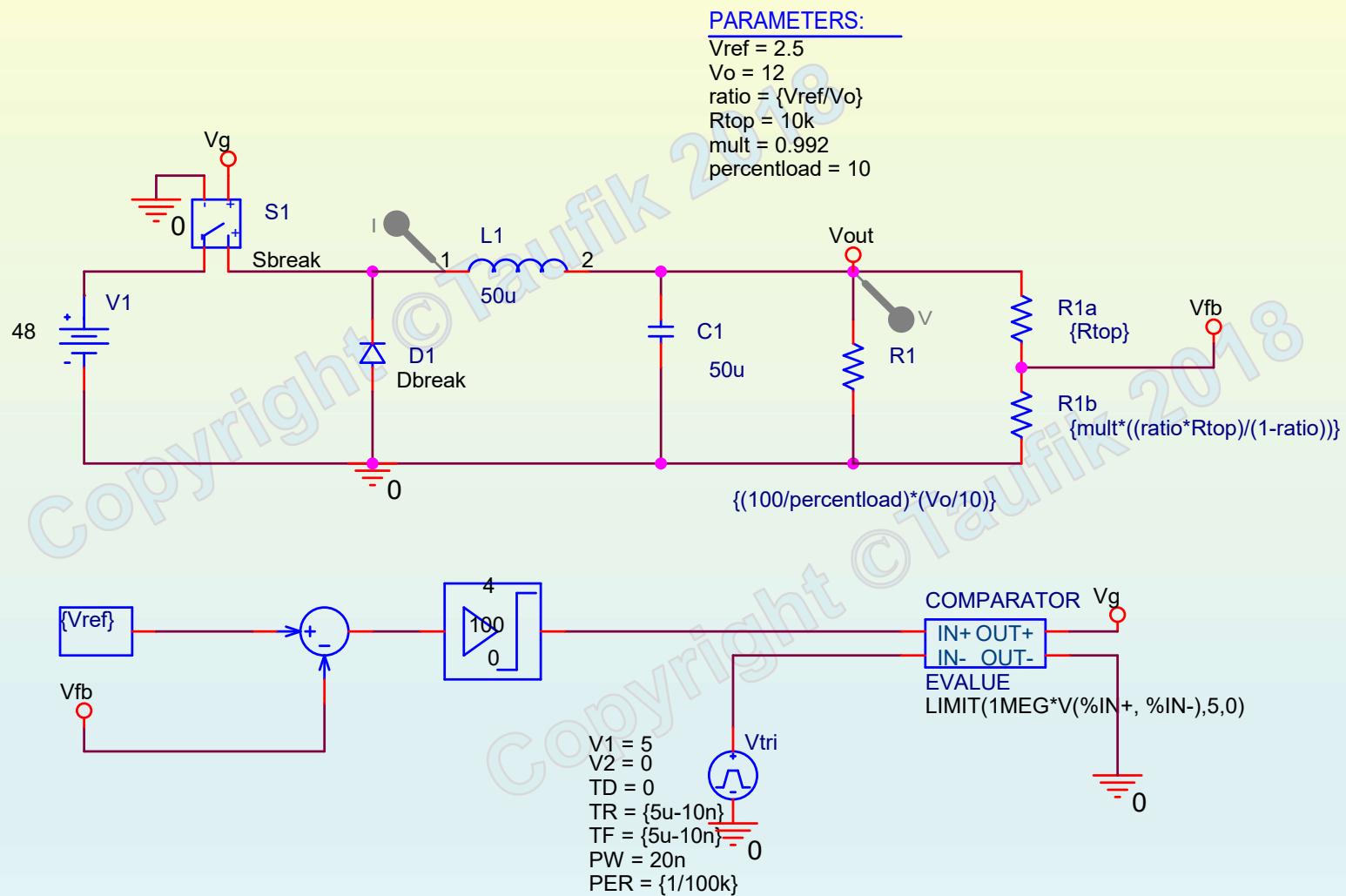
$$I_{crms} = 0.742A$$

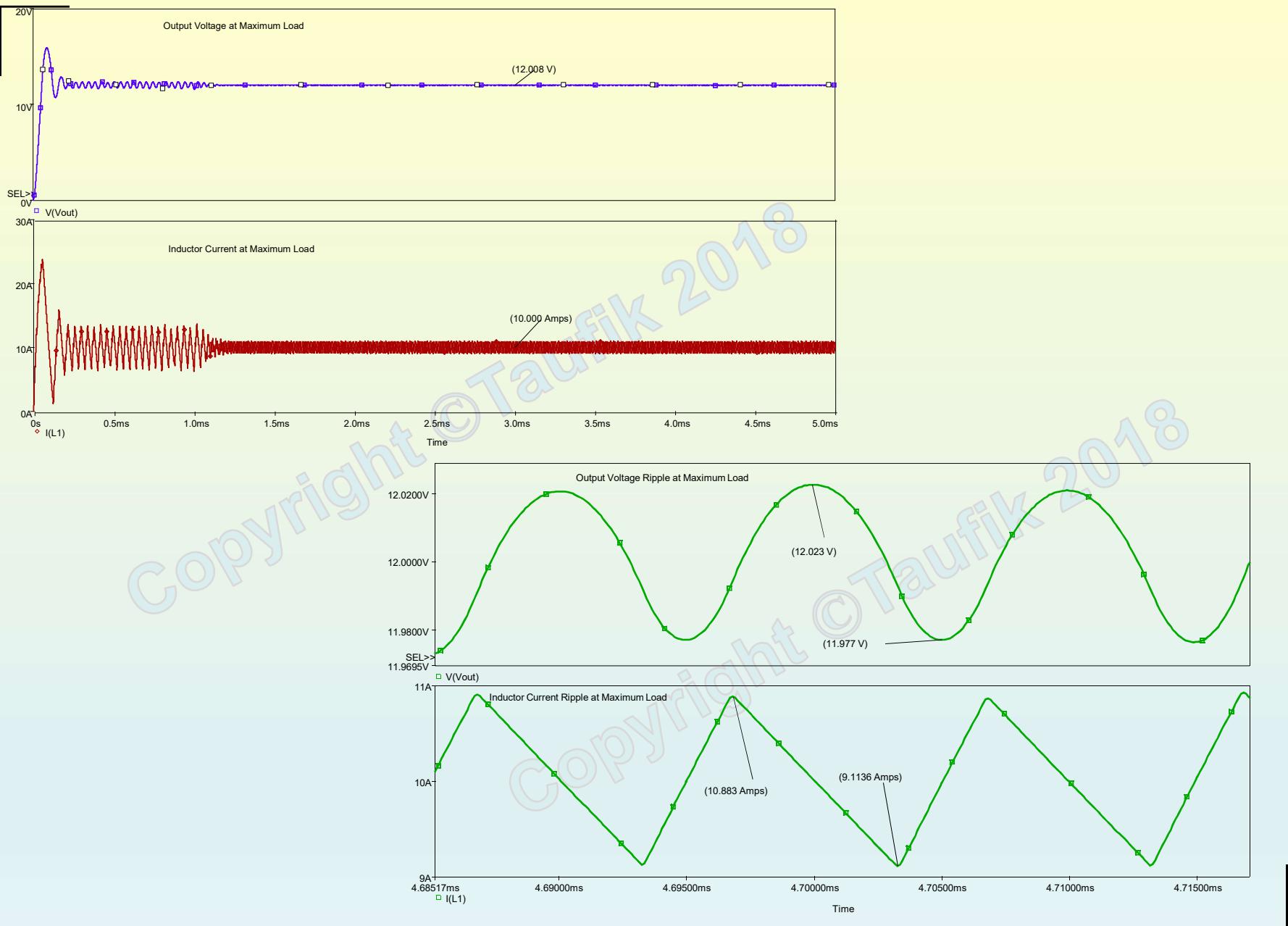
Power Loss in the Capacitor

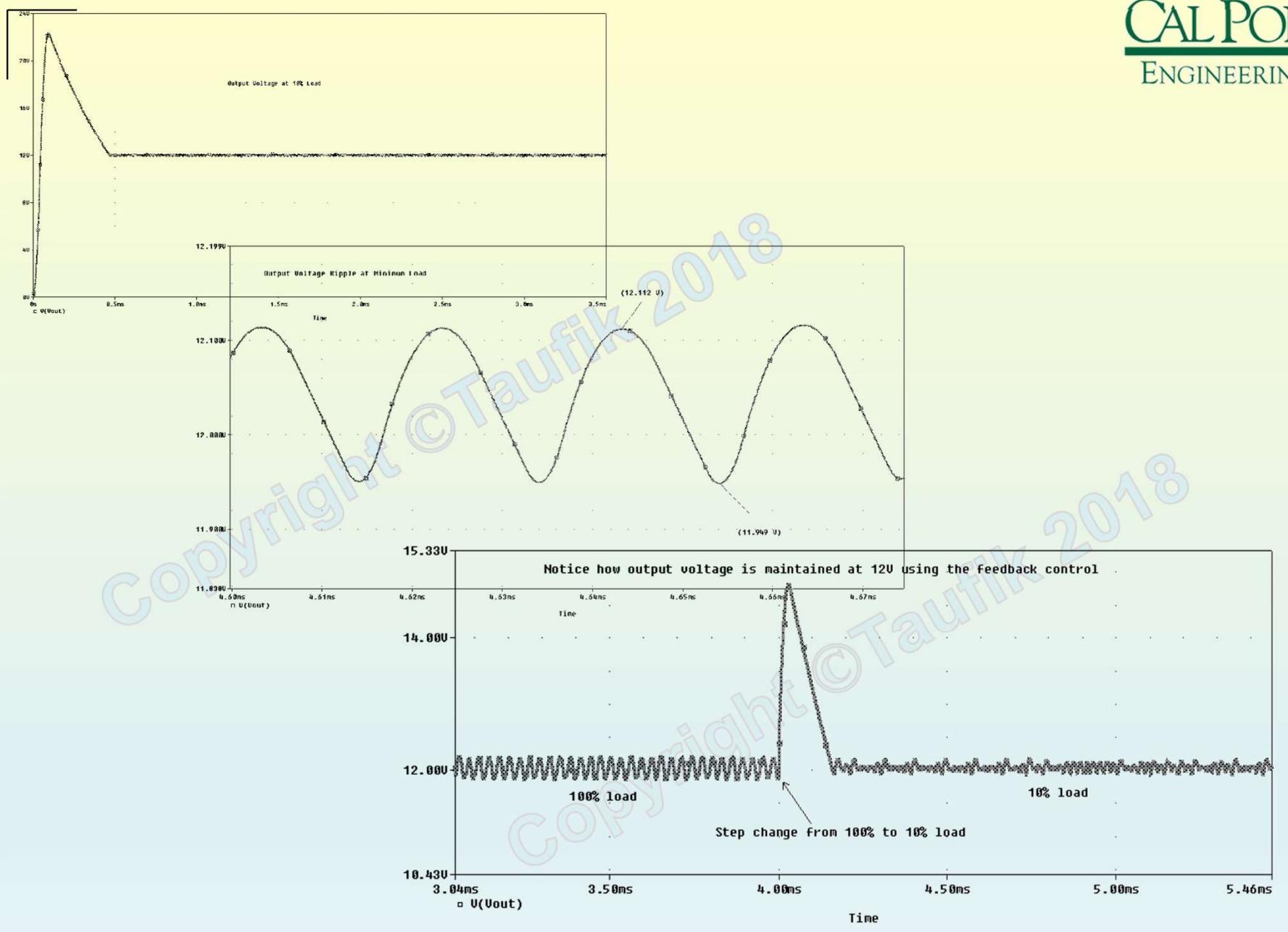
$$P_{cap} := I_{crms}^2 ESR$$

$$P_{cap} = 2.388 \times 10^{-3} W$$

## Using OrCAD Pspice Schematics





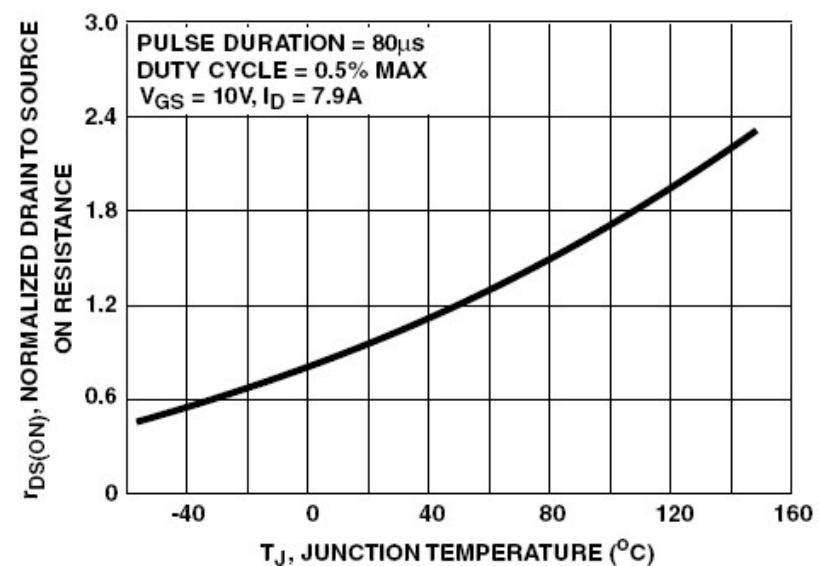
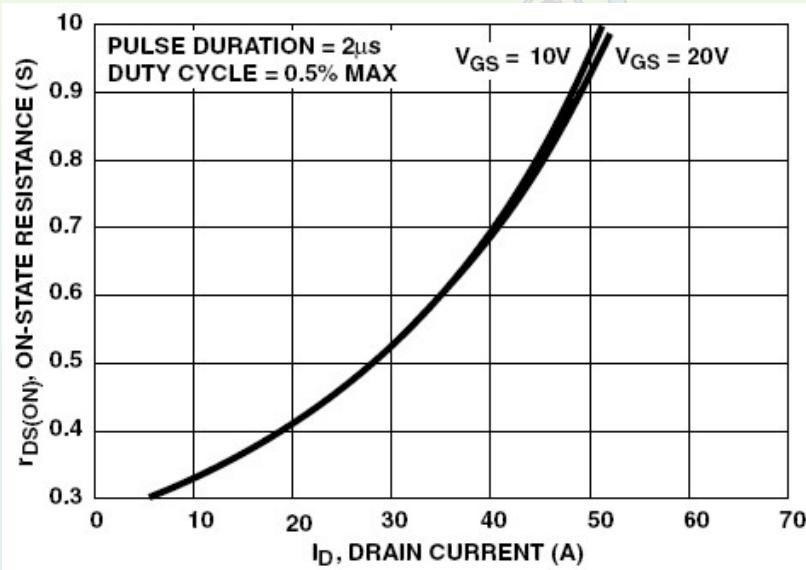


## Non-ideal Buck: Loss Considerations

- When efficiency estimation is required in the design, losses in Buck circuit should be considered
- Several major losses to consider:
  - Static loss of MOSFET
  - Switching loss of MOSFET
  - MOSFET Gate Drive Losses
  - Static loss of diode
  - Switching loss of diode
  - Inductor's copper loss
  - Capacitor's ESR loss

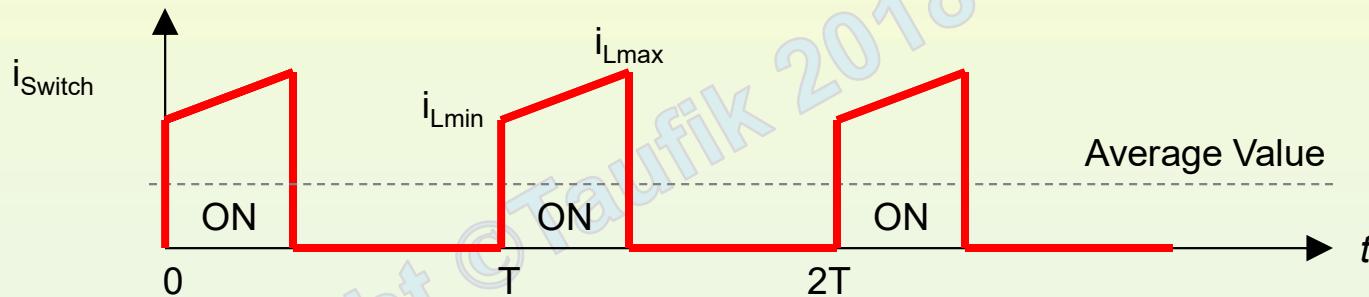
# Static Loss of MOSFET

- With MOSFET, its on resistance  $R_{DSon}$  directly impacts the conduction (static) loss
- $R_{DSon}$  depends on applied gate voltage and MOSFET's junction temperature



# Static Loss of MOSFET

- Recall, switch current:



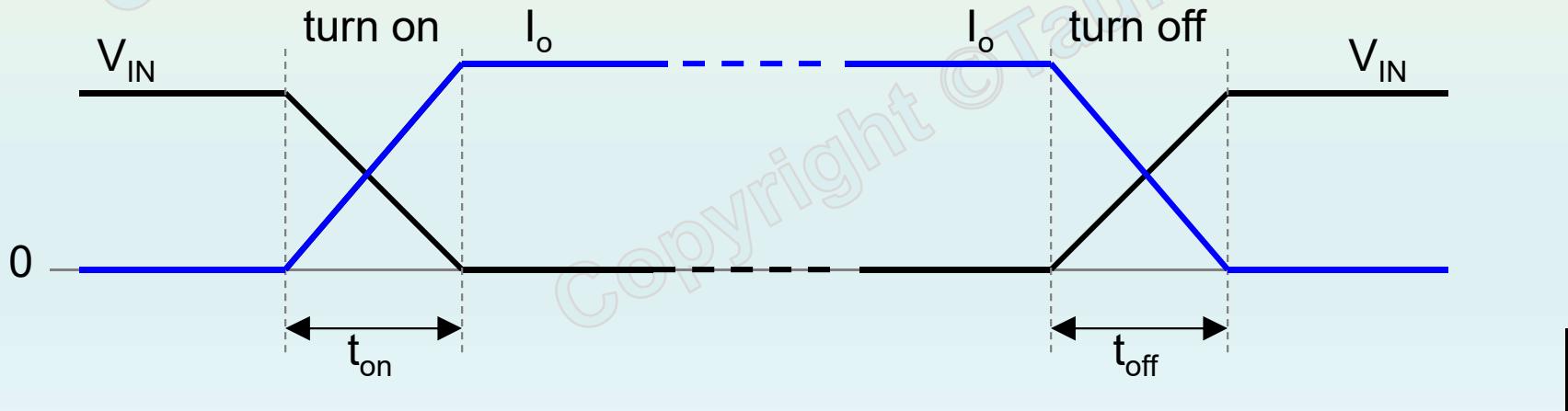
- Static loss for MOSFET with  $R_{DSon}$ :

$$P_{\text{static}} = I_{\text{switch-rms}}^2 \cdot R_{DSon}$$

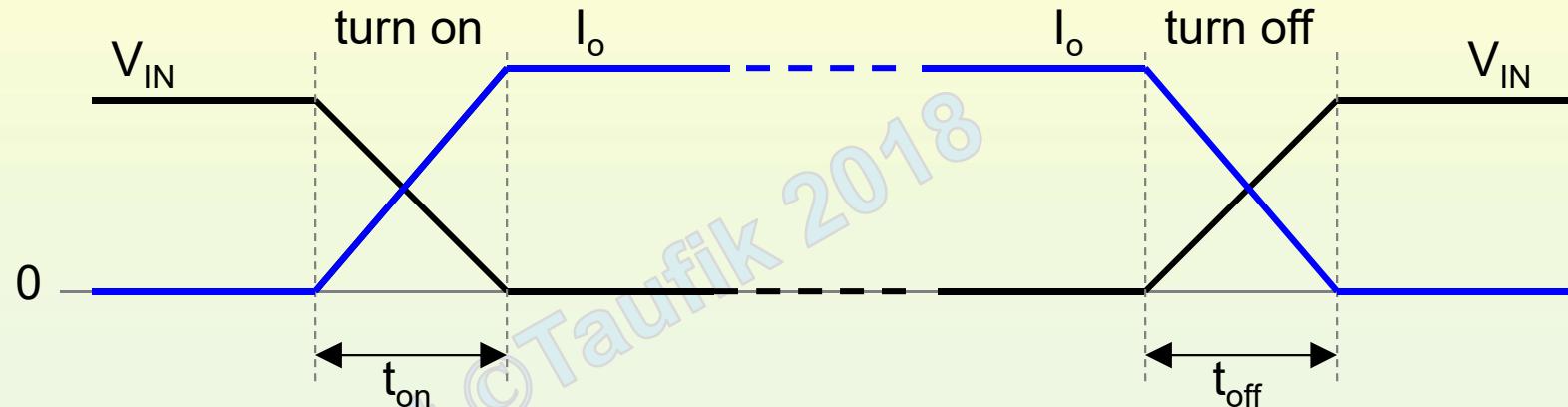
$$P_{\text{static}} = \left( I_o \sqrt{D} \sqrt{\left( 1 + \left[ \frac{\Delta i_L}{2 \cdot I_o} \right] \right)} \right)^2 \cdot R_{DSon}$$

# Switching Loss of MOSFET

- The switching loss depends on how the voltage and current overlaps
- May be approximated with a scenario where voltage and current start moving simultaneously and reach their endpoints
- The overlap causes power loss ( $V \times I$ )
- Will assume to occur both at turn-on and turn-off transitions



# Switching Loss of MOSFET



$$P(t_{on}) = \frac{I_o V_{in} t_{on}}{6T}$$

$$P(t_{off}) = \frac{I_o V_{in} t_{off}}{6T}$$

$$P_{switching} = P(t_{on}) + P(t_{off}) = \frac{I_o V_{in} t_{on}}{6T} + \frac{I_o V_{in} t_{off}}{6T}$$

$$P_{switching} = \frac{I_o V_{in}}{6T} (t_{on} + t_{off})$$

## Switching Loss of MOSFET & Gate Drive Loss

- When MOSFET is off, its output capacitance  $C_{oss}$  is being charged → translates to loss

$$P_{Coss} = \frac{1}{2} C_{oss} V_{in}^2 f_s$$

- Gate drive loss comes from the total gate charge  $Q_{gate}$  and the gate drive voltage  $V_{gate}$  used

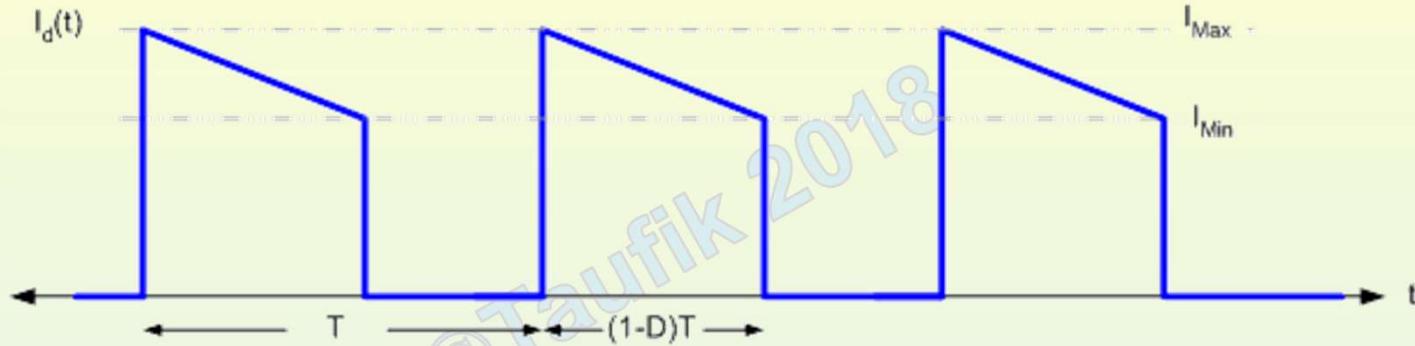
$$P_{gate} = \frac{1}{2} Q_{gate} V_{gate} f_s$$

# Static Loss of Diode: Forward Loss

- Losses that occur during diode's fully on (forward loss) and fully off (reverse loss) conditions
- Forward loss come from the product of diode's forward voltage ( $V_F$ ) and forward current ( $I_F$ ), in addition to the rms loss due to diode dynamic resistance,  $r_d$

$$P_{forward} = \underbrace{V_f \cdot \bar{I}_f}_{\text{Average Values}} + \underbrace{\tilde{I}_f^2 \cdot r_d}_{\text{RMS Value}}$$

# Static Loss of Diode: Forward Loss



$$P_{forward} = V_f \cdot \bar{I}_f + \tilde{I}_f^2 \cdot r_d \quad \text{From datasheet}$$

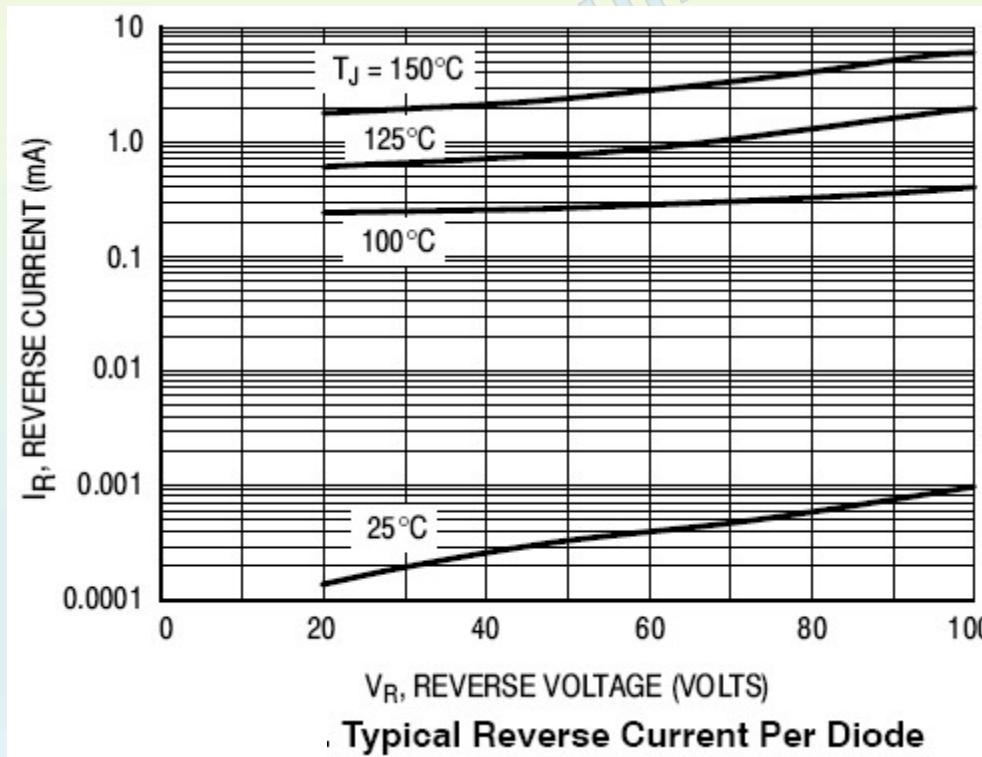
$$\bar{I}_f = (1 - D) \cdot \bar{I}_o$$

$$\tilde{I}_f = \sqrt{\frac{(1-D)}{3} [I_{max}^2 + I_{min}^2 + I_{max} \cdot I_{min}]}$$

# Static Loss of Diode: Reverse Loss

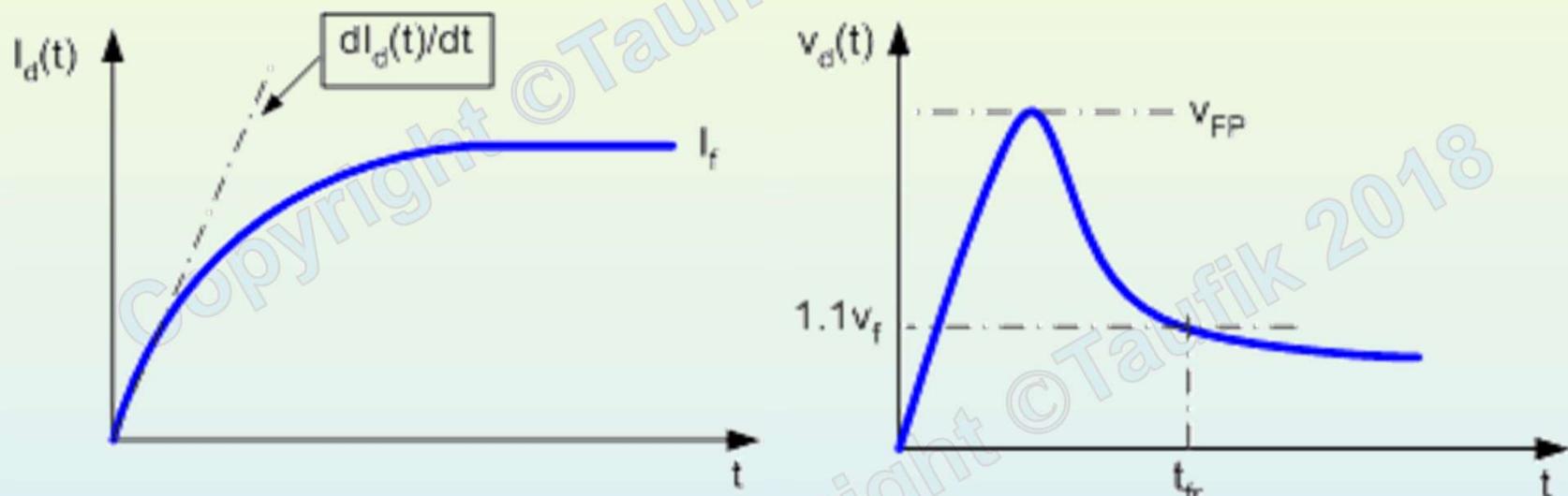
- Loss occurs when the diode is in the fully off or non-conducting condition

$$P_{reverse} = V_r \cdot I_r \cdot (1 - D)$$



# Switching Loss of Diode: Turn On Loss

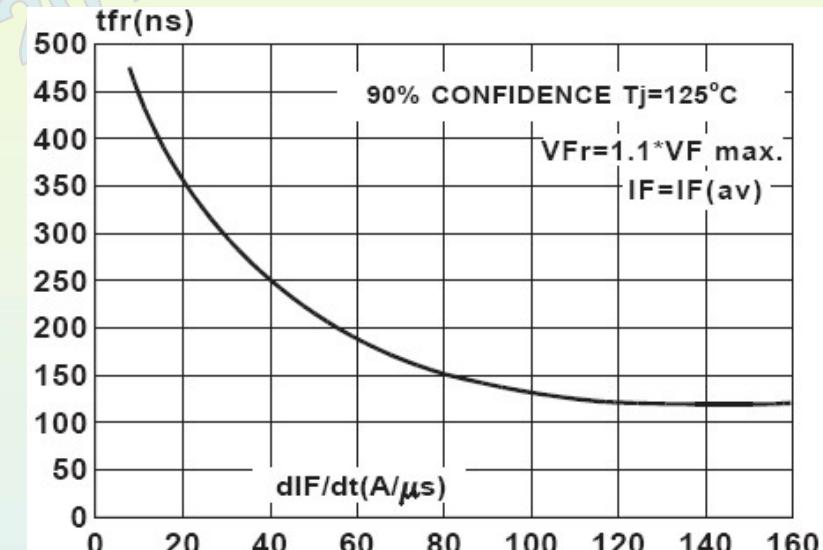
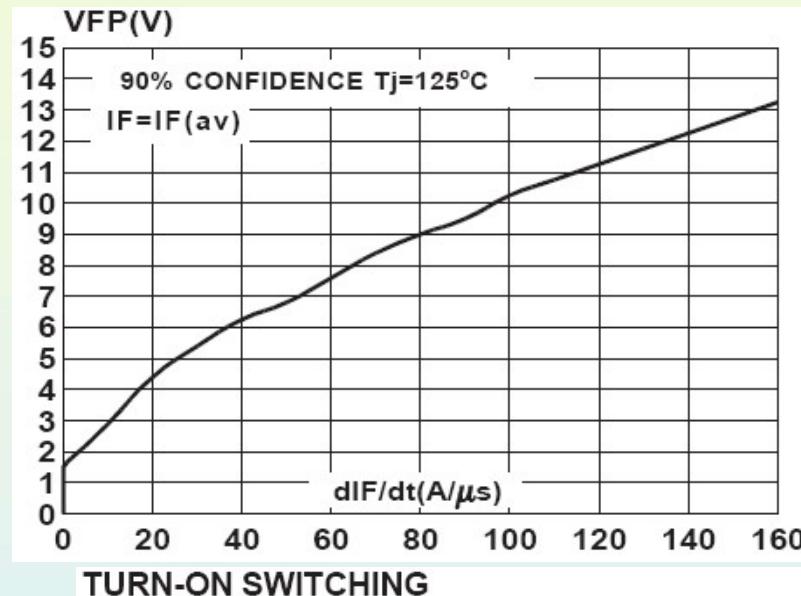
- The switching behavior at turn-on is characterized by a low value of peak forward voltage ( $V_{FP}$ ) and forward recovery time ( $t_{fr}$ )



$$P_{ON} = 0.4 \cdot (V_{FP} - V_f) \cdot t_{fr} \cdot I_f \cdot f$$

# Switching Loss of Diode: Turn On Loss

- Both  $V_{FP}$  and  $t_{fr}$  are normally plotted against  $dI_d(t)/dt$  in the datasheet, whereas  $dI_d(t)/dt$  itself is also available in the datasheet for a given set of conditions

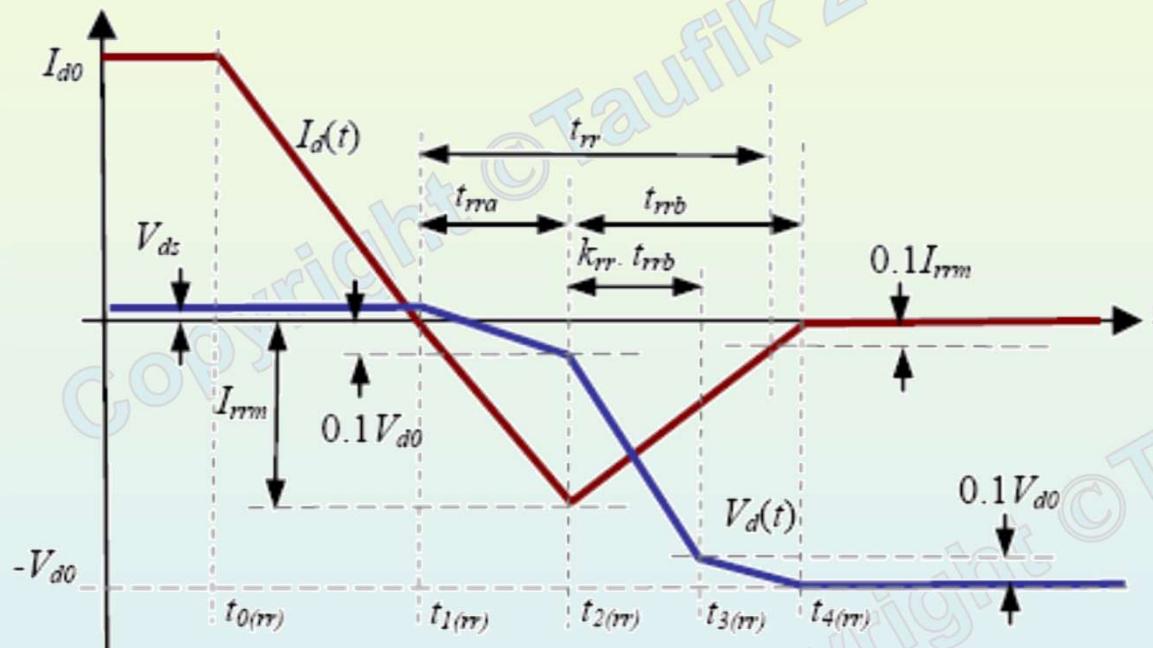


TURN-ON SWITCHING

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{fr}$	Forward recovery time	$T_j = 25^\circ C$ $I_F = 8 A$ , $dI_F/dt = 64 A/\mu s$ measured at, $1.1 \times V_{F\max}$			500	ns
$V_{FP}$	Peak forward voltage	$T_j = 25^\circ C$ $I_F = 8 A$ , $dI_F/dt = 64 A/\mu s$			10	V

# Switching Loss of Diode: Turn Off Loss

- Turn-off loss constitutes appreciable switching losses due to the overlapping of diode voltage and current at turn-off with its associated reverse-recovery time



$$t_{rra} = I_{rrm} \sqrt{\frac{I_{d0}}{\left(\frac{dI_d}{dt}\right|_{t_{1(rr)}}}}$$

$$t_{rrb} = 1.11 \cdot (t_{rr} - t_{rra})$$

$$[t_{2rr}, t_{3rr}] = k_{rr} \cdot t_{rrb}$$

$$P_{off} = 0.5V_{ds}I_{d0} \left( \frac{I_{d0}}{\left(\frac{dI_d}{dt}\right|_{t_{1(rr)}}} \right) + 0.033V_{d0}I_{rrm}t_{rra} + V_{d0}I_{rrm}(0.467 - 0.433k_{rr} + 0.15k_{rr}^2)t_{rrb}$$

# Inductor's Copper Loss

- Inductor's winding is made of copper and hence inherently it will have resistive loss



- With inductor's dc resistance of  $R_L$  and inductor's rms current, the copper loss of inductor is:

$$P_L = \tilde{I}_L^2 R_L$$

$$\tilde{I}_L = I \sqrt{1 + \frac{1}{3} \left( \frac{\Delta i_L}{2I} \right)^2}$$

# Inductor's Core Loss

- Factors affecting core loss: switching frequency F, temperature, flux swing B
- General form:

$$\text{Core Loss} = (\text{Core Loss}/\text{Unit Volume}) \times \text{Volume}$$

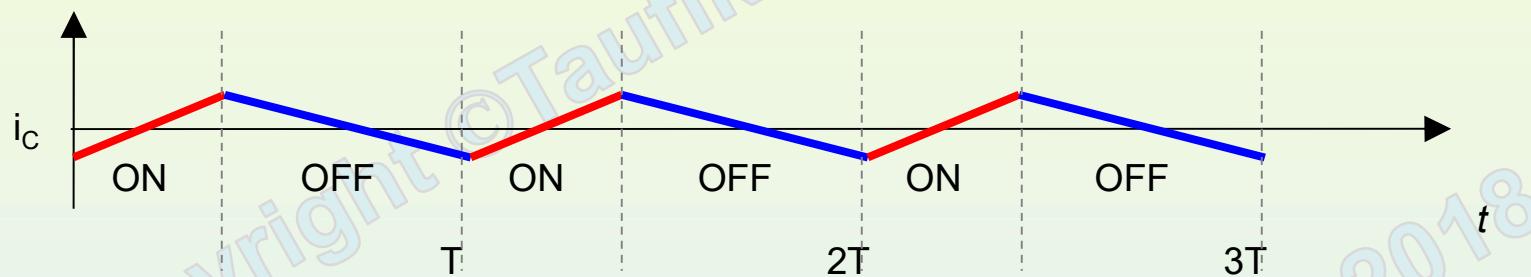
Where,

$$\text{Core Loss}/\text{Unit Volume} = k_1 \times B^{k_2} \times F^{k_3}$$

- Constants  $k_1$ ,  $k_2$ , and  $k_3$  are normally provided by the core manufacturers

# Capacitor's ESR Loss

- Real world capacitors possess ESR (Equivalent Series Resistance)
- ESR can measured with, for example, Capacitor Wizard



- Loss due to Capacitor's ESR is:  $P_{ESR} = \tilde{I}_C^2 \cdot ESR$

$$\tilde{I}_C = \frac{\Delta i_L}{2\sqrt{3}}$$

# Buck Design With Losses

## Buck Design with Losses

Taufik

Maximum Output Power:	$P_{\text{omax}} := 120\text{W}$	$\mu \equiv 1 \cdot 10^{-6}$
Nominal Output Voltage:	$V_{\text{on}} := 12\text{V}$	$m \equiv 1 \cdot 10^{-3}$
Nominal Input Voltage:	$V_{\text{in}} := 24\text{V}$	
Switching Frequency:	$f_s := 250\text{kHz}$	
Minimum Percent CCM:	$I_{\text{ccm}} := 10\%$	
Maximum Ripple Percentage:	$V_{\text{opp}} := 2\%$	

### Design Calculations and Sizing Components:

Nominal Duty Cycle:

$$D := \frac{V_{\text{on}}}{V_{\text{in}}} = 0.5$$

Critical Inductance:

$$L_c := \frac{(1 - D) \cdot \left( \frac{V_{\text{on}}^2}{I_{\text{ccm}} \cdot P_{\text{omax}}} \right)}{2 \cdot f_s} = 12.000 \text{H} \cdot \mu$$

Choose  $L > L_c$

$L_o := 200 \mu\text{H}$  with assumed DC resistance of:  $R_{L_o} := 100\text{m}\Omega$

Peak Inductor Current:

$$I_{\text{lopk}} := V_{\text{on}} \cdot \left[ \frac{1}{V_{\text{on}}^2} + \frac{(1 - D)}{2 \cdot L_o \cdot f_s} \right] = 10.06\text{A}$$

Switch Voltage:

$$V_{\text{swmax}} := V_{\text{in}} = 24\text{V}$$

Switch Current:

$$I_d := D \cdot \frac{P_{\text{omax}}}{V_{\text{on}}} = 5\text{ A}$$

#### Choose MOSFET IRF7471 40V 10A Rdson 13mΩ

Diode Vrrm:  $V_{rrm} := V_{inom} = 24\text{V}$

Diode Forward Current:  $I_f := (1 - D) \cdot \frac{P_{omax}}{V_{inom}} = 5\text{A}$

#### Choose MBR3040

Capacitor Voltage Rating:  $V_{cap} := V_{inom} + \left( \frac{V_{opp} \cdot V_{inom}}{2} \right) = 12.12\text{V}$

Capacitance:  $C_o := \frac{(1 - D)}{8 \cdot L_o \cdot F_s^2 \cdot V_{opp}} = 250 \times 10^{-3} \text{F}\cdot\mu$

RMS Current Rating:  $I_{caprms} := \frac{(1 - D) \cdot V_{inom}}{2\sqrt{3} \cdot L_o \cdot F_s} = 0.035\text{A}$

#### Choose a 25V 50uF capacitor

### Power Loss Calculations

MOSFET Loss Calculations:  $R_{dson} := 13\text{m}\cdot\Omega$        $n := 0..11$

$Load_n :=$

0.01
5
10
20
30
40
50
60
70
80
90
100

Output Current Array:

$$I_{o_n} := \left( \frac{\frac{Load_n}{100} \cdot P_{omax}}{V_{inom}} \right)$$

Static Loss:

$$I_{drms_n} := I_{o_n} \cdot \sqrt{D} \cdot \sqrt{1 + I_{ccm}}$$

$$P_{mos1_n} := \left( I_{o_n} \cdot \sqrt{D} \cdot \sqrt{1 + I_{ccm}} \right)^2 R_{dson}$$

Switching Loss:       $t_{on1} := 12\text{ns}$        $t_{off1} := 15\text{ns}$        $C_{oss} := 700\text{pF}$        $Q_g := 21\text{nC}$

$$P_{mos2} := \frac{I_o_n \cdot V_{inom} (t_{on1} + t_{off1}) \cdot F_s}{6} \quad V_g := 12\text{V}$$

$$P_{coss} := \frac{1}{2} \cdot C_{oss} \cdot V_{inom}^2 \cdot F_s = 0.05\text{W} \quad P_{gate} := \frac{1}{2} \cdot Q_g \cdot V_g \cdot F_s = 0.032\text{W}$$

$$P_{mostot} := P_{mos1} + P_{mos2} + P_{coss} + P_{gate}$$

### Diode Loss Calculations

$$I_{favg} := I_o_n \cdot (1 - D)$$

From Diode Datasheet:

$$V_f :=$$

0.02V
0.46V
0.5V
0.58V
0.61V
0.64V
0.66V
0.68V
0.7V
0.71V
0.73V

Dynamic Resistance:

$$R_d := \frac{0.62\text{V} - 0.4\text{V}}{4\text{A} - 0.5\text{A}} = 0.063\Omega$$

Peak to peak  
Inductor Current

$$\Delta I_L := \frac{V_{inom} \cdot (1 - D)}{L_o \cdot F_s} = 0.12\text{A}$$

$$I_{frms} := \sqrt{\frac{(1 - D)}{3} \cdot \left[ \left( I_o_n + \frac{\Delta I_L}{2} \right)^2 + \left( I_o_n - \frac{\Delta I_L}{2} \right)^2 + \left( I_o_n - \frac{\Delta I_L}{2} \right) \cdot \left( I_o_n + \frac{\Delta I_L}{2} \right) \right]}$$

$$P_{d1} := V_f \cdot I_{favg} + \left( I_{frms} \right)^2 R_d$$

From Datasheet:       $V_r := V_{inom} - V_{out}$        $I_r := 0.00015\text{A}$

$$P_{d2} := V_r I_r (1 - D) = 0.001\text{W}$$

Assume:  $t_{fr} := 500\text{ns}$        $V_{fp} := 10\text{V}$

$$P_{d3n} := 0.4 \left( V_{fp} - V_{f_n} \right) \cdot t_{fr} \cdot I_{favg_n} \cdot F_s$$

$$P_{dtotn} := P_{d1n} + P_{d2} + P_{d3n}$$

### Inductor Loss Calculation

$$IL_{rmsn} := I_{on} \cdot \sqrt{1 + \frac{1}{3} \cdot \left( \frac{\Delta IL}{2 \cdot I_{on}} \right)^2}$$

$$PL_{on} := \left( IL_{rmsn} \right)^2 \cdot R_{Lo}$$

### Capacitor Loss Calculation

Assume:  $ESR := 150\text{m}\Omega$

$$I_{crms} := \frac{\Delta IL}{2\sqrt{3}} = 0.035\text{A}$$

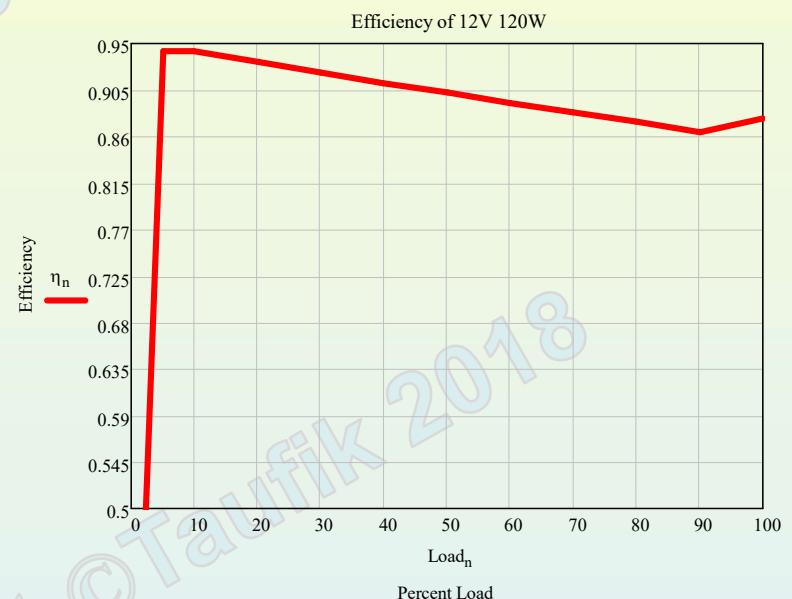
$$P_c := I_{crms}^2 \cdot ESR$$

### Total Loss Calculation

$$P_{totaln} := P_{mostotn} + P_{dtotn} + PL_{on} + P_c$$

$$P_{on} := V_{on} \cdot I_{on}$$

$$\text{Efficiency} ==> \eta_n := \frac{P_{on}}{P_{on} + P_{totaln}}$$



# Efficiency Improvements

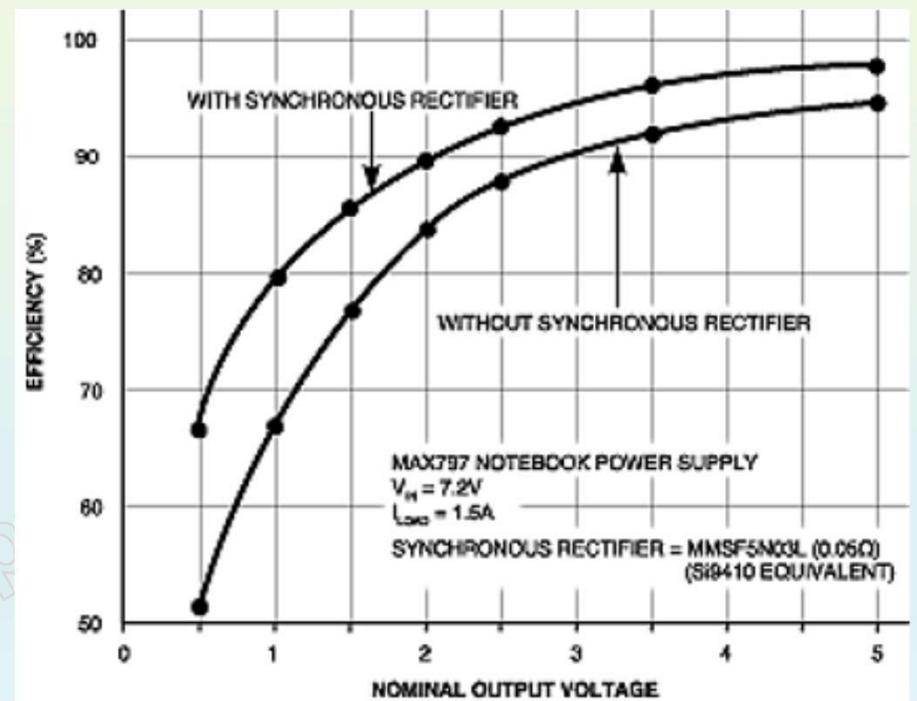
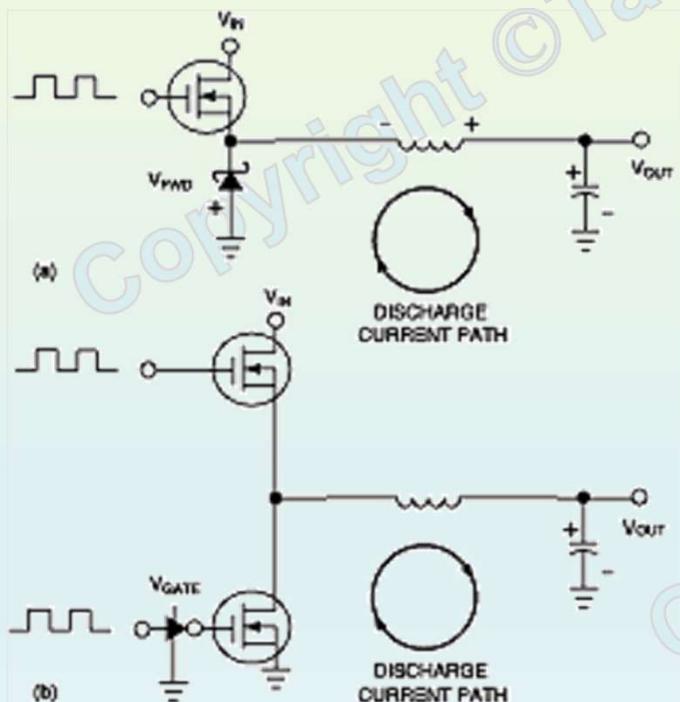
- Ways to improve converter's efficiency:
  - MOSFET
    - Low  $R_{dson}$  for High Duty Cycle
    - Low Gate Charge for Low Duty Cycle
    - Paralleling for High Current
  - Schottky Diode
    - Low forward drop
    - Short recovery time
  - Inductor
    - Multiple parallel windings such as Bifilar (two parallel windings), Trifilar (three parallel windings)

# Efficiency Improvement

- Capacitors
  - Low ESR
  - Paralleling caps (increasing capacitance while reducing ESRs)
- Lower inductor current ripple
  - Reduce rms loss (inductor and output capacitor)
  - Increase switching frequency or inductance
    - Switching loss and real-estate trade off
- Lower gate drive voltage
- Use of Synchronous MOSFET in place of diode, especially for low voltage and high current output

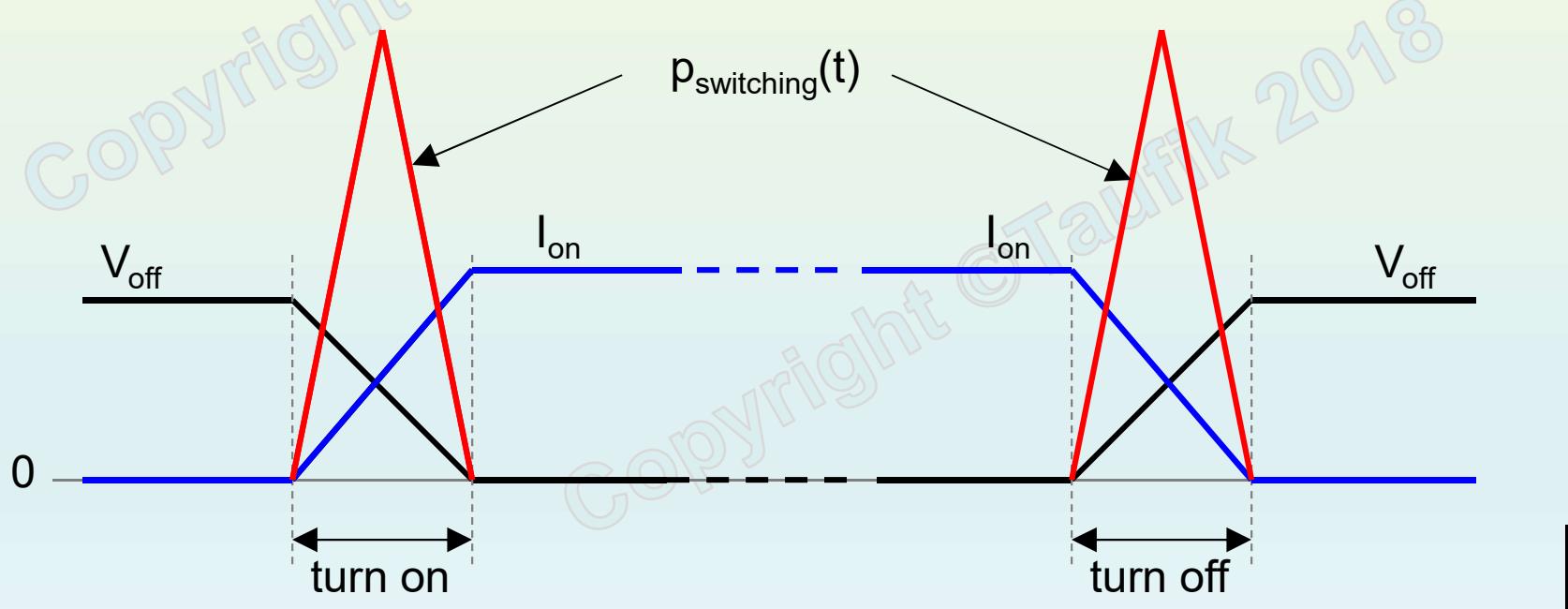
# Synchronous Rectification

- Replaces freewheeling schottky with MOSFET
- Especially beneficial on low duty cycle and high current applications
- Due to required dead time and slow MOSFET's body diode, a Schottky is connected across the Synchronous MOSFET
- MOSFET + Schottky = FETKY combo such as IRF7326D2



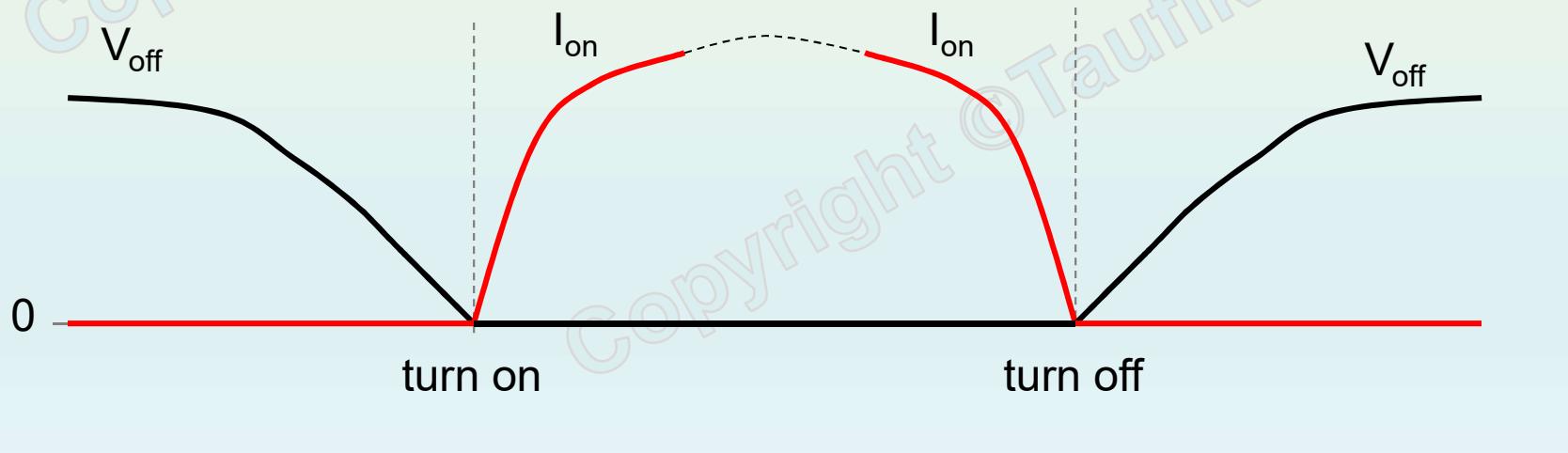
# Soft-Switching

- Prevents hard-switching or the overlapping of switch's voltage and current during turn-on and turn-off transitions
  - switching losses which is proportional to switching frequency
- Use of resonant circuit to shape switch voltage and/or current waveforms to inherently go to zero at which switching transition is initiated → zero switching loss



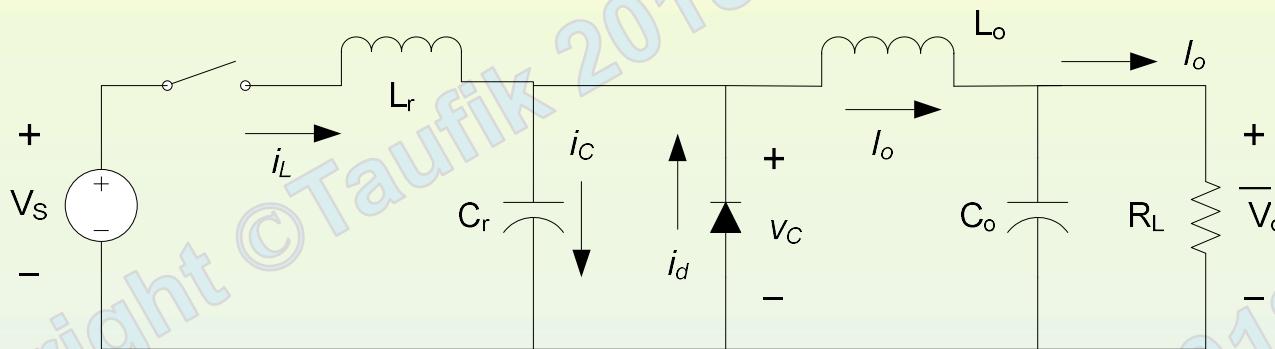
# Soft-Switching

- Quasi-resonant buck topologies such as Zero-Voltage and Zero Current Resonant Switch Buck converter
- Needs constant-on or constant-off controllers such as UC1865 - UC1868, UC1861 – UC1864, MC34067 and MC33067, TDA4605-3, TDA4605-2

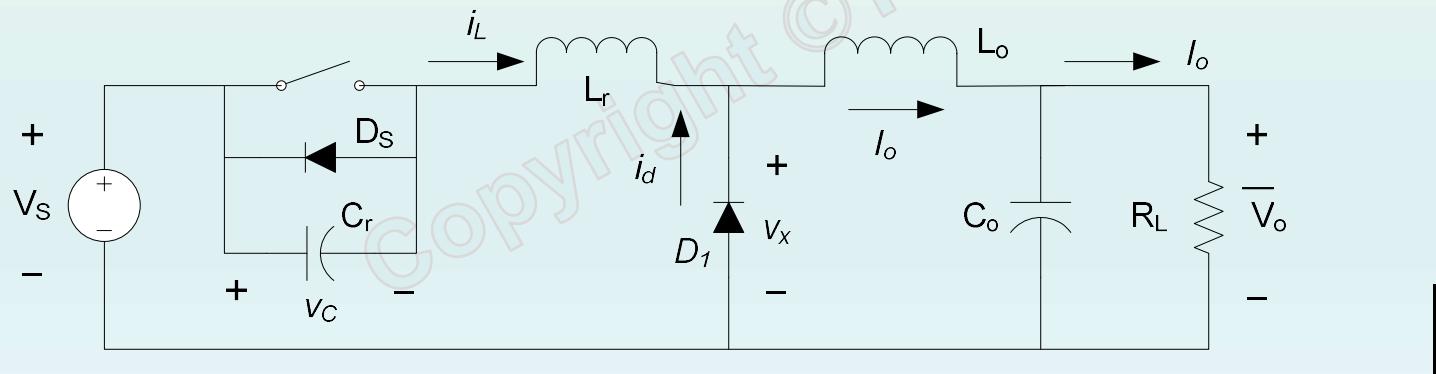


# Soft-Switching

- Zero-Current Resonant Switch Buck
  - Turns switch OFF at zero current



- Zero-Voltage Resonant Switch Buck
  - Turns switch ON at zero voltage



# PWM Controller

- Recall two basic methods: Voltage Mode and Current Mode
- Current Mode is widely used due to its many benefits over Voltage Mode
- Advantages of Current Mode Controller
  - Easy Compensation
    - With voltage-mode requires a type III compensator to stabilize the system due to the sharp phase drop after the filter resonant frequency
    - Current-mode control looks like a single-pole system, since the inductor has been controlled by the current loop
    - Improves the phase margin, making the converter easier to control
    - A type 2 compensator is adequate, simplifying the design process

# PWM Controller

- CCM and DCM Operation
  - Compensator design not possible with voltage-mode that can provide good performance in both CCM and DCM
  - With current-mode, crossing the boundary between the two types of operation is not a problem
    - allowing the power stage to operate much more efficiently
- Line Rejection
  - Closing the current loop gives a lot of attenuation of input noise, even with only a moderate gain in the voltage feedback loop
  - With voltage-mode control, far more gain (or feed forward) is needed in the main feedback loop to achieve the same performance

# PWM Controller

- For the sake of example, we'll use UC184x or MIC38HC4x family

 Unitrode Products  
from Texas Instruments



UC1842/3/4/5  
UC2842/3/4/5  
UC3842/3/4/5

## Current Mode PWM Controller

### FEATURES

- Optimized For Off-line And DC To DC Converters
- Low Start Up Current (<1mA)
- Automatic Feed Forward Compensation
- Pulse-by-pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500khz Operation
- Low Ro Error Amp

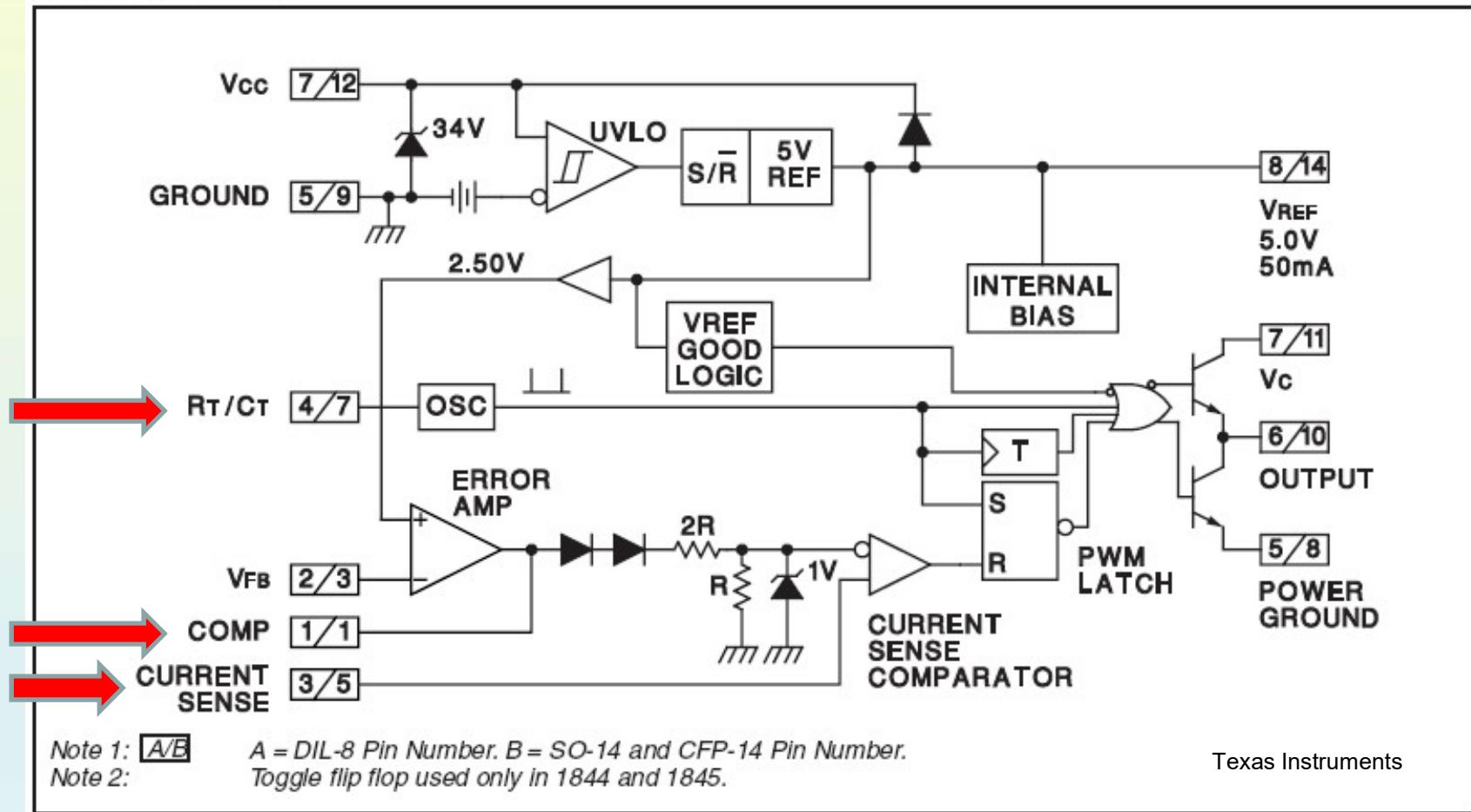
### DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N Channel MOSFETs, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.4V and 7.6V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

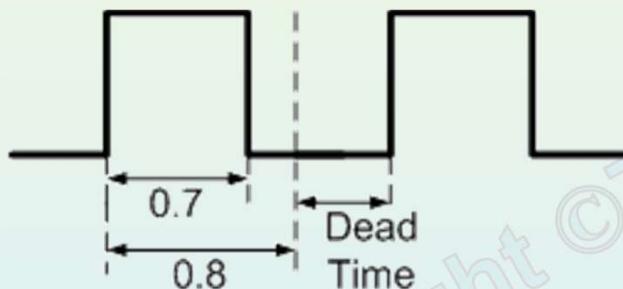
# PWM Controller

BLOCK DIAGRAM



# PWM Controller

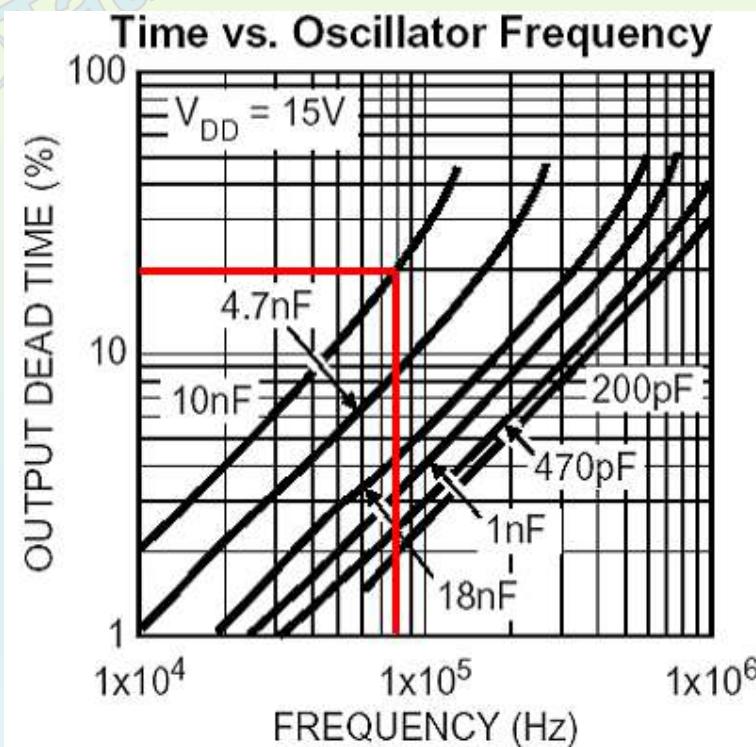
- Selecting Timing Resistor and Timing Capacitor
  - Maximum Duty Cycle and Switching Frequency have to be determined first
  - Percent Dead time would then be computed from Dmax
  - Using % Dead time along with Switching Frequency, we can then use plots provided in the data sheet to determine the required timing capacitor and timing resistor
- Example: Let's say that Dmax was calculated to be 70% or 0.7. Add safety factor to Dmax. Say 10% such that Dmax' = 0.8



- The dead time is therefore  $= 100\% - 80\% = 20\%$
- If switching frequency used is 80 kHz, then the value for % dead time along with switching frequency can be used to determine the required Timing Capacitor
- This is done by using the plot provided in the data sheet.

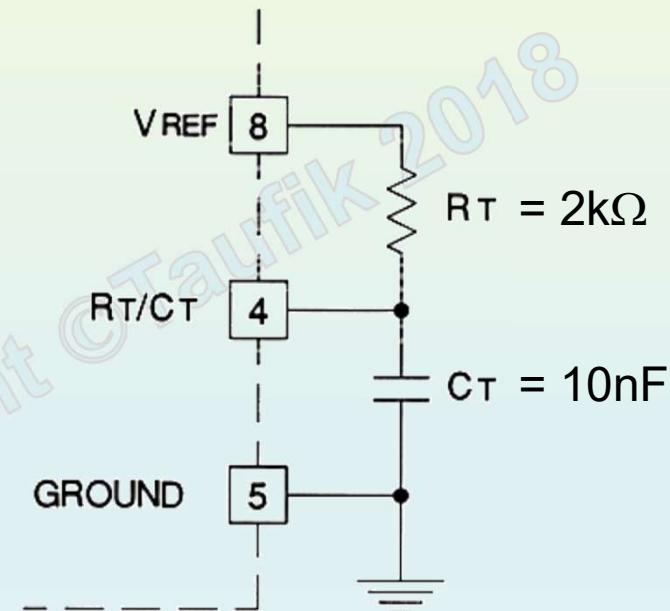
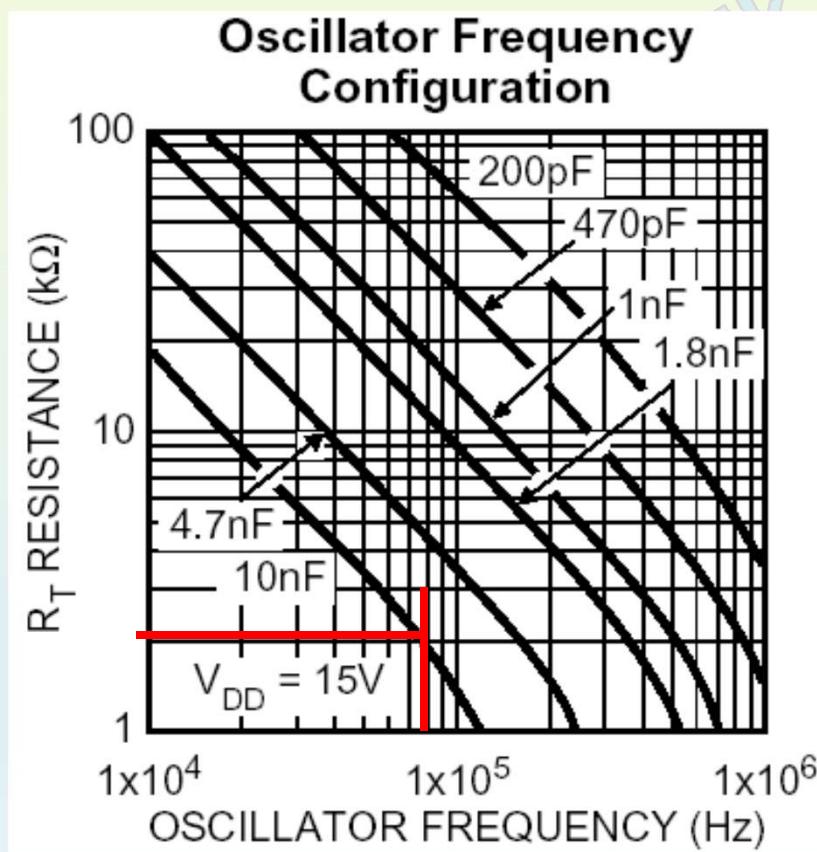
# PWM Controller

- From plot, 80 kHz intersects the 20% dead time at approximately Timing Capacitor value of 10 nF.
- Next, the timing resistor is found from the plot which is also provided in the data sheet



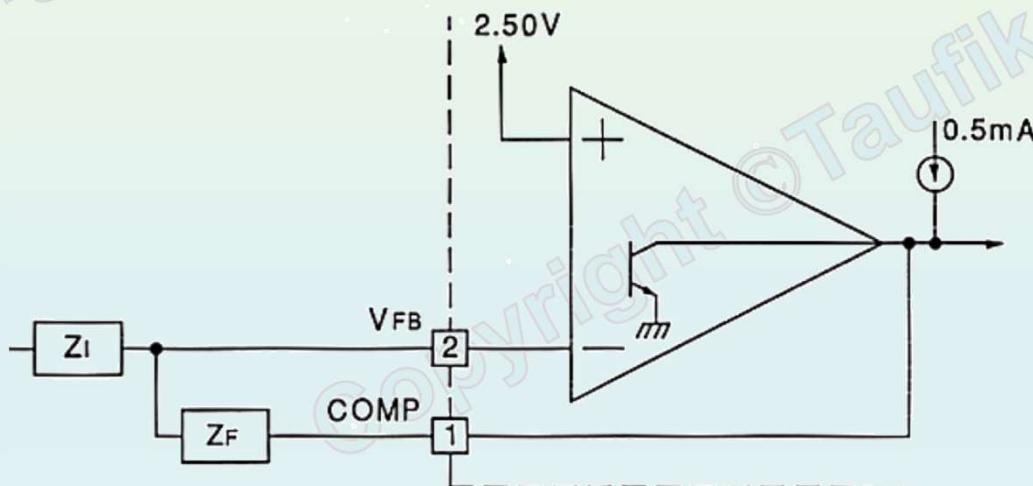
# PWM Controller

- Plot shows that 80kHz intersects the timing capacitor plot for 10 nF at timing resistance approximately equals to 2k $\Omega$
- So, in order to provide the 20% dead time at 80 kHz switching frequency, the timing components are:  $C_T = 10 \text{ nF}$  and  $R_T = 2 \text{ k}\Omega$

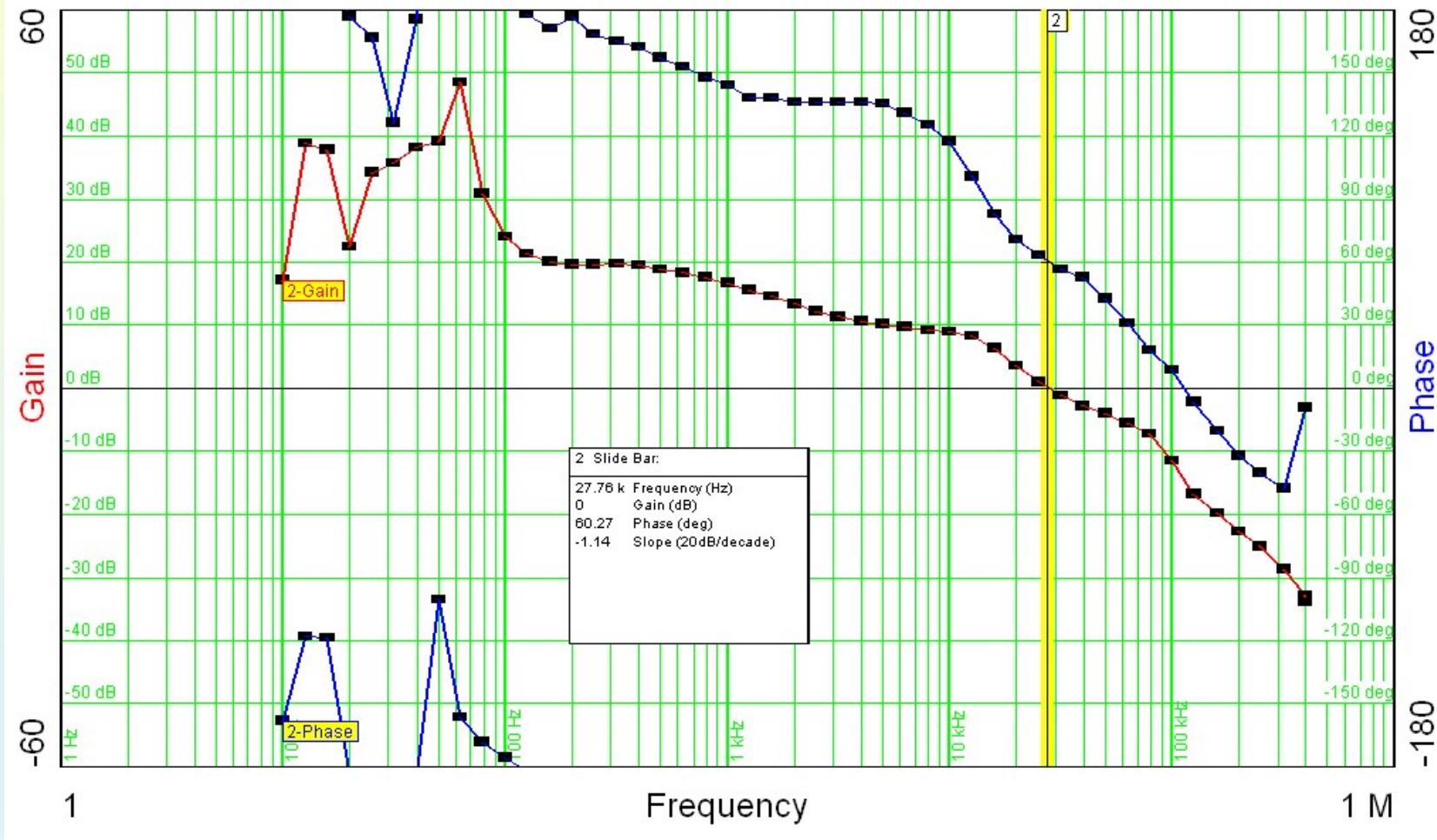


# PWM Controller

- Feedback Compensation
  - As a start, typically a small capacitor is placed on  $Z_F$  (such as 2200 pF) for feedback compensation
  - Once a prototype is built, the feedback compensation will be investigated to give the desired gain and phase margin and stability (over wide range of load)
  - Involves the decision of whether to use type II or III compensator



# PWM Controller



# PWM Controller

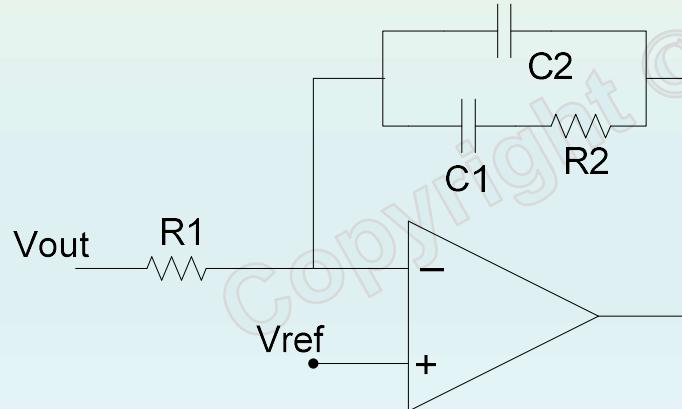
- Steps for selecting components in Type 2
  - Choose cross-over frequency  $F_{cross}$  to be around 1/3 of switching frequency  $F_{switch}$
  - The required pole frequency  $F_{p0}$  that yields the desired crossover frequency of the open loop gain (where  $H_0$  is dc gain of the plant)
  - Calculate capacitor  $C_1$  where  $R_1$  should have been selected when setting the voltage divider
  - Calculate  $R_2$  using the previously calculated  $C_1$  and the output pole of the plant  $F_p$
  - Calculate capacitor  $C_3$  where  $F_{esr}$  is the location of the ESR zero

$$F_{p0} = \frac{F_{cross}}{H_o}$$

$$C_1 = \frac{1}{2\pi R_1 F_{p0}}$$

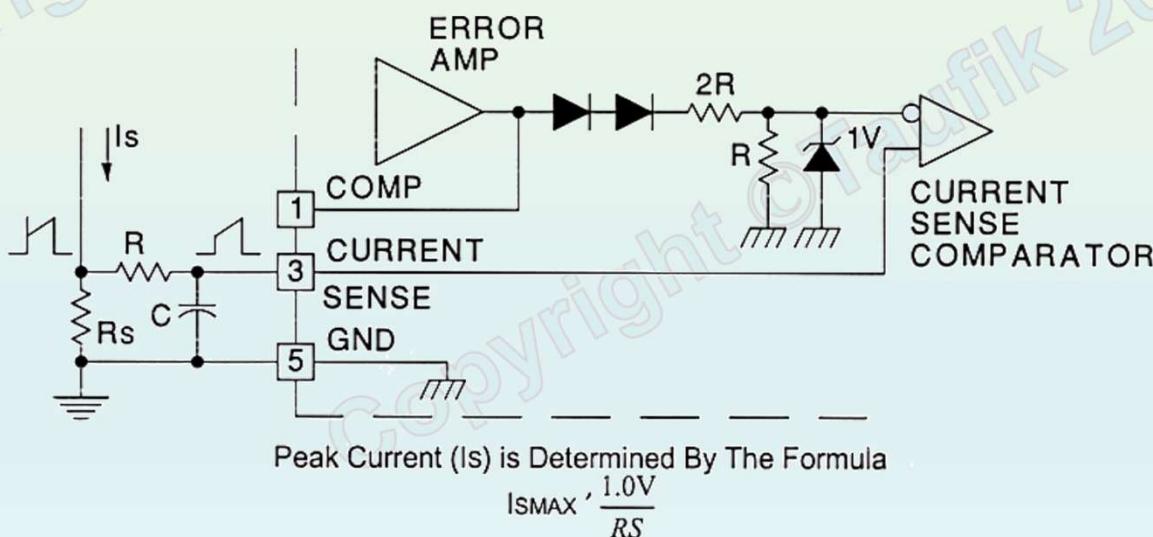
$$R_2 = \frac{1}{2\pi C_1 F_p}$$

$$C_3 = \frac{1}{2\pi ESR \cdot F_{esr}}$$



# PWM Controller

- Current Sensing Resistor
    - Need to calculate power rating of the sensing resistor. This involves calculating worst case  $I_{rms}$  through the sensing resistor, and then compute  $P = (I_{rms})^2 * R_{sense}$
    - A low pass RC filter circuit is also needed to eliminate leading spike on the pulse voltage resulted from current being sensed
    - Ensure that voltage out of the filter is less than 1V (for this controller). If not, then reduce the value of  $R_{sense}$



# Layout Considerations

- Separate power path from signal path
- Use rounded edges instead of sharp edges on traces
- Ensure the trace is wide enough to carry current
- Keep trace inductance low (preferably by reducing length, not increasing width) for the critical path (switch and diode paths)
  - Noise spikes may appear in input and output, and to the controller chip
  - Avoid using a current probe (a loop of wire) for diode and switch due to additional inductance it will produce

# Layout Considerations

- Provision of good Input decoupling since input capacitor is in the critical path
  - Besides the usual bulk capacitor, also put a small ceramic capacitor at the supply end to ground, and another one close to the switch to ground
- Provision of good decoupling with a small ceramic capacitor between input and ground pins
- Try using shielded inductor, and position the inductor away from the controller and feedback trace
- In multi-layer boards, dedicate one layer for ground

### Power Electronics Lab at Cal Poly State University

- 6 Instructional Lab Benches, 2 Project/Thesis Benches
- For further information, contact Power Electronics Lab Coordinator, Dr. Taufik at [taufik@calpoly.edu](mailto:taufik@calpoly.edu)



Copyright © 2018





Taufik was born in Jakarta, Indonesia. He received his BS in Electrical Engineering with minor in Computer Science from Northern Arizona University (Cum Laude) in 1993, MS in Electrical Engineering from University of Illinois Chicago in 1995, and Doctor of Engineering from Cleveland State University in 1999. He joined the Electrical Engineering department at Cal Poly State University in 1999 where he is currently a tenured Full Professor. He received numerous teaching awards, most notably the 2012 Outstanding Teaching Award from the American Society of Engineering Education - Pacific Southwest Section. He is a Senior Member of IEEE and has industry experience with several companies including Capstone Microturbine, Rockwell Automation, Picker International, San Diego Gas & Electric, APD Semiconductor, Diodes Inc., Partoe Inc., Enerpro, Renewable Power Conversion and Sempra Energy. His research areas include power electronics, power systems, rural electrification, energy harvesting, renewable energy and smart grid. He has published over 200 papers in technical journals and conference papers. He holds one US Patent, and he has served on the editorial review boards of several engineering journals. He is also an Adjunct Faculty in the College of Engineering at Universitas Pertamina.