

Mikroişlemci Sistemleri

Dr. Öğr. Üyesi Erkan Uslu

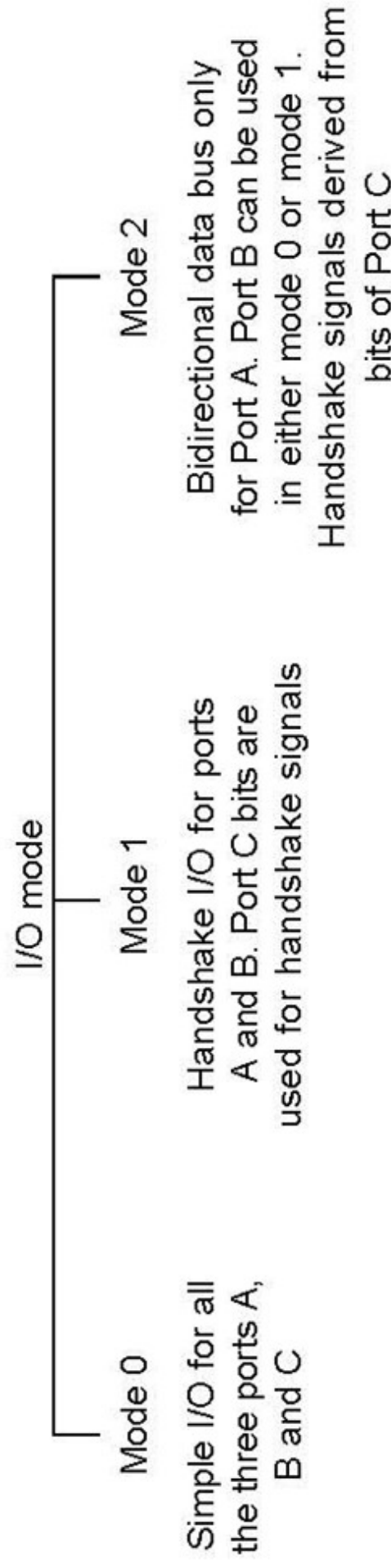
4

YTÜ-CE

Ders-4 Konular

- 8255 modları
 - Mod 0
 - LED ve Buton
 - 7 parçalı gösterge
 - 3x4 tuş tarama
 - BSR (Bit set reset)
 - Mod 1
 - Mod 2

8255 Modlar

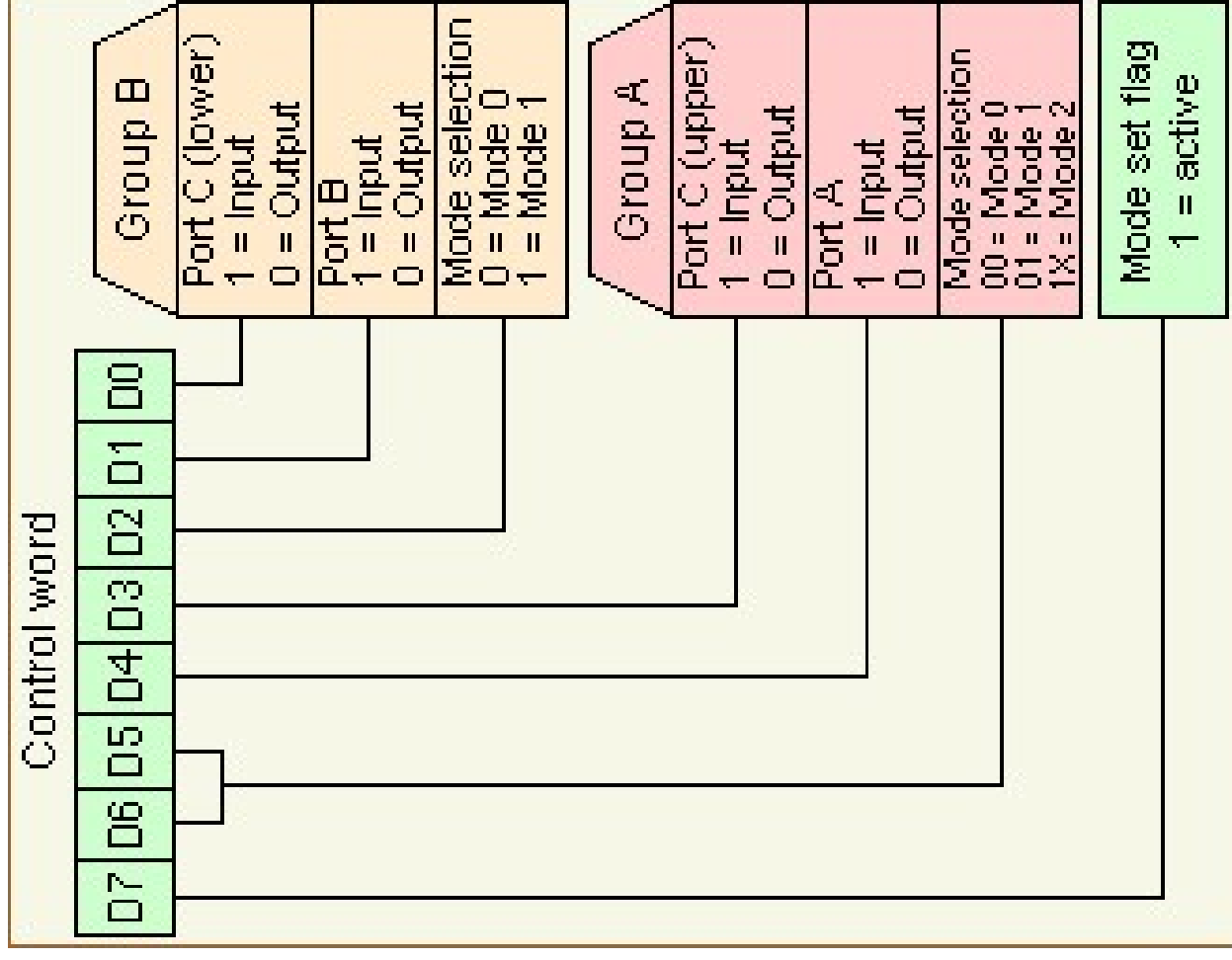


8255

Kontrol

Yazmacı →

Mod 0

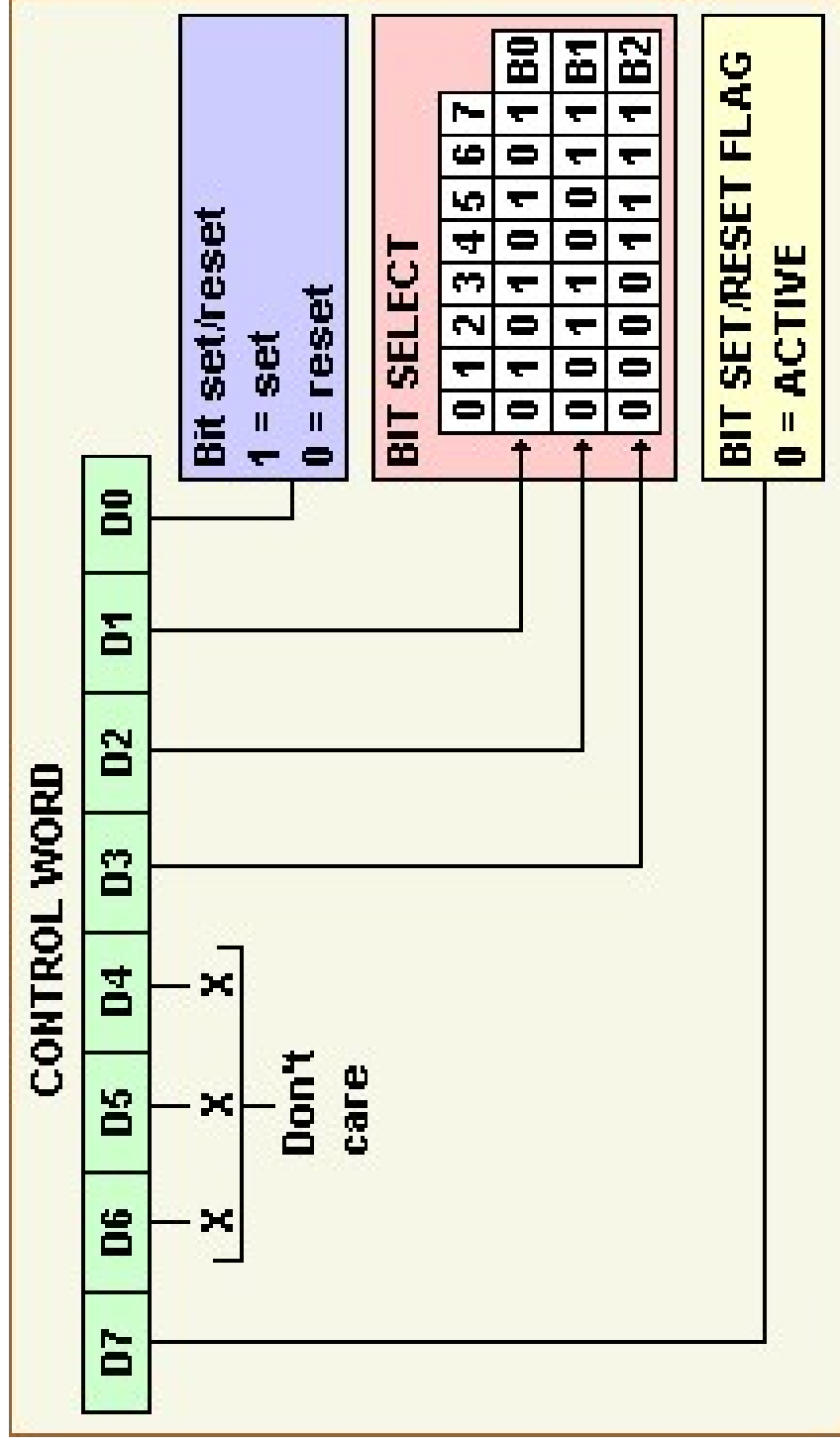


8255

Kontrol

Yazmacı →

BSR



BSR Mod Örneği

- Örnek:
- 80H adresinden itibaren ardışık çift adreslere yerleştirilmiş bir 8255'de
 - PC2'yi lojik 1 olacak şekilde
 - PC6'da ise duty cycle'ı %66 olan bir kare dalga üretecek şekilde

programlayın

BSR Mod Örneği

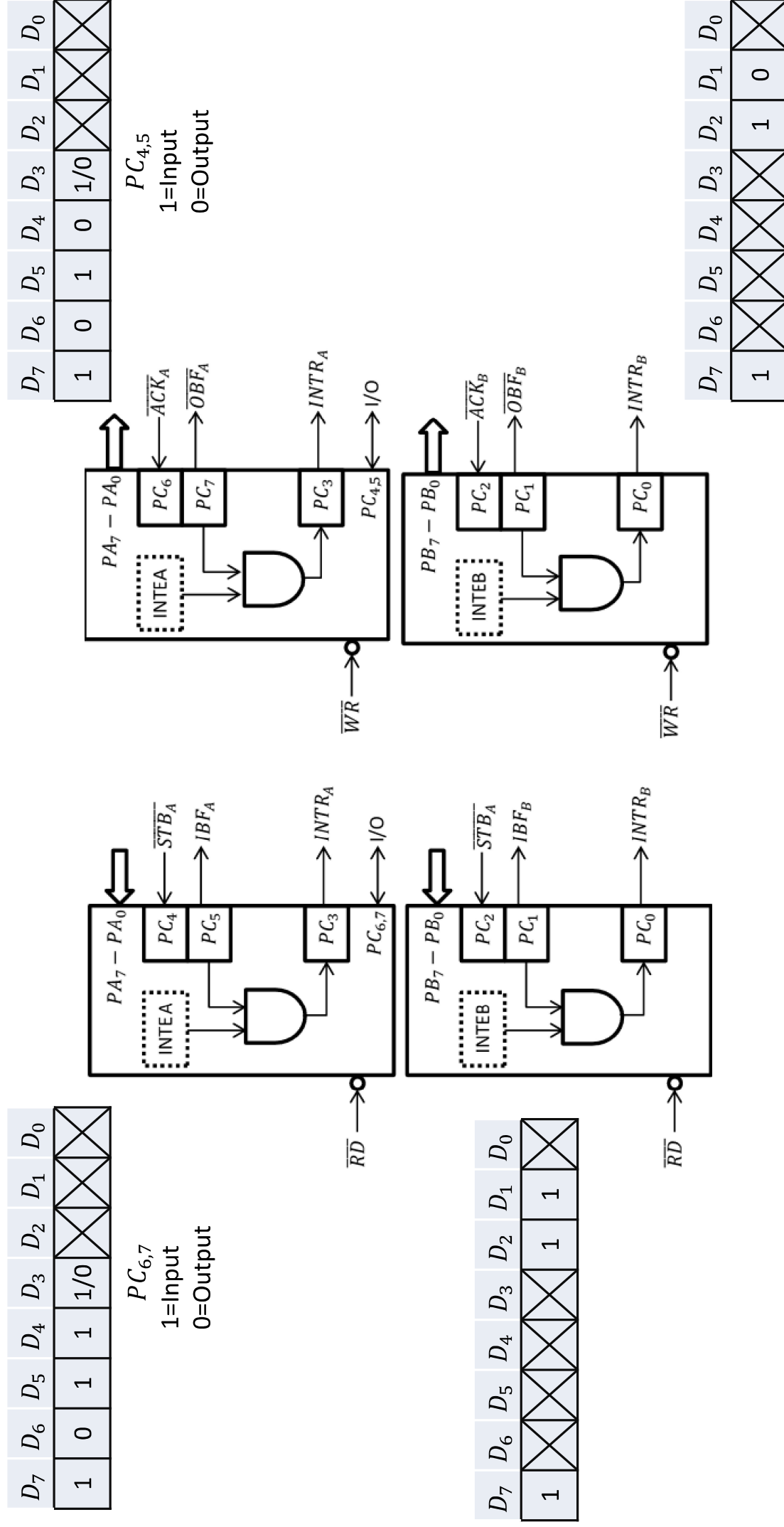
- MOV AL, 00000101B
OUT 86H, AL
- AGAIN MOV AL, 0xxx1101
 OUT 86H, AL
 CALL Delay
 CALL Delay
 MOV AL, 0xxx1100
 OUT 86H, AL
 CALL Delay
 JMP AGAIN

8255 Mod 1

- Handshaking sinyalleri ile kontrollü tek yönlü veri gönderme veya almayı sağlar. (Mod 2'de handshaking sinyalleri ile çift yönlü veri iletimi)
- PORTA ve/veya PORTB Mod 1 için tek yönlü olarak veri iletimi için kullanılırken, PORTC uçları handshaking işaretleri için kullanılır.

8255 Mod 1

- Grup A ve Grup B ayrı ayrı Mod 1 için programlanabilir.
- Her grupta 8 bit veri 4 bit kontrol işareti vardır.



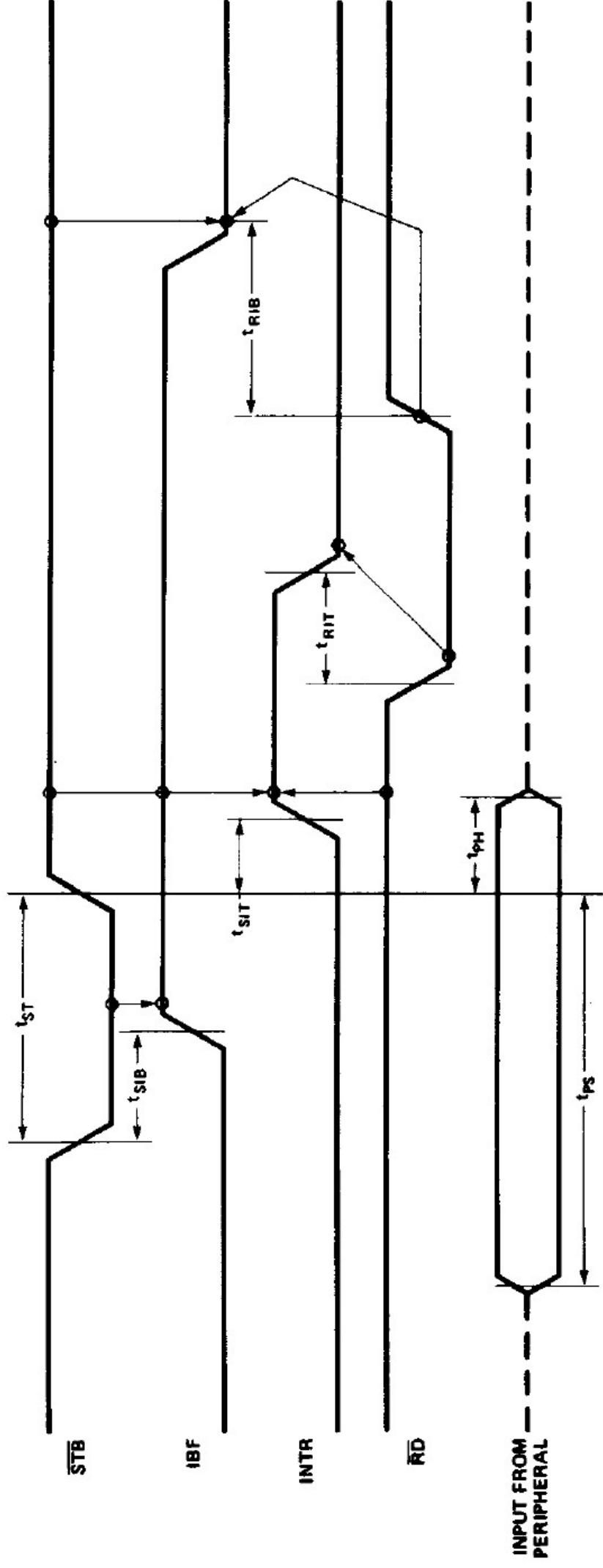
8255 Mod 1 - Input

- \overline{STB} : A “low” on this input loads data into the input latch
- IBF : A “high” on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by \overline{STB} input being low and is reset by the rising edge of the \overline{RD} input

8255 Mod 1 - Input

- INTR : A “high” on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the \overline{STB} is a “1” IBF is a “1” and INTE is a “1”. It is reset by the falling edge of \overline{RD}
- INTEA : Controlled by bit set/reset of PC4
- INTEB : Controlled by bit set/reset of PC2

8255 Mod 1 – Input Timing



8255 Mod 1 - Output

- \overline{OBF} : goes “0” to indicate that the CPU has written data out to the specified port. The \overline{OBF} will be set by the rising edge of the \overline{WR} input and reset by \overline{ACK} input being low
- \overline{ACK} : A “0” on this input informs the 82C55A that the data from Port A or Port B has been accepted

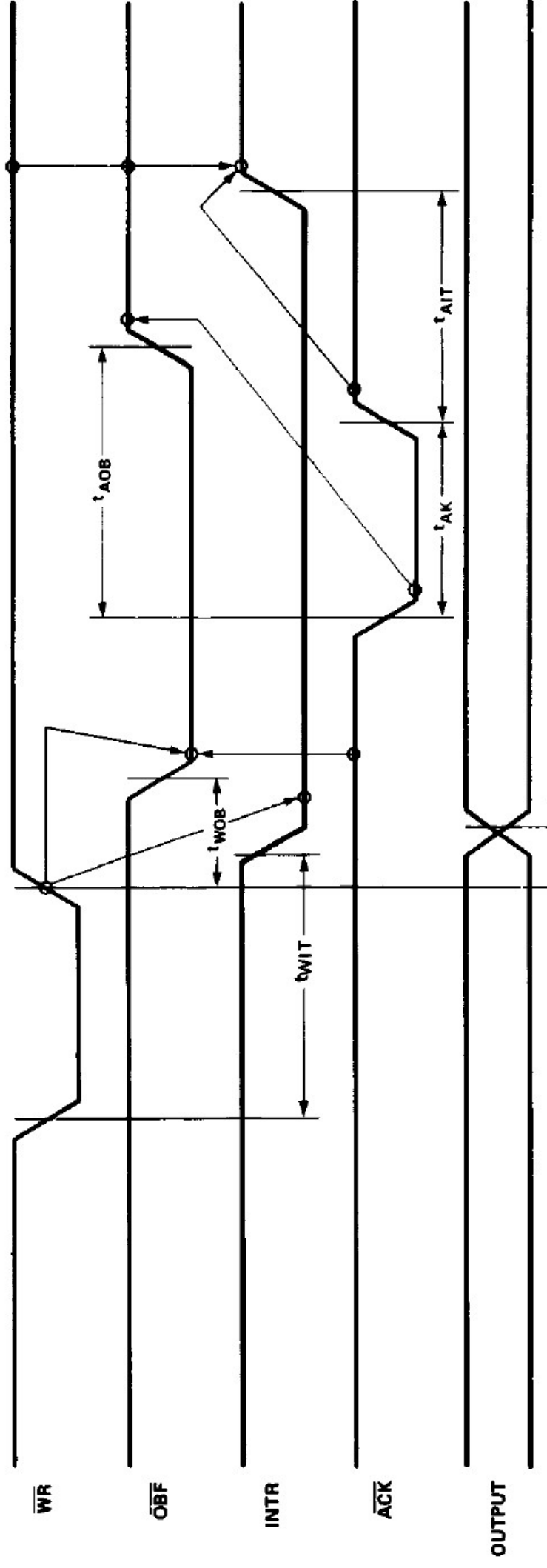
8255 Mod 1 - Output

- INTR : A “0” on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when \overline{ACK} is a “1”, \overline{OBF} is a “1” and INTE is a “1”. It is reset by the falling edge of \overline{WR} .

8255 Mod 1 - Output

- INTEA : Controlled by bit set/reset of PC6
- INTEB : Controlled by bit set/reset of PC2

8255 Mod 1 – Output Timing



8255 Mod 1 – Status Word

- 8255 mod 1 için ayarlanmış PORTC'den yapılan okumalar STATUS WORD'dür
- OBF, IBF, INTR değerleri ile I/O için kullanılan PORTC uçları okunabilir

8255 Mod 1 – Status Word

- Input

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
GROUP A				GROUP B			

- Output

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OBF_A	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	OBF_B	$INTR_B$
GROUP A				GROUP B			

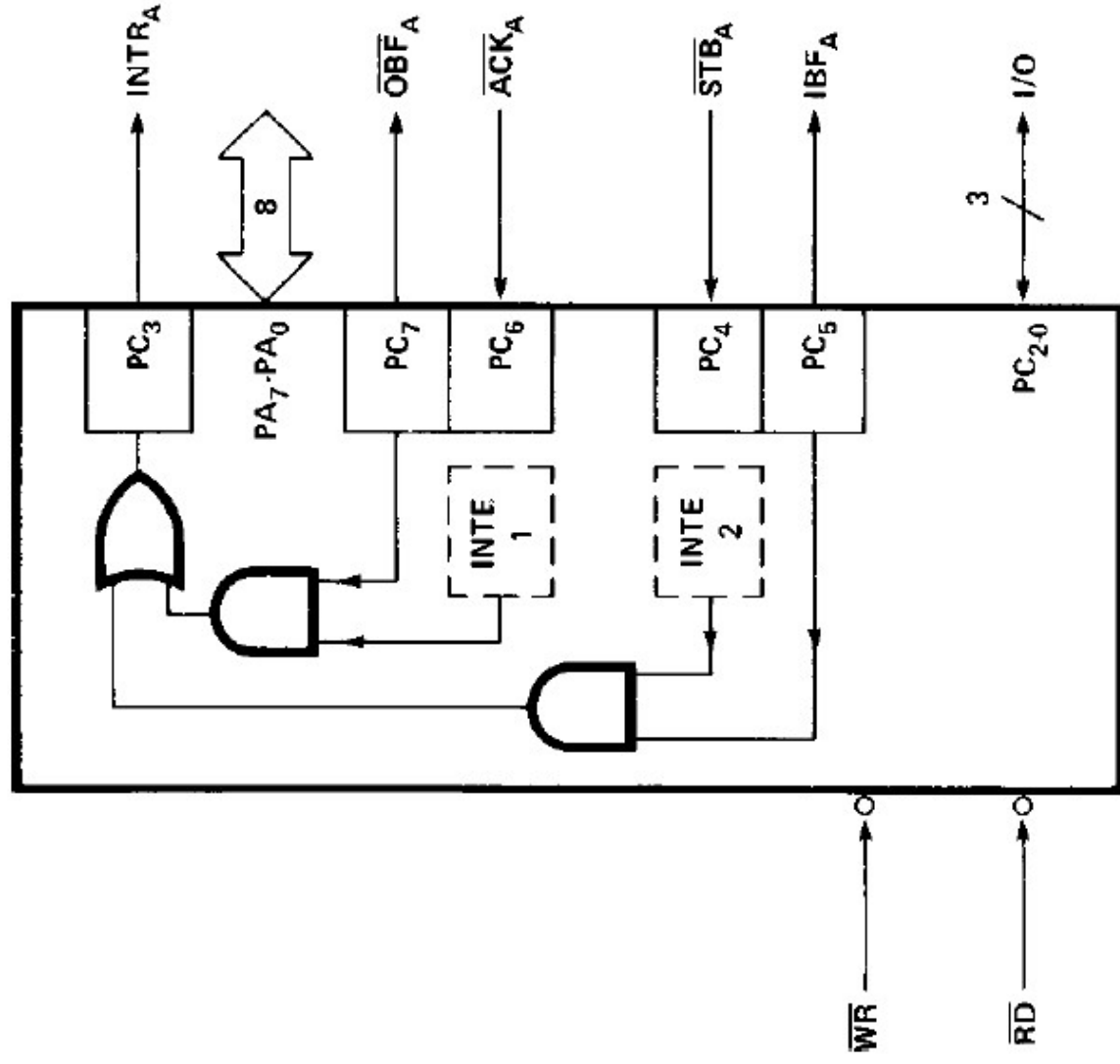
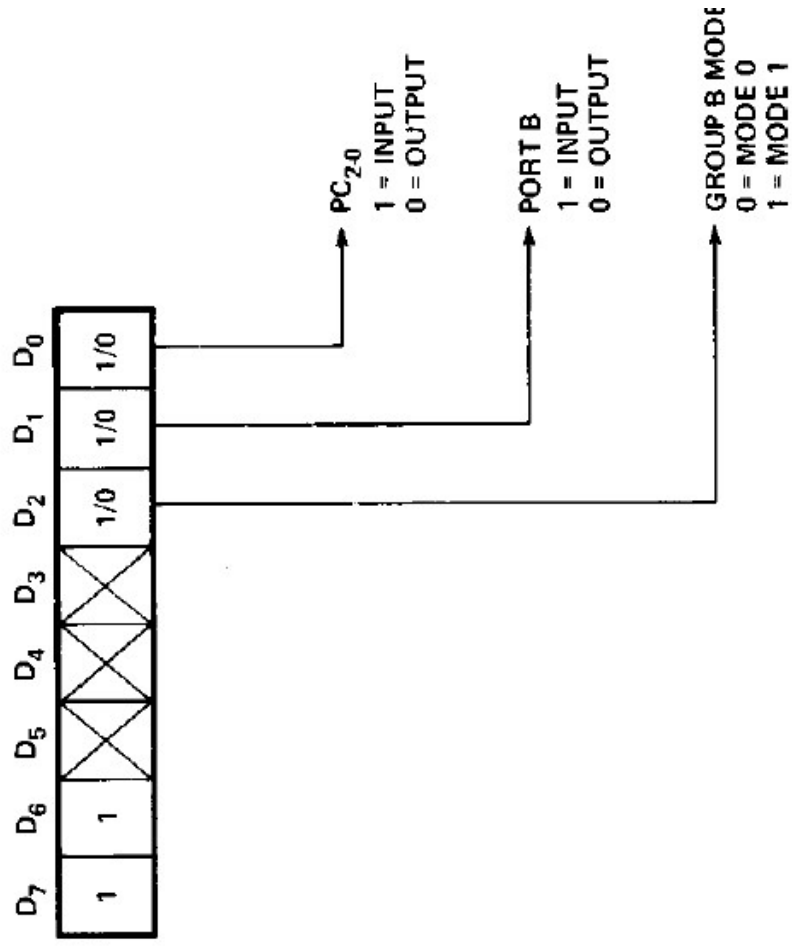
8255 Mod 1

- 8255 Grup A Mod 1 output, 8255 Grup B Mod 1 input yönlü ayarlanarak, bunlar arasında handshaking tabanlı I/O işlemleri nasıl yapılabilir?

8255 Mod 2

- Strobed bidirectional bus I/O
- Sadece Grup A mod 2 destekler
- 1 adet 8 bit çift yönlü port (PORTA), ve 5 handshaking kontrol işareti mevcuttur

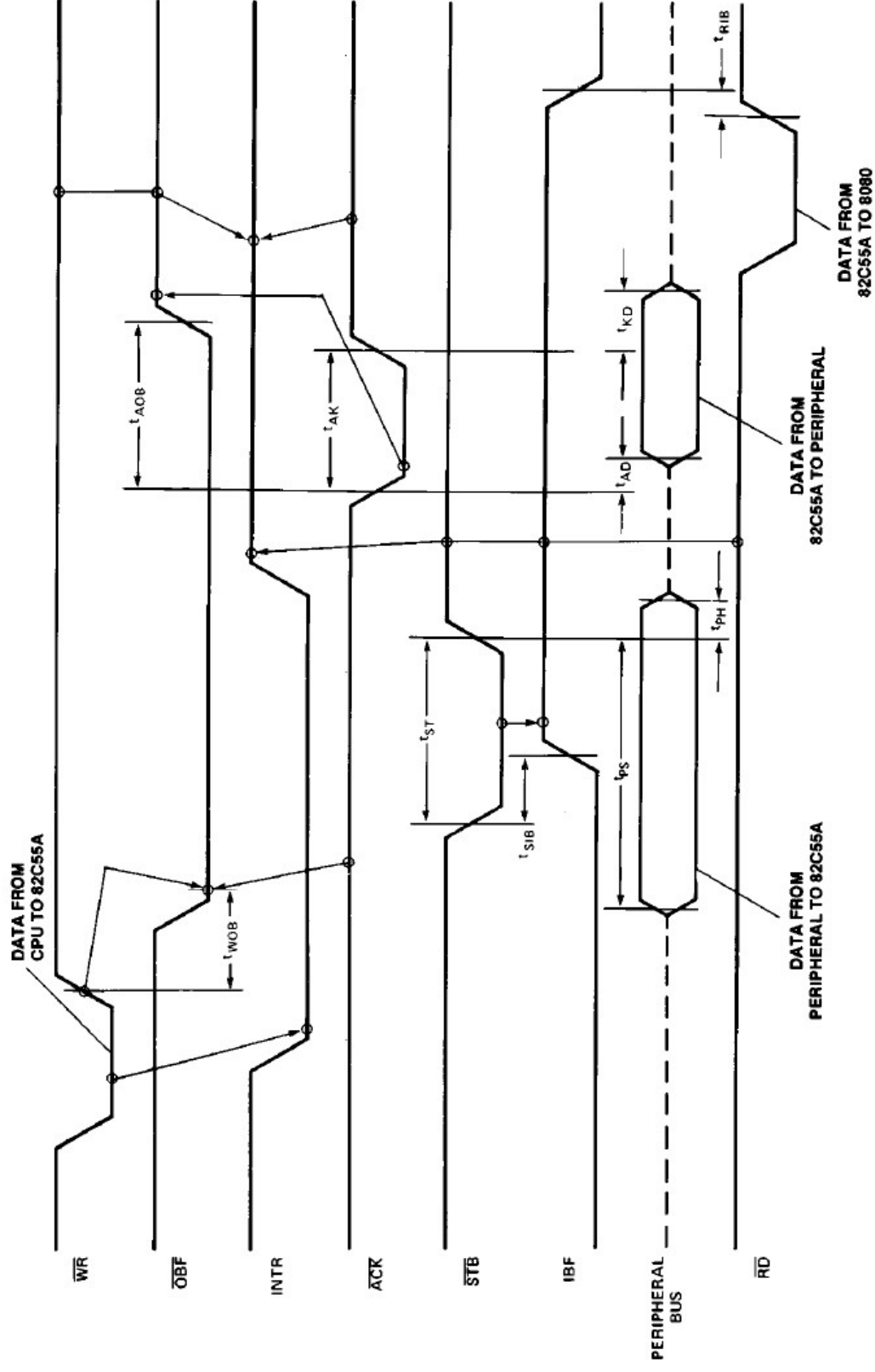
CONTROL WORD



8255 Mod 2

- INTE 1 : Controlled by bit set/reset of PC6
- INTE 2 : Controlled by bit set/reset of PC4

8255 Mod 2 - Timing



8255 Mod 2 – Status Word

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
$OBFA$	$INTE_1$	$IBFA$	$INTE_2$	$INTR_A$			
GROUP A				GROUP B			

8255

Modlar:

Özet

Tablo

	MODE 0	
	IN	OUT
PA0	IN	OUT
PA1	IN	OUT
PA2	IN	OUT
PA3	IN	OUT
PA4	IN	OUT
PA5	IN	OUT
PA6	IN	OUT
PA7	IN	OUT
PB0	IN	OUT
PB1	IN	OUT
PB2	IN	OUT
PB3	IN	OUT
PB4	IN	OUT
PB5	IN	OUT
PB6	IN	OUT
PB7	IN	OUT
PC0	IN	OUT
PC1	IN	OUT
PC2	IN	OUT
PC3	IN	OUT
PC4	IN	OUT
PC5	IN	OUT
PC6	IN	OUT
PC7	IN	OUT

MODE 1	
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
INTR _B	INTR _B
IBF _B	OB _F <u>B</u>
<u>STB</u> _B	ACK _B
INTRA	INTRA
<u>STB</u> _A	I/O
IBF _A	I/O
I/O	<u>ACK</u> _A
I/O	OB _F <u>A</u>

MODE 2	GROUP A ONLY
	↔
	↔
	↔
	↔
	↔
	↔
	↔
	↔
	—
	—
	—
	—
	—
	—
	—
	I/O
	I/O
	I/O
	INTRA
	<u>STB</u> _A
	IBF _A
	<u>ACK</u> _A
	OB _F <u>A</u>

MODE 0
OR MODE 1
ONLY