Structured ASIC

CMPE584 - Reconfigurable Computing

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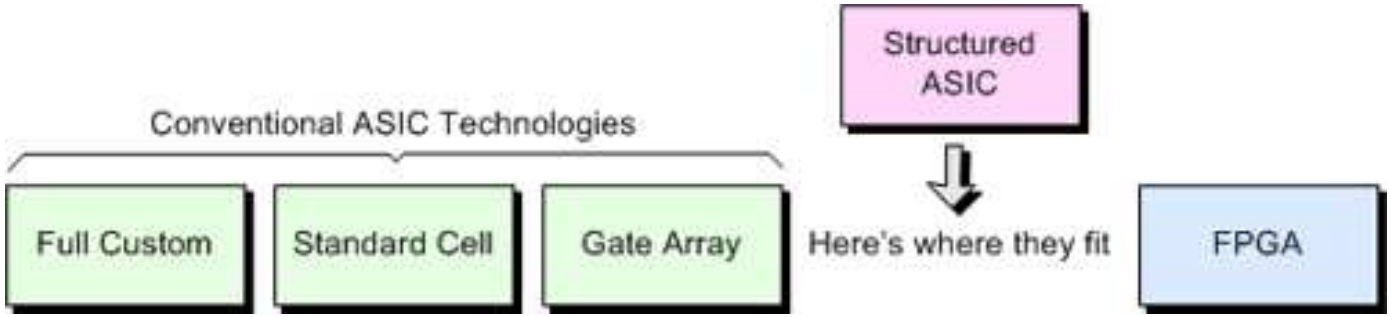
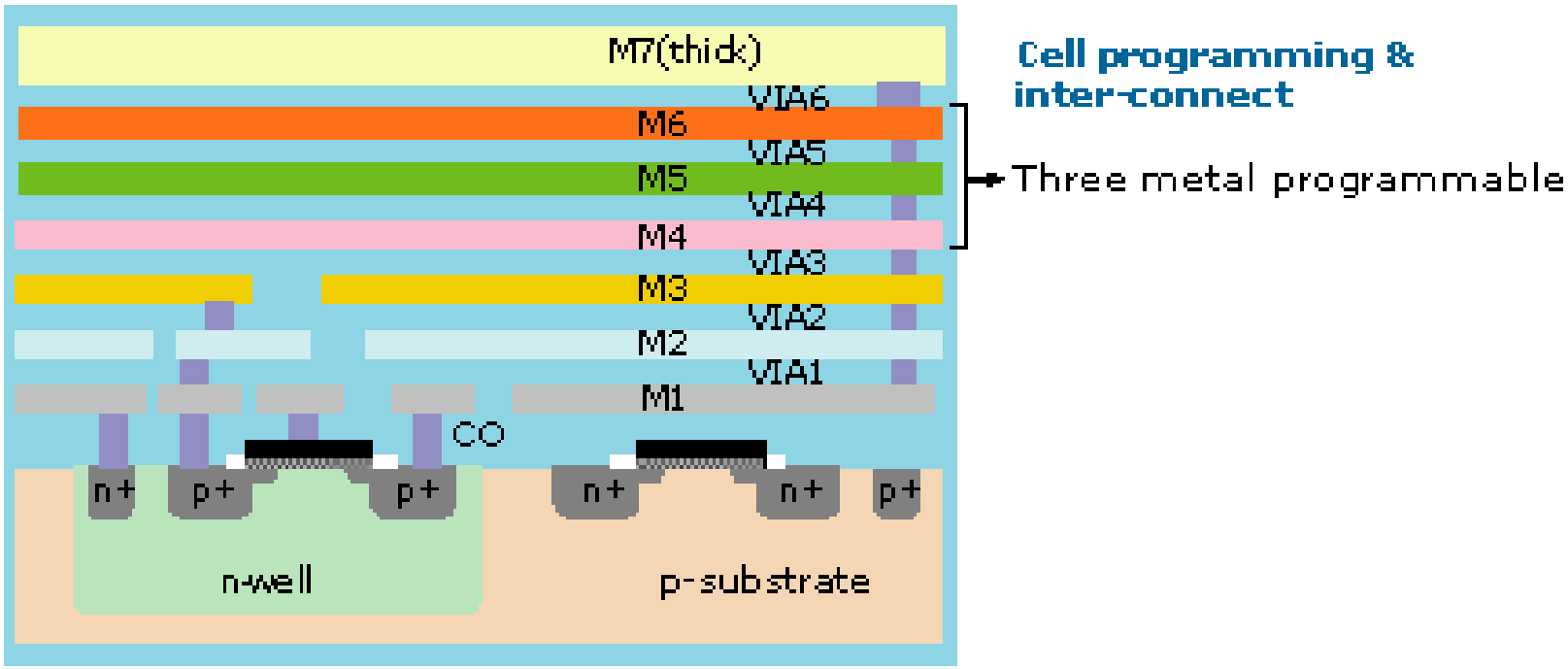
What is a structured ASIC?

- It is an intermediate technology between ASIC and FPGA.
- It is a pre-configured (or hardwired) FPGA application.



What is a structured ASIC?

Simply it is metal-layer configurable ASIC.



Acronyms used in this presentation

- SEU: Single Event Upset is a change of state caused by a high-energy particle strike to a sensitive node in a micro-electronic device, such as in a microprocessor, semiconductor memory, or power transistors.
- NRE: Non-recurring engineering (NRE) refers to the one-time cost of researching, developing, designing, and testing a new product.
- S-ASIC: Structured Application Specific Integrated Circuit
- ASSP: Application Specific Standart Products

Uses of Structured ASIC

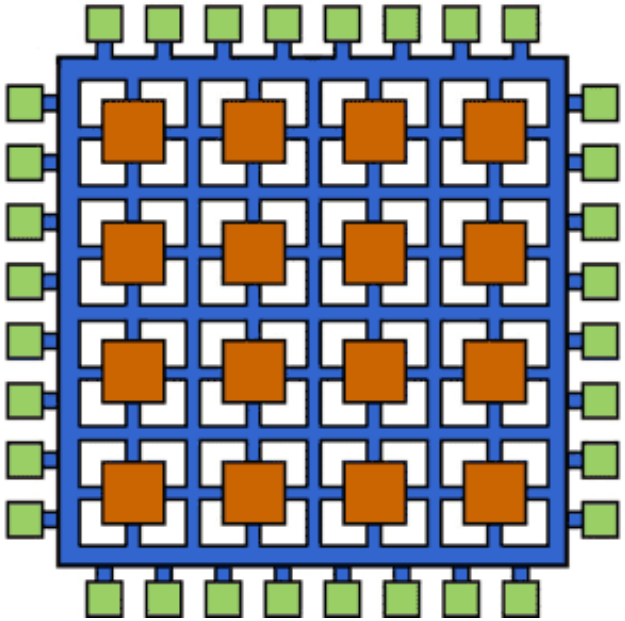
- It is used for reducing SEU (Invented then)
- It is used for easy prototyping.
- It is used for lowering costs for low and mid volume application.
- It is used for when something needed between FPGA and ASIC.

Benefits

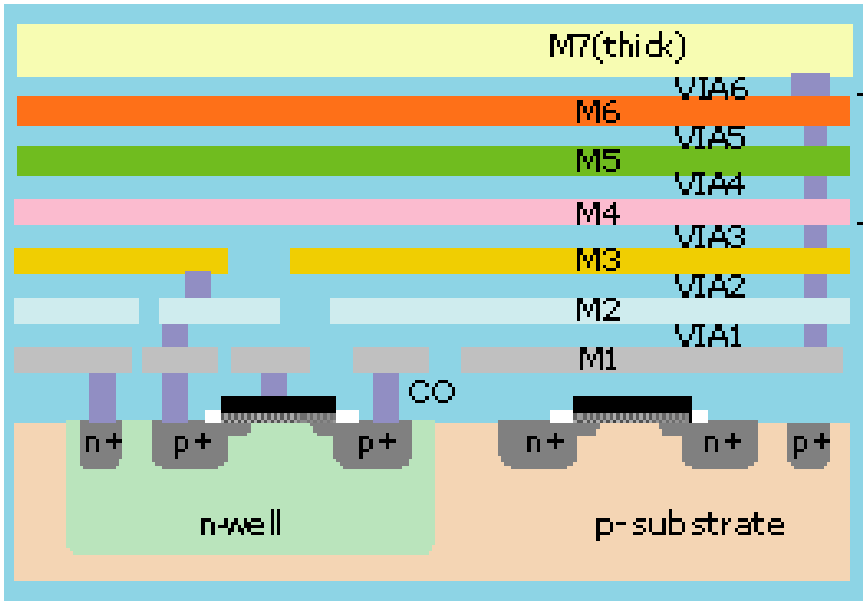
- It offers higher performance, a characteristic of ASIC,
- It offers lower power requirements, a characteristic of ASIC
- It offers low NRE cost, a characteristic of FPGA.

Inside S-ASIC

Topview



Layers



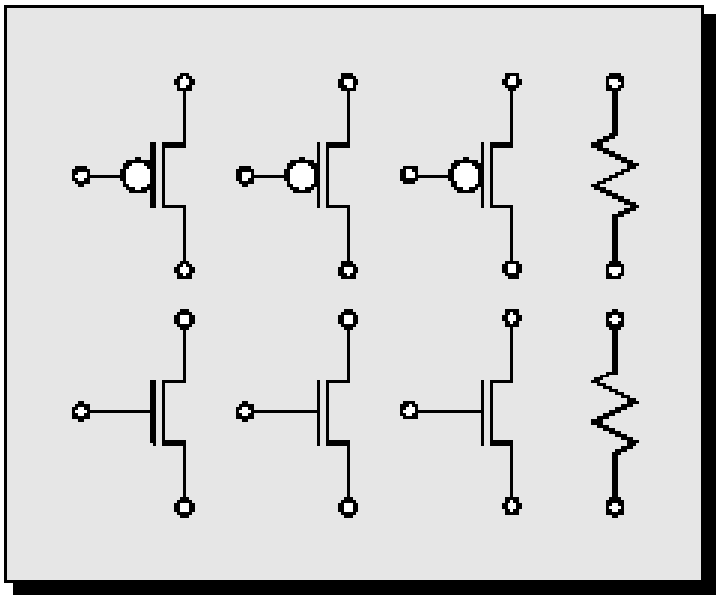
Granularity

Granularity defines the minimum configurable unit.

- Fine-grained requires many connection in and out of a structured element.
- Coarser granularities reduce connections but decreases the element functionality.

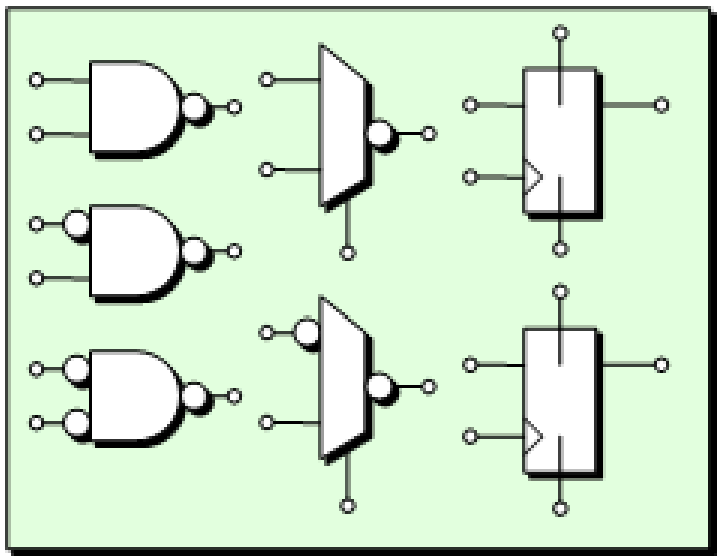
Fine Grain

Fine-grained asics are configurable as resistors, caps, or basic logic gates.

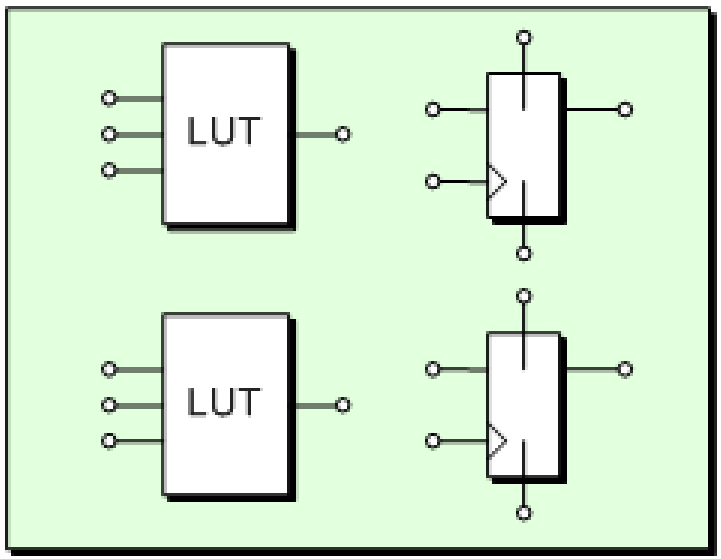


Mid Grain

Mid-grained(sometimes coarse-grained) asics are configurable as blocks, like FPGA blocks. it shows both memory and sequantial element properties.



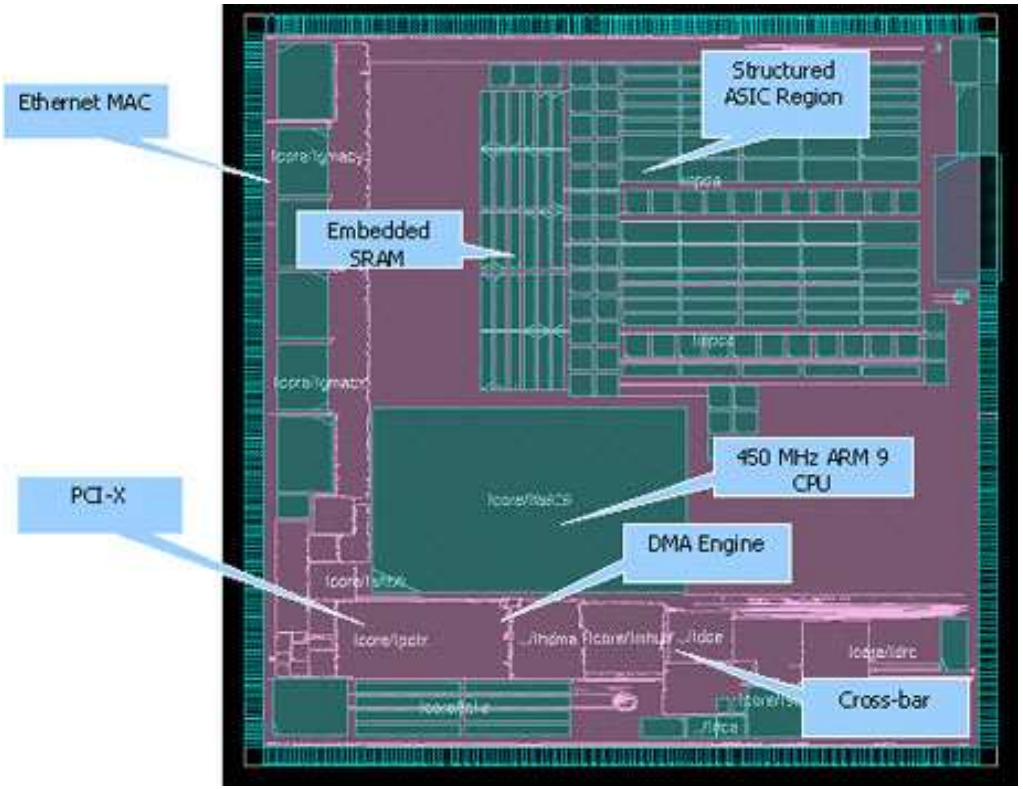
(a) Gate, mux, and flop-based



(b) LUT and flop-based

Coarse Grain

Coarse-grained ones are configurable like cpu and some pheripherals are enabled or disabled.



Clock Network

Nearly all types of S-ASIC contain a clock network.

- Some global clocks, and more local clocks.
- Helps to meet timing requirements easily.

Advantages

- Lot more! Some importants are,
- Structured ASIC combines the advantages of both ASIC and FPGA.
- Power efficiency, better performance.
- Low turn-over rate while developing ASIC.
- S-ASIC devices has a clock network, ASIC doesnt.
- 1:3:12 power consumption ratios (ASIC:S-ASIC:FPGA)
- FPGA to ASIC conversion comes with smaller packaging.
- More secure, against reverse engineering, or hacking.
- Hybrid ASICs very good option for projects with requirements are not defined well or changing.

Disadvantages

- It is not fully customizable like ASIC.
  - We cannot tweak, customize or modify unit smaller than vendor determined.
  - For example, we cannot change W values of a transistor group.
- It is not field programmable, it is one-time programmable when manufacturing.
- You may need to redesign or change the design methodology when FPGA to S-ASIC

S-ASIC combines advantages of both technologies

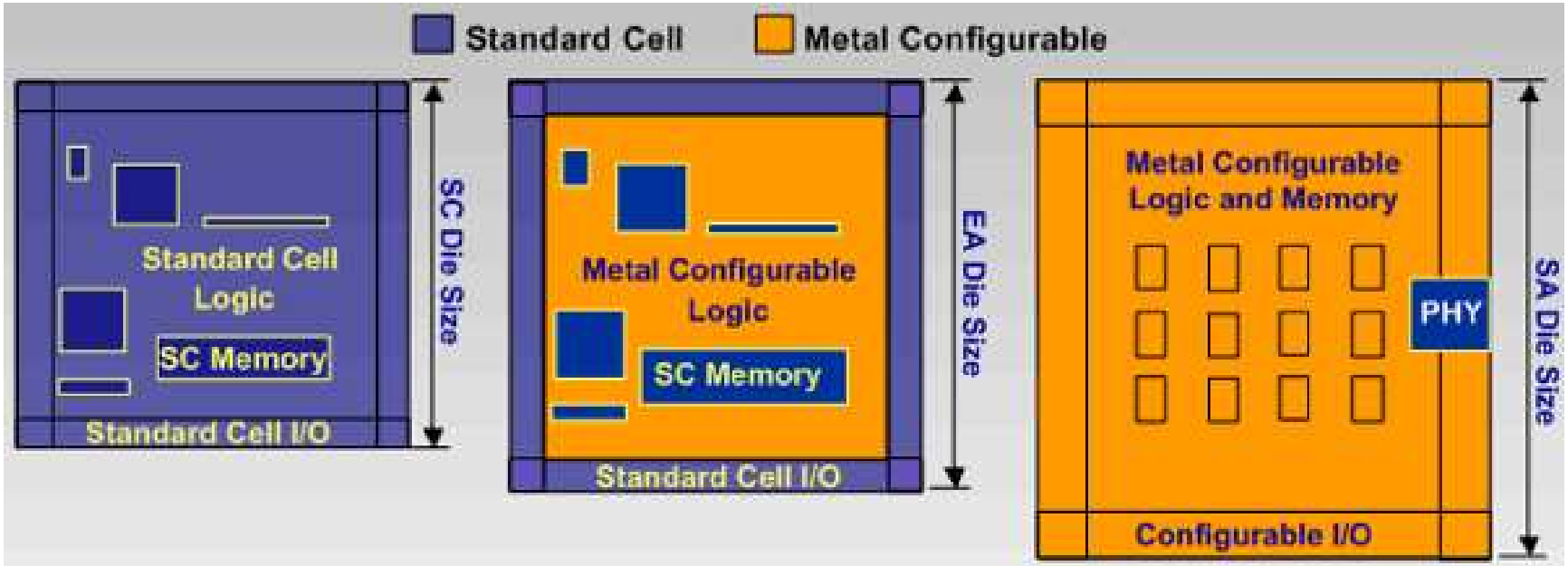
FPGA

- Easy to design
- Short development time
- Low NRE Cost
- Design size is limited
- Design complexity limited
- Performance limited
- High power consumption
- High per-unit cost
- SEU sensitive

ASIC

- Difficult to design
- Long development time
- High NRE costs
- Support large designs
- Support complex designs
- High performance
- Low power consumption
- Low per-unit cost
- lower SEU sensivity

Comparison to ASIC and FPGA

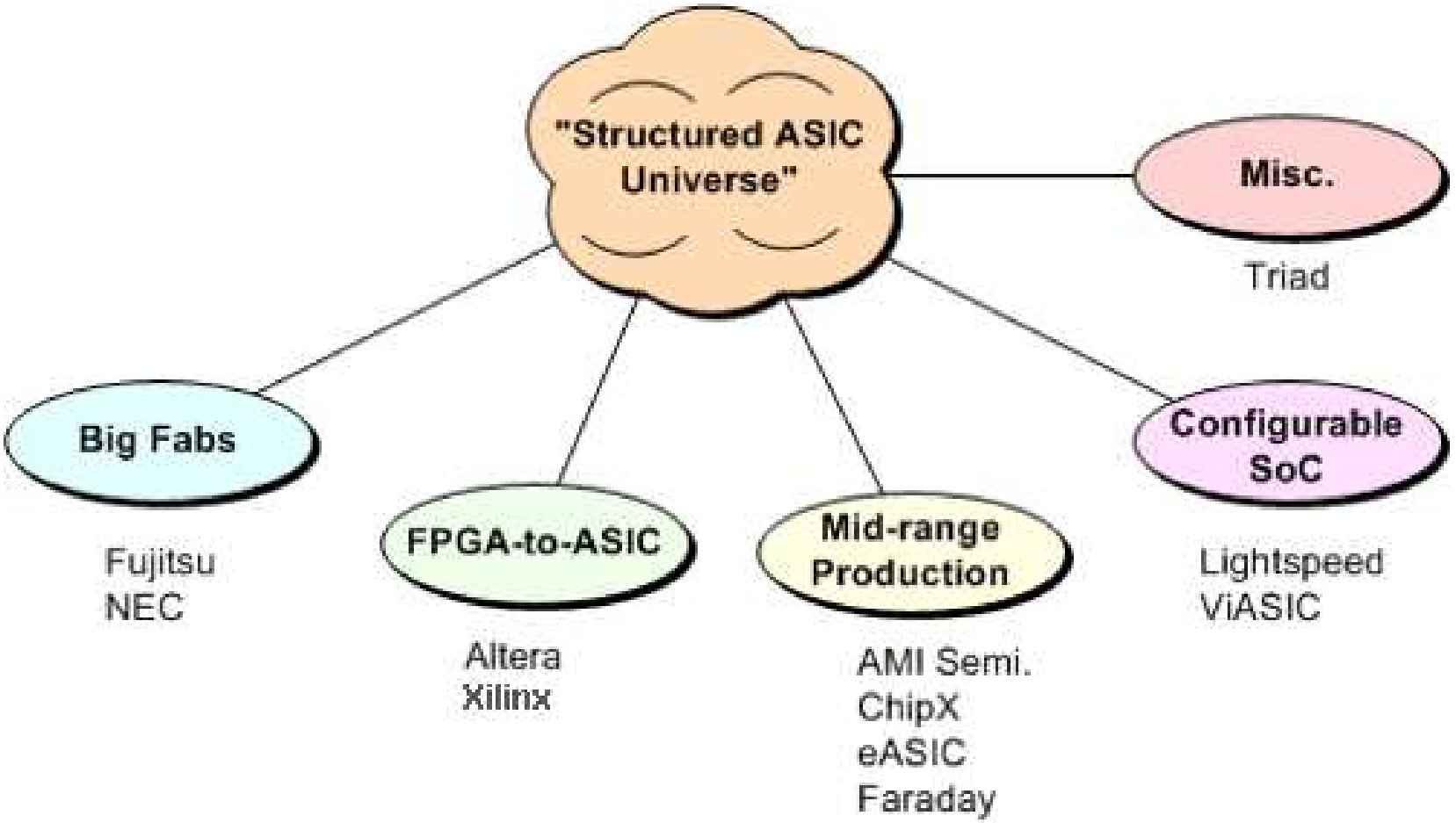


Standard Cell ASIC
Best fit
Accommodates analog IP
Smallest die size
Higher NRE
Change requires full masks

Embedded Array ASIC
Excellent fit
Accommodates analog IP
Fastest spins with near SC size
Higher NRE
Easy logic re-configuration

Structured ASIC
Good fit if available
Some IP built in
Fastest time to market
Lowest NRE
Fully configurable in metal
Low minimum order quantity (MOQ)

Structured ASIC Companies



Big Fabs

- They also provide (and require) their tools.
- When a new process technology appears, that is generally tested by producing S-ASIC or FPGA.
- Because of it is not effective in high volumes, LSI and Fujitsu abandoned.

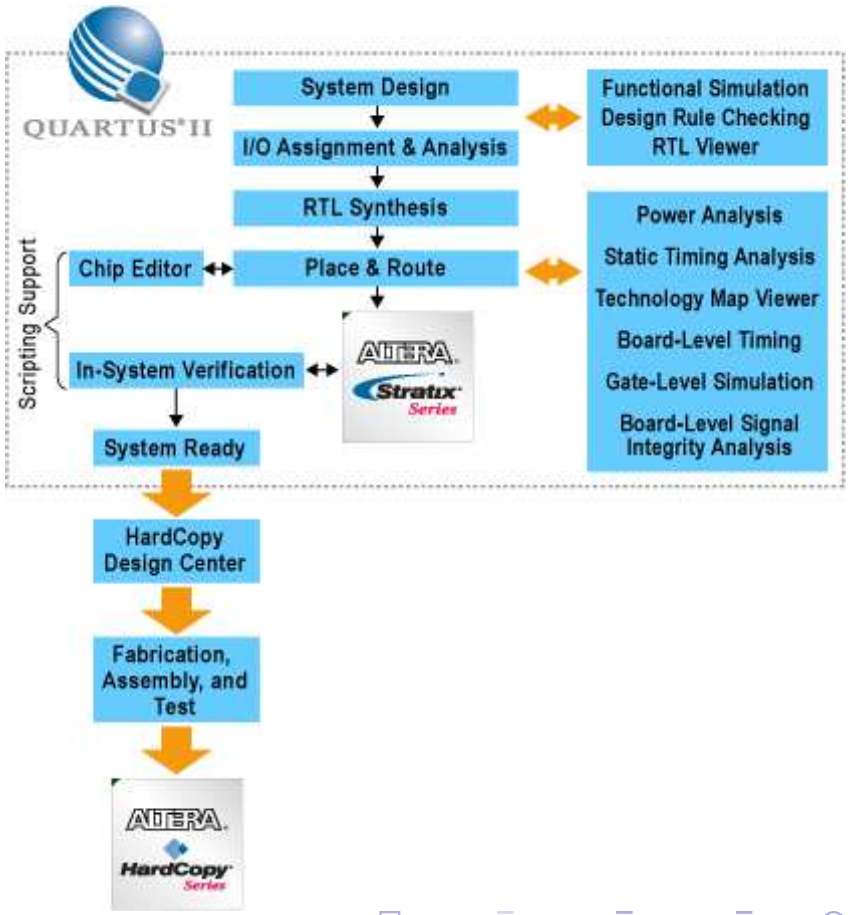
Xilinx EasyPath

- Please note, Xilinx is a fabless company, which contracts to Samsung and TSMC.
- Almost all xilinx devices is supported.(not all)
- 3 Months production time.

Cost Drivers	EasyPath	S-ASIC	ASIC
Unit Price	Low	Lower	Lowest
NRE	< $100K	< $250K	$500K – $1M+
Time to Volume	< 1 Qtr	2 – 4 Qtr	> 4 Qtr
Qualification Cost	None	High	High
Re-spin Responsibility	None	Often	Very Often

Altera Hardcopy

- %5 of total revenue
- One tool, One methodology, One manufacturer
- Downto 40nm process
- Upto 12 Million gates in a device
- May Include Altera 6.5gbps transreceivers



Mid-range Production

- Each company have different approach.
- Real S-ASIC companies!
- chipx `http://www.chipx.com`
  - Coarse grain ASIC products, with clocks, memory controller, buses are ready
- Faraday `http://www.faraday-tech.com`
  - Ready to deploy SoC also with SW.
- easic `http://www.easic.com`
  - FPGA vendor like but in mid-volumes only.
  - Developed its tools and IDE, available free.

Configurable SOC

- Actually these companies provides ASIC with a small configurable area.
- They are simply SoC development contractors.
- Less configurable devices. Having 1 - 2 metal layer programmable.

Misc

- Other companies that doesnt fit any category.
  - triad `http://www.triad.com`
  - ASIC products, with pre-sythesized op-amps, filters, DACs
  - FPGA like granularity with more analog devices.

Market Status

- Some people thinks it is a revolution
- However, some companies abandoned it. because,
  - Flow issues
  - Over promising
  - Poor execution
  - but many companies still in operation.
- Highly innovative, low and mid volume designs use it.
- Aerospace/Defense companies uses it.
- The way of easy FPGA-to-ASIC conversion.
- EDA tools for S-ASIC should be developed.

References

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Thank you

Questions ?