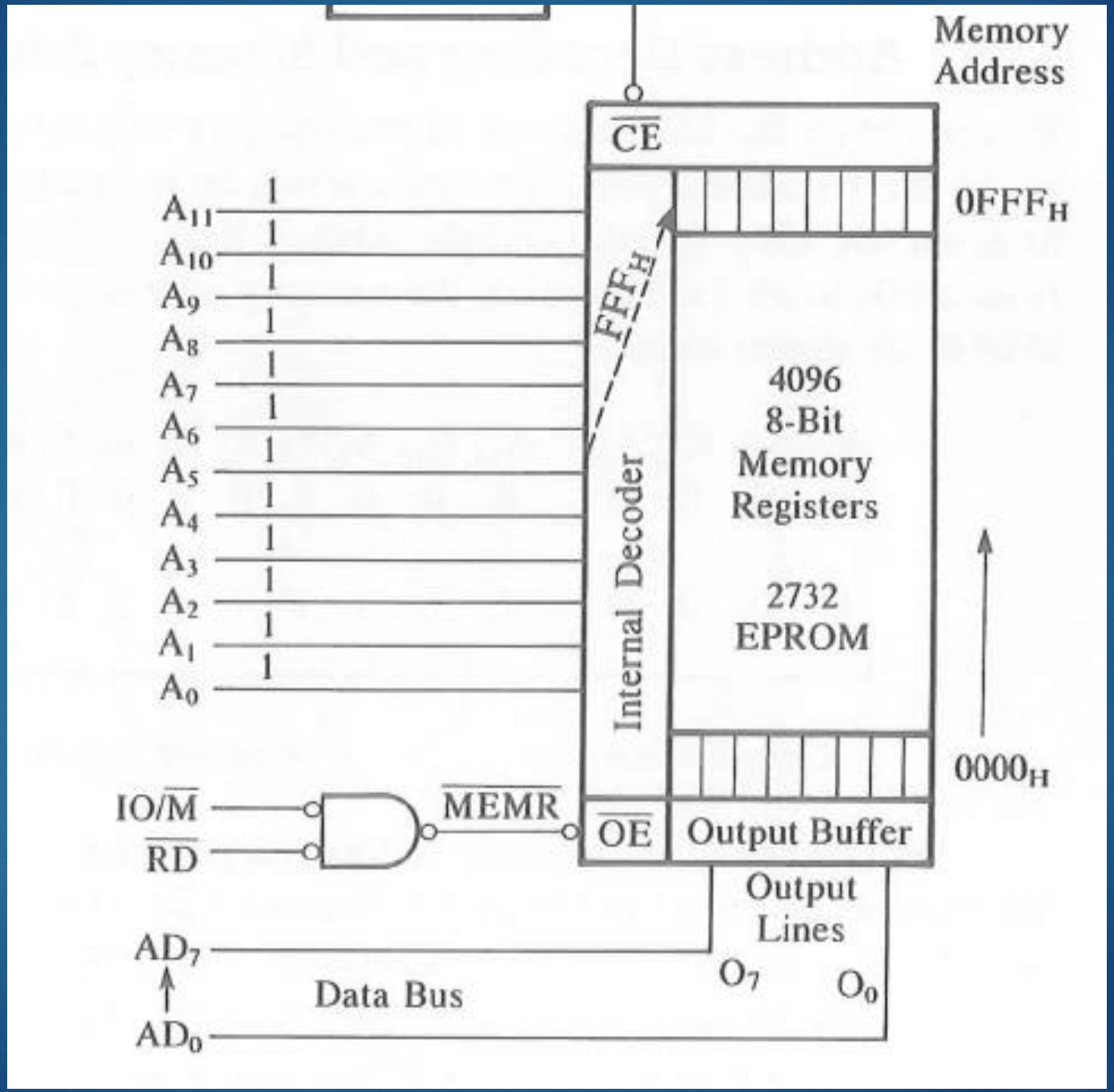
Address Decoding

ADDRESS DECODING

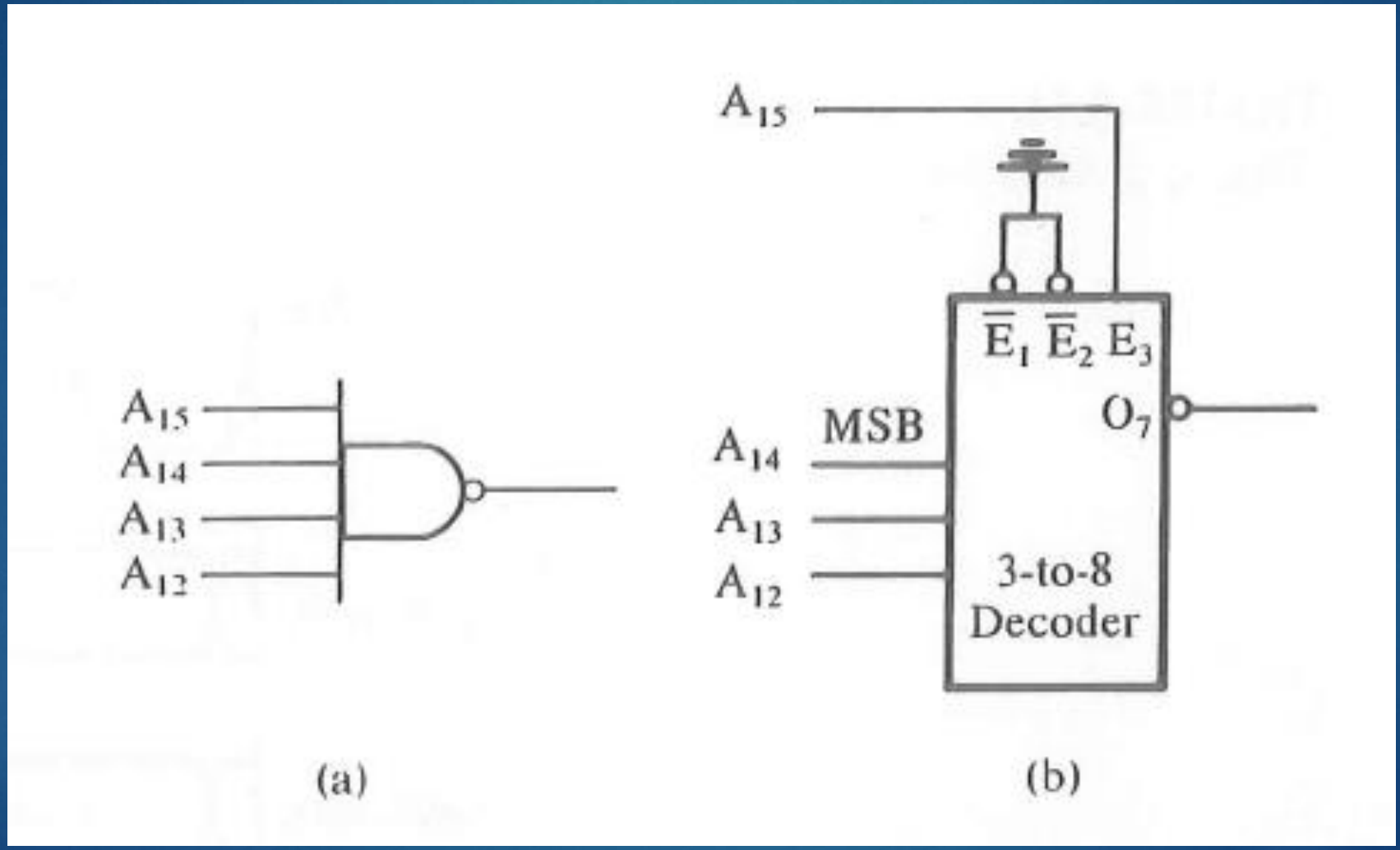
- In order to attach a memory device to the microprocessor, it is necessary to **decode** the address sent from the microprocessor.
- Decoding makes the memory function at a unique section or partition of the memory map.
- Without an address decoder, only one memory device can be connected to a microprocessor, which would make it virtually useless.

Why Decode Memory

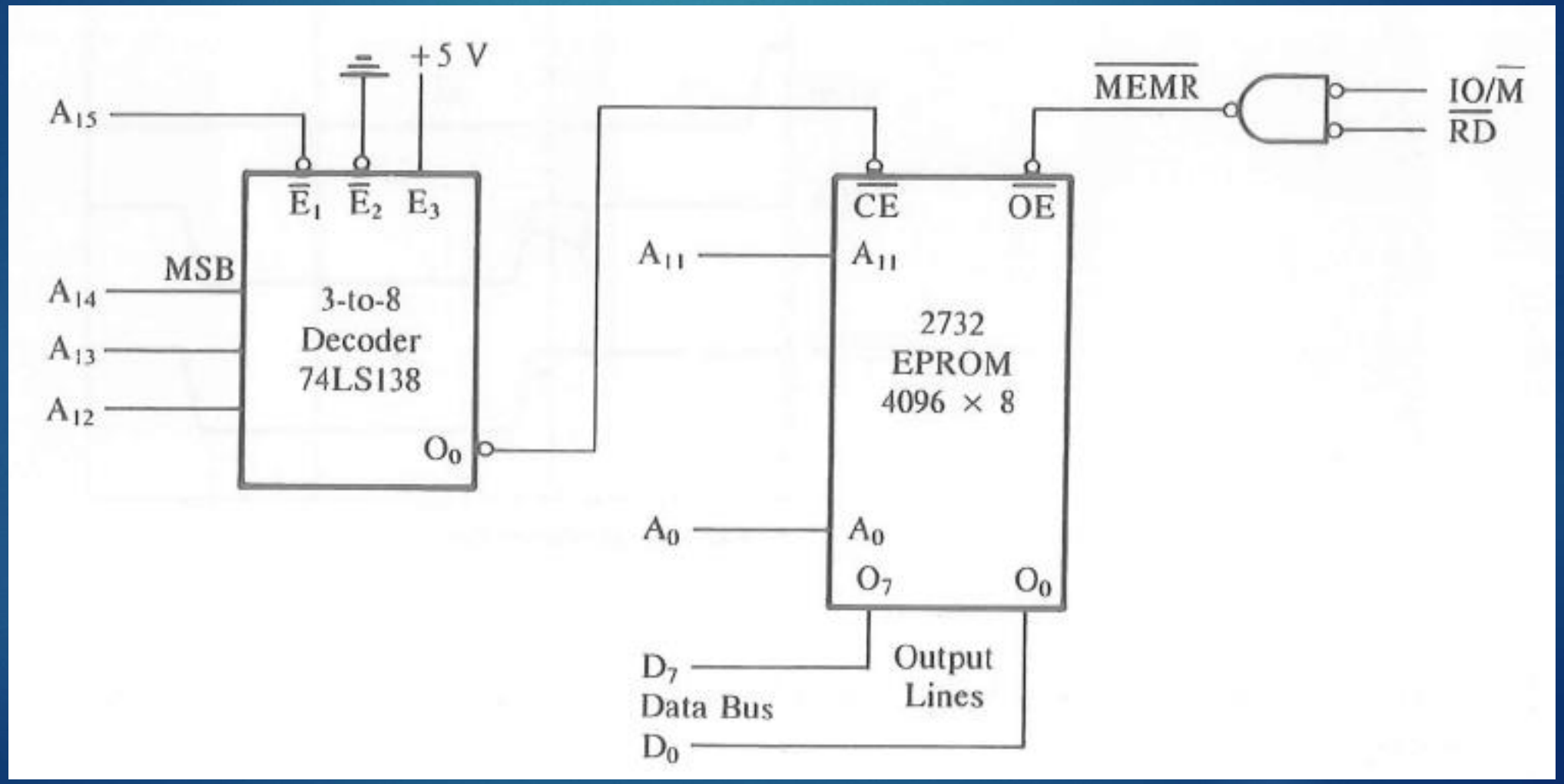
- The 8085 has 16 address connections and the 2716 EPROM has 11 connections.
- The 8085 sends out a 16-bit memory address whenever it reads or writes data.
  - because the 2716 has only 11 address pins, there is a mismatch that must be corrected
- The decoder corrects the **mismatch** by decoding address pins that do not connect to the memory component.


Memory Address
CE
A_{11}
A_{10}
A_9
A_8
A_7
A_6
A_5
A_4
A_3
A_2
A_1
A_0
FFF_H
Internal Decoder
4096 8-Bit Memory Registers
2732 EPROM
$0FFF_H$
0000_H
IO/$\overline{M}$
$\overline{RD}$
$\overline{MEMR}$
$\overline{OE}$
Output Buffer
Output Lines
AD_7
AD_0
Data Bus
O_7
O_0

Interfacing the 2732 EPROM (4096x8)



Interfacing the 2732 EPROM (4096x8)



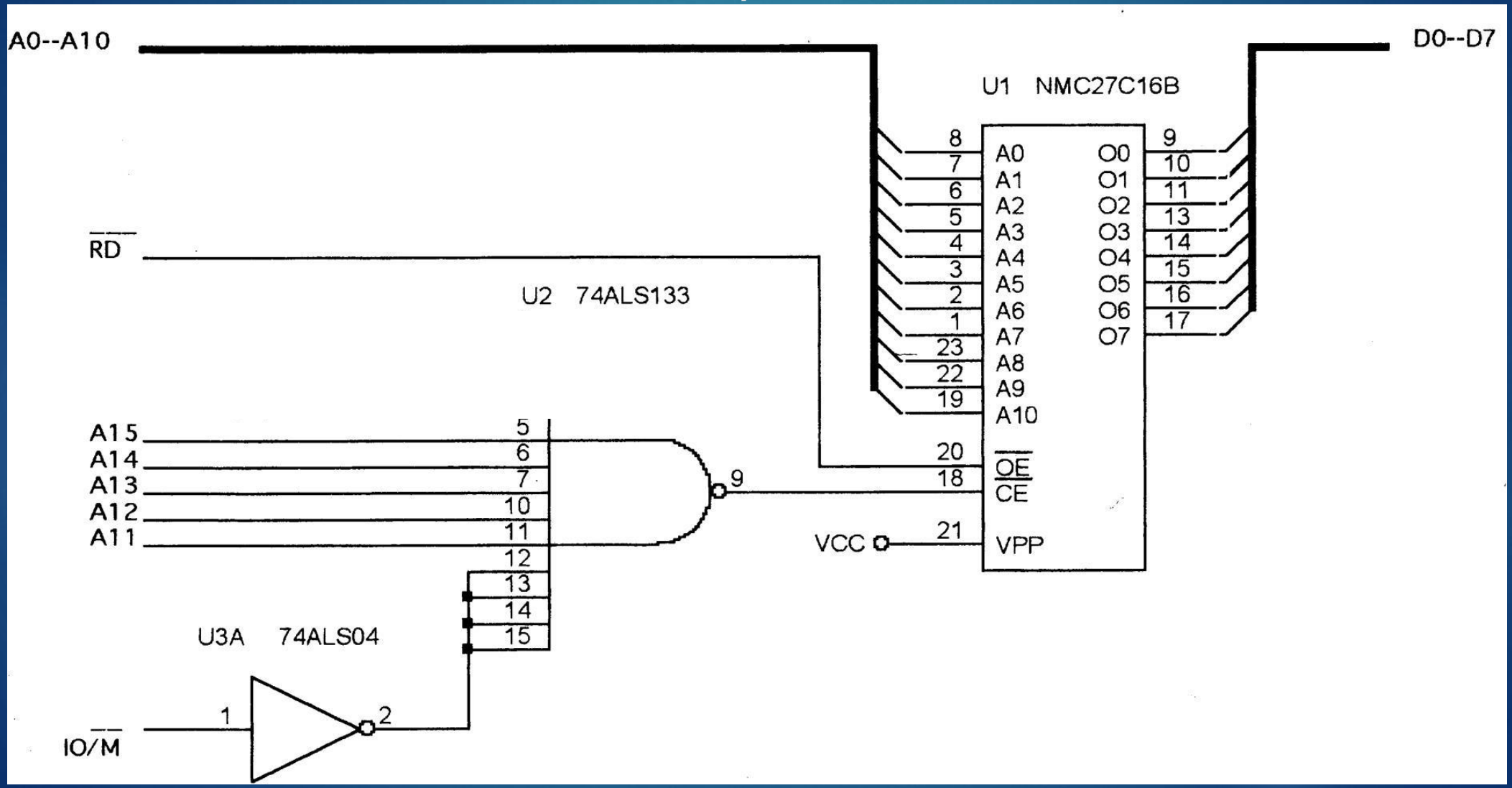
A simple NAND gate decoder that selects a 2716 EPROM for memory location F800H–FFFFH

- If the 16-bit binary address, decoded by the NAND gate, is written so that the leftmost nine bits are 1s and the rightmost 11 bits are **don't cares (X)**, the actual address range of the EPROM can be determined.
  - a don't care is a logic 1 or a logic 0, whichever is appropriate
- Because of the excessive cost of the NAND gate decoder and inverters often required, this option requires an **alternate** be found.

Simple NAND Gate Decoder

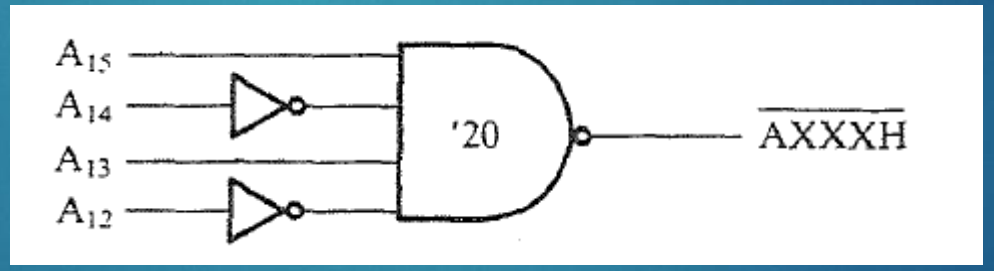
- When the 2K x 8 EPROM is used, address connections A10–A0 of 8085 are connected to address inputs A10–A0 of the EPROM.
  - the remaining nine address pins (A19–A11) are connected to a NAND gate decoder
- The **decoder** selects the EPROM from one of the 2K-byte sections of the 1M-byte memory system in the 8085 microprocessor.
- In this circuit a NAND gate decodes the memory address, as seen in Figure.

A simple NAND gate decoder that selects a 2716 EPROM for memory location F800H–FFFFH



Example 5-2 (Brey-Chapter 5)

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	(A X X X H)
								or								
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	(A 0 0 0 H)
								to								
1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	(A F F F H)



2000H to 27FFH address decoder truth table.

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	or 2000H
								to								
0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	or 27FFH

$$A15 + A14 + \overline{A13} + A12 + A11 = \overline{2000H \text{ to } 27FFH}$$

A15	A14	A13	A12	A11	Out
0	0	0	0	0	1
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	1
0	1	1	0	0	1
0	1	1	0	1	1
0	1	1	1	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	1

2000H to 27FFH address decoder truth table.

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	or 2000H
								to								
0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	or 27FFH

$$A15 + A14 + \overline{A13} + A12 + A11 = \overline{2000H \text{ to } 27FFH}$$

DeMorgan's theorem is used on the left-hand side

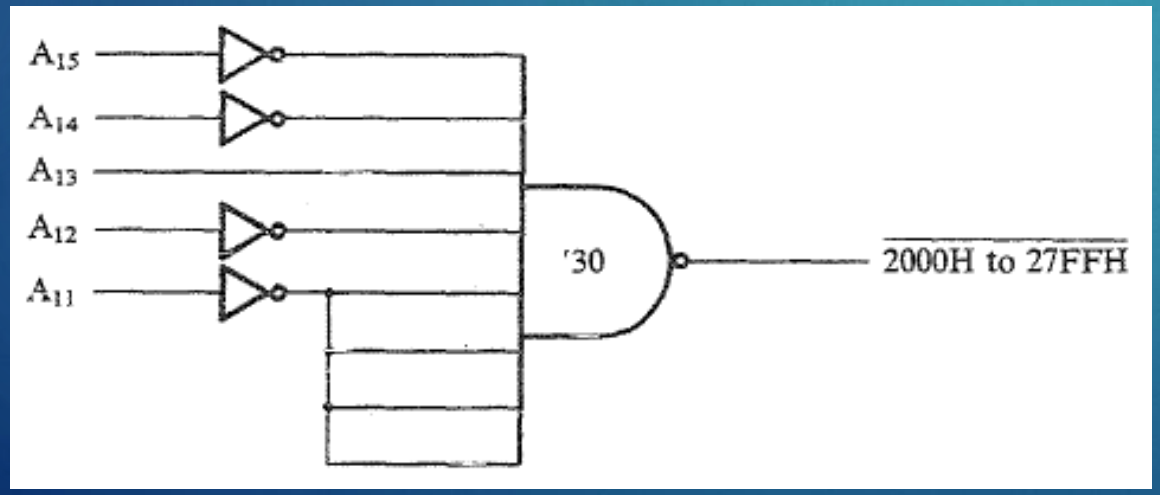
$$\overline{\overline{A15} \cdot \overline{A14} \cdot A13 \cdot \overline{A12} \cdot \overline{A11}} = \overline{2000H \text{ to } 27FFH}$$

A15	A14	A13	A12	A11	Out
0	0	0	0	0	1
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	1
0	1	1	0	0	1
0	1	1	0	1	1
0	1	1	1	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	1

2000H to 27FFH address decoder truth table.

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	or 2000H
								to								
0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	or 27FFH

$$\overline{\overline{A15} \cdot \overline{A14} \cdot A13 \cdot \overline{A12} \cdot \overline{A11}} = \overline{2000H \text{ to } 27FFH}$$



implemented with an eight-input NAND gate (the 74LS30 eight-input NAND) and inverters (the 74LS04 hex inverter).

A15	A14	A13	A12	A11	Out
0	0	0	0	0	1
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	1
0	1	1	0	0	1
0	1	1	0	1	1
0	1	1	1	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	1

The 3-to-8 Line Decoder (74LS138)

3 to 8 Line Decoder

Inputs			Outputs							
x	y	z	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

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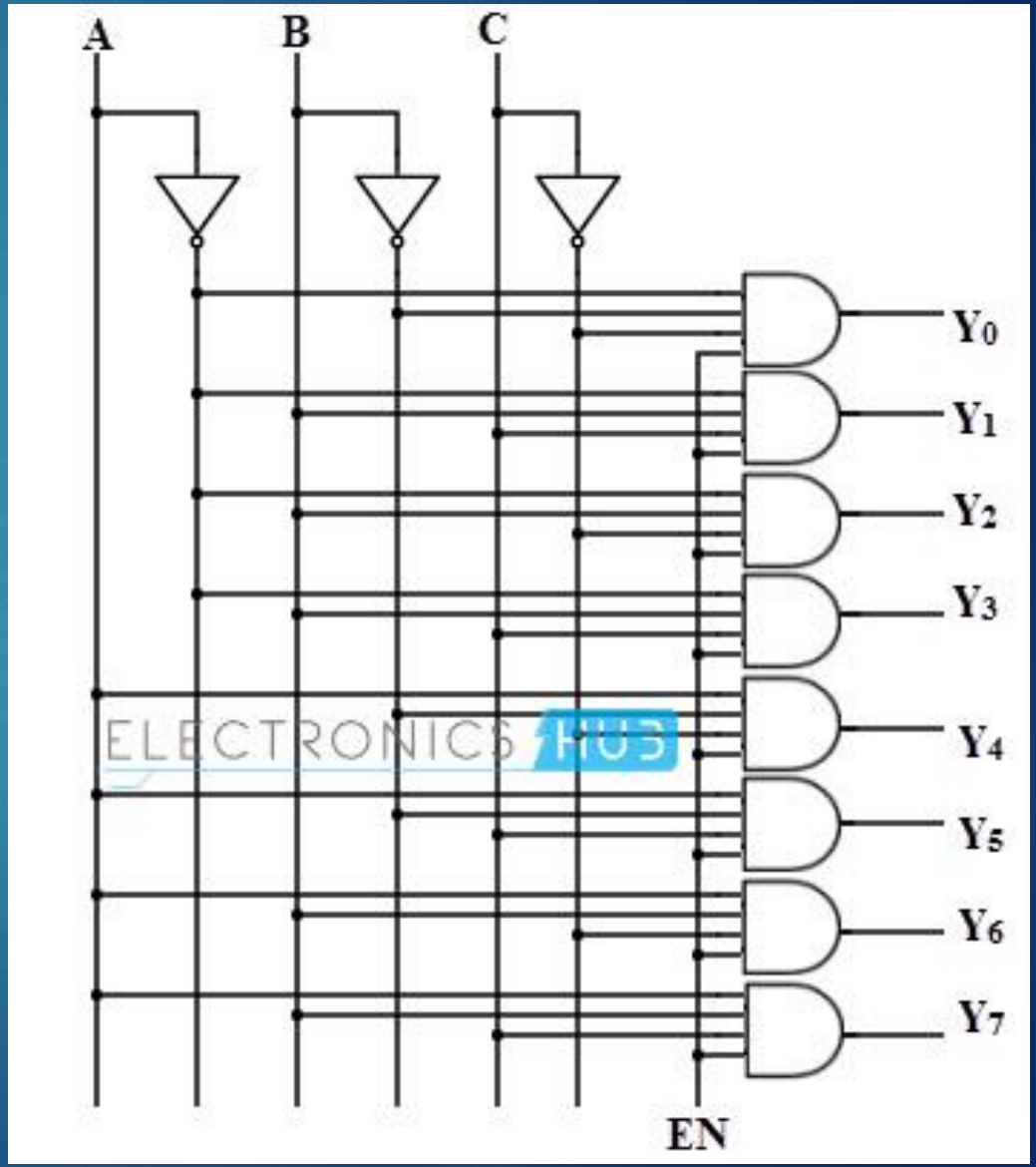
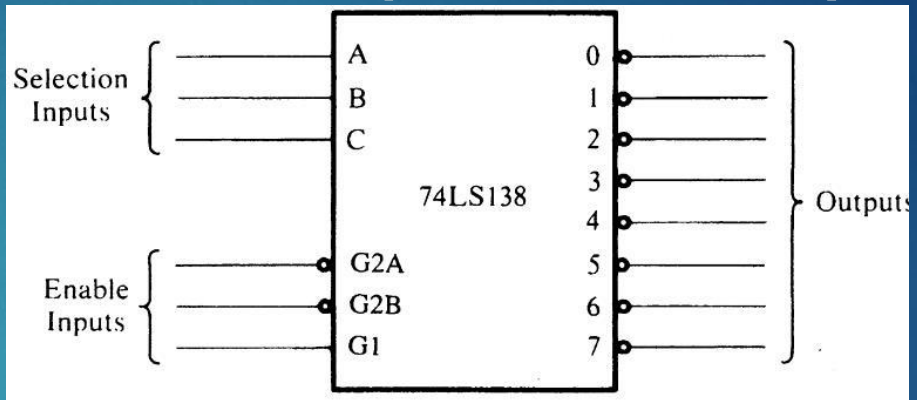


The 3-to-8 Line Decoder (74LS138)

- a common integrated circuit decoder found in many systems is the 74LS138 3-to-8 line decoder.



Inputs						Outputs							
Enable			Select										
$\overline{G2A}$	$\overline{G2B}$	G1	C	B	A	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

- Suppose that a given system requires eight EPROMs of the 2716-type to function at memory addresses 0000H through 3FFFH.

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	or 0000H
								to								
0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	or 3FFFH

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	or 0000H
								to								
0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	or 3FFFH

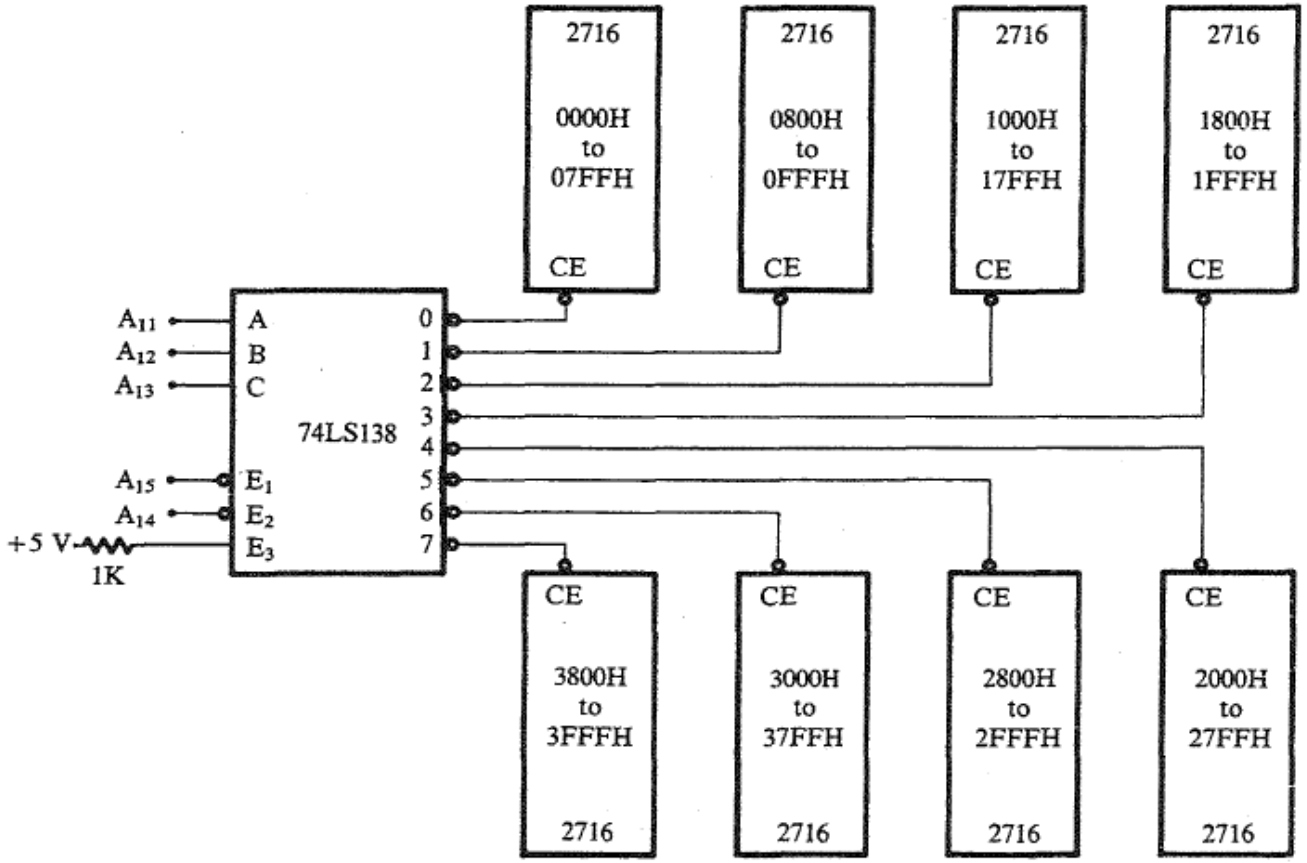


FIGURE 5–15 A circuit that will select one of the eight EPROMs if the correct address appears on the inputs of the 74LS138 3-to-8 line decoder.

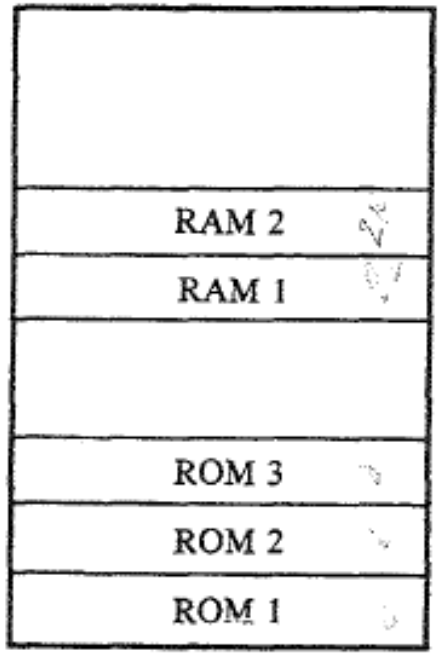
Static Memory System

- Static memory systems are found in applications requiring only a small amount of RAM for implementation.
- Because ROM is always static, the principles in this section apply to the ROM section in any system.
- The first step in developing any system memory is the **memory map.**
- A memory map illustrates which segments are to be used for RAM, and, in some cases, where the I/0 resides.

Memory Map

- System requires 12K bytes of memory for program storage in ROM and 4K bytes of memory for data storage in RAM.
- The segments for both types of memory were arbitrarily chosen for this example problem.

Memory map



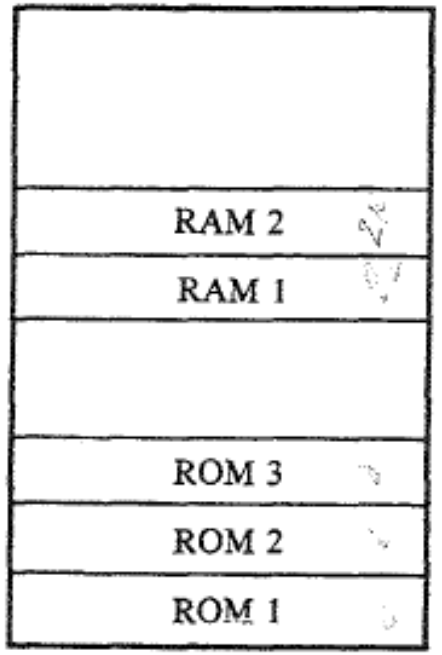
6800H to 6FFFH
6000H to 67FFH
2000H to 2FFFH
1000H to 1FFFH
0000H to 0FFFH

	A_{15} A_{14} A_{13} A_{12}	A_{11} A_{10} A_9 A_8	A_7 A_6 A_5 A_4	A_3 A_2 A_1 A_0
ROM	0 0 0 0	X X X X	X X X X	X X X X
	to			
ROM	0 0 1 0	X X X X	X X X X	X X X X
RAM	0 1 1 0	X X X X	X X X X	X X X X
	to			
RAM	0 1 1 0	X X X X	X X X X	X X X X

Memory Map

- Once the memory has been mapped, the ROM and RAM boundary addresses are written in binary, so that a decoder can be selected for the system.
- In both cases, the address bits that are internally decoded by the memory devices are drawn as don't cares. The remaining address bit positions must be decoded by an external memory address decoder to select or enable the memory devices at the appropriate time.
- Since these ROM and RAM sections have different numbers of address bits to be externally decoded, two decoders are required for this application.

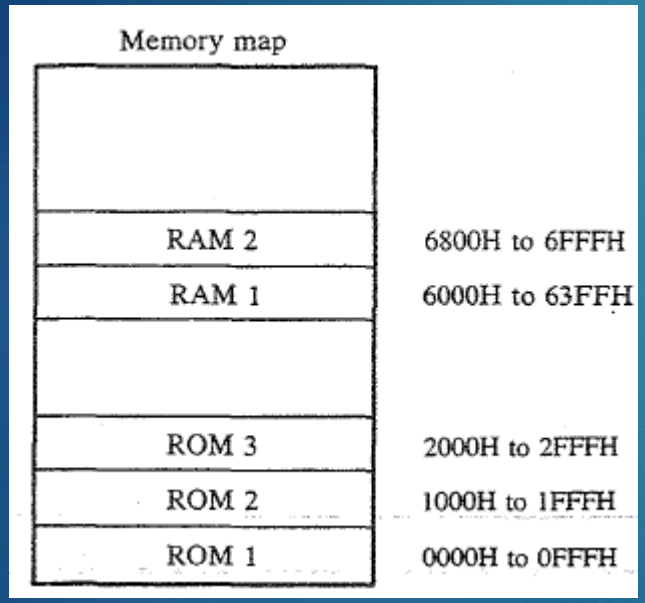
Memory map



6800H to 6FFFH
6000H to 67FFH
2000H to 2FFFH
1000H to 1FFFH
0000H to 0FFFH

	A_{15} A_{14} A_{13} A_{12}	A_{11} A_{10} A_9 A_8	A_7 A_6 A_5 A_4	A_3 A_2 A_1 A_0
ROM	0 0 0 0	X X X X	X X X X	X X X X
	to			
ROM	0 0 1 0	X X X X	X X X X	X X X X
RAM	0 1 1 0	X X X X	X X X X	X X X X
	to			
RAM	0 1 1 0	X X X X	X X X X	X X X X

Incompletely Specified Memory System



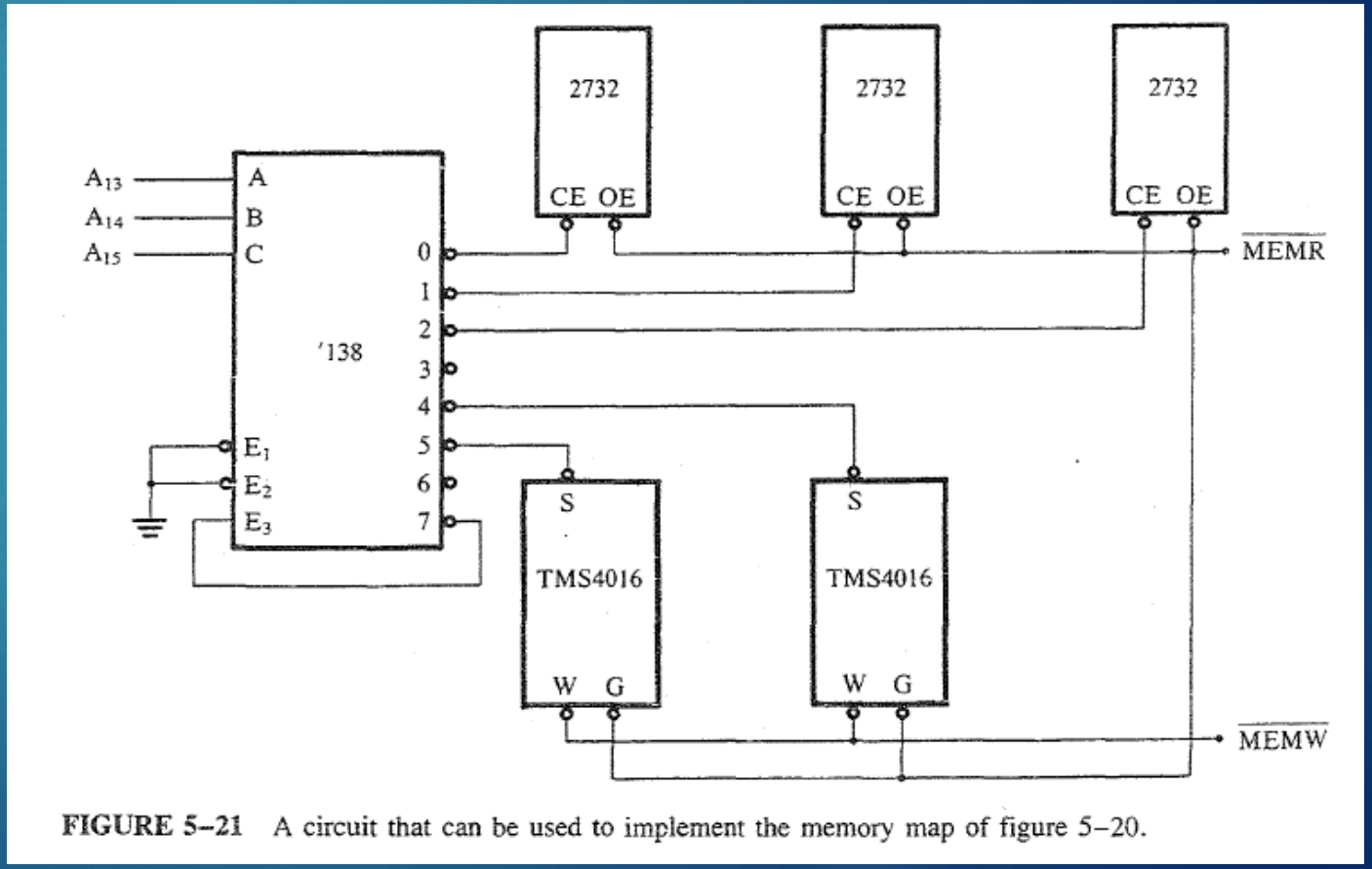


FIGURE 5–21 A circuit that can be used to implement the memory map of figure 5–20.

Absolute Decoding

- The decoding in which all available address line (16 lines in memory mapped and 8 lines in peripheral mapping) are used for decoding to generate a unique address is called absolute

Partial Decoding

- The decoding in which all available address line(16 lines in memory mapping and 8 lines in peripheral mapping) are not used for decoding resulting in multiple address for same port is called partial decoding.