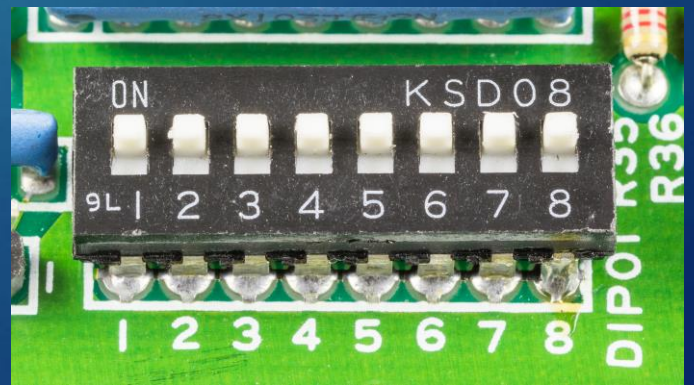
Basic Input/Output Interface Circuitry

Switches

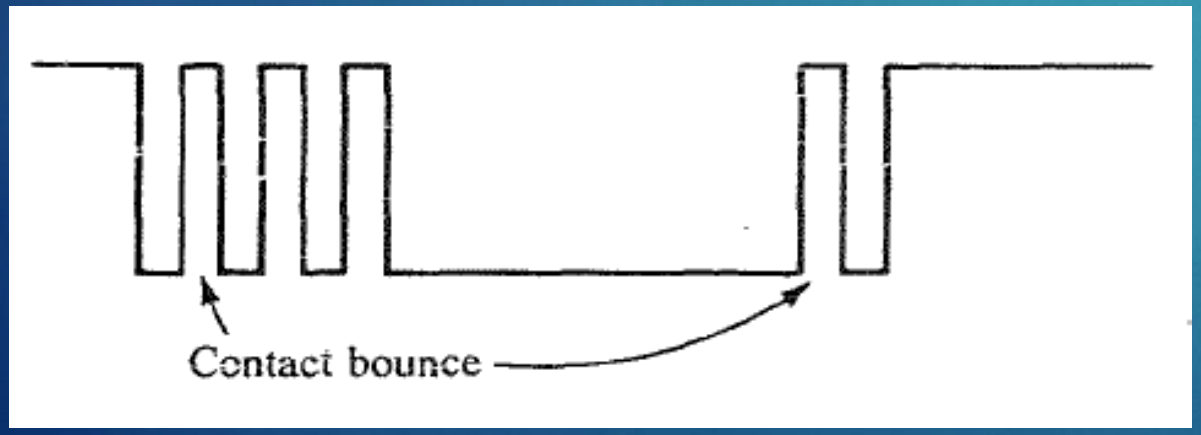
- Almost all switches in use today are single pole, single throw toggle or push button switches.
- In the past, digital electronic circuitry used the single pole, double throw switch because of **contact bounce**.
- Contact bouncing occurs in any mechanical switch and produces many connections or contacts when thrown.
- They bounce in the same way that a hammer bounces when dropped on a hard surface, and this can cause serious problems in most digital systems.



DIP (dual in-line package) Switches

Bouncing-Debouncing

FIGURE 6–1 Contact bounce occurs when a switch is closed and may also occur when it is opened.



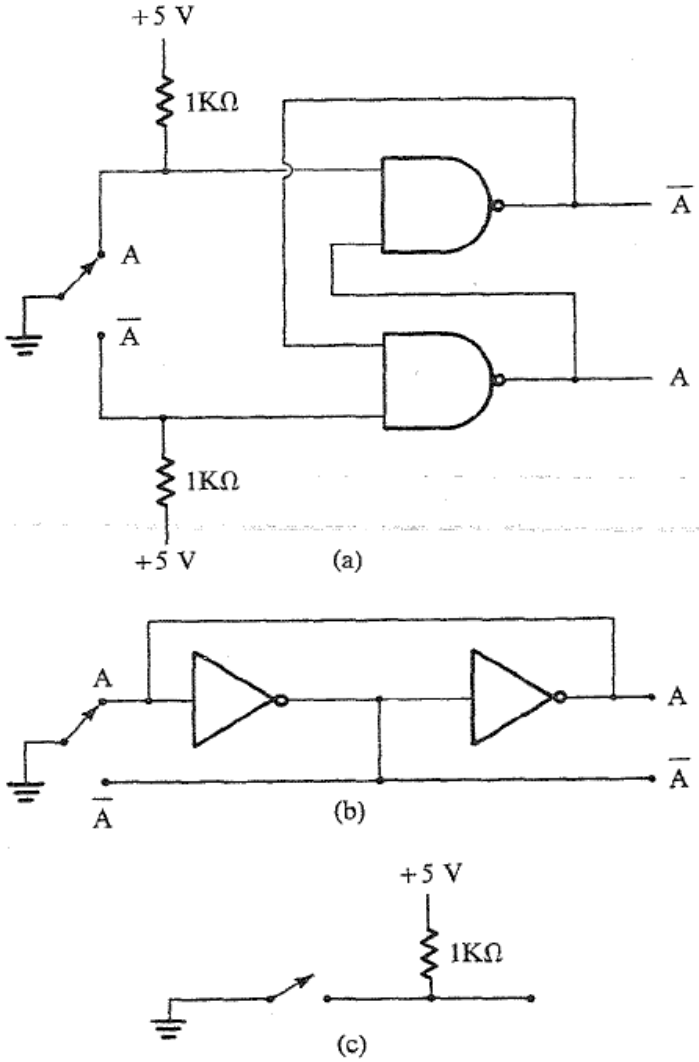


FIGURE 6–2 Switch interface circuitry: (a) a SPDT switch connected to a NAND gate contact bounce eliminator, (b) a SPDT switch connected to an inverter contact bounce eliminator, (c) a SPST switch setup to be connected to a microprocessor based system with software contact bounce elimination.

Interfacing Switches

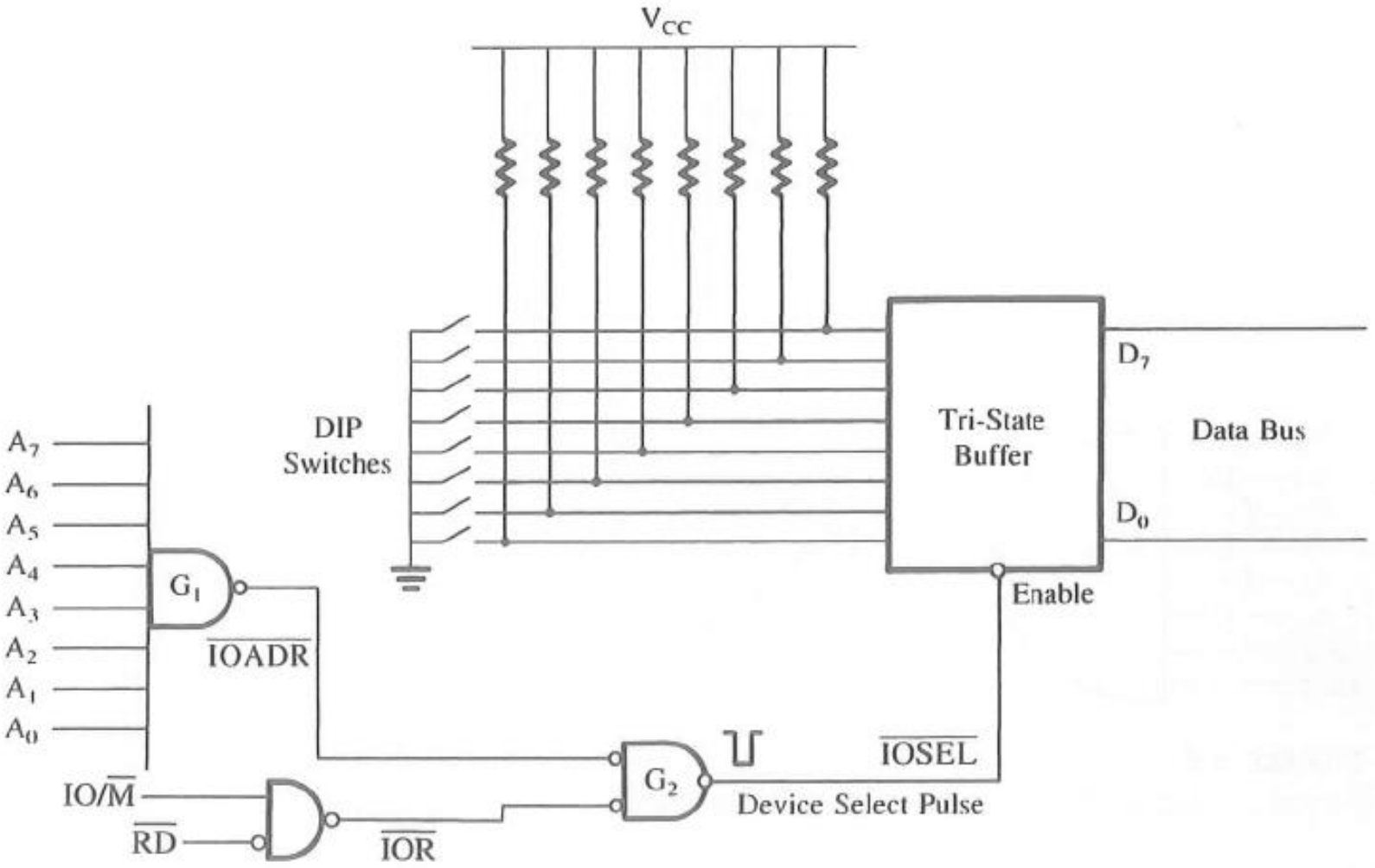
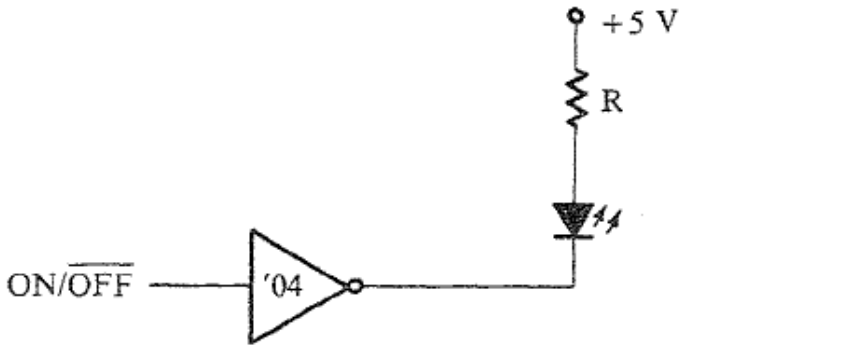


FIGURE 5.6
Decode Logic for a Dip-Switch Input Port

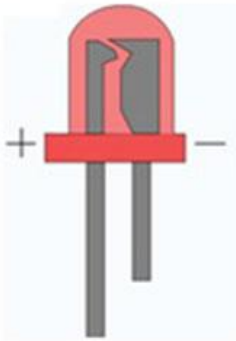
LED-Light Emited Diode

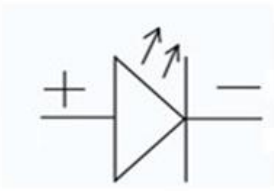
- The display devices in common use today vary considerably from those of the past.
- One of the most common is the simple light-emitting diode, or LED.
- Astandard TTL component drives the LED.
- Most single LEDs require approximately IO mA of current flow to be illuminated at full brilliance.
- Since the forward voltage drop across an LED is approximately 1.65 V, the value of the current limiting resistor would be 330 n in this example.

FIGURE 6–3 A single light emitting diode (LED) connected to an inverter driver.



$$R = \frac{5\ V - 1.65\ V}{Iave} = \frac{3.35v}{Iave}$$





Interfacing LEDs

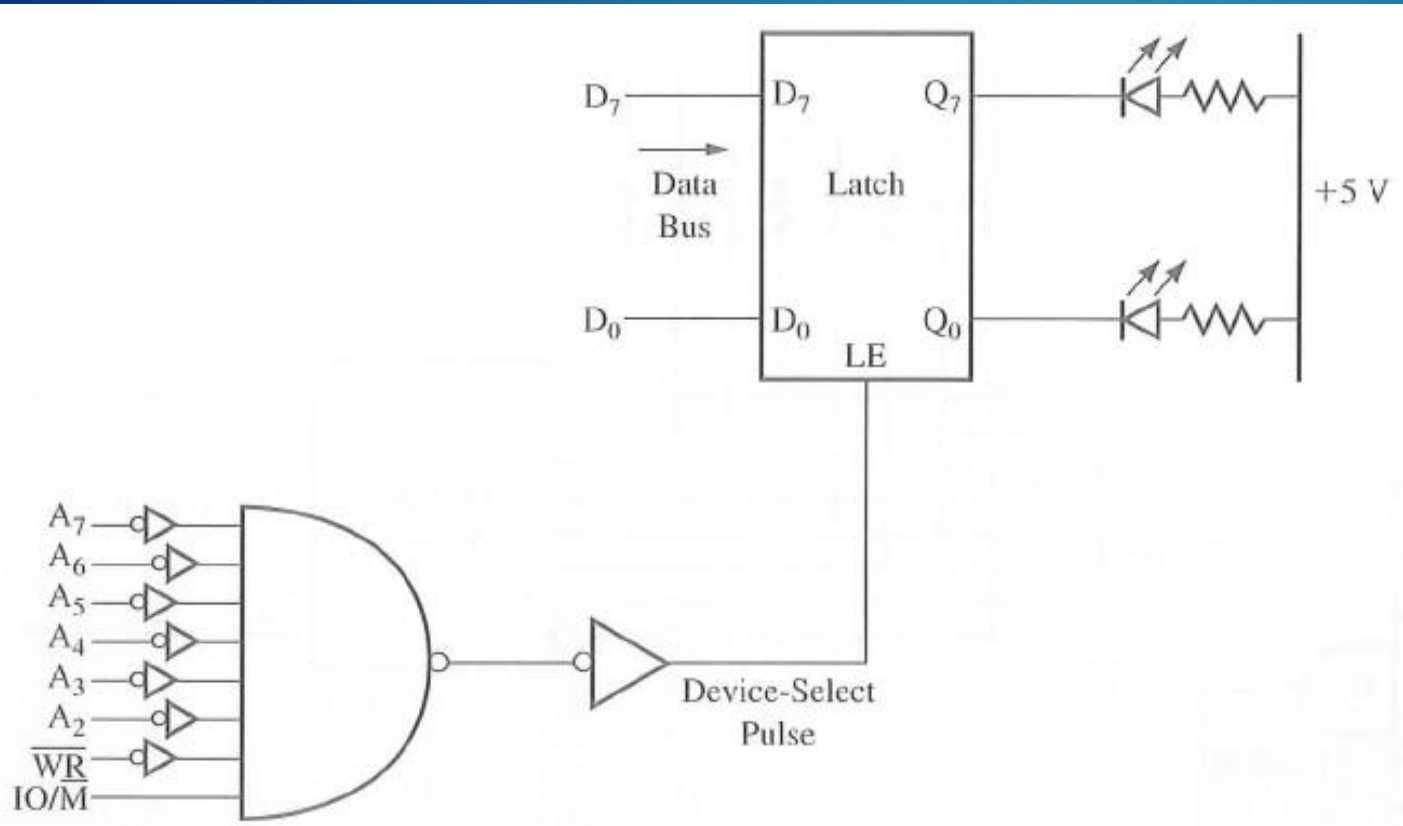
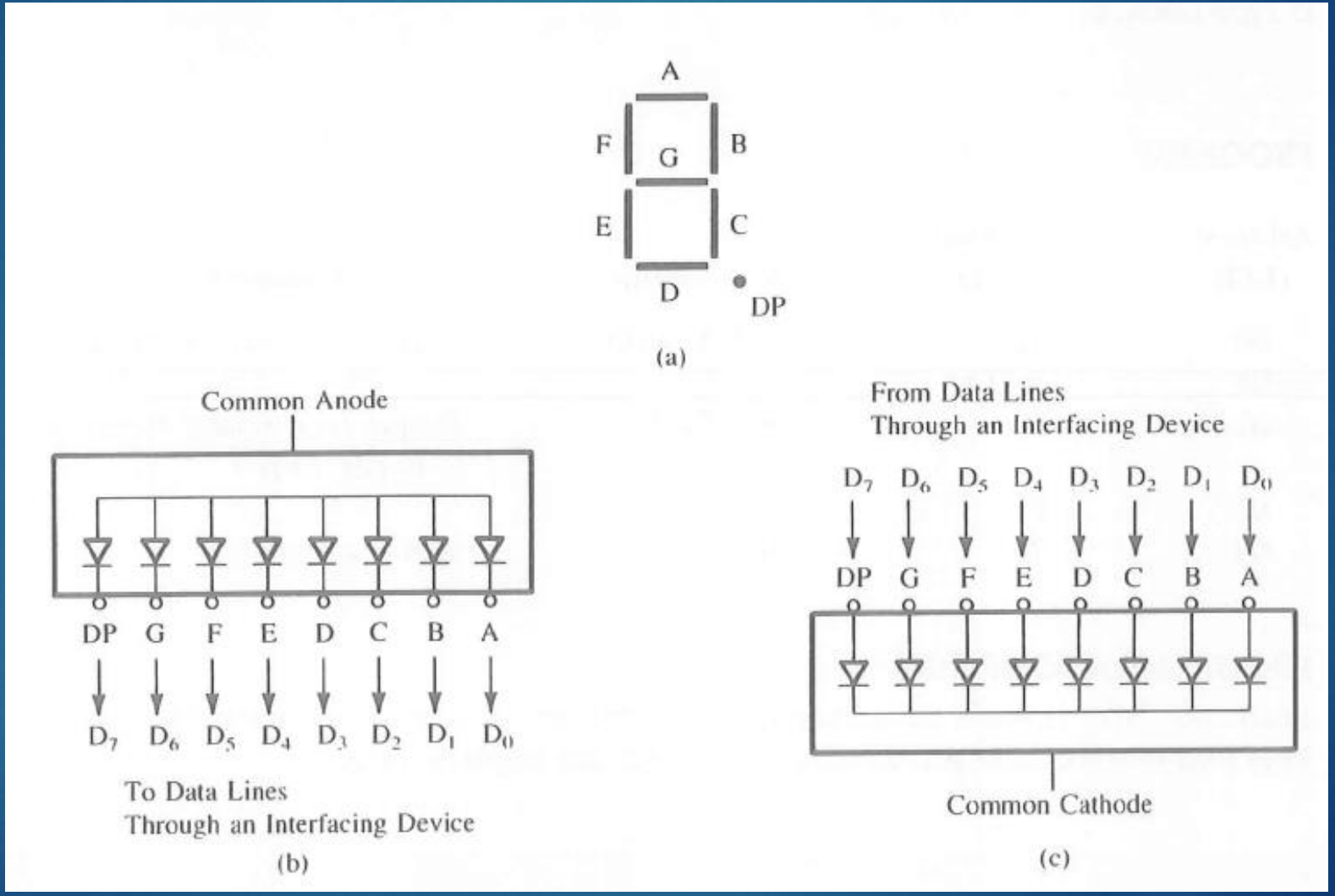


FIGURE 5.5
Partial Decoding: Output Latch with Multiple Addresses

7-Segment Display

- Seven-segment LED display whose internal structure is nothing more than a single LED for each of the lettered segments.
- Drivers for this device can be the same as those indicated in figure 6-3.
- In many cases displays are multiplexed and may require much more current.
- In such cases, you are most likely to find high-current drivers such as transistors or Darlington pairs used in place of the TTL logic gate drivers.

7-Segment Display



Liquid Crystal Displays - LCD

- This type of device is more common in calculators and digital watches than in other areas because it is commonly available in only these formats.
- It has the advantage of being highly visible in bright light where other devices are extremely difficult to see.
- It also uses an extremely low amount of power, which makes it ideal for most applications.

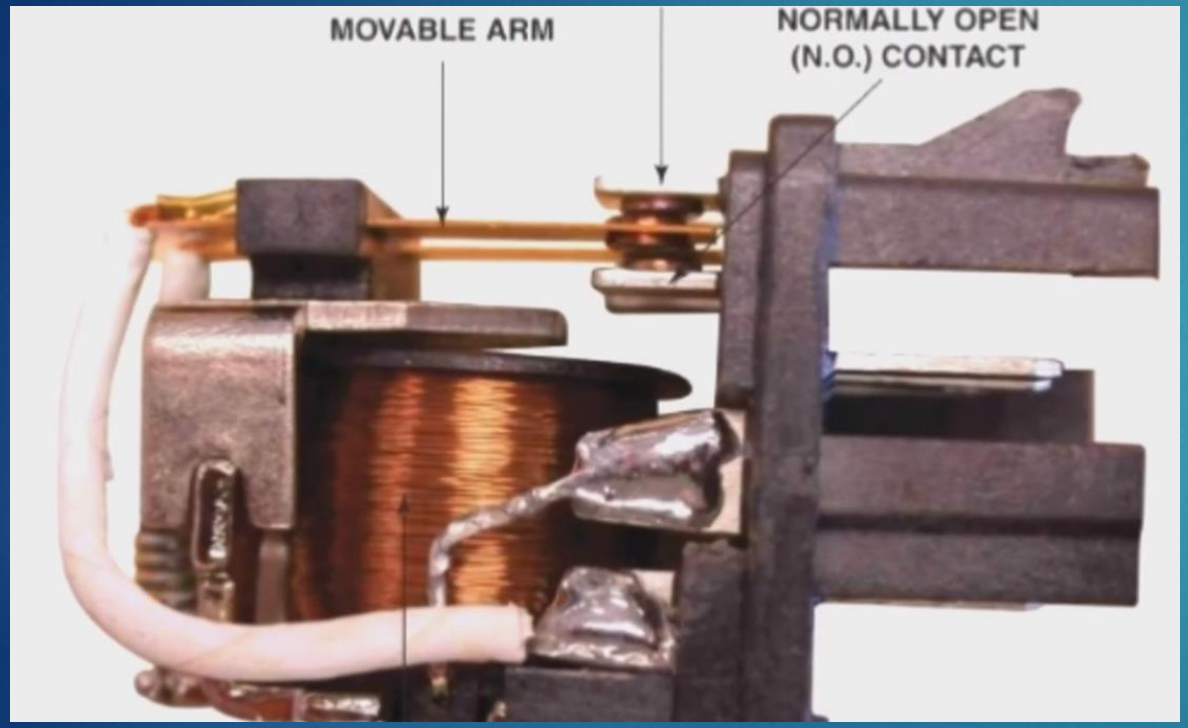
Relays

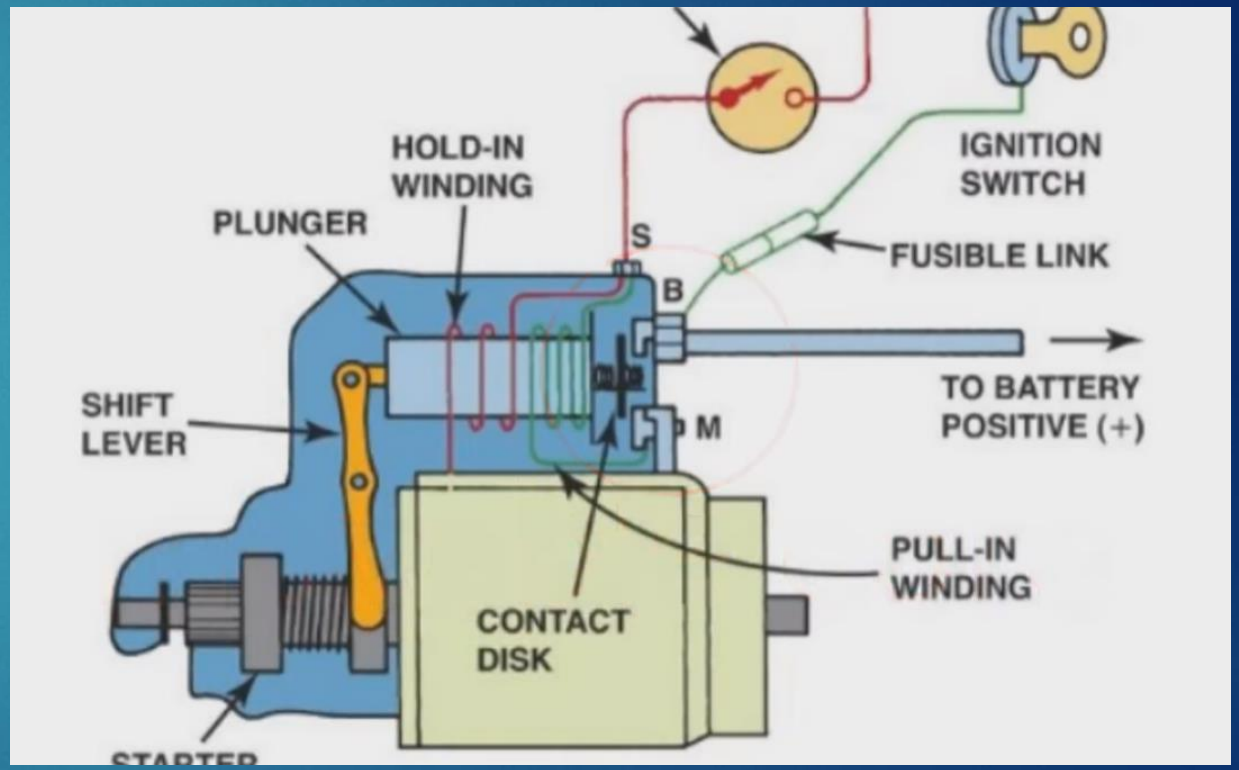
- Relays are used primarily to switch many different voltages at one time or to switch very high voltages.
- One of the most common electro-mechanical switches in a vehicle, the main job of a relay is to allow a low power signal to control a higher powered circuit, or to allow multiple circuits to be controlled by one signal.
- Relays come in a host of designs, from solid-state, which has no moving parts and use semiconductors to control the flow of power, to electromagnetic relays, which uses magnets to physically open and close a switch.A common type of relay you find is a Mini ISO relay, a general purpose relay that comes in an industry standard footprint and fits the needs of many electrical applications such as lighting, starting, horn, heating, and cooling.

Solenoids

- Applications for solenoids include moving mechanical devices such as printing characters on printers.
- One of the most common electro-mechanical switches in a vehicle, the main job of a relay is to allow a low power signal to control a higher powered circuit, or to allow multiple circuits to be controlled by one signal.
- Relays come in a host of designs, from solid-state, which has no moving parts and use semiconductors to control the flow of power, to electromagnetic relays, which uses magnets to physically open and close a switch.
- A common type of relay you find is a Mini ISO relay, a general purpose relay that comes in an industry standard footprint and fits the needs of many electrical applications such as lighting, starting, horn, heating, and cooling.

Relay vs Selenoid

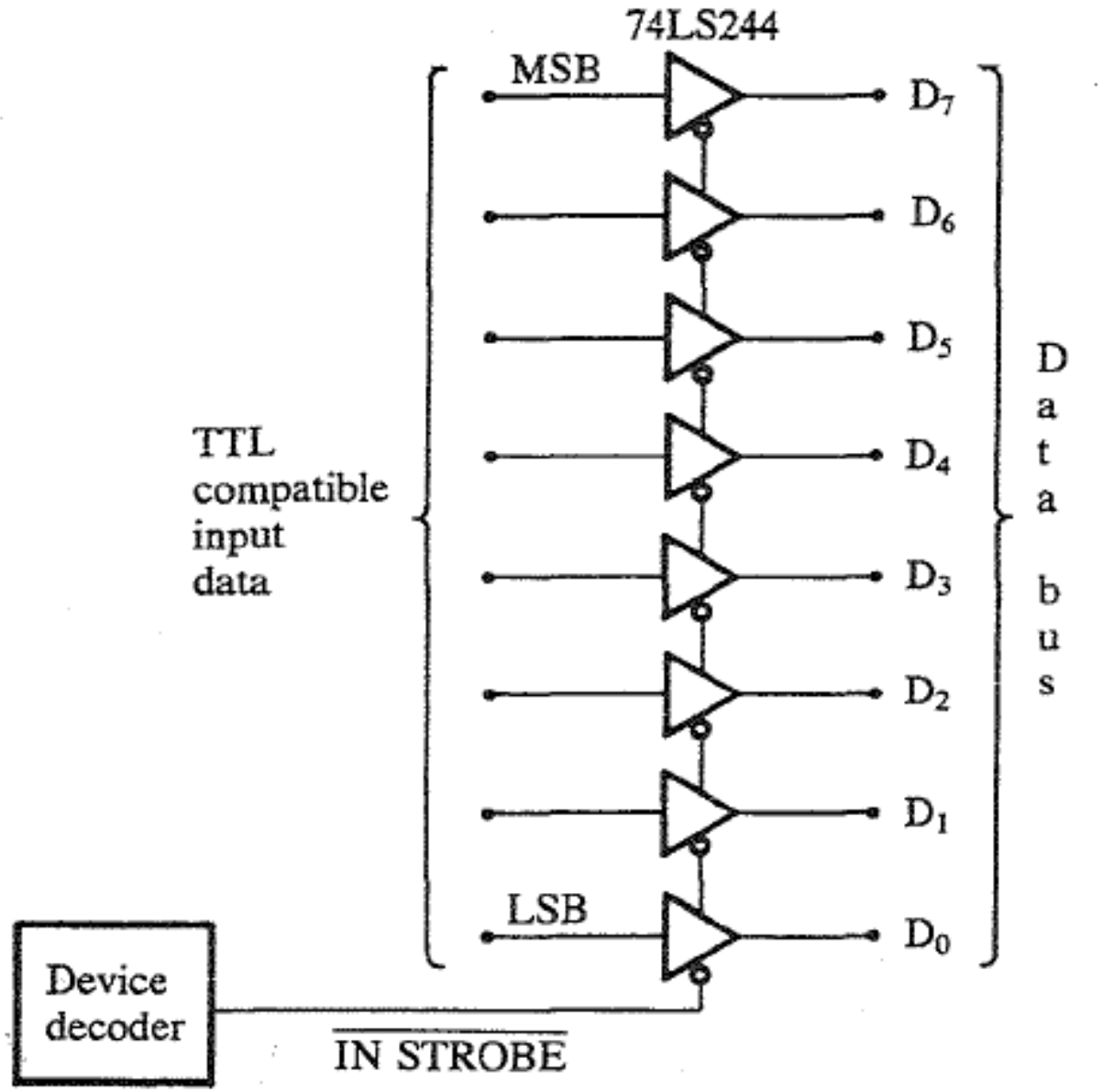




Interface point

- Interface point is the point at which a TTL-compatible input or output device releases or accepts data.
- An input device releases data to the microprocessor, and an output device accepts data from the microprocessor.
- All input and output devices require the same basic interface circuitry.
- The most effective digital switch available is the three-state buffer. Figure 6-10
- illustrates a set of eight buffers, the 74LS244 octal buffer, connected to an 8-bit TTLcompatible input device.
- Examples of TTL-compatible input devices are binary switches, the output of an analog-to-digital converter, and many other types of peripheral interface components.
- The decoder selects the device by producing a logic zero at its output, which enables (turns on) the three-state buffers. In most microprocessors, this strobe is normally active for about 300-1000 ns.

FIGURE 6–10 A typical TTL-compatible input interface circuit illustrating the three-state bus buffers that drive the microprocessor bus.



INPUT/OUTPUT Device Selection

- **Memory mapped I/0** and **isolated I/0** are the two basic input/output schemes in use.
- Memory mapped I/0 treats the inpu/output device as if it were a location in the memory.
- Isolated I/0 treats it separately from the memory.
- Both schemes are usable in most applications, since it is rare that the entire memory is used for program and data storage.

Memory Mapped I/O

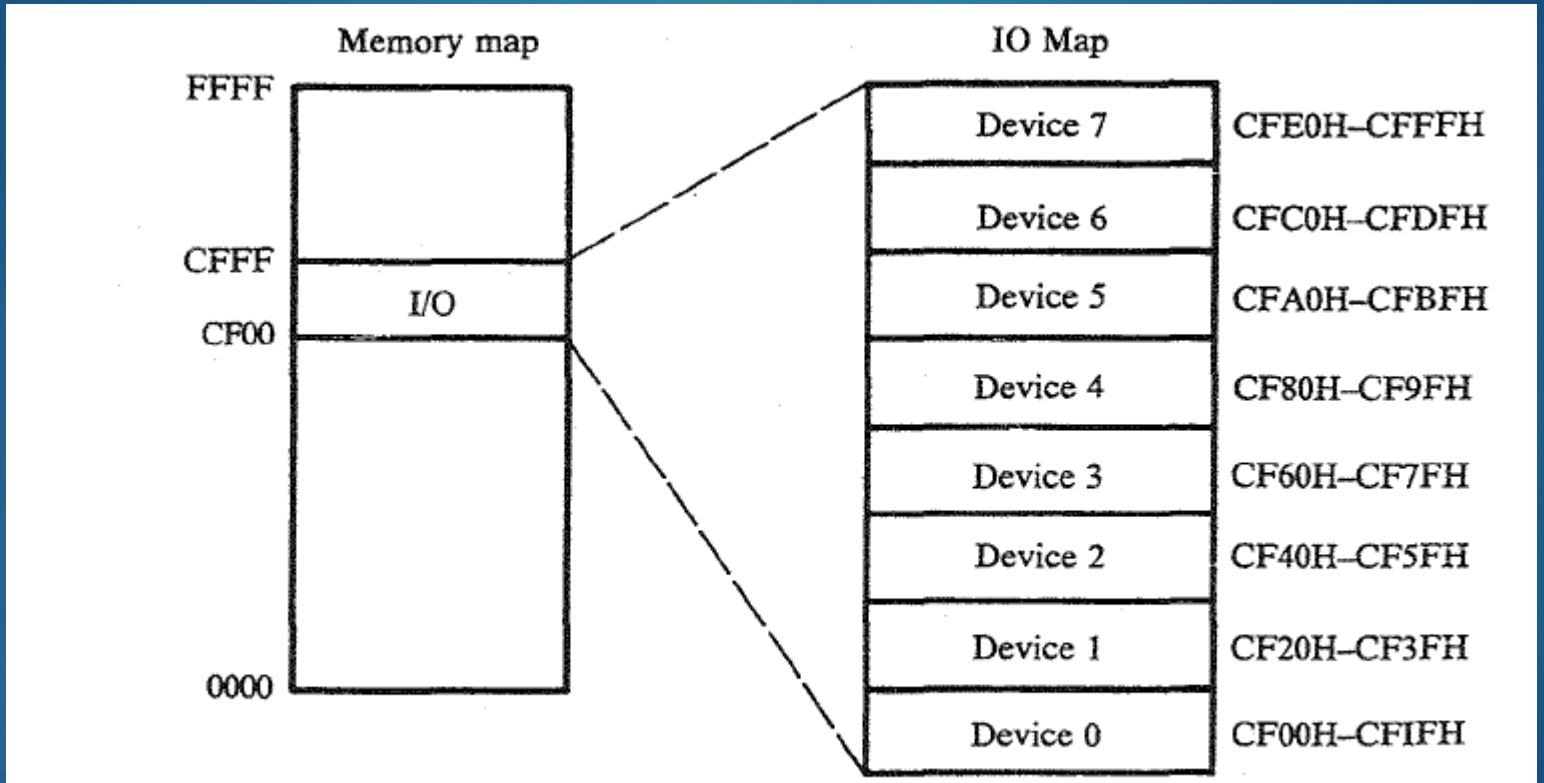


FIGURE 6–12 An example memory and I/O map for memory mapped I/O page CFXX.

Memory Mapped I/O

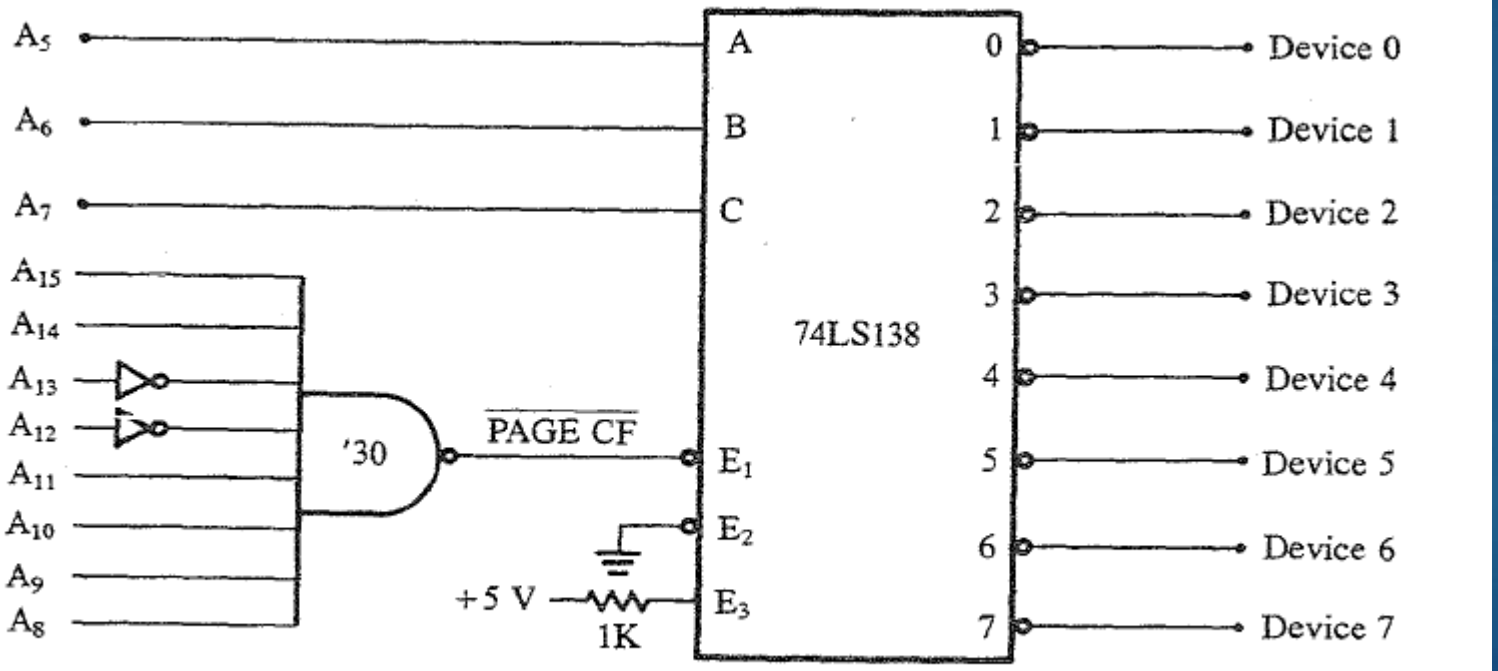


FIGURE 6–13 The memory mapped I/O port decoder for the map illustrated in figure 6–12.

Isolated I/O –(I/O Mapped I/O)

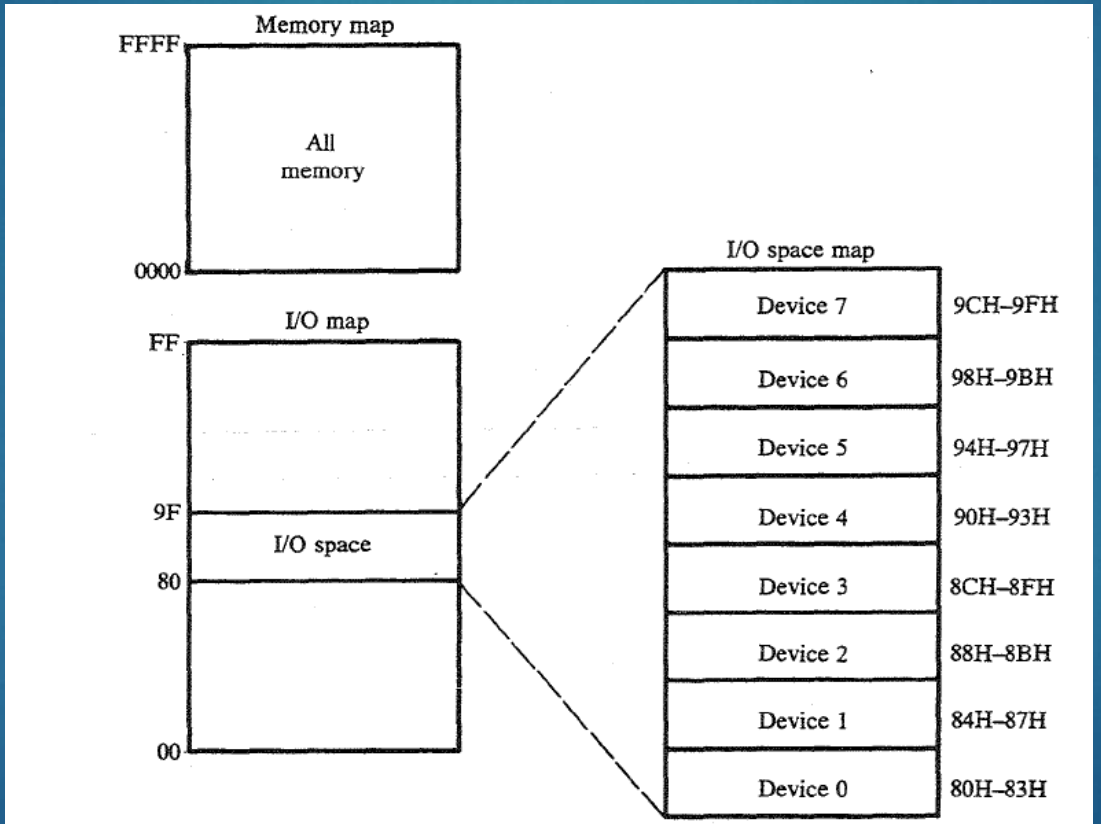
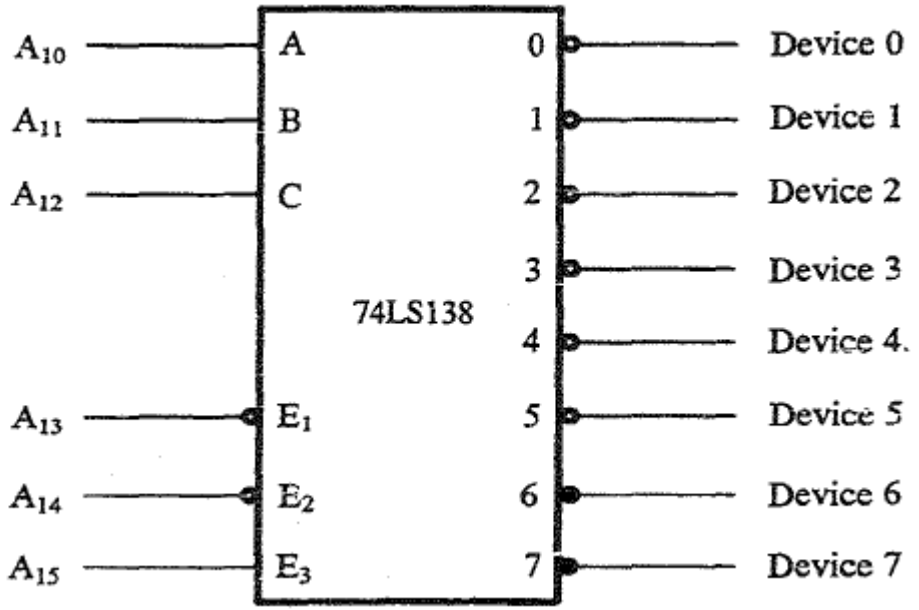


FIGURE 6–14 An example memory map and I/O map for an isolated I/O system.

Isolated I/O –(I/O Map I/O)

FIGURE 6–15 The isolated I/O port decoder for the I/O map illustrated in figure 6–14.



The block diagram (Figure 5.3) illustrates these steps for interfacing an I/O device. In Figure 5.3, address lines A_7–A_0 are connected to a decoder, which will generate a unique pulse corresponding to each address on the address lines. This pulse is combined with the control signal to generate a device select pulse, which is used to enable an output latch or an input buffer.

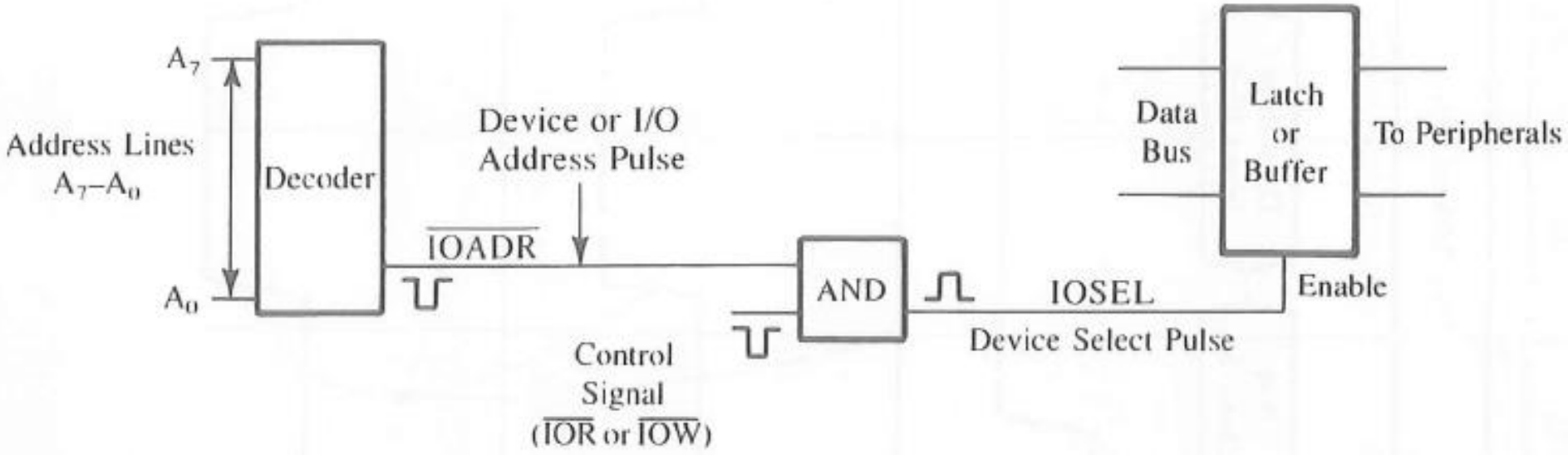


FIGURE 5.3
Block Diagram of I/O Interface

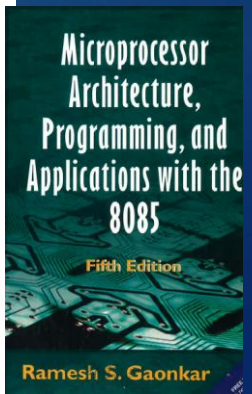


Figure 5.4 shows a practical decoding circuit for the output device with address 01H. Address lines A_7–A_0 are connected to the 8-input NAND gate that functions as a decoder. Line A_0 is connected directly, and lines A_7–A_1 are connected through the inverters. When the address bus carries address 01H, gate G_1 generates a low pulse; otherwise, the output remains high. Gate G_2 combines the output of G_1 and the control signal $\overline{IOW}$ to generate an I/O select pulse when both input signals are low. Meanwhile (as was shown in the timing diagram—Figure 5.1, machine cycle M_3), the contents of the accumulator are placed on the data bus and are available on the data bus for a few microseconds and, therefore, must be latched for display. The I/O select pulse clocks the data into the latch for display by the LEDs.

FIGURE 5.3
Block Diagram of I/O Interface

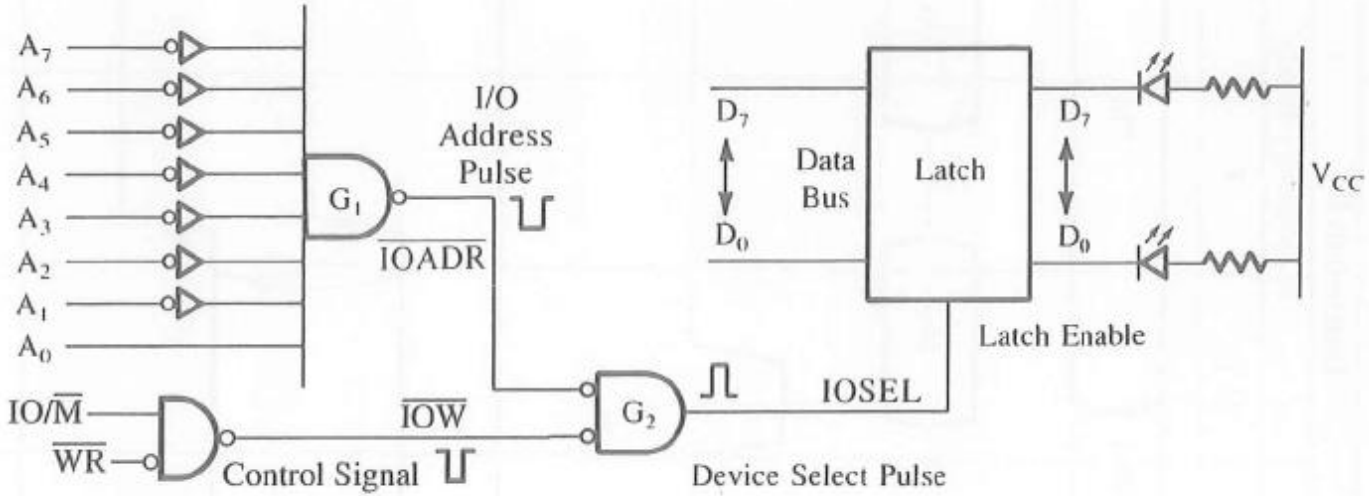
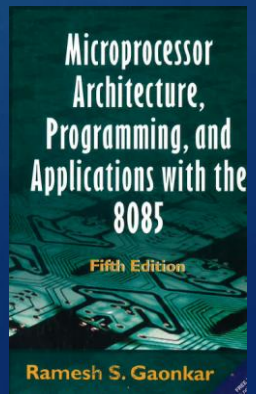


FIGURE 5.4
Decode Logic for LED Output Port

NOTE: To use this circuit with the 8085, the bus AD_7–A_0 must be demultiplexed.



I/O Strobe Generation – Memory Map I/O

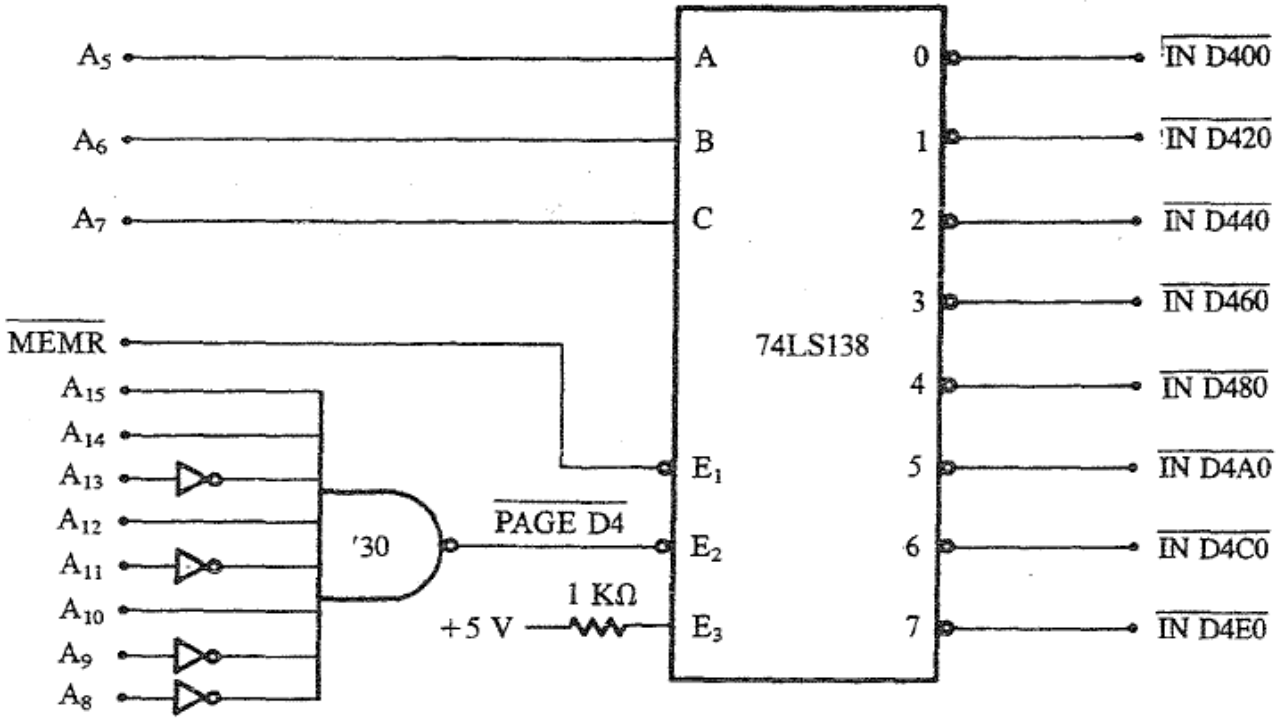
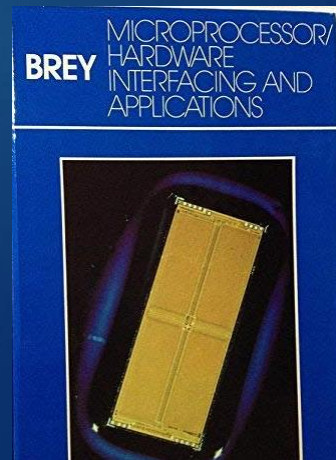


FIGURE 6–16 A circuit that will develop eight different memory mapped I/O strobes. These signals will only go low for a read from the indicated ranges of memory.



I/O Strobe Generation – Isolated I/O

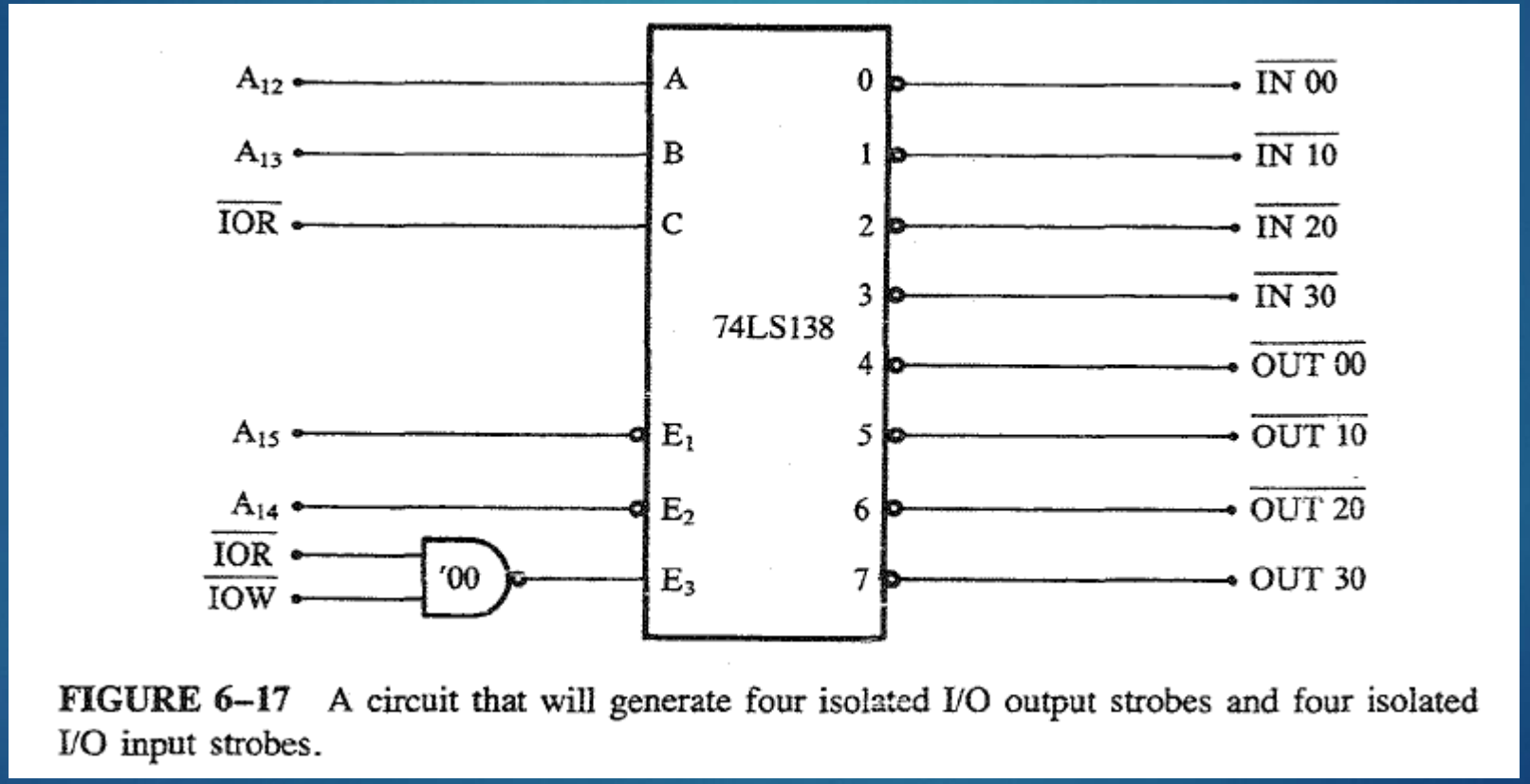
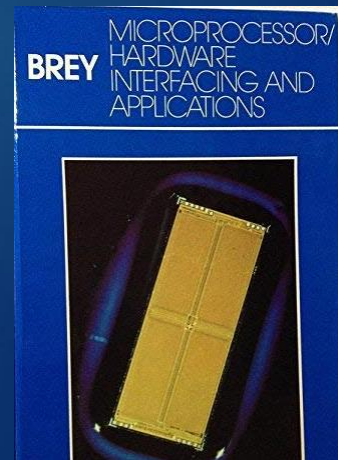


FIGURE 6–17 A circuit that will generate four isolated I/O output strobes and four isolated I/O input strobes.



LED Display for Binary Data

PROBLEM STATEMENT

1. Analyze the interfacing circuit in Figure 5.8(a), identify the address of the output port, and explain the circuit operation.
2. Explain similarities between (a) and (b) in Figure 5.8.
3. Write instructions to display binary data at the port.

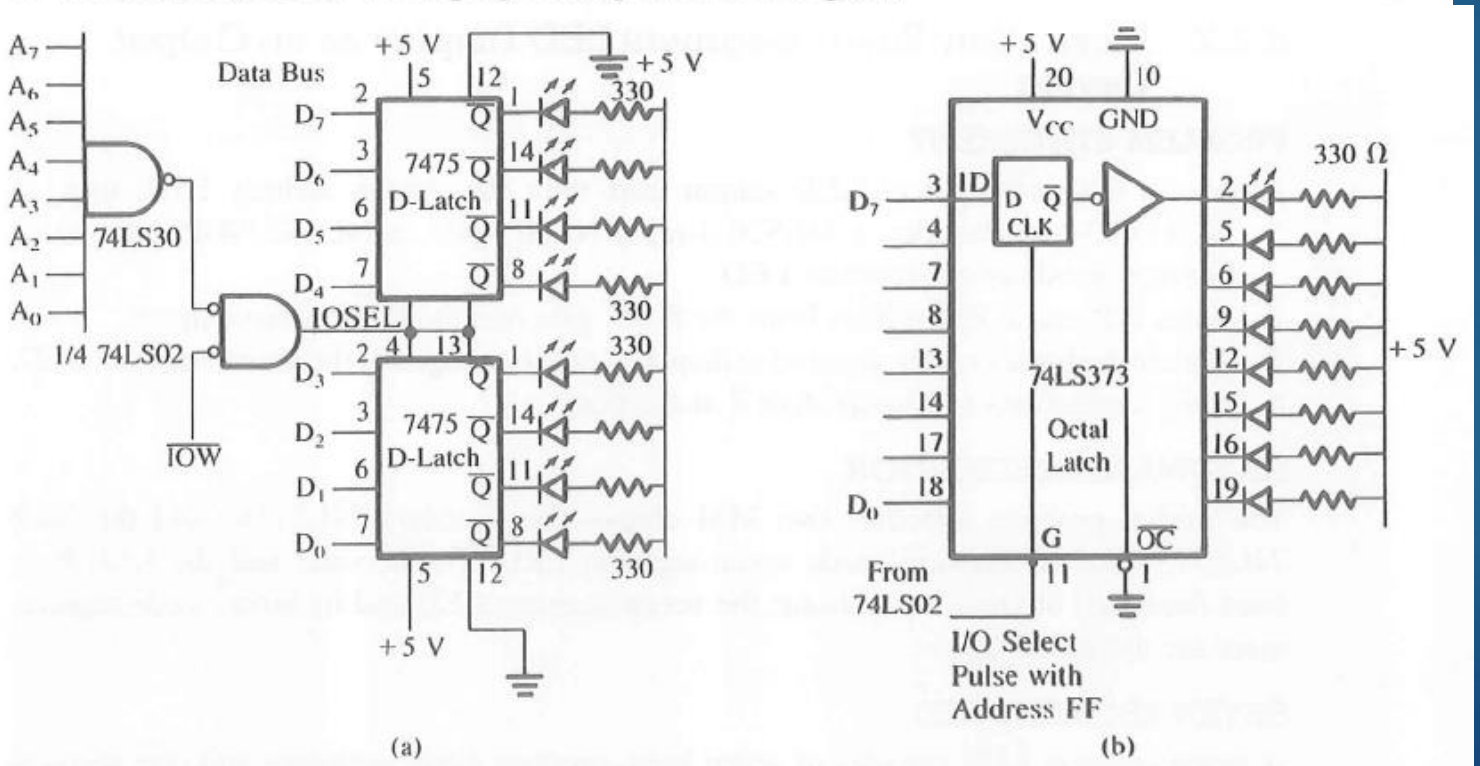
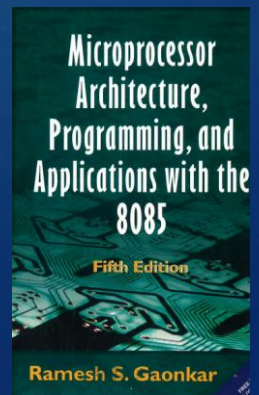


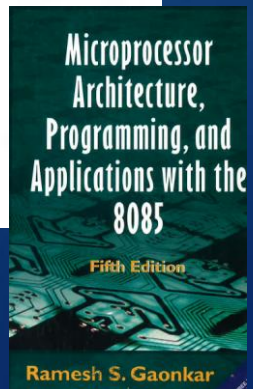
FIGURE 5.8
Interfacing LED Output Port Using the 7475 D-Type Latch (a) and Using the 74LS373 Octal D-Type Latch (b)



LED Display for Binary Data

PROGRAM

Address (LO)	Machine Code	Mnemonics	Comments
00	3E	MVI A,DATA	;Load accumulator with data
01	DATA*		
02	D3	OUT FFH	;Output accumulator contents
			; to port FFH
03	FF		
04	76	HLT	;End of program



Sevem Segment LED Display as an Output

PROBLEM STATEMENT

1. Design a seven-segment LED output port with the device address F5H, using a 74LS138 3-to-8 decoder, a 74LS20 4-input NAND gate, a 74LS02 NOR gate, and a common-anode seven-segment LED.
2. Given $\overline{WR}$ and IO/$\overline{M}$ signals from the 8085, generate the $\overline{IOW}$ control signal.
3. Explain the binary codes required to display 0 to F Hex digits at the seven-segment LED.
4. Write instructions to display digit 7 at the port.

1. It is a common-anode seven-segment LED, and logic 0 is required to turn on a segment.
2. To display digit 7, segments A, B, and C should be turned on.
3. The binary code should be

Data Lines	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Bits	X	1	1	1	1	0	0	0	= 78H
Segments	NC	G	F	E	D	C	B	A	

The code for each digit can be determined by examining the connections of the data lines to the segments and the logic requirements.

Sevem Segment LED Display as an Output

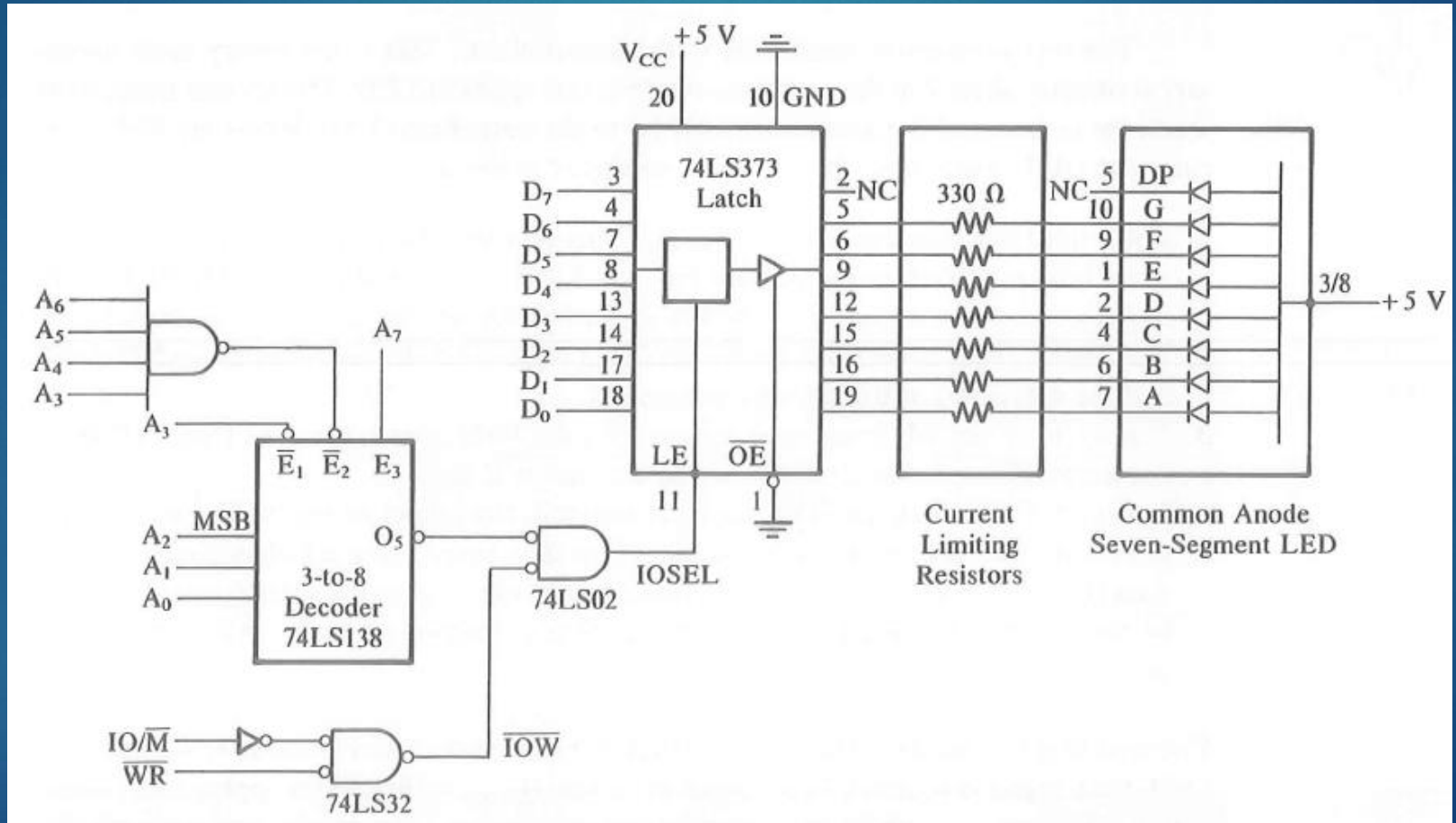


FIGURE 5.10
Interfacing Seven-Segment LED

Sevem Segment LED Display as an Output

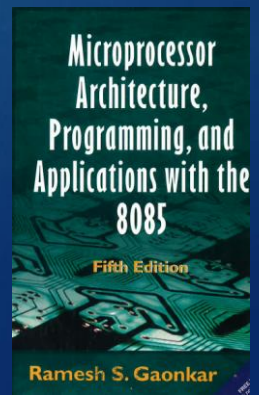
To design an output port with the address F5H, the address lines A_7–A_0 should have the following logic:

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	1	1	1	0	1	0	1	= F5H

This can be accomplished by using A_2, A_1, and A_0 as input lines to the decoder. A_3 can be connected to active low enable $\overline{E}_1$, and the remaining address lines can be connected to $\overline{E}_2$ through the 4-input NAND gate. Figure 5.10 shows an output port with the address F5H. The output O_5 of the decoder is logically ANDed with the control signal $\overline{IOW}$ using the NOR gate (74LS02). The output of the NOR gate is the I/O select pulse that is used to enable the latch (74LS373). The control signal $\overline{IOW}$ is generated by logically ANDing $IO/\overline{M}$ and $\overline{WR}$ signals in the negative NAND gate (physically OR gate 74LS32).

Instructions The following instructions are necessary to display digit 7 at the output port:

```
MVI A,78H     ;Load seven-segment code in the accumulator
OUT F5H       ;Display digit 7 at port F5H
HLT           ;End
```



Data Input from DIP Switches

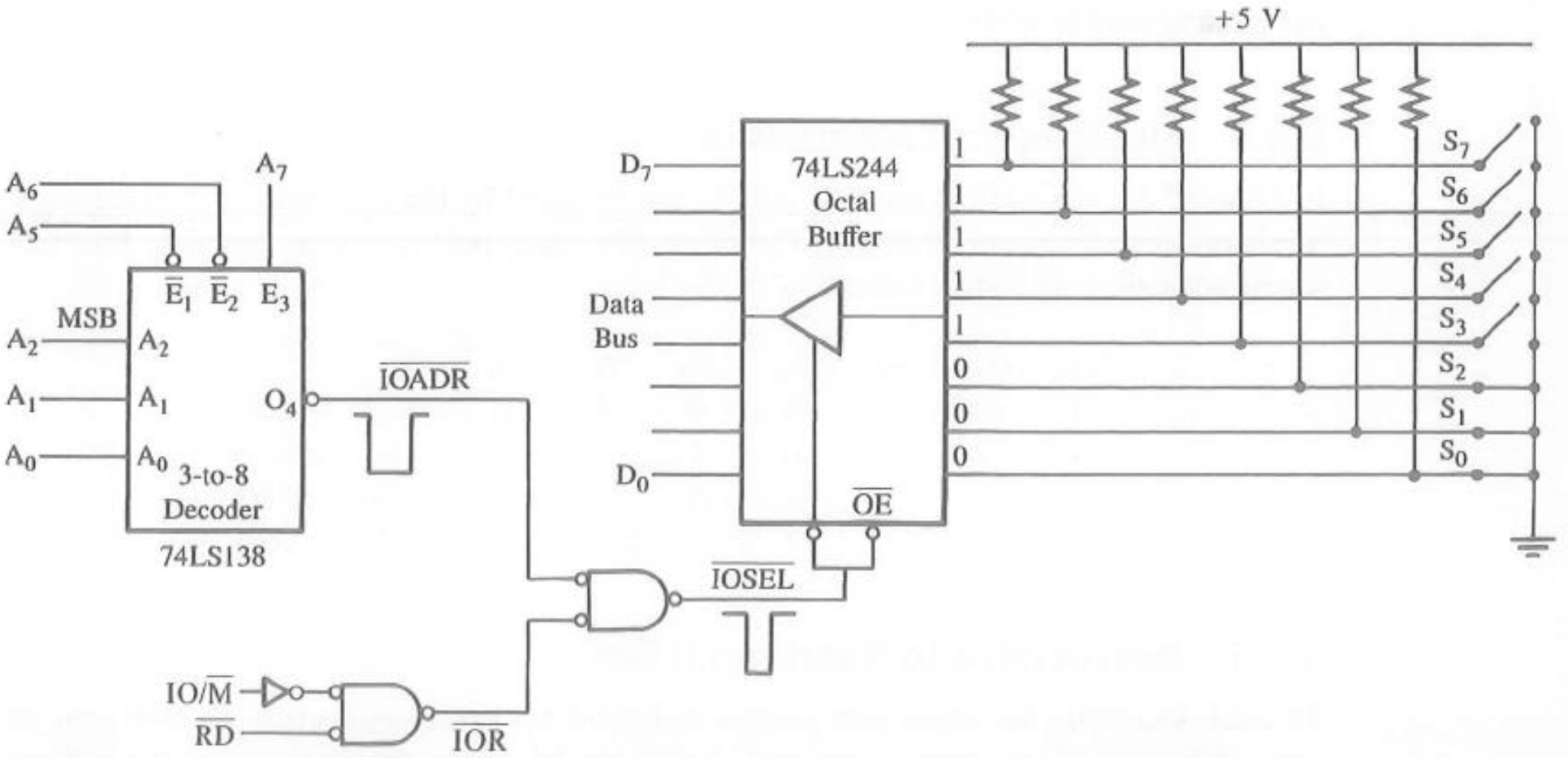
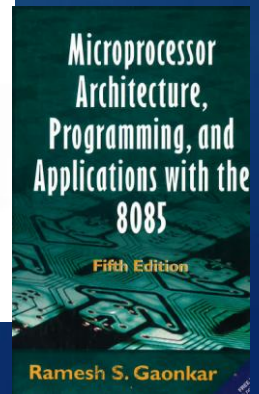


FIGURE 5.11
Interfacing DIP Switches



Control System Using Memory Mapped I/O

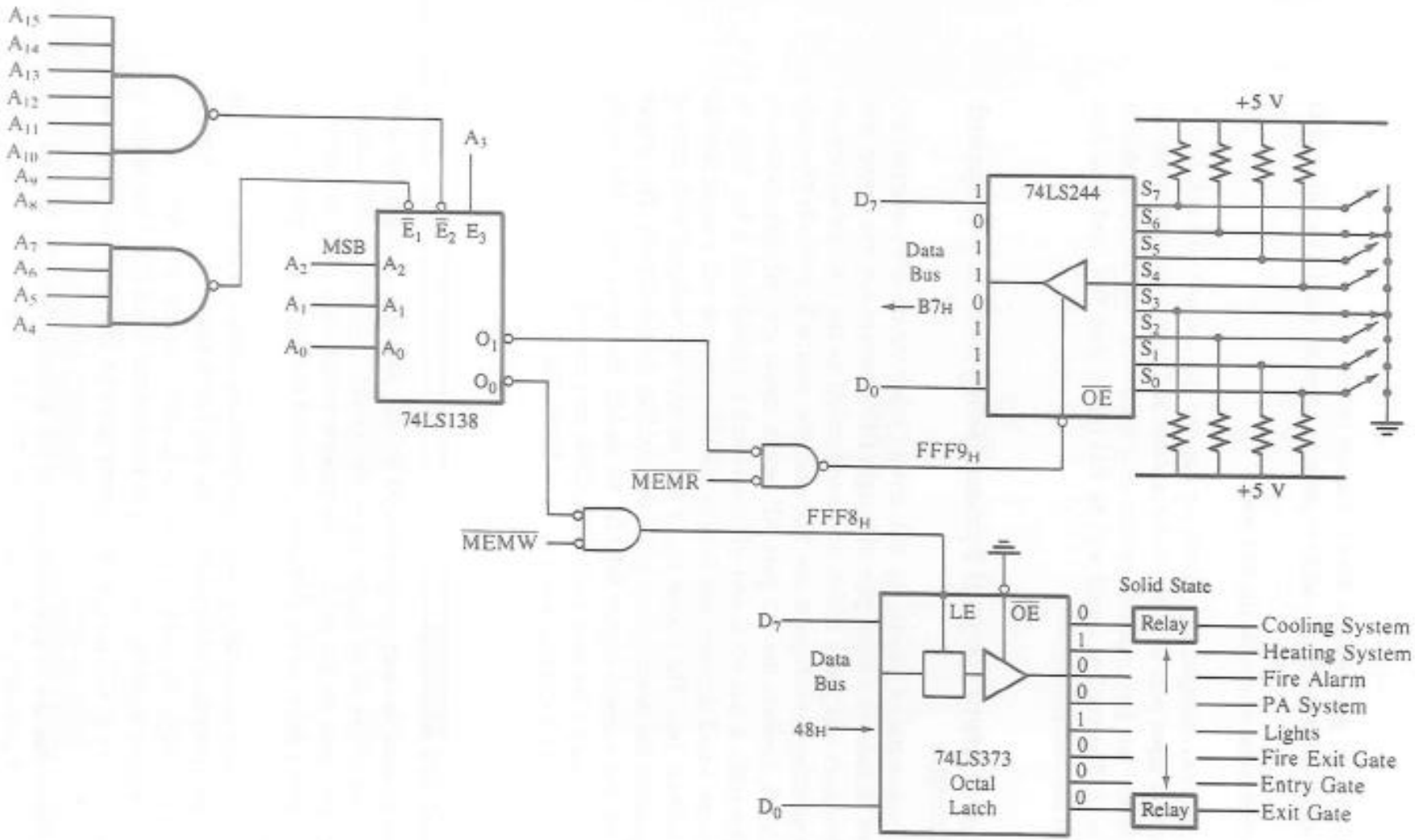
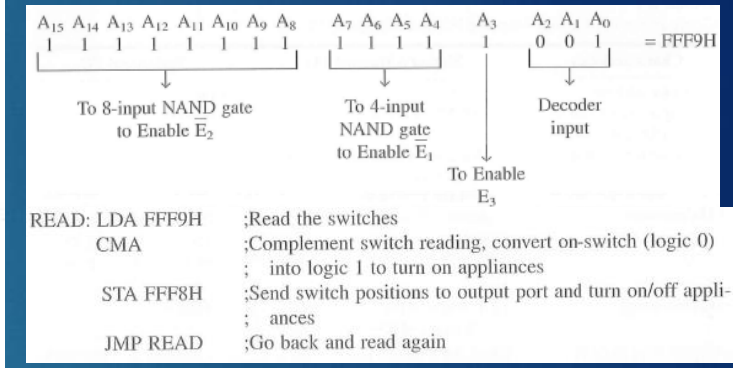
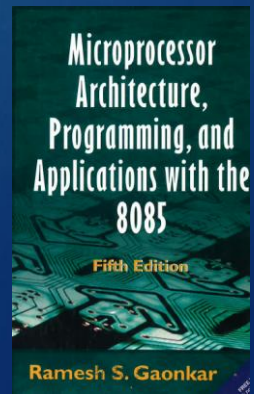


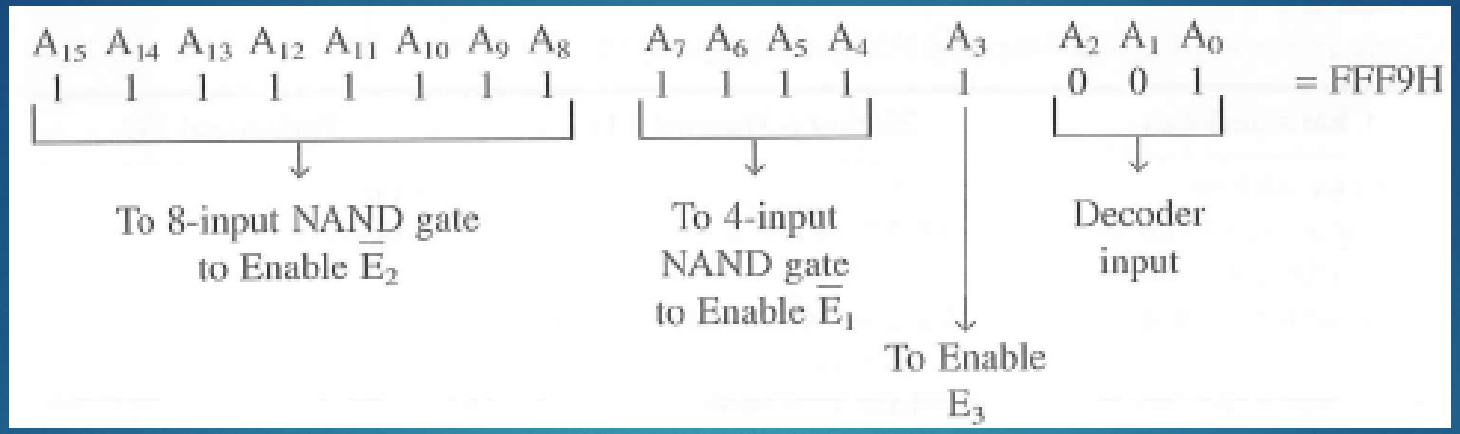
FIGURE 5.13
Memory-Mapped I/O Interfacing




```
READ: LDA FFF9H    ;Read the switches
      CMA          ;Complement switch reading, convert on-switch (logic 0)
                   ;  into logic 1 to turn on appliances
      STA FFF8H    ;Send switch positions to output port and turn on/off appli-
                   ;  ances
      JMP READ     ;Go back and read again
```



Control System Using Memory Mapped I/O




```
READ: LDA FFF9H     ;Read the switches
      CMA           ;Complement switch reading, convert on-switch (logic 0)
                    ;   into logic 1 to turn on appliances
      STA FFF8H     ;Send switch positions to output port and turn on/off appli-
                    ;   ances
      JMP READ      ;Go back and read again
```

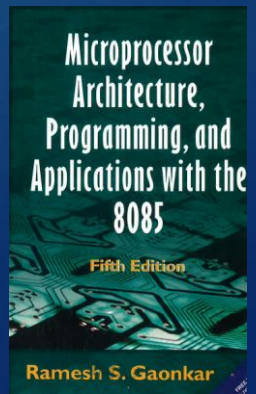


TABLE 5.1
Comparison of Memory-Mapped I/O and Peripheral I/O

Characteristics	Memory-Mapped I/O	Peripheral I/O
1. Device address	16-bit	8-bit
2. Control signals for Input/Output	$\overline{MEMR}$/$\overline{MEMW}$	$\overline{IOR}$/$\overline{IOW}$
3. Instructions available	Memory-related instructions such as STA; LDA; LDAX; STAX; MOV M,R: ADD M; SUB M; ANA M: etc.	IN and OUT
4. Data transfer	Between any register and I/O	Only between I/O and the accumulator
5. Maximum number of I/Os possible	The memory map (64K) is shared between I/Os and system memory	The I/O map is independent of the memory map; 256 input devices and 256 output devices can be connected
6. Execution speed	13 T-states (STA,LDA) 7 T-states (MOV M,R)	10 T-states
7. Hardware requirements	More hardware is needed to decode 16-bit address	Less hardware is needed to decode 8-bit address
8. Other features	Arithmetic or logical operations can be directly performed with I/O data	Not available