4 DIGIT SEVEN SEGMENT DISPLAY- SECOND AND SPLIT-SECOND COUNTER

FOR THE VERILOG CODES:

https://www.edaplayground.com/x/HSRP

FOR THE NEXYS3 FPGA BOARD CODES:

```
NET "clk" LOC="B8";
NET "reset_i" LOC="H13";
NET "start_i" LOC="E18";
NET "anodes_o<0>" LOC="F17";
NET "anodes_0<1>" LOC="H17";
NET "anodes_o<2>" LOC="C18";
NET "anodes_o<3>" LOC="F15";
NET "seven_seg_o<0>" LOC="L18";
NET "seven_seg_o<1>" LOC="F18";
NET "seven_seg_o<2>" LOC="D17";
NET "seven_seg_o<3>" LOC="D16";
NET "seven_seg_o<4>"_LOC="G14";
 NET "seven_seg_o<5>" LOC="J17";
NET "seven_seg_o<6>" LOC="H14";
```