CSE224 Term Project – Ozlem Yalciner (20210702080)

Testbench

```
// Code your testbench here
// or browse Examples
`timescale 1ns / 1ns

module tb;
parameter SIZE = 14, DEPTH = 2**14;

reg clk;
initial begin
  clk = 1;
  forever
  #5 clk = ~clk;
end

reg rst;
initial begin
  rst = 1;
  repeat (10) @(posedge clk);
  rst <= #1 0;
  repeat (300) @(posedge clk);
  $finish;
end

reg interrupt;
initial begin
  interrupt = 1'b0;
  repeat (56) @(negedge clk);
```

```
  interrupt <=#1 1;
  @ (posedge clk);
   interrupt <=#1 0;
end

wire wrEn;
wire [SIZE-1:0] addr_toRAM;
wire [31:0] data_toRAM, data_fromRAM;

VerySimpleCPU inst_VerySimpleCPU(
  .clk(clk),
  .rst(rst),
  .wrEn(wrEn),
.data_fromRAM(data_fromRAM),
  .addr_toRAM(addr_toRAM),
  .data_toRAM(data_toRAM),
  .interrupt (interrupt)

);

  blram #(SIZE, DEPTH) inst_blram(
  .clk(clk),
  .i_we(wrEn),
  .i_addr(addr_toRAM),
  .i_ram_data_in(data_toRAM),
  .o_ram_data_out(data_fromRAM)
);
initial begin
     $dumpfile("dump.vcd"); $dumpvars;
```

```
blram.memory[0] = 32'h900d0000;
blram.memory[1] = 32'hd0033;
blram.memory[2] = 32'h800d4034;
blram.memory[3] = 32'h600d4032;
blram.memory[4] = 32'hc00ec035;
blram.memory[5] = 32'h100d8001;
blram.memory[6] = 32'hd00dc000;
blram.memory[50] = 32'h3f;
blram.memory[51] = 32'h9;
blram.memory[52] = 32'h0;
blram.memory[53] = 32'h0;
blram.memory[54] = 32'h0;
blram.memory[55] = 32'h1;
blram.memory[56] = 32'h39;
blram.memory[57] = 32'h100d8001;
blram.memory[58] = 32'hd0100000;
blram.memory[59] = 32'h3c;
blram.memory[60] = 32'h100c8001;
blram.memory[61] = 32'h600d0032;
blram.memory[62] = 32'hc0100034;
blram.memory[63] = 32'hd00e0000;
blram.memory[64] = 32'h41;
   end
endmodule
```