Middle East Technical University - Department of Computer Engineering

CENG 232

Logic Design

Spring 2019-2020

Lab Assignment 2

Due date: Friday, March 16, 2020, 23:59

1 Introduction

This laboratory aims to get you familiar with some of the most important IC components like multiplexers and decoders. You will draw the circuit using Logisim tool with the given gates.

The logisim submission will be different from the demo circuit you will build in lab. It will contain an additonal output and related IC components to generate that output.

2 IC Pool

- 74LS08 (AND)
- 74LS32 (OR)
- 74LS04 (Inverter)
- 74LS02 (NOR)
- 74LS00 (NAND)
- 74LS153 (Multiplexer)
- 74LS86 (XOR)
- 74LS138 (Decoder)

3 Lab Work

Suppose we would like to implement a hypothetical 7-bit computer's controller part. The controller part receives 7-bit long instructions, decodes and executes them. Every 7-bit instruction consists of 3-bit opcode (operation code), 2-bit first operand, 2-bit second operand as shown below.

$$\text{Instruction: } 0010011 \rightarrow 001 - 00 - 11$$

$$\text{opcode: } 001, \text{first operand: } 00, \text{second operand: } 11$$

Since the opcode is 3-bit long, the computer can only process 8 (7 of them are subject of this assignment) different instructions which are OR, AND, NOR, XOR, Subtraction, Addition, Equality Check. Controller applies operation determined by opcode onto the first operand and second operand then sets the result to its output. Table below depicts the controller operations for given opcodes.

Instruction Set							
Opcode			First Operand		Second Operand		Output
3^{rd} bit	2^{nd} bit	1^{st} bit	2^{nd} bit	1^{st} bit	2^{nd} bit	1^{st} bit	
O2	O1	O0	A1	A0	B1	B0	
0	0	0	a1	a0	b1	b0	$A \vee B$
0	0	1	a1	a0	b1	b0	$A \wedge B$
0	1	0	a1	a0	b1	b0	$\neg(A \vee B)$
0	1	1	a1	a0	b1	b0	$A \oplus B$
1	0	0	a1	a0	b1	b0	$A - B$
1	0	1	a1	a0	b1	b0	$A + B$
1	1	0	a1	a0	b1	b0	$A == B$

$\oplus$: XOR, $\vee$: OR, $\wedge$: AND, $\neg$: NOT, $+$: Addition, - : Subtraction : $==$: Equality Check

a1,a0,b1,b0 $\in \{0, 1\}$

Opcode = 03O2O1, First Operand = A = A1A0, Second Operand = B = B1B0

3.1 Output

Output of controller consists of 1 pin indicating the sign of the result and 8 pins each of which represents a numerical value between 0 and 7. Operands of the controller (A and B) are unsigned 2-bit integers. All operations except Subtraction yields non-negative numerical values. Subtraction operation generates negative results whenever B > A. When controller issues an operation and yields a result, the pin that corresponds to numerical value of the result is active. If results is a negative number the sign pin is active (1), otherwise inactive (0). Pin names and their numerical values are the following: L7 : 7, L6 : 6, L5 : 5, L4 : 4, L3 : 3, L2 : 2, L1 : 1, L0 : 0.
Here is an example of states of output pins for Subtraction operation (OPCODE = 100).

First Operand		Second Operand		Output								
A1	A0	B1	B0	S	L7	L6	L5	L4	L3	L2	L1	L0
0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	0	0	0	0	1	0
0	0	1	0	1	0	0	0	0	0	1	0	0
0	0	1	1	1	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	0	0	0	1
0	1	1	0	1	0	0	0	0	0	0	1	0
0	1	1	1	1	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	1	0	0
1	0	0	1	0	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	1	1	0	0	0	0	0	0	1	0
1	1	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	0	1

Here is another example, including Opcodes.

Opcode			First Operand		Second Operand		Output								
O2	O1	O0	A1	A0	B1	B0	S	L7	L6	L5	L4	L3	L2	L1	L0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0
1	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0
1	0	1	0	1	1	1	0	0	0	0	1	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0
1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	1
1	1	0	1	1	1	1	0	0	0	0	0	0	0	1	0

You are supposed to implement this controller as your second lab work. You need to use ”input pins” for instruction (3-bit opcode, 2-bit first operand, 2-bit second operand) and ”output pins” for the output of controller from the Toolbar at the top of Logisim. Set their labels correctly using the following names. **Please, only set ”label” property of the ”pin” objects, do not add a ”label” object onto the Logisim canvas.**

4 Logisim-Only Part

In your Logisim submission you are expected to implement all the functionality of this hypothetical computer. All 9 outputs must be implemented. **Due to hardware restrictions** Subtraction operation and S output are removed from your Lab work.

5 Input-Output Sharing Rule for Free and Demo Sessions

This assignment requires 7 inputs and 9 outputs for Logisim part. Since there are not sufficiently many inputs and outputs on CADET for each individual, for free and demo sessions we have had to reduce number of output pins. Only L3, L2, L1, L0 outputs will be used and grading will be done accordingly. All inputs usage is mandatory to test six operations so we ask you to share Opcode pins (3 pins) with your partners.

6 Free Session

There will be a *free session week* after your homework is announced. You will have 2 hours in your free session slot. During the free session, you will try to build your circuit on a breadboard by using IC components, and you will practice how to handle possible problems related to physical circuit.

7 Demo Session

There will be a 2-hour-long *demo session week* following the free session week. In the demo session:

- You will take a short quiz about the logic concepts that involve the coverage of this lab.
- You will reconstruct your circuit on your breadboard (without the Subtraction operation).
- You will show that the circuit drawn in Logisim works as specified (without the Subtraction operation).
- An example solution will be published before the first demo session.

8 Labelling Specifications

- You have to use **pins** for your inputs and outputs. Only set **label property** of the **pin** objects, do not add a **label object**.
- Your input pins should be labelled as O2, O1, O0, A1, A0, B1, B0.
- Your output pins should be labelled as S, L7, L6, L5, L4, L3, L2, L1, L0
- Label properties are case-sensitive. Note that all labels consist of an uppercase letter followed by a number. **Please be very careful on correct naming of labels.**
- If you need to feed any input with a constant value, you can use a constant gate. This gate is under CENG232 gates. We will only set values for O2, O1, O0, A1, A0, B1, B0.
- You will receive grade **penalty** unless labeling is done properly.

9 Deliverables

- Submit the circuit named e1234567.circ prepared in Logisim, which is your preliminary work, until the specified deadline. Do not forget to replace e1234567 with your 7-digit student ID.
- The evaluation of the submission will be a **black-box test**.
- In demo session, you will reconstruct and show that the circuit drawn in Logisim works. This part will be graded in lab.
- You should use CENG version of Logisim which is available on ODTUClass course page. Circuits designed with other Logisim versions, other tools or that are not named properly **will not be graded**!

10 What to Bring in the Lab

- Print-out of submitted file of the circuit.
- Chips and their data-sheets. www.alldatasheet.com
- Pencil, as you will have a quiz at the very beginning of the DEMO lab.

11 Cheating Policy

All the lab work should be individual and there is zero tolerance policy for cheating. See the course website for further information about cheating policy.

12 References

CENG Logisim Version.