Middle East Technical University | Department of Computer Engineering

CENG 232

Logic Design

Spring 2019-2020

Lab 1

Due date: 28 February 2020, Friday, 23:55
No late submissions

1 Introduction

This laboratory aims to get you familiar with basic logic gates and combinational circuit design. You will simplify the circuit that is explained below and draw the circuit using Logisim tool with the given gates.

2 IC Pool

- 74LS04 (Inverter)
- 74LS08 (AND)
- 74LS32 (OR)

3 Lab Work

In this assignment, you are expected to perform the operations described in the following section.

3.1 Specifications

Suppose A and B are 2-bit binary **input** numbers and X, Y and Z are 1-bit binary **output** numbers. A and B are represented with A_1, A_0, B_1 and B_0 bits respectively where A_1 and B_1 are the most significant bits and A_0 and B_0 are the least significant bits of the relevant number. Your circuit will take A and B as inputs and give the outputs X,Y and Z with the following instructions:

$$\mathbf{X} = \begin{cases} 1 & A + B > 2 \\ 0 & \text{otherwise} \end{cases}$$

$$\mathbf{Y} = \begin{cases} 1 & \text{A} \mod \text{B} = 1 \\ 0 & \text{otherwise} \end{cases}$$

$$\mathbf{Z} = \begin{cases} 1 & (\text{A} \ll \text{B}) > (\text{B} \ll \text{A}) \\ 0 & \text{otherwise} \end{cases}$$

You have to use "input pins" and "output pins" for your inputs and outputs, respectively, from the Toolbar at the top of Logisim. Set their labels correctly using the following names. **Please, only set "label" property of the "pin" objects, do not add a "label" object onto the Logisim canvas.**

Input pins: A1, A0, B1, B0.
Output pins: X, Y, Z.

Each pin corresponds to a digit in a 2-bit binary number. If it is set, then the value of the digit is 1 if reset, then the value of the digit is 0.
Note that $A \mod B$ is not undefined when B is 0, because modulation is not division. You are trying to find out what remains.The result will simply be A when B is 0.

3.2 Input Output Examples

1. Suppose $A_1A_0 = 00$ and $B_1B_0 = 10$. In this case, A=0 and B=2 in decimal.
   $A + B = 2$
   Since $A + B > 2$ does not hold, the output X is 0.

2. Suppose $A_1A_0 = 10$ and $B_1B_0 = 01$. In this case, A=2 and B=1 in decimal.
   $A + B = 3$
   Since $A + B > 2$ holds, the output X is 1.

3. Suppose $A_1A_0 = 01$ and $B_1B_0 = 01$. In this case, A=1 and B=1 in decimal.
   $A \mod B = 0$
   Since $A \mod B = 0$, the output Y is 0.

4. Suppose $A_1A_0 = 01$ and $B_1B_0 = 10$. In this case, A=1 and B=2 in decimal.
   $A \mod B = 1$
   Since $A \mod B = 1$, the output Y is 1.

5. Suppose $A_1A_0 = 01$ and $B_1B_0 = 10$. In this case, A=1 and B=2 in decimal.
   $A \ll B = 4$ and $B \ll A = 4$
   Since $(A \ll B) == (B \ll A)$, the output Z is 0.

6. Suppose $A_1A_0 = 01$ and $B_1B_0 = 11$. In this case, A=1 and B=3 in decimal.
   $A \ll B = 8$ and $B \ll A = 6$
   Since $(A \ll B) > (B \ll A)$, the output Z is 1.

4 Free Session

There will be a "free session week" starting from February 25 till February 28 (Your specific session will be announced later). You will have 2 hours in your free session slot. During the free session, you will try to build your circuit on a breadboard by using IC components, and you will practice how to handle possible problems related to physical circuit.

5 Demo Session

There will be a 2-hour-long "demo session week" following the free session week. In demo session:

- You will take a short quiz about the logic concepts that involve the coverage of this lab.

- You will reconstruct your circuit on your breadboard.
- You will show that the circuit drawn in Logisim works as specified.

6 Deliverables

1. Submit the circuit named `e1234567.circ` prepared in Logisim, which is your preliminary work, until the specified deadline. Do not forget to replace `e1234567` with your 7-digit student ID. The evaluation of the submission will be a black-box test. **You should use CENG version of Logisim which is available on ODTUClass course page. Circuits designed with other Logisim versions, other tools or not named properly will not be graded!**
2. In demo session, you will reconstruct and show that the circuit drawn in Logisim works. This part will be graded in lab. Please note that submission of a working circuit is a must to attend DEMO lab sessions.

7 What to Bring in the Lab

- Print-out submitted file of the circuit.
- Lab materials and data-sheets of chips. www.alldatasheet.com
- Pencil and eraser, as you will have a quiz at the very beginning of the DEMO lab.

8 Cheating Policy

All the lab work should be **individual** and there is zero tolerance policy for cheating. See the course website for further information about cheating policy.

9 References

CENG Logism Version.