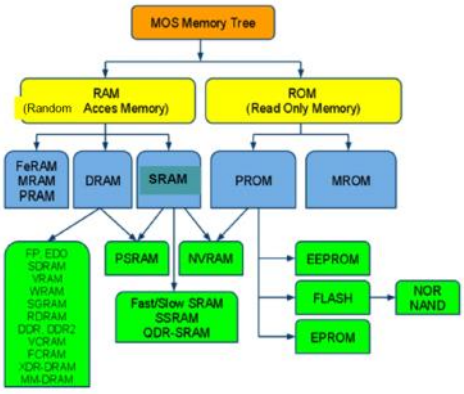
Semiconductor Memories

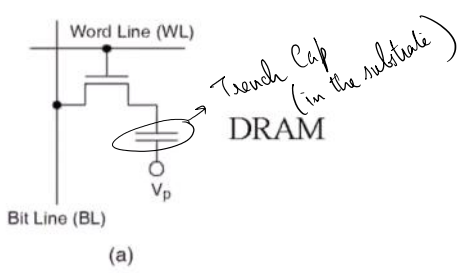
Monday, November 22, 2021 3:41 PM

Overview of Semiconductor memory types

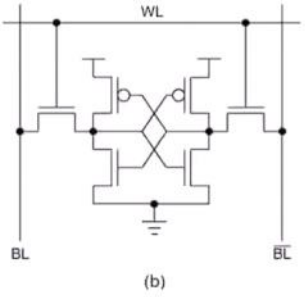


MOS = Metal Oxide Semiconductor
RAM = Random Access Memory
DRAM = Dynamic Random Access Memory
SDRAM = Synchronized Dynamic Random Access Memory
FERAM = Ferroelectric Random Access Memory
MRAM = Magneto-resistive Random Access Memory
PRAM = Phase-change Random Access Memory
VRAM = Video Random Access Memory
WRAM = Window Random Access Memory
SGRAM = Synchronous Graphics Random Access Memory
RDRAM = Rambus Random Access Memory
DDR = Double Data Rate
DDR2 = Double Data Rate 2 (second generation)
VCRAM = Virtual Channel Random Access Memory
FCRAM = Fast Cycle Random Access Memory
XDR-DRAM = Extreme Data Rate Random Access Memory
MM-RAM = Multi Media Random Access Memory
PSRAM = Pseudo-Static Random Access Memory
NV-RAM = Non-Volatile Random Access Memory
SSRAM = Static Synchronous Random Access Memory
QDR-DRAM = Quad Data Rate Dynamic Random Access Memory
ROM = Read Only Memory
PROM = Programmable Read Only Memory
MROM = Mask Read Only Memory
EPROM = Erasable Programmable Read Only Memory
EEPROM = Electrically Erasable Programmable Read Only Memory

Equivalent Circuits of Memory Cells

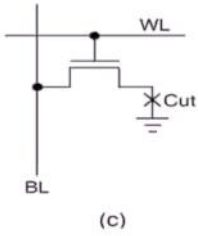


DRAM

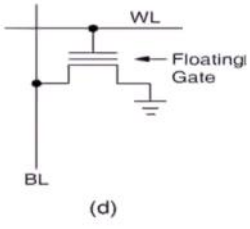


SRAM

SRAM, DRAM - info gone when removed power.

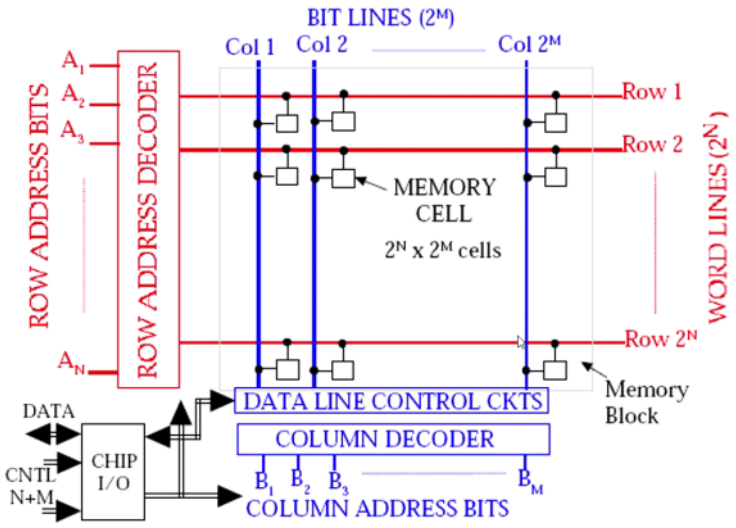


MASK (Fuse) ROM



EPROM (EEPROM)

Typical Random-Access Memory Array Organization



word lines are polysilicon that forms gates

Some Issues in Determining the Memory Array Organization

- Typically we want an aspect ratio that is nearly one
- How to divide up the row, column address decoding?
  - Consider an 8K x 32 SRAM = 256 Kb = 2^{18} with $2^{18} = 2^9$ rows x 2^9 columns as an example
    - Row decoder is 9 to 512 decoder. Every 32 (2^5) columns is a 'word', and we only need to decode words. So, column decoder needs to decode 16 words, that is, we only need a 4 to 16 column decoder
  - Assertion of word line accesses all cells in a row
    - Not all bits that are read from a row may be used
    - Loading on word line is high!
  - Bit lines connect all cells in a column, only one cell in a column can ever be ON at a time
    - Would like to keep the bitline swing low to preserve power
  - Critical path typically runs through row decode and word line assertion
    - Use hierarchical decoding to break a large array into smaller arrays

↳ Row decoder is complex than Column
↳ Sequence of events: first activate word lines then Bit lines
↳ Rows are Polysilicon that form gates

8K x 32 SRAM = 256 kb

$2^8 \cdot 2^{10}$ bit

2^{18}

2^9 Rows, 2^9 Colum

Aspect Ratio = 1

Row decoder 9 to 512 decoder

Column → 32 SRAM → 2^9 columns

2^9

2^4 words, 2^5

2^5 words