International Test Conference (India)

Building on the Test EcoSystem to enable and support electronics growth in ASIA

July 10-12, 2017, Bangalore, India

Call for papers

International Test Conference is the world's premier venue dedicated to the electronic test of devices, boards and systems—covering the complete cycle from design verification, design-for-test, design-for-manufacturing, silicon debug, manufacturing test, system test, diagnosis, reliability and failure analysis, and back to process and design improvement. At ITC, design, test, and yield professionals can confront challenges faced by the industry, and learn how these challenges are being addressed by the combined efforts of academia, design tool and equipment suppliers, designers, and test engineers. This ITC conference will be focusing on Test technology development in Asia and India but the submissions may not be limited to topics related to this region. Topics related to DFT and test development across multi geographical regions will be of special interest.

This conference is being held in India under the International Test conference banner to invite researchers, industry teams to present their development work which has a focus on ASIA. This includes design teams which have multiple national presences and are developing designs and products across multiple sites across the world.

Authors are invited to submit original, unpublished papers describing recent work in the field of test and design. In addition, authors are invited to submit high quality, practical, industry best practices. Submissions simultaneously under review or accepted by another conference, symposium or journal, will be summarily rejected.

Submissions must include:

- Title of paper.
- Name, affiliation, e-mail address of each author.
- The corresponding author(s). ITC will communicate with the corresponding author(s).
- One or two topic(s) from the topic list, or a description of your topic.
- An electronic copy of a complete paper up **to 10 pages**, or an extended summary up to 6 pages. **Submissions less than 4 pages are rarely accepted.**
- An abstract of 500 words or less to be entered online.

Paper submission deadline: Mar 31, 2017
Author notification: May 19, 2017
Final manuscript due: June 16, 2017

Authors are also invited to submit a single-page poster proposal. Posters are a useful way of presenting late-breaking results, getting feedback on an innovative method, or participating without having to write a full paper. Acceptance as a poster does not preclude submission of a more complete work as an ITC paper in 2017. Poster proposal abstracts should be no longer than a single page.

Poster submission deadline: April 21, 2017
Author notification: June 2, 2017
Final manuscript due: June 16, 2017

For detailed information about the submission process, requirements and deadlines, the selection process and any other questions regarding the program itself or contact information, please consult the ITC web site at http://www.itctestweekindia.org or email the program chair navin.bishnoi@globalfoundries.com

ITC India invites submissions on the latest advances in test, validation and diagnosis of ICs, boards and systems

Topics of interest include (not limited to):

3D/2.5D Test
Adaptive Test in Practice
ATE/Probe Card Design
Advances in Boundary Scan
Bring Up
Data Driven Methods
Data Exchange and Infrastructure
Defect-Oriented Testing
DFM and Test Diagnosis
Economics of Test
End-to-End Data Analysis
Embedded BIST & DFT
Emerging Defect Mechanisms
Hardware Security and Trust
IoT Testing
Jitter, High-Speed I/O and RF Test
Known-Good-Die testing
Memory Test and Repair
MEMS Testing
Mixed-Signal and Analog Test
New Technologies and Test
On-Chip Test Compression
Online Test
Pre- and Post- Silicon Validation
Power Issues in Test
Protocol-aware Test
Reliability and Resilience
Scan Based Test
SoC/SiP/NoC Test
Silicon Debug
Simulation and Test
System Test (Applications)
System Test (Hardware/Software)
Test-to-Design Feedback
Test Escape Analysis
Test Flow Optimizations
Test Generation and Validation
Test Resource Partitioning
Test Standards
Test Time Analysis and Reduction
Testing High Speed Optics/Photonics
Timing Test
Yield Analysis and Optimization