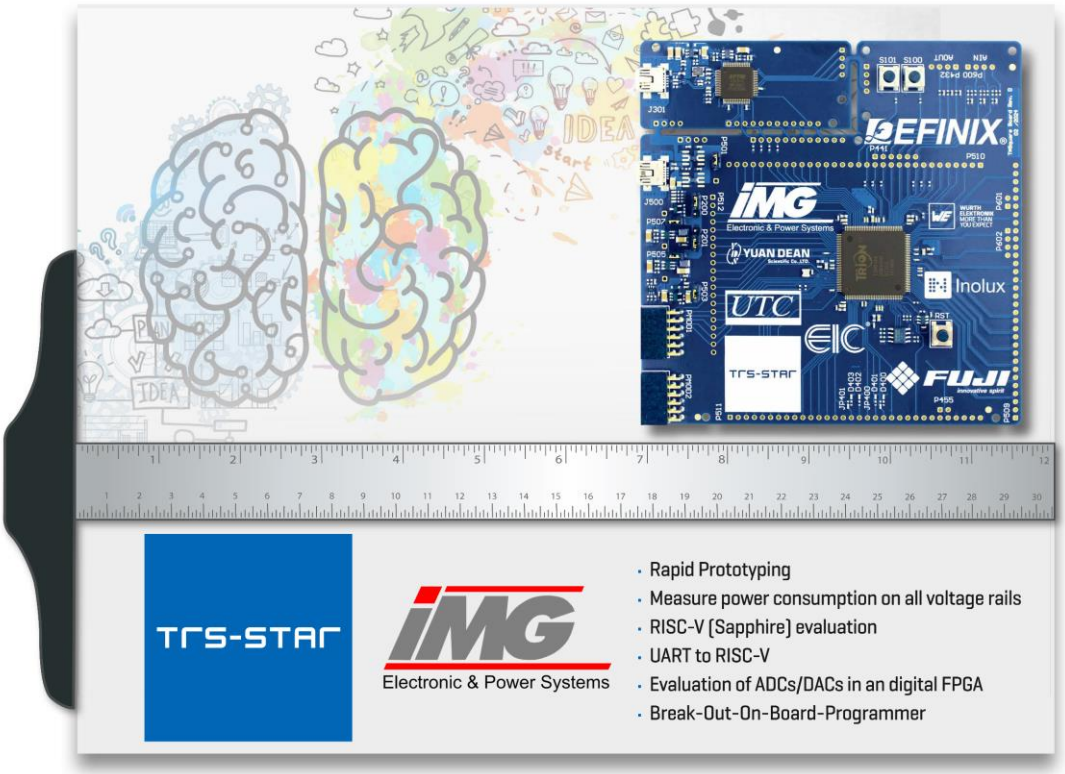
T*Square T20 Education Board

Getting started

Be creative with T*Square Boards



Getting started		created:	MG	date:	2024-04-22
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		approved:		date:	
File name:	TSquare-Board_Dokumentation				
IMG Electronic & Power Systems GmbH		Version:	1.4	page 1 of 30	

1. Overview

The T*Square T20 Education board is a flexible and universally applicable board for evaluating your own FPGA designs with the Trion family from the manufacturer Efinix Inc. The modules are equipped with either the Trion T20Q100 (with internal SPI flash memory for configuration bitstreams, non-volatile user data and RISC-V application code) or with the Trion T20Q144 plus 16 Mbit external SPI-flash. The board is supplied with power via one of the two USB sockets. To carry out current and voltage measurements, additional jumpers and probe test points are provided on the board, which enable the supply paths to be interrupted or the current to be measured using a multimeter for instance. This makes it easy to determine the power consumption. Furthermore, a FTDI4232 is available as a programming interface, which means that the customer is not obliged to purchase an additional programmer. Nevertheless, the integrated programmer can also be separated and used as a “stand-alone”, for example to program other boards, provide a UART or to operate GPIOs. The individual functional blocks are shown in the block diagram below:

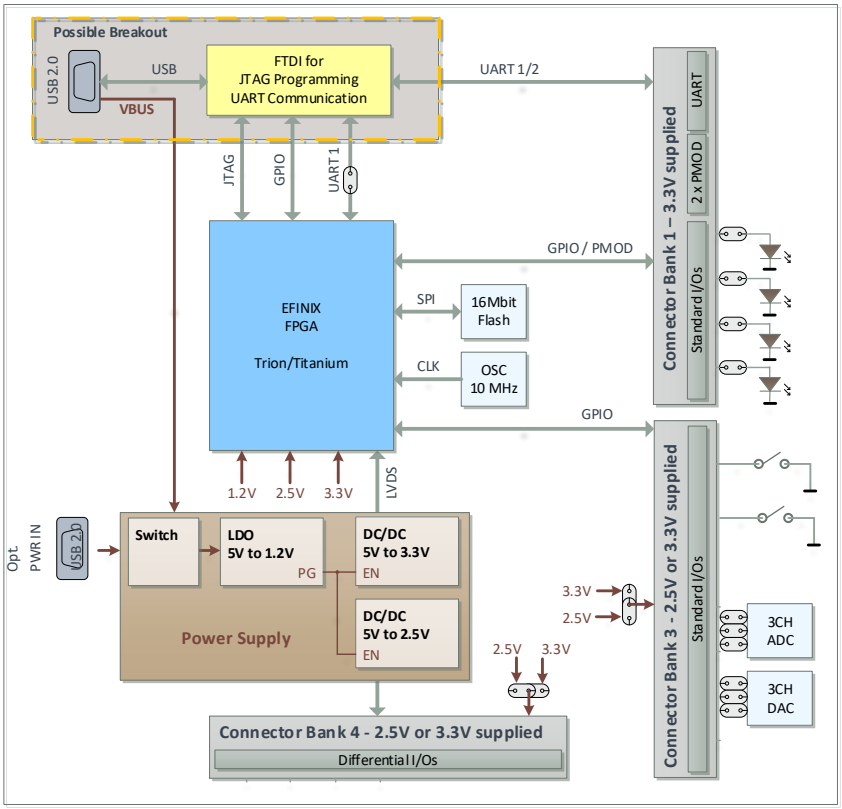

Figure 1: Overview

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2. What's in the box

- T*Square board 120mm x 120mm
- USB cable, length 100 cm
- Pin headers for self-assembly
- Socket headers for self-assembly
- ESD packaging
- 2.56mm Jumpers

3. Downloads

Free Efinity® software is available to operate the board. The Efinity® software provides a complete tool flow from RTL design to bitstream generation, including synthesis, place-and-route, and timing analysis. All other required data is also available as a download.

- Schematics and layouts:
  - T20-100 Education Board: https://shorturl.at/pwBTV
  - T20-144 Education Board: https://shorturl.at/bghvT
- Example project: tbd.
- Tools: https://www.trs-star.com/en/efinity-software
- Useful links:
  - EFINIX: https://www.efinixinc.com
  - FTDI: https://ftdichip.com/products/ft4232hq
  - IMG: https://shorturl.at/hijx6
  - TRS-STAR: https://shorturl.at/cBMQ3

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4. Hardware

The figure below shows the most important connections and controls such as LEDs, buttons, jumpers and pin headers. For detailed information about the individual functions, please regard the schematic documents available at the listed download links and also table 1 listing the pins and jumpers.

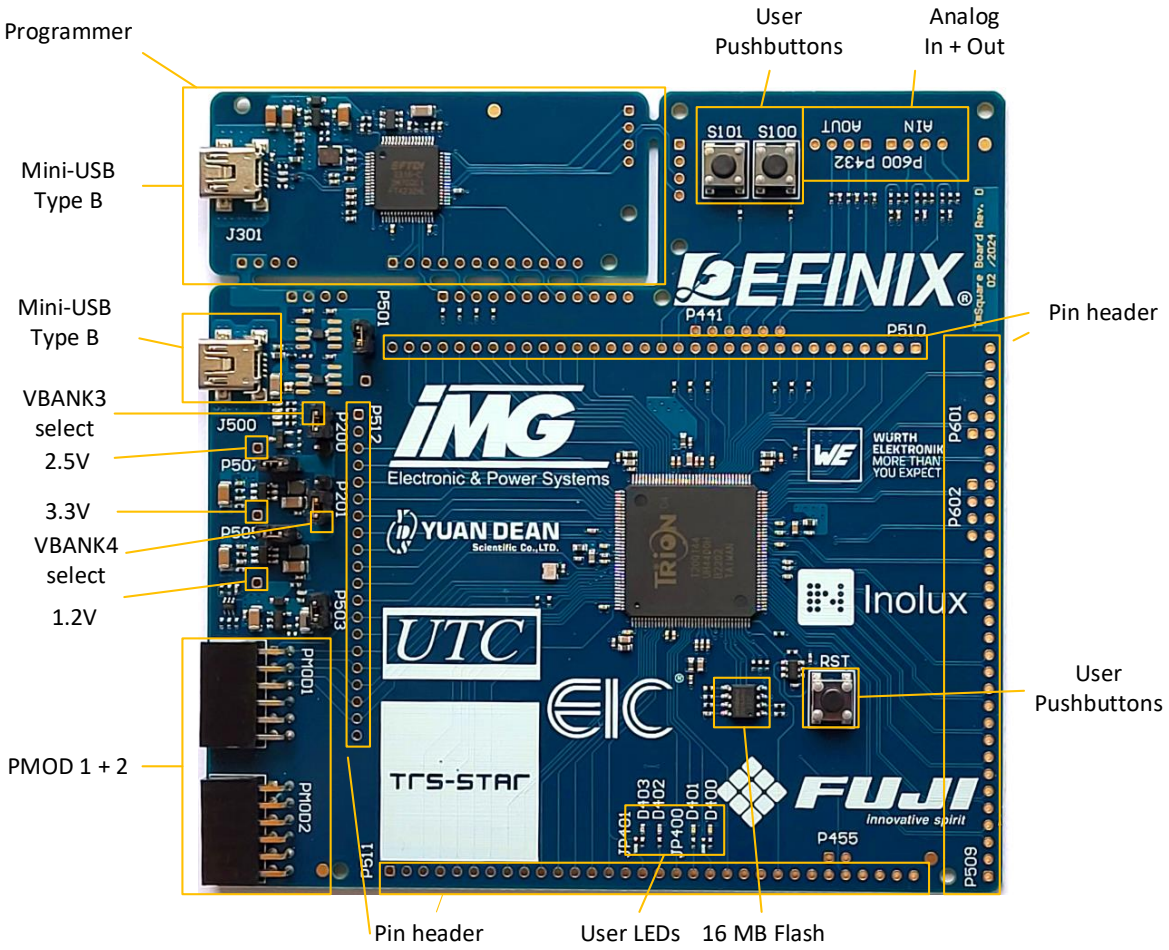

Figure 2: connections and jumpers

Table 1 below shows the user connections and jumpers with their respective functions. For more detailed information, please consult the schematics documents listed under “Downloads”.

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Designator	Description
J301	USB port
J500	USB port for power supply, OR'ed with J301 USB power
JP400	Selects the driving pin for LED400
JP401	Selects the driving pin for LED401
P200	Supply voltage selection for Bank 3: 2.5V / 3.3V
P201	Supply voltage selection for Bank 4: 2.5V / 3.3V
P432	3x Analog out 0 … 3.3V
P441	connects the GPIOR 133…149 to the analogue interface
P455	UART
P501	Current tap for 5.0V supply
P503	Current tap for 1.2V supply
P505	Current tap for 3.3V supply
P507	Current tap for 2.5V supply
P509	Pin header bank 4
P510	Pin header bank 3
P511	Pin header bank 1
P512	Pin header bank 3
P600	3x Analog in 0 … 3.3V
P601	connects the GPIOB to the analogue interface
P602	connects the GPIOB to the analogue interface

Table 1: Pins and jumpers

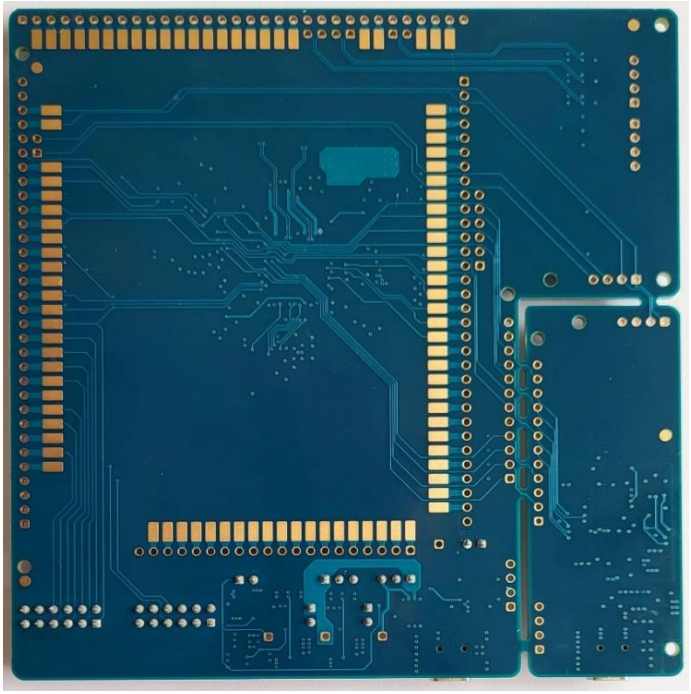

Figure 3: Additional wires and connections can be soldered on the bottom side.

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5. Separation of the programming board

The programming board is designed in such way that it optionally can be separated from the FPGA board. It can now be used as a “stand alone” programming board to program other boards with it. To do this, the two outermost break away tabs should be carefully separated using a light-duty flush cutting wire cutter.

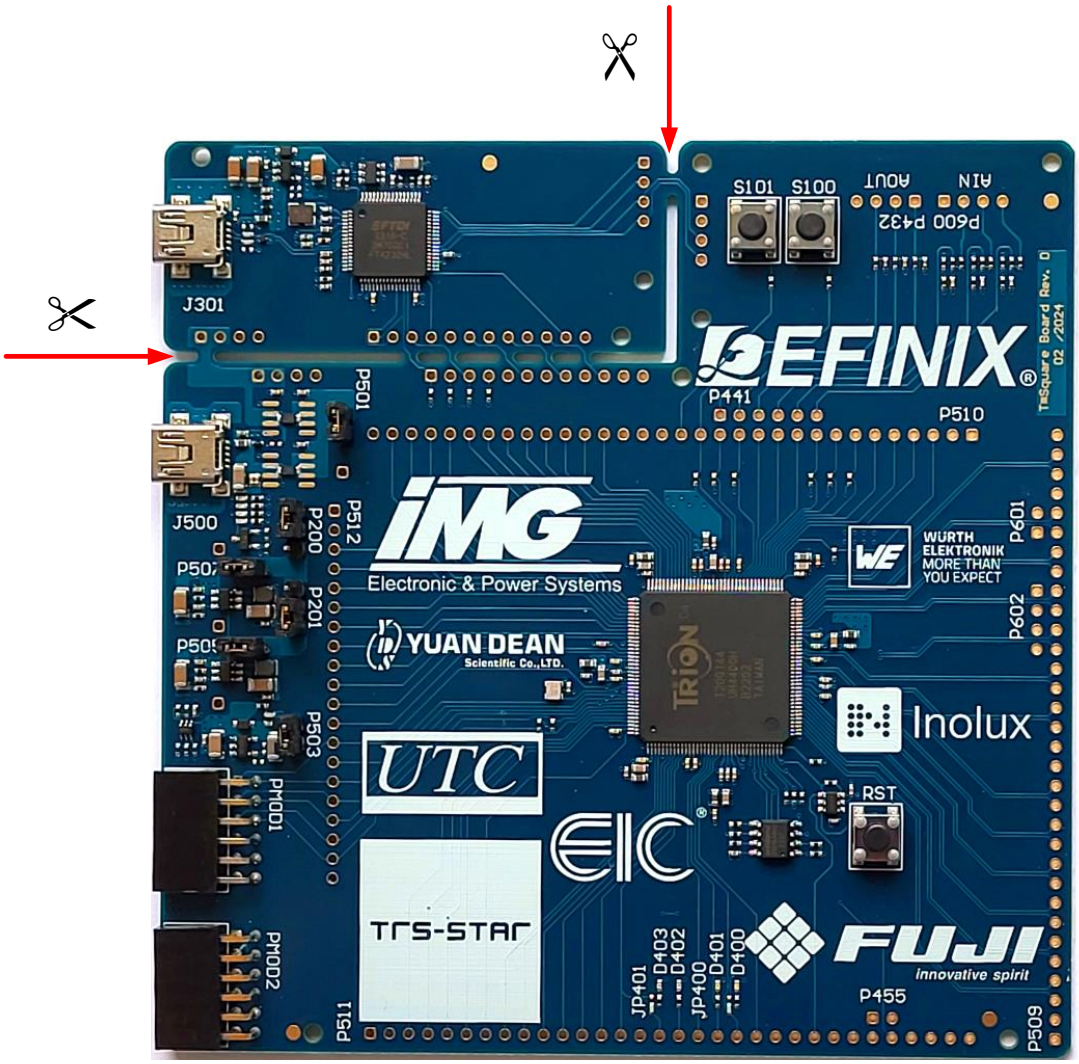

Figure 4: breakout board's cutting scheme

Now the small board can be broken out. If small burrs or frays are visible in the copper after breaking it off, these can be straightened with fine sandpaper to avoid short circuits or cuts. Using the pin and socket headers (not included), the programmer can be plugged back into the FPGA board if necessary. For this purpose, the plugs and sockets must be soldered accordingly by the customer.

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6. Software

6.1 Efinity® software

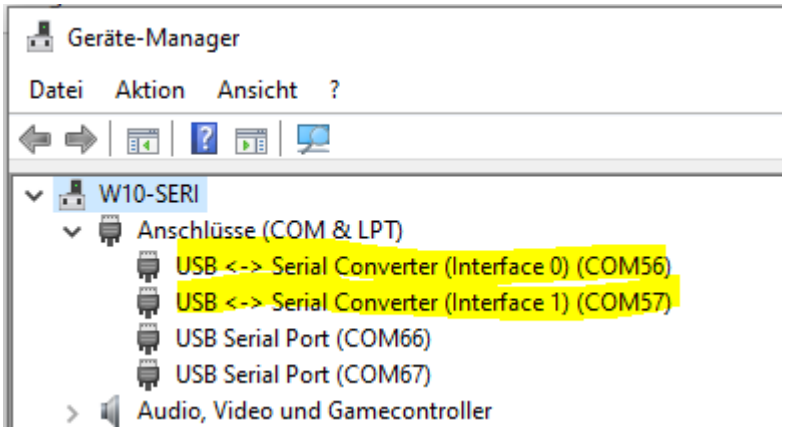
The Efinity® software provides a complete RTL-to-bitstream flow. With a simple, easy to use GUI interface and command-line scripting support, the software provides the tools you need to build designs for Titanium and Trion® FPGAs. The software runs on the Windows, Ubuntu, and CentOS/Red Hat Enterprise operating systems.

For a detailed description of the installation process of the Efinity® software please refer to the Efinity Software Installation User Guide.

6.2 T*Square T20 Education board specific settings (Microsoft Windows)

Please follow the steps 1 to 7 to install the driver:

1. Connect the T*Square T20 Education board with the included usb cable with your computer. The board will be powered up immediately.
2. Open the **Device Manager** and verfiy that the **USB <-> Serial Converter (Interface 0** and **1)** are present



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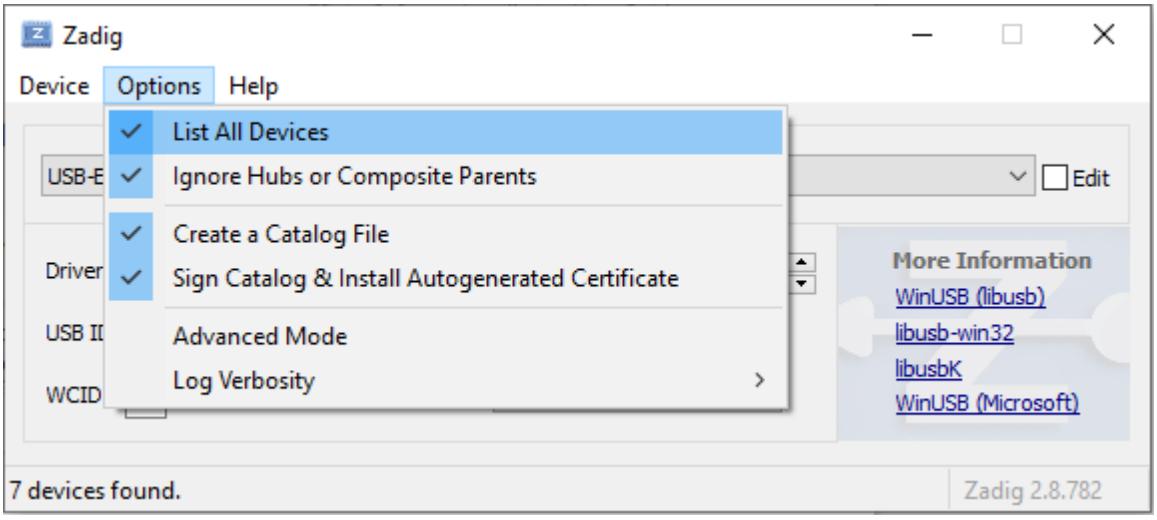
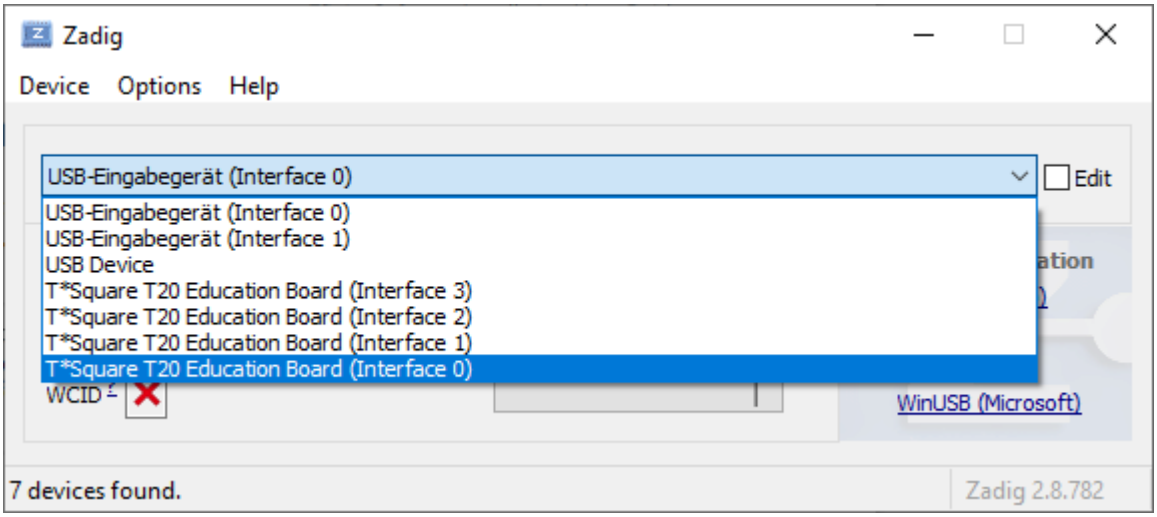
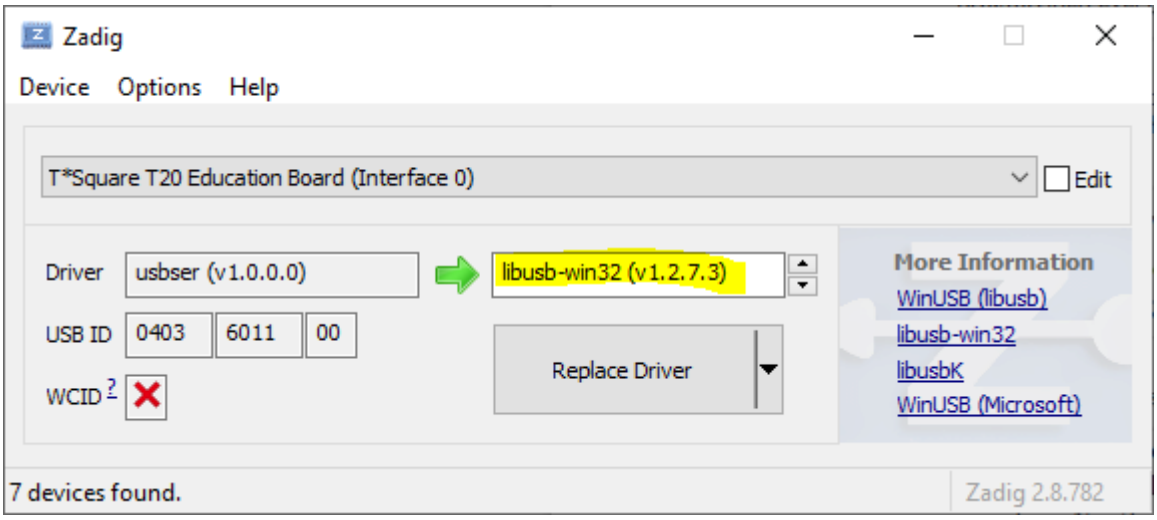
3. Open the Zadig software and select **Options -> List All Devices**



4. Now you can select the entry **T*Square T20 Education Board (Interface 0)**



5. Please choose the libusb-win32 driver and push the **Replace Driver** button



6. Repeate step 4 and 5 with **T*Square T20 Education Board (Interface 1)** selected and then close the Zadig software.

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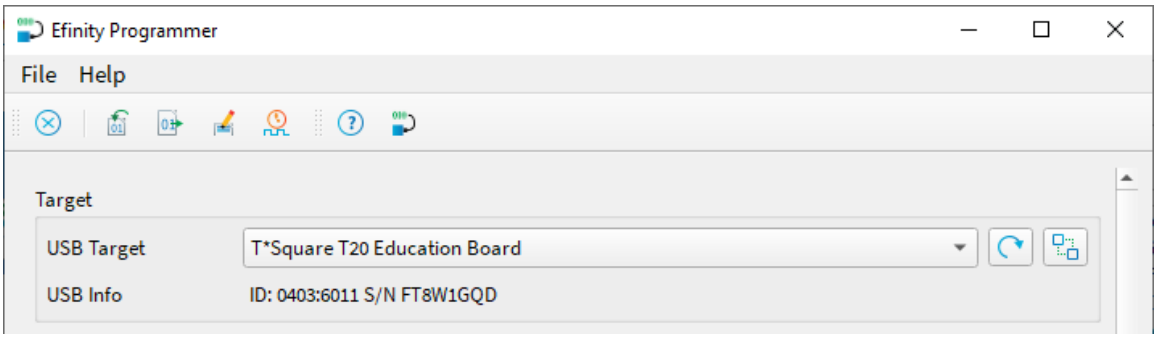
7. After powercycling the board (unplug and replug the usb cable) you can program the FPGA with the onboard programmer.



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7. Pin headers

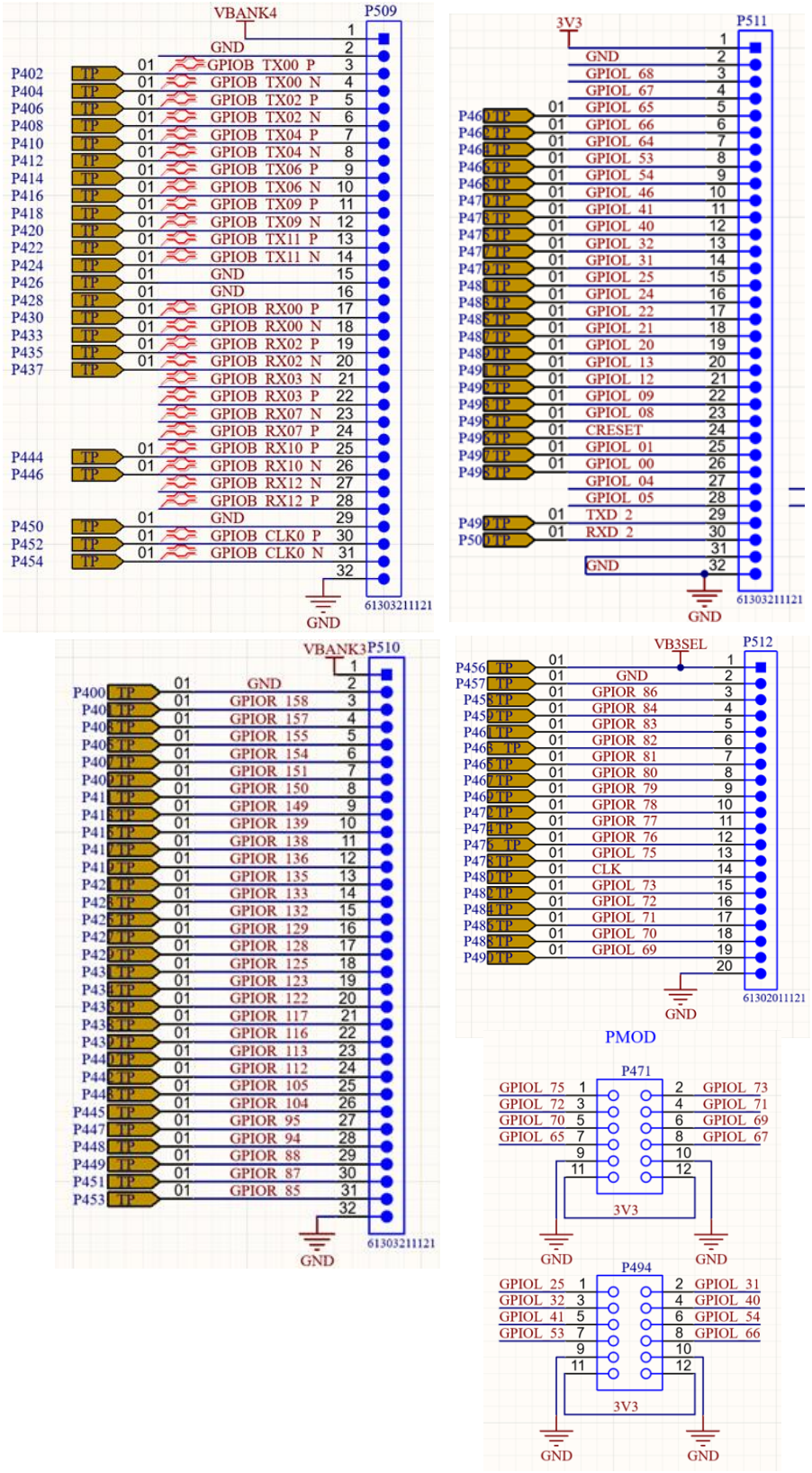

Figure 5: Pin headers

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7.1 T20Q144

7.1.1 P509

Table 2: pin header P509 – T20Q144

PIN Number	T20Q144 PIN	Signal	alternative use	Bank
1		VBANK4		4B
2		GND		
3	38	GPIOB_TX00_P		4B
4	39	GPIOB_TX00_N		4B
5	40	GPIOB_TX02_P		4B
6	41	GPIOB_TX02_N		4B
7	42	GPIOB_TX04_P		4B
8	43	GPIOB_TX04_N		4B
9	45	GPIOB_TX06_P		4B
10	46	GPIOB_TX06_N		4B
11	47	GPIOB_TX09_P		4B
12	48	GPIOB_TX09_N		4B
13	53	GPIOB_TX11_P		4B
14	54	GPIOB_TX11_N		4B
15		GND		
16		GND		
17	55	GPIOB_RX00_P		4A
18	56	GPIOB_RX00_N		4A
19	58	GPIOB_RX02_P		4A
20	59	GPIOB_RX02_N		4A
21	60	GPIOB_RX03_N	AIN3_N	4A
22	61	GPIOB_RX03_P	AIN3_P	4A
23	65	GPIOB_RX07_N	AIN2_N	4A
24	66	GPIOB_RX07_P	AIN2_P	4A
25	67	GPIOB_RX10_P		4A
26	68	GPIOB_RX10_N		4A
27	69	GPIOB_RX12_N	AIN1_N	4A
28	70	GPIOB_RX12_P	AIN1_P	4A
29		GND		
30	71	GPIOB_CLK0_P		4A
31	72	GPIOB_CLK0_N		4A
32		GND		

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7.1.2 P510

Table 3: pin header P510 – T20Q144

PIN Number	T20Q144 PIN	Signal	alternative use	Bank
1		VBANK3		
2		GND		
3	74	GPIOR_158		3E
4	75	GPIOR_157		3E
5	76	GPIOR_155		3E
6	77	GPIOR_154		3E
7	78	GPIOR_151		3E
8	79	GPIOR_150		3E
9	80	GPIOR_149	AIN1 1Bit DACout	3E
10	81	GPIOR_139	AIN2 1Bit DACout	3D
11	82	GPIOR_138	AIN3 1Bit DACout	3D
12	83	GPIOR_136	AOUT1	3D
13	84	GPIOR_135	AOUT2	3D
14	86	GPIOR_133	AOUT3	3D
15	87	GPIOR_132	Push Button S100	3D
16	89	GPIOR_129	Push Button S101	3D
17	90	GPIOR_128		3D
18	92	GPIOR_125		3D
19	93	GPIOR_123		3C
20	97	GPIOR_122		3C
21	98	GPIOR_117		3C
22	99	GPIOR_116		3C
23	100	GPIOR_113		3C
24	101	GPIOR_112		3C
25	95	GPIOR_105		3B
26	103	GPIOR_104		3B
27	105	GPIOR_95		3B
28	106	GPIOR_94		3B
29	109	GPIOR_88		3A
30	110	GPIOR_87		3A
31	111	GPIOR_85		3A
32		GND		

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7.1.3 P511

Table 4: pin header P511 - T20Q144

PIN Number	T20Q144 PIN	Signal	alternative use	Bank
1		3V3		
2		GND		
3	139	GPIOL_68		
4	140	GPIOL_67	PMOD1 P8	1E
5	141	GPIOL_65	PMOD1 P7	1E
6	142	GPIOL_66	PMOD2 P8	1E
7	144	GPIOL_64		1E
8	3	GPIOL_53	PMOD2 P7	1D
9	4	GPIOL_54	PMOD2 P6	1D
10	6	GPIOL_46		1D
11	7	GPIOL_41	PMOD2 P5	1C
12	8	GPIOL_40	PMOD2 P4	1C
13	10	GPIOL_32	PMOD2 P3	1C
14	11	GPIOL_31	PMOD2 P2	1C
15	14	GPIOL_25	PMOD2 P1	1B
16	15	GPIOL_24		1B
17	16	GPIOL_22		1B
18	17	GPIOL_21		1B
19	18	GPIOL_20		1B
20	19	GPIOL_13		1B
21	20	GPIOL_12		1B
22	28	GPIOL_09		1A
23	29	GPIOL_08		1A
24	35	CRESET		1A
25	30	GPIOL_01		1A
26	31	GPIOL_00		1A
27	32	GPIOL_04	TXD_1	1A
28	33	GPIOL_05	RXD_1	1A
29	FTDI Port D	TXD_2		
30	FTDI Port D	RXD_2		
31		GND		
32		GND		

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7.1.4 P512

Table 5: pin header P512 - T20Q144

PIN Number	T20Q144 PIN	Signal	alternative use	Bank
1		VB3SEL		
2		GND		
3	112	GPIOR_86		3A
4	113	GPIOR_84		3A
5	114	GPIOR_83		3A
6	115	GPIOR_82		3A
7	116	GPIOR_81		3A
8	117	GPIOR_80		3A
9	118	GPIOR_79		3A
10	119	GPIOR_78		3A
11	123	GPIOR_77		3A
12	124	GPIOR_76		3A
13	131	GPIOL_75	PMOD1 P1	1E
14	132	CLK		1E
15	134	GPIOL_73	PMOD1 P2	1E
16	135	GPIOL_72	PMOD1 P3	1E
17	136	GPIOL_71	PMOD1 P4	1E
18	137	GPIOL_70	PMOD1 P5	1E
19	138	GPIOL_69	PMOD1 P6	1E
20		GND		

7.1.5 PMOD1 and PMOD2

Note: PMOD modules have to be connect up-side-down. This means that the topside has to face the ground.

Table 6: pin header PMOD1 - T20Q144

PIN Number	T20Q144 PIN	Signal	alternative use	Bank
1	131	GPIOL_75	P512-P13	1E
2	134	GPIOL_73	P512-P15	1E
3	135	GPIOL_72	P512-P16	1E
4	136	GPIOL_71	P512-P17	1E
5	137	GPIOL_70	P512-P18	1E
6	138	GPIOL_69	P512-P19	1E
7	141	GPIOL_65	P511-P05	1E
8	140	GPIOL_67	P511-P04	1E
9		GND		

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10		GND		
11		3V3		
12		3V3		

Table 7: pin header PMOD2 - T20Q144

PIN Number	T20Q144 PIN	Signal	alternative use	Bank
1	14	GPIOL_25	P511-P15	1B
2	11	GPIOL_31	P511-P14	1C
3	10	GPIOL_32	P511-P13	1C
4	8	GPIOL_40	P511-P12	1C
5	7	GPIOL_41	P511-P11	1C
6	4	GPIOL_54	P511-P09	1D
7	3	GPIOL_53	P511-P08	1D
8	142	GPIOL_66	P511-P06	1E
9		GND		
10		GND		
11		3V3		
12		3V3		

7.1.6 Push buttons and user LEDs

Table 8: push buttons - T20Q144

SW Number	T20Q144 PIN	Signal	alternative use	Bank
S100	87	GPIOR_132	P510-P15	3D
S101	89	GPIOR_129	P510-P16	3D

Table 9: user LEDs - T20Q144

LED	T20Q144 PIN	Signal	alternative use	Bank
D400	19	GPIOL_13	P511-P20	1B
D401	18	GPIOL_20	P511-P19	1B
D402	16	GPIOL_22	P511-P17	1B
D403	15	GPIOL_24	P511-P16	1B

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7.1.7 UART

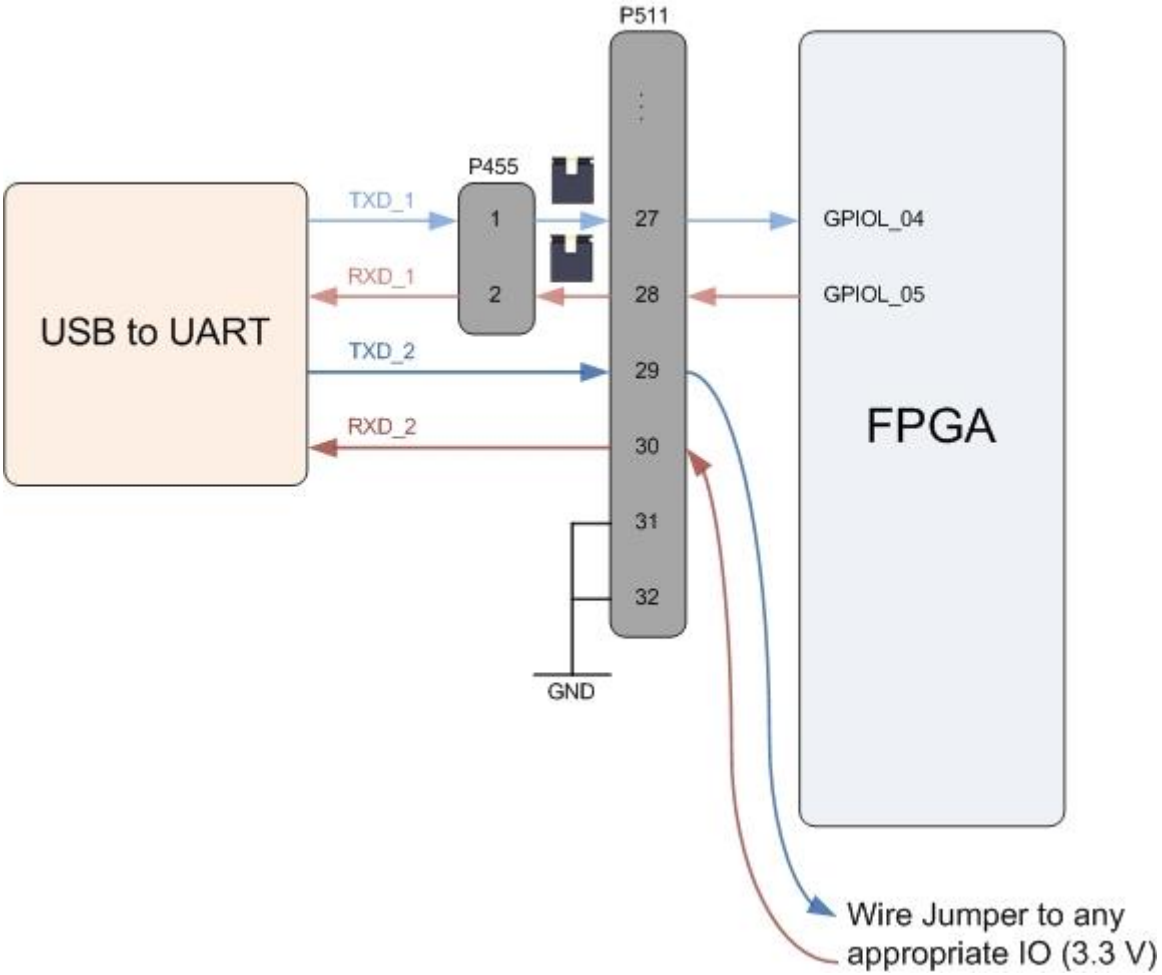

Figure 6: UART

Table 10: uart - T20Q144

Pin	T20Q144 PIN	Signal	alternative use	Bank
TXD_1	32	TXD_1	Connect P455-P1 with P511-P27 (GPIOL_04)	1A
RXD_1	33	RXD_1	Connect P455-P2 with P511-P28 (GPIOL_05)	1A
TXD_2		TXD_2		
RXD_2		RXD_2		

Note: Signal names are from the host point of view. For example, TXD_1 comes from the USB-UART bridge and goes to the FPGA, therefore it is an input signal for the FPGA (RXD_1).

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7.1.8 Analog out

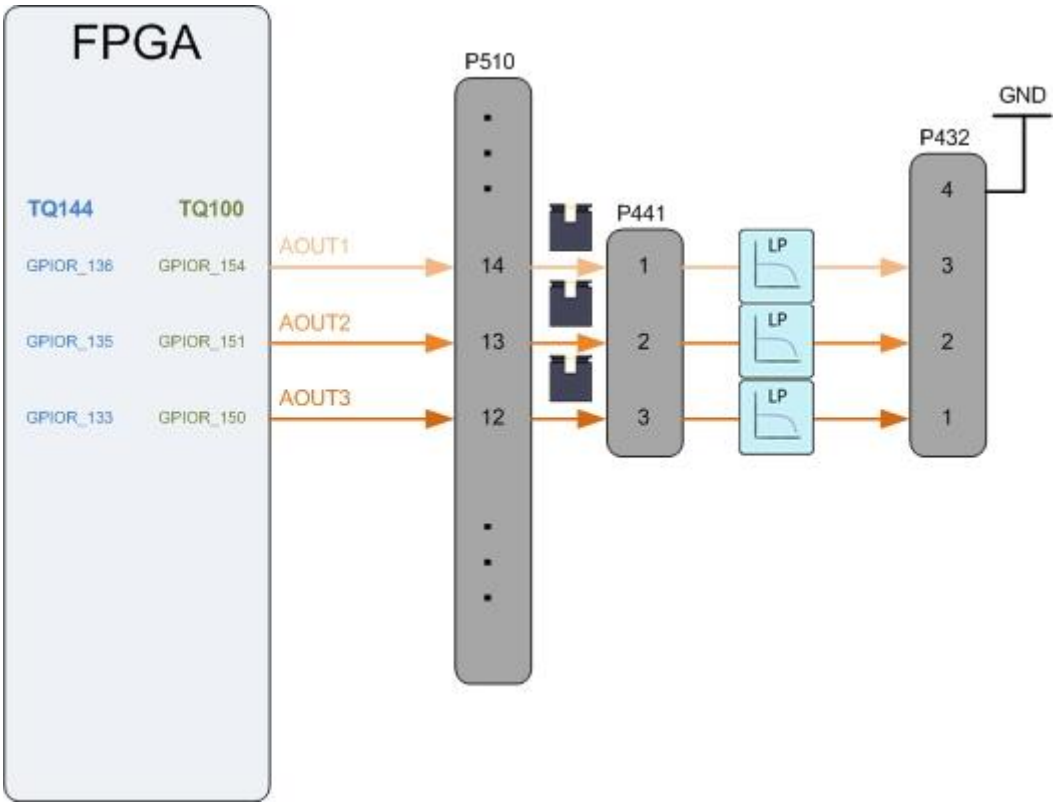

Figure 7: Analog out

Table 11: Analog out - T20Q144

DAC Number	T20Q144 PIN	Signal	alternative use	Bank
1	83	GPIOR_136	P510 P12	3D
2	84	GPIOR_135	P510 P13	3D
3	86	GPIOR_133	P510 P14	3D

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7.1.9 Analog in

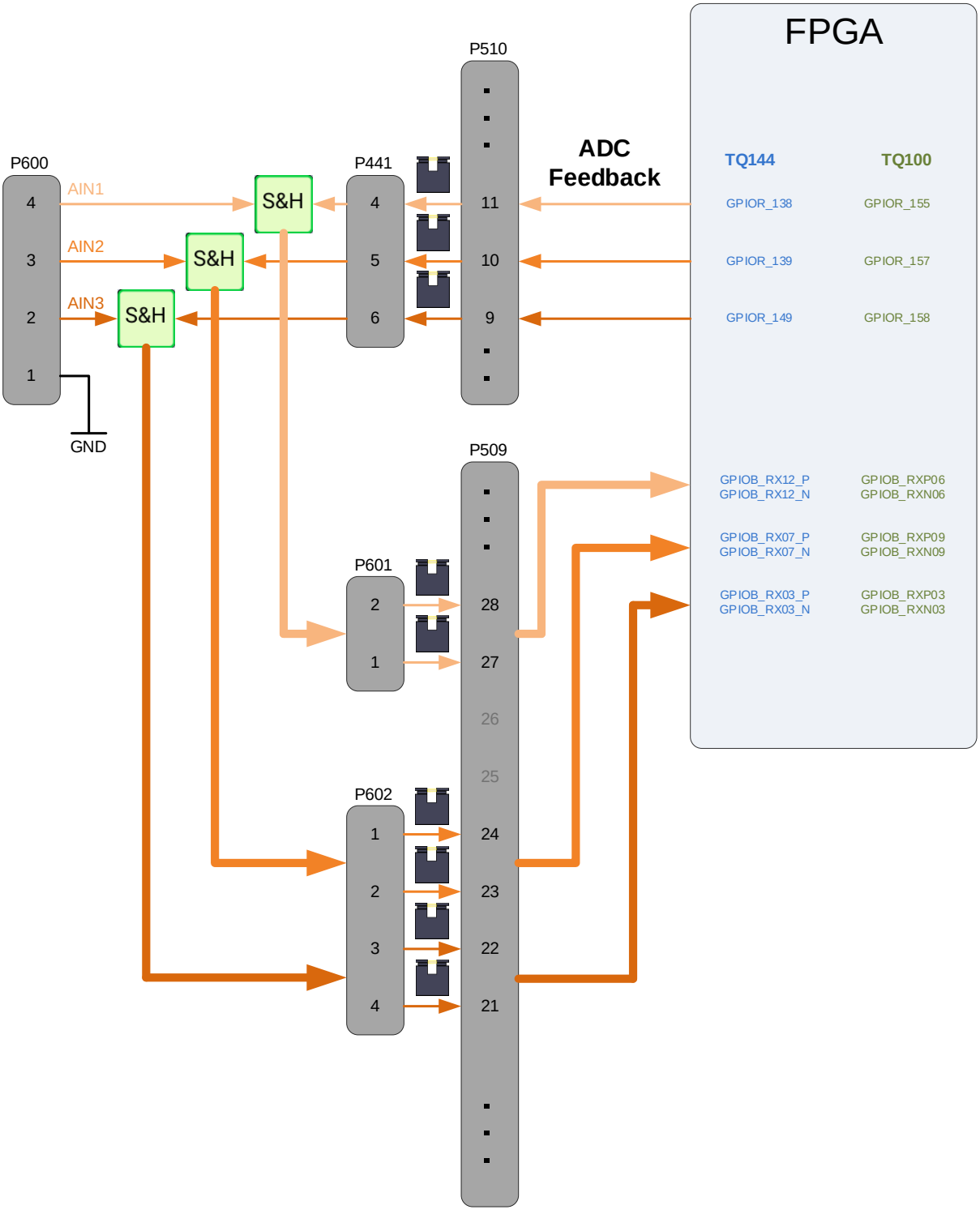

Figure 8: Analog in

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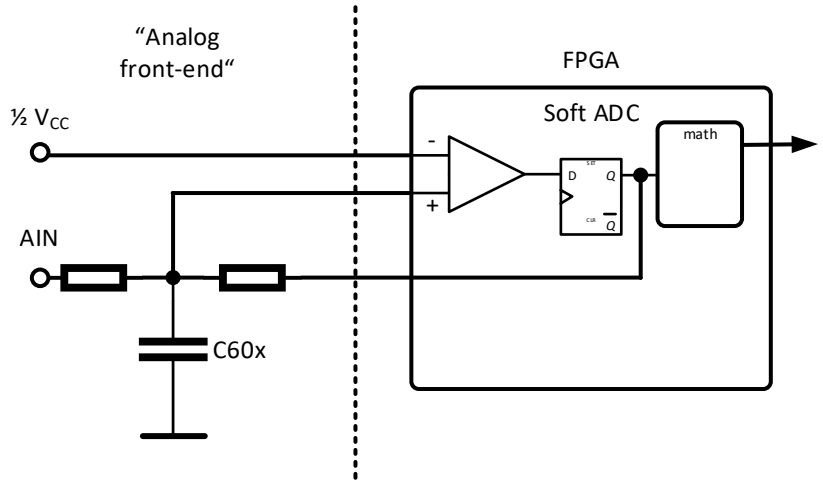
Table 12: Analog in - T20Q144

ADC Signal	T20Q144 PIN	Resource TQ144	Signal Schematic	Description / alternative use	Bank
AIN1	82	GPIOR_138	GPIOR_138	ADC Feedback out via P510-P11	3E
AIN1_P	70	GPIOB_RX12_P	GPIOB_RX12_P	Positive LVDS input via P509-P28	4A
AIN1_N	69	GPIOB_RX12_N	GPIOB_RX12_N	Negative LVDS input via P509-P27	4A
AIN2	81	GPIOR_139	GPIOR_139	ADC Feedback out via P510-P10	3E
AIN2_P	66	GPIOB_RX07_P	GPIOB_RX07_P	Positive LVDS input via P509-P24	4A
AIN2_N	65	GPIOB_RX07_N	GPIOB_RX07_N	Negative LVDS input via P509-P23	4A
AIN3	80	GPIOR_149	GPIOR_149	ADC Feedback out via P510-P09	3E
AIN3_P	61	GPIOB_RX03_P	GPIOB_RX03_P	Positive LVDS input via P509-P22	4A
AIN3_N	60	GPIOB_RX03_N	GPIOB_RX03_N	Negative LVDS input via P509-P21	4A

In order to use different sampling rates, the filter capacitors of the three analogue inputs are equipped with different values, which result in different cutoff frequencies of the analogue source signal:

- AIN1: C600 = 100pF => f_G= 159,2 kHz
- AIN2: C602 = 220pF => f_G= 72,3 kHz
- AIN3: C601 = 1000pF=> f_G=15,9 kHz



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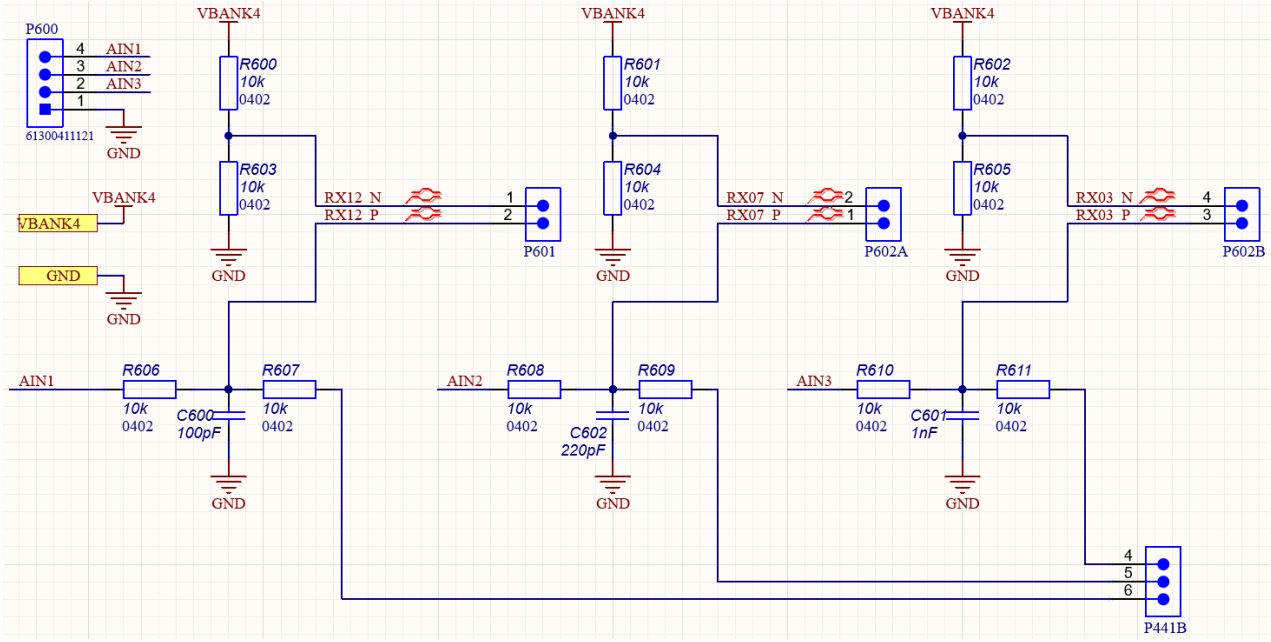
The exact resistance values can be taken from the schematic section below:



If other cut-off frequencies are required, simply use the free filter calculator tool on TRS-Star's webpage:

German: https://www.trs-star.com/service/kalkulatoren/hochpass-und-tiefpassfilter

English: https://www.trs-star.com/en/service/calculators/low-pass-and-high-pass-filter

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7.2 T20Q100

7.2.1 P509

Table 13: pin header P509 – T20Q100

PIN Number	T20Q100 PIN	Resource TQ100	Signal Schematic	alternative use	Bank
1		VBANK4	VBANK4		
2		GND	GND		
3			nc		
4			nc		
5			nc		
6			nc		
7			nc		
8			nc		
9	29	GPIOB_TXP01	GPIOB_TX06_P		4B
10	30	GPIOB_TXN01	GPIOB_TX06_N		4B
11	32	GPIOB_TXP04	GPIOB_TX09_P		4B
12	33	GPIOB_TXN04	GPIOB_TX09_N		4B
13	35	GPIOB_TXP07	GPIOB_TX11_P		4B
14	36	GPIOB_TXP07	GPIOB_TX11_N		4B
15		GND	GND		
16		GND	GND		
17	37	GPIOB_TXP10	GPIOB_RX00_P		4B
18	38	GPIOB_TXN10	GPIOB_RX00_N		4B
19	40	GPIOB_RXP00	GPIOB_RX02_P		4A
20	41	GPIOB_RXN00	GPIOB_RX02_N		4A
21	43	GPIOB_RXN03	GPIOB_RX03_N	AIN3_N	4A
22	44	GPIOB_RXP03	GPIOB_RX03_P	AIN3_P	4A
23	48	GPIOB_RXN07	GPIOB_RX07_N	AIN2_N	4A
24	49	GPIOB_RXP07	GPIOB_RX07_P	AIN2_P	4A
25			nc		
26			nc		
27	47	GPIOB_RXN06	GPIOB_RX12_N	AIN1_N	4A
28	46	GPIOB_RXP06	GPIOB_RX12_P	AIN1_P	4A
29		GND	GND		
30	51	GPIOB_CLKP0	GPIOB_CLK0_P		4A
31	52	GPIOB_CLKN0	GPIOB_CLK0_N		4A
32		GND	GND		

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7.2.2 P510

Table 14: pin header P510 - T20Q100

PIN Number	T20Q100 PIN	Resource TQ100	Signal Schematic	alternative use	Bank
1		VBANK3	VBANK3		
2		GND	GND		
3			nc		
4			nc		
5			nc		
6			nc		
7			nc		
8			nc		
9	53	GPIOR_158	GPIOR_149	AIN1 1Bit DACout	3E
10	54	GPIOR_157	GPIOR_139	AIN2 1Bit DACout	3E
11	55	GPIOR_155	GPIOR_138	AIN3 1Bit DACout	3E
12	56	GPIOR_154	GPIOR_136	AOUT1	3E
13	57	GPIOR_157	GPIOR_135	AOUT2	3E
14	58	GPIOR_150	GPIOR_133	AOUT3	3E
15	59	GPIOR_149	GPIOR_132	Push Button S100	3E
16	62	GPIOR_133	GPIOR_129	Push Button S101	3D
17	63	GPIOR_132	GPIOR_128		3D
18	65	GPIOR_123	GPIOR_125		3C
19	66	GPIOR_122	GPIOR_123		3C
20	67	GPIOR_117	GPIOR_122		3C
21	68	GPIOR_116	GPIOR_117		3C
22	71	GPIOR_94	GPIOR_116		3B
23	73	GPIOR_88	GPIOR_113		3A
24	74	GPIOR_87	GPIOR_112		3A
25			nc		
26			nc		
27			nc		
28			nc		
29			nc		
30			nc		
31					
32		GND	GND		

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7.2.3 P511

Table 15: pin header P511 - T20Q100

PIN Number	T20Q100 PIN	Resource TQ100	Signal Schematic	alternative use	Bank
1		3V3	3V3		
2		GND	GND		
3			nc		
4	94	GPIOL_67	GPIOL_67	PMOD1 P8	1E
5	100	GPIOL_46	GPIOL_65	PMOD1 P7	1D
6	95	GPIOL_66	GPIOL_66	PMOD2 P8	1E
7			nc		1E
8	99	GPIOL_54	GPIOL_53	PMOD2 P7	1D
9	98	GPIOL_53	GPIOL_54	PMOD2 P6	1D
10			nc		1D
11	2	GPIOL_41	GPIOL_41	PMOD2 P5	1C
12	3	GPIOL_40	GPIOL_40	PMOD2 P4	1C
13	4	GPIOL_32	GPIOL_32	PMOD2 P3	1C
14	5	GPIOL_31	GPIOL_31	PMOD2 P2	1C
15	7	GPIOL_24	GPIOL_25	PMOD2 P1	1B
16	8	GPIOL_12	GPIOL_24		1B
17	9	GPIOL_21	GPIOL_22		1B
18			nc		1B
19	10	GPIOL_20	GPIOL_20		1B
20	14	GPIOL_13	GPIOL_13		1B
21			nc		1B
22	18	GPIOL_09	GPIOL_09		1A
23	19	GPIOL_08	GPIOL_08		1A
24	20	CRESET	CRESET		1A
25	26	GPIOL_01	GPIOL_01		1A
26	24	GPIOL_00	GPIOL_00		1A
27	23	GPIOL_04	GPIOL_04	TXD_1	1A
28	22	GPIOL_05	GPIOL_05	RXD_1	1A
29	FTDI Port D	TXD_2	TXD_2		
30	FTDI Port D	RXD_2	RXD_2		
31		GND	GND		
32		GND	GND		

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7.2.4 P512

Table 16: pin header P512 - T20Q100

PIN Number	T20Q100 PIN	Resource TQ100	Signal Schematic	alternative use	Bank
1		VB3SEL	VB3SEL		
2		GND	GND		
3			nc		
4			nc		
5			nc		
6	77	GPIOR_79	GPIOR_82		3A
7	78	GPIOR_78	GPIOR_81		3A
8	79	GPIOR_77	GPIOR_80		3A
9			nc		
10	80	GPIOR_76	GPIOR_78		3A
11			nc		
12			nc		
13	85	GPIOL_75	GPIOL_75	PMOD1 P1	1E
14	86	GPIOL_74	CLK		1E
15	87	GPIOL_73	GPIOL_73	PMOD1 P2	1E
16	89	GPIOL_72	GPIOL_72	PMOD1 P3	1E
17	88	GPIOL_71	GPIOL_71	PMOD1 P4	1E
18	92	GPIOL_70	GPIOL_70	PMOD1 P5	1E
19	93	GPIOL_69	GPIOL_69	PMOD1 P6	1E
20		GND	GND		

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7.2.5 PMOD1 and PMOD2

Note: PMOD modules have to be connect up-side-down. This means that the topside has to face the ground.

Table 17: pin header PMOD1 - T20Q100

PIN Number	T20Q100 PIN	Resource TQ100	Signal Schematic	alternative use	Bank
1	85	GPIOL_75	GPIOL_75	P512 P13	1E
2	87	GPIOL_73	GPIOL_73	P512 P15	1E
3	89	GPIOL_72	GPIOL_72	P512 P16	1E
4	88	GPIOL_71	GPIOL_71	P512 P17	1E
5	92	GPIOL_70	GPIOL_70	P512 P18	1E
6	93	GPIOL_69	GPIOL_69	P512 P19	1E
7	100	GPIOL_46	GPIOL_65	P511 P05	1D
8	94	GPIOL_67	GPIOL_67	P511 P04	1E
9		GND	GND		
10		GND	GND		
11		3V3	3V3		
12		3V3	3V3		

Table 18: pin header PMOD2 - T20Q100

PIN Number	T20Q100 PIN	Resource TQ100	Signal Schematic	alternative use	Bank
1	7	GPIOL_24	GPIOL_25	P511 P15	1B
2	5	GPIOL_31	GPIOL_31	P511 P14	1C
3	4	GPIOL_32	GPIOL_32	P511 P13	1C
4	3	GPIOL_40	GPIOL_40	P511 P12	1C
5	2	GPIOL_41	GPIOL_41	P511 P11	1C
6	98	GPIOL_53	GPIOL_54	P511 P09	1D
7	99	GPIOL_54	GPIOL_53	P511 P08	1D
8	95	GPIOL_66	GPIOL_66	P511 P06	1E
9		GND	GND		
10		GND	GND		
11		3V3	3V3		
12		3V3	3V3		

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7.2.6 Push buttons and user LEDs

Table 19: push buttons - T20Q100

SW Number	T20Q100 PIN	Resource TQ100	Signal Schematic	alternative use	Bank
S100	59	GPIOR_149	GPIOR_132	P510 P15	3E
S101	62	GPIOR_133	GPIOR_129	P510 P16	3D

Table 20: user LEDs - T20Q100

LED Number	T20Q100 PIN	Resource TQ100	Signal Schematic	alternative use	Bank
D400	7	GPIOL_24	GPIOL_25	P511 P15	1B
D401	10	GPIOL_20	GPIOL_20	P511 P19	1B
D402	9	GPIOL_21	GPIOL_22	P511 P17	1B
D404	5	GPIOL_31	GPIOL_31	P511 P14	1C

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7.2.7 UART

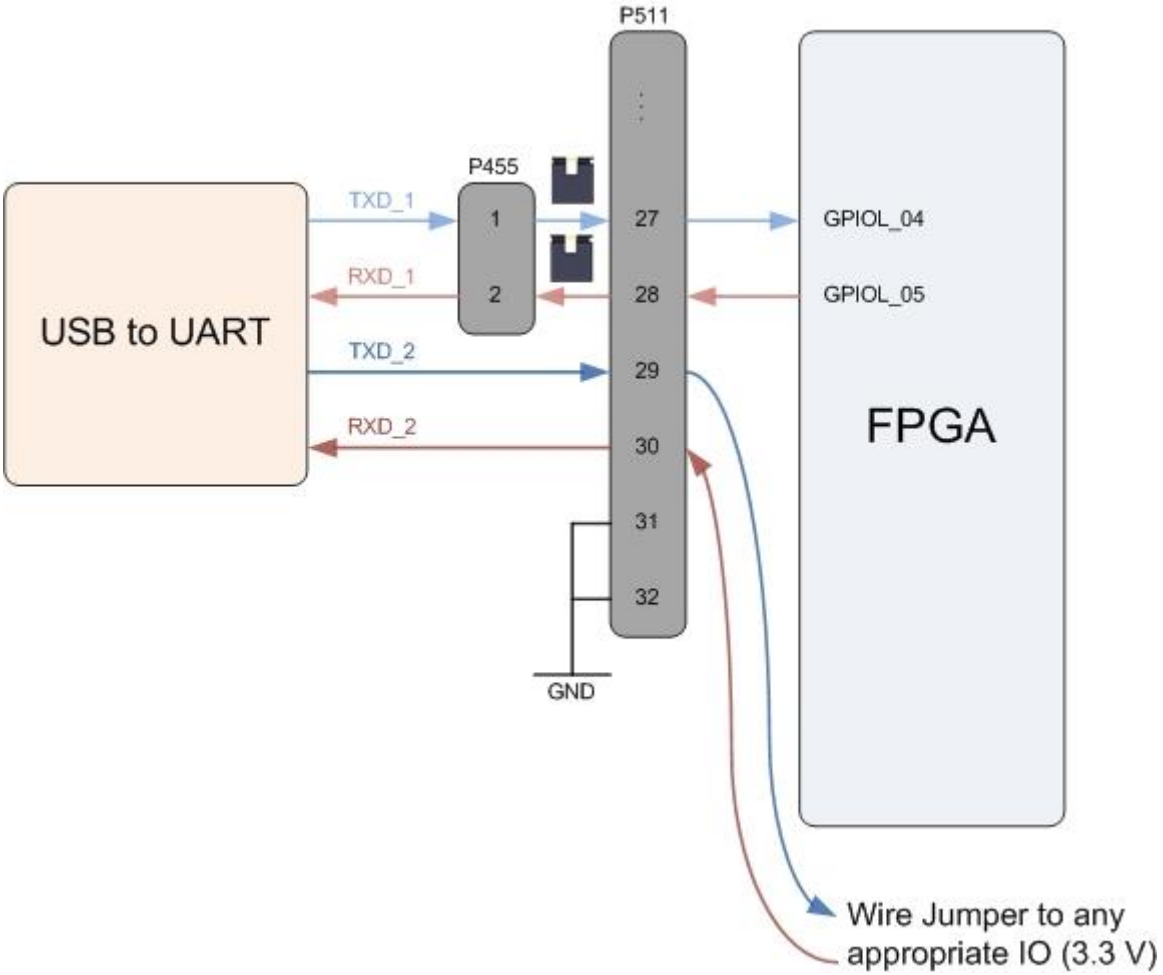

Figure 9: UART - T20Q100

Table 21: UART - T20Q100

Pin	T20Q100 PIN	Resource TQ100	Signal Schematic	alternative use	Bank
TXD_1	23	GPIOL_04	TXD_1	Connect P455-P1 with P511-P27 (GPIOL_04)	1A
RXD_1	22	GPIOL_05	RXD_1	Connect P455-P2 with P511-P28 (GPIOL_05)	1A
TXD_2			TXD_2		
RXD_2			RXD_2		

Note: Signal names are from the host point of view. For example, TXD_1 comes from the USB-UART bridge and goes to the FPGA, therefore it is an input signal for the FPGA (RXD_1).

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7.2.8 Analog out

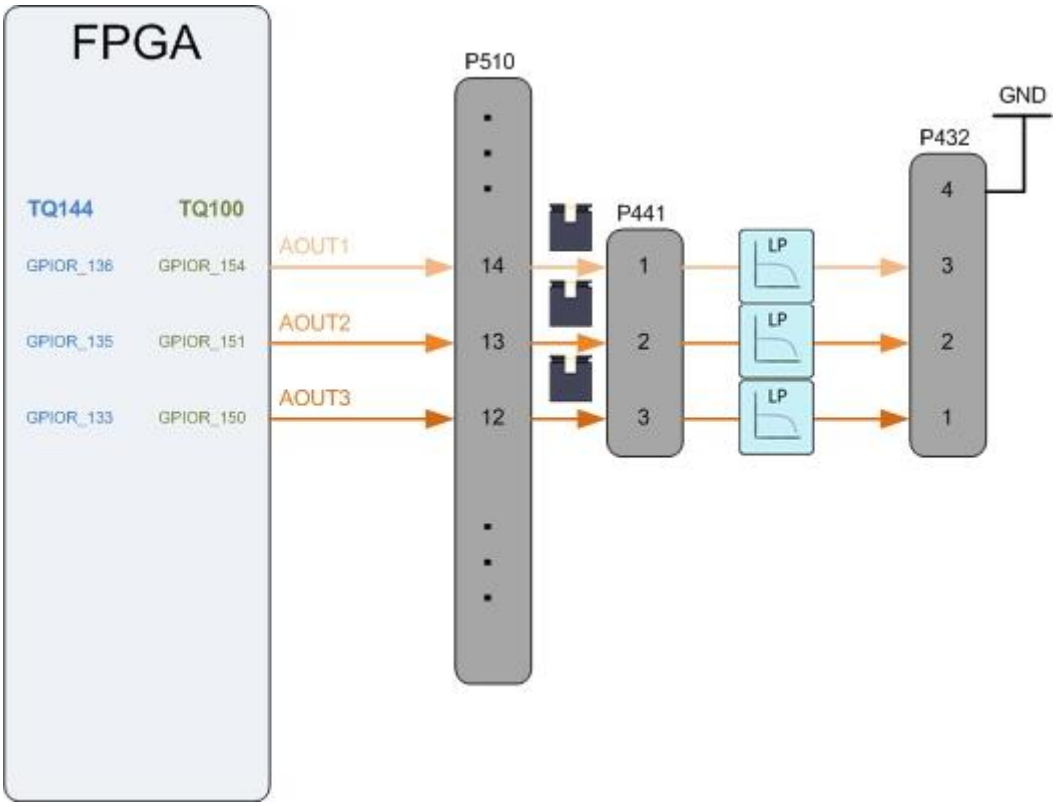

Figure 10: Analog out - T20Q100

Table 22: Analog out - T20Q100

DAC Number	T20Q100 PIN	Resource TQ100	Signal Schematic	alternative use	Bank
1	56	GPIOR_154	GPIOR_136	P510 P12	3D
2	57	GPIOR_151	GPIOR_135	P510 P13	3D
3	58	GPIOR_150	GPIOR_133	P510 P14	3D

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7.2.9 Analog in

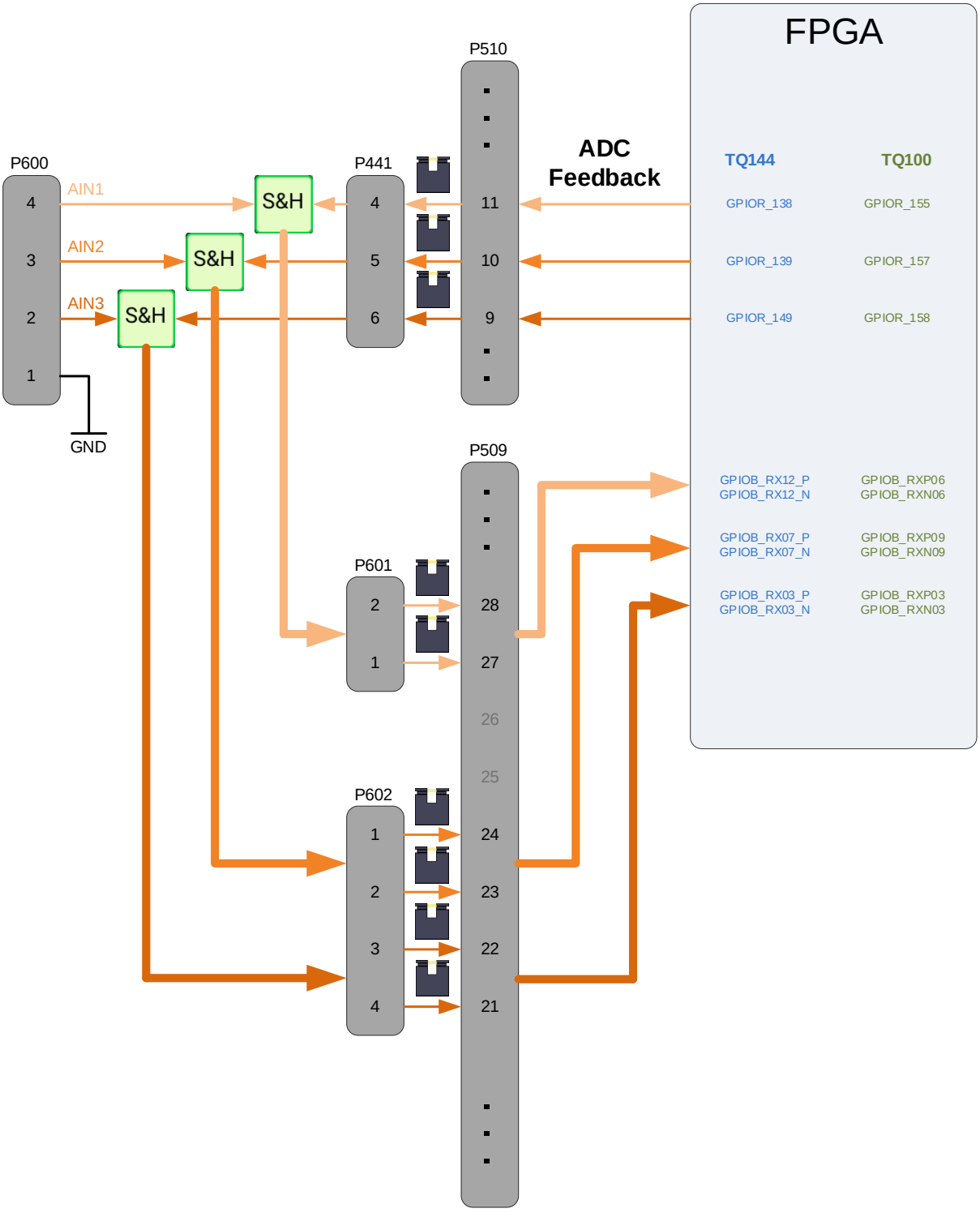

Figure 11: Analog in TQ100/144

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Table 23 Analog in - T20Q100

ADC Signal	T20Q100 PIN	Resource TQ100	Signal Schematic	Description / alternative use	Bank
AIN1	55	GPIOR_155	GPIOR_138	ADC Feedback out via P510-P11	3E
AIN1_P	46	GPIOB_RXP06	GPIOB_RX12_P	Positive LVDS input via P509-P28	4A
AIN1_N	47	GPIOB_RXN06	GPIOB_RX12_N	Negative LVDS input via P509-P27	4A
AIN2	54	GPIOR_157	GPIOR_139	ADC Feedback out via P510-P10	3E
AIN2_P	49	GPIOB_RXP09	GPIOB_RX07_P	Positive LVDS input via P509-P24	4A
AIN2_N	48	GPIOB_RXN09	GPIOB_RX07_N	Negative LVDS input via P509-P23	4A
AIN3	53	GPIOR_158	GPIOR_149	ADC Feedback out via P510-P09	3E
AIN3_P	44	GPIOB_RXP03	GPIOB_RX03_P	Positive LVDS input via P509-P22	4A
AIN3_N	43	GPIOB_RXN03	GPIOB_RX03_N	Negative LVDS input via P509-P21	4A

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