Timer / Counter

Second Release
wide frequency range

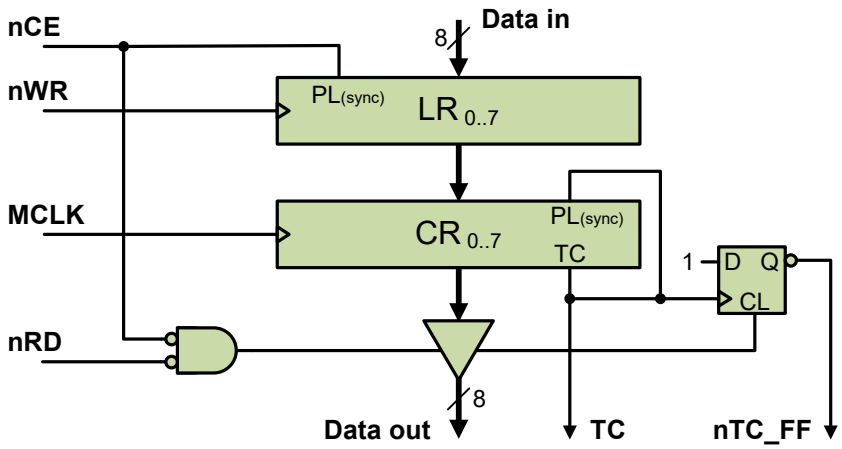
ISEL
INSTITUTO SUPERIOR DE ENGENHARIA DE LISBOA

SASO_TIMER_v2

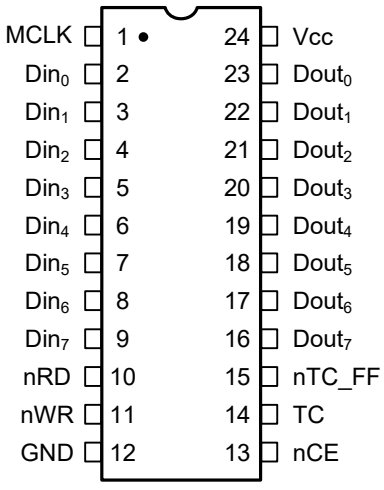
General Description

The SASO_TIMER implements a down counter/timer with 8-bit length. On the rising edge of the *MCLK,* the *Counter Register* (*CR*) value is decremented. When *CR0..7* equals to zero *Terminal Count (TC)* is set active during the second half of MCLK and the flag *nTC_FF* is activated. The *Counter Register* is then reloaded with the value that has been preloaded into the *Load Register* (*LR*) renewing consecutive operation cycles.
Flag *nTC_FF* is cleared when a reading of the timer occurs.

Functional Block Diagram



Pin Configuration



SkinnyDIP

Top View

Rev. 2015/16 v2.0 pM/hm

CUPL Implementation

```
Name     TIMER_v2 ;
PartNo   00 ;
Date     21/12/2015 ;
Revision 2.0 ;
Designer PM/hm ;
Company  CCISEL ;
Assembly None ;
Location  ;
Device   v750c ;

/* *************** INPUT PINS *********************/
PIN  1        = MCLK                              ;
PIN  [2..9]   = [Din0..7]                          ;
PIN  10       = !RD                               ;
PIN  11       = !WR                               ;
PIN  13       = !CE                               ;

/* *************** OUTPUT PINS *********************/
PIN  14       = TC                                ;
PIN  15       = !TC_FF                             ;
PIN  [16..23] = [CR7..0]                          ;

/* ***************** PINNODES ************************/
PINNODE  [27..34] = [LR0..7]                      ;

/* *************** BODY ****************************/

/* Load Register definition */
[LR0..7].ar    = 'b'0;
[LR0..7].sp    = 'b'0;
[LR0..7].ck    = !WR;

[LR0..7].d = CE & [Din0..7] # !CE & [LR0..7] ;

/* Counter Register definition */
[CR0..7].ar    = 'b'0;
[CR0..7].sp    = 'b'0;
[CR0..7].ckmux = MCLK;

/* CR0.t = (!TC & 'b'1) # (TC & (CR0 $ LR0)) */
CR0.t = !TC  # (CR0 $ LR0) ;

$REPEAT i = [1..7]
   CR{i}.t = (!TC & ![CR0..{i-1}]:&) # (TC & (CR{i} $ LR{i})) ;
$REPEND

zero = ![CR0..7]:& ;

/* TC is a glitch free signal,
constrained to the second half of MCLK */
TC = zero & !MCLK ;

/* Terminal Count flip-flop definition */
TC_FF.sp = 'b'0;
TC_FF.d  = 'b'1;

TC_FF.ck = TC;

/* reading the Timer <=> nTC_FF acknowledgement */
RD_Timer = RD & CE ;

[CR0..7].oe = RD_Timer ;
   TC_FF.ar = RD_Timer ;
```

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