2017 Digital IC Design

Homework 5: Color Transform Engine

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NAME	林聖軒								
Student ID P76061425									
Simulation Result									
Testfixture 1 (YUV -> RGB)									
Functional simulation			Pass			Gate-leve	Pass		
Testfixture 2					2 (R	(RGB -> YUV)			
Pattern 1	Functional		Grade	Gate-level		Grade	Gate-level	37726.3ns	
	simulation		A	simulation		A	simulation time		
Pattern 2	Functional		Grade	Gate-level		Grade	Gate-level	37726.3ns	
	simulation		Α	simulation		Α	simulation time		
Pattern 3	Functional		Grade	Gate-level		Grade	Gate-level	37726.3ns	
	simulation		Α	simulation		A	simulation time		
Minimum CYCLE in Gate-level simulation					1	37726.3ns			
** Congratulations! All data have been generated successfully! ** Congratulations! All data have been generated successfully! ** ** Note: *finish : C://Users/eric/Desktop/HW5/testfixture1.v(126) ** Time: 150301 ns					# - # - # + # + # + # + # + # + # + # +	**Congratulations! All data have been generated successfully! **Function 1 (YUV->RGB) FASS			
# SO Your Error Ratio: # (Square Distance of YUV)/(Square of All YUV Signal) = 0.000002 # Your Score Level: A # Congratulations! CTE's Function2 Successfully!					# (S	(Square Distance of YUV)/(Square of All YUV Signal) = 0.000002 Your Score Level: A Congratulations! CTE's Function2 Successfully!			
#					* * 1	<pre># ** Note: \$finish : C:/Users/eric/Desktop/md_fn2_post/testfixture2.v(200) # Time: 37750400 ps Iteration: 0 Instance: /test</pre>			
your pre-sim result of Testfixture 2, pattern 2						your post-sim result of Testfixture 2, pattern 2			

```
Square Distance of All YUV = 43.000000
                                                                             Square Distance of All YUV = 43.000000
  Square of All YUV Signal = 22233632.000000
                                                                             Square of All YUV Signal = 22233632.000000
 (Square Distance of YUV)/(Square of All YUV Signal) = 0.000002
                                                                            (Square Distance of YUV)/(Square of All YUV Signal) = 0.000002
 Your Score Level: A
 Congratulations! CTE's Function2 Successfully!
                                                                             Congratulations! CTE's Function2 Successfully!
                                                                            # ** Note: &finish : C:/Users/eric/Desktop/md_fn2_post/testfixture2.v(200)
# Time: 37750400 ps Iteration: 0 Instance: /test
  ** Note: $finish : C:/Users/eric/Desktop/HW5/testfixture2.v(200)
Time: 150400 ns | Iteration: 0 | Instance: /test
                                                                            # 1
# Break in Module test at C:/Users/eric/Desktop/md_fn2_post/testfixture2.v line 200
 Break in Module test at C:/Users/eric/Desktop/HW5/testfixture2.v line 200
  your pre-sim result of Testfixture 2,
                                                                               your post-sim result of Testfixture 2,
                           pattern 3
                                                                                                        pattern 3
# Square Distance of All YUV = 38.000000
                                                                             Square Distance of All YUV = 38.000000
 Square of All YUV Signal = 21561234.000000
                                                                            Square of All YUV Signal = 21561234.000000
                                                                           # So Your Error Ratio:
# (Square Distance of YUV)/(Square of All YUV Signal) = 0.000002
                                                                           # (Square Distance of YUV)/(Square of All YUV Signal) = 0.000002
                                                                            Your Score Level: A
 Your Score Level: A
                                                                            Congratulations! CTE's Function2 Successfully!
Congratulations! CTE's Function2 Successfully!
# ** Note: $finish : C:/Users/eric/Desktop/HW5/testfixture2.v(200)
# Time: 150400 ns | Iteration: 0 | Instance: /test
                                                                          *** Note: Sfinish : C:/Users/eric/Desktop/md_fn2_post/testfixture2.v(200)

† Time: 37750400 ps Iteration: 0 Instance: /test
                                                                           # 1
# Break in Module test at C:/Users/eric/Desktop/md_fn2_post/testfixture2.v line 200
# Break in Module test at C:/Users/eric/Desktop/HW5/testfixture2.v line 200
                                                           Synthesis Result
                                                                         495
Total logic elements
                                                                         ()
Total memory bit
                                                                         0
Embedded multiplier 9-bit element
(your flow summary)
Flow Summary
                                                     Successful - Tue Dec 26 14:42:43 2017
      Flow Status
      Quartus II Version
                                                     10.0 Build 262 08/18/2010 SP 1 SJ Full Version
      Revision Name
                                                    CTE
      Top-level Entity Name
                                                    Cyclone II
      Family
      Device
                                                    EP2C70F896C8
      Timing Models
                                                    Final
      Met timing requirements
           | al logic elements | 495 | 68,416 ( < 1 /v ) | 77 | 68,416 ( < 1 % ) | 77 | 68,416 ( < 1 % ) |

    Total logic elements

                                                   495 / 68,416 ( < 1 % )
                                                   495 / 68,416 ( < 1 % )
      Total registers
                                                    70 / 622 ( 11 % )
      Total pins
      Total virtual pins
      Total memory bits
                                                    0 / 1,152,000 (0 %)
      Embedded Multiplier 9-bit elements 0 / 300 (0 %)
      Total PLLs
                                                     0/4(0%)
```

Description of your design

根據 HW5 的作業說明,依照 op_mode 訊號來分辨是做 function1 還是function2,並控制 counter、busy、out_vaild 做不同的行為來符合需求,function1 的部分寫一個循序電路吃 clock 用來將 yuv_in 循序吃進大小為 3 的 array,並依序放成 Y、U、V,並餵給一個循序電路做矩陣運算,用位移的方式達到小數乘法的概念,再做四捨五入後將 output 結果丟出來檢查。function2 的部分用同樣用循序電路來將 24bit 的 rgb_in 依照位置切出各 8bit 的 R、G、B,吃進大小為 3 的 array,再將 array 的資料給組合電路做矩陣運算,循環小數的部分先將該小數乘 1024 來達到位移 10bit 的效果並擷取整數部分的 10bit 精度,用該數對 RGB 做相應矩陣乘法後再做正數四捨五入、負數五捨六入,並將結果再右移 10bit 恢復成正確所需數字,最後把結果丟給yuv_out。

Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in \underline{ns})