

2017 Digital IC Design Homework 3: Approximate Average

NAME	林聖軒																																						
Student ID	P76061425																																						
Simulation Result																																							
Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	148296(ns)																																		
(your pre-sim result)			(your post-sim result)																																				
<pre> VSIM 2> run -all # # # All data have been generated successfully! # #-----PASS----- # # # ** Note: \$finish : C:/Users/eric/Desktop/DIC HW3/testfixture.v(122) # Time: 148296 ns Iteration: 2 Instance: /test # 1 # Break in Module test at C:/Users/eric/Desktop/DIC HW3/testfixture.v line 122 VSIM 3> </pre>			<pre> VSIM 16> run -all # # # All data have been generated successfully! # #-----PASS----- # # # ** Note: \$finish : C:/Users/eric/Desktop/DIC HW3/testfixture.v(122) # Time: 148296 ns Iteration: 2 Instance: /test # 1 # Break in Module test at C:/Users/eric/Desktop/DIC HW3/testfixture.v line 122 </pre>																																				
Synthesis Result																																							
Total logic elements		560																																					
Total memory bit		0																																					
Embedded multiplier 9-bit element		0																																					
<div style="border: 1px solid black; padding: 5px;"> <p>Flow Summary</p> <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Flow Status</td> <td>Successful - Sat Nov 25 14:50:03 2017</td> </tr> <tr> <td>Quartus II Version</td> <td>10.0 Build 262 08/18/2010 SP 1 S3 Full Version</td> </tr> <tr> <td>Revision Name</td> <td>CS</td> </tr> <tr> <td>Top-level Entity Name</td> <td>CS</td> </tr> <tr> <td>Family</td> <td>Cyclone II</td> </tr> <tr> <td>Device</td> <td>EP2C70F896C8</td> </tr> <tr> <td>Timing Models</td> <td>Final</td> </tr> <tr> <td>Met timing requirements</td> <td>Yes</td> </tr> <tr> <td>Total logic elements</td> <td>560 / 68,416 (< 1 %)</td> </tr> <tr> <td> Total combinational functions</td> <td>560 / 68,416 (< 1 %)</td> </tr> <tr> <td> Dedicated logic registers</td> <td>72 / 68,416 (< 1 %)</td> </tr> <tr> <td>Total registers</td> <td>72</td> </tr> <tr> <td>Total pins</td> <td>20 / 622 (3 %)</td> </tr> <tr> <td>Total virtual pins</td> <td>0</td> </tr> <tr> <td>Total memory bits</td> <td>0 / 1,152,000 (0 %)</td> </tr> <tr> <td>Embedded Multiplier 9-bit elements</td> <td>0 / 300 (0 %)</td> </tr> <tr> <td>Total PLLs</td> <td>0 / 4 (0 %)</td> </tr> </table> </div>						Flow Status	Successful - Sat Nov 25 14:50:03 2017	Quartus II Version	10.0 Build 262 08/18/2010 SP 1 S3 Full Version	Revision Name	CS	Top-level Entity Name	CS	Family	Cyclone II	Device	EP2C70F896C8	Timing Models	Final	Met timing requirements	Yes	Total logic elements	560 / 68,416 (< 1 %)	Total combinational functions	560 / 68,416 (< 1 %)	Dedicated logic registers	72 / 68,416 (< 1 %)	Total registers	72	Total pins	20 / 622 (3 %)	Total virtual pins	0	Total memory bits	0 / 1,152,000 (0 %)	Embedded Multiplier 9-bit elements	0 / 300 (0 %)	Total PLLs	0 / 4 (0 %)
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Description of your design																																							
<p>使用兩個 block，一個 block 用來存餵進來的 input 和 reset，第二個 block 用來做平均數的計算。第一個 block 當正緣時會將 input 值放進 data 陣列的第一格，data 的其他往後放一格，依此類推共 9 格，若 reset 為 1 則將 data 的資料清成 0。第二個 block 用來做平均數計算，先將 data 的 9 筆資料加起來除 9 算平均，再用 data 複製給 data2 陣列幫助選擇近似平均數，若大於平均數的值必不會選到，則設成 0，再選擇剩餘最大的數，最後再依 function(4)算出結果。</p>																																							

Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)