2017 Digital IC Design Homework 3: Approximate Average

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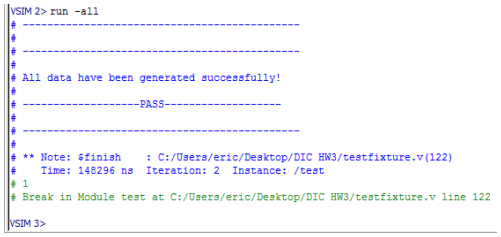
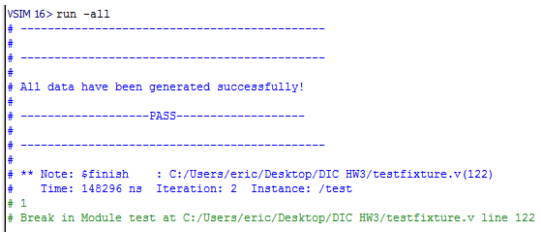
Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	148296(ns)

(your pre-sim result)

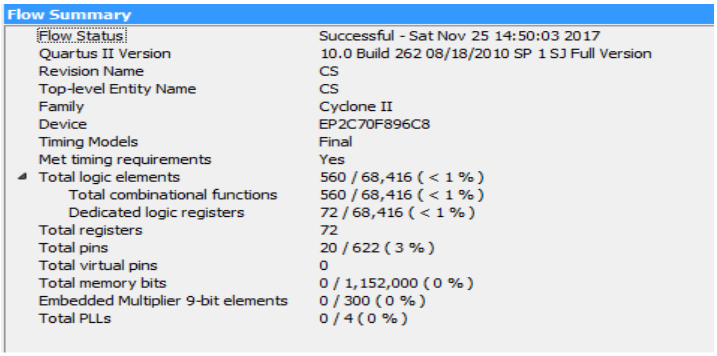


(your post-sim result)



Synthesis Result

Total logic elements	560
Total memory bit	0
Embedded multiplier 9-bit element	0



Description of your design

使用兩個 block，一個 block 用來存餵進來的 input 和 reset，第二個 block 用來做平均數的計算。第一個 block 當正緣時會將 input 值放進 data 陣列的第一格，data 的其他往後放一格，依此類推共 9 格，若 reset 為 1 則將 data 的資料清成 0。第二個 block 用來做平均數計算，先將 data 的 9 筆資料加起來除 9 算平均，再用 data 複製給 data2 陣列幫助選擇近似平均數，若大於平均數的值必不會選到，則設成 0，再選擇剩餘最大的數，最後再依 function(4)算出結果。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*