2017 Digital IC Design
Homework 4: Edge-Based Line Average interpolation

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Simulation Result

Test pattern 1	Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	9633.850(ns)
Test pattern 2	Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	9633.850(ns)

your pre-sim result of two test patterns

```
VSIM 261> run -all
# ------------------------------------------------------------
# \^0^/ All data have been generated successfully! \^0^/
# ------------------------------------------------------------
# ** Note: $stop    : C:/Users/eric/Desktop/HW4/testfixture.v(67)
#    Time: 21355 ns  Iteration: 0  Instance: /test
# Break in Module test at C:/Users/eric/Desktop/HW4/testfixture.v line 67
VSIM 261> run -all
# ------------------------------------------------------------
# \^0^/ All data have been generated successfully! \^0^/
# ------------------------------------------------------------
# ** Note: $stop    : C:/Users/eric/Desktop/HW4/testfixture.v(67)
#    Time: 21355 ns  Iteration: 0  Instance: /test
# Break in Module test at C:/Users/eric/Desktop/HW4/testfixture.v line 67
```

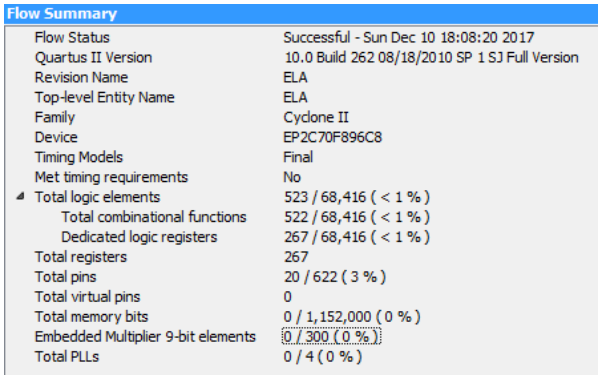
your post-sim result of two test patterns

```
VSIM 32> run -all
# ------------------------------------------------------------
# \^0^/ All data have been generated successfully! \^0^/
# ------------------------------------------------------------
# ** Note: $stop    : C:/Users/eric/Desktop/postsim2222/testfixture.v(67)
#    Time: 9633850 ps  Iteration: 0  Instance: /test
# Break in Module test at C:/Users/eric/Desktop/postsim2222/testfixture.v line 67

# ------------------------------------------------------------
# \^0^/ All data have been generated successfully! \^0^/
# ------------------------------------------------------------
# ** Note: $stop    : C:/Users/eric/Desktop/postsim2222/testfixture.v(67)
#    Time: 9633850 ps  Iteration: 0  Instance: /test
# Break in Module test at C:/Users/eric/Desktop/postsim2222/testfixture.v line 67
```

Synthesis Result

Total logic elements	523
Total memory bit	0
Embedded multiplier 9-bit element	0



Flow Summary	
Flow Status	Successful - Sun Dec 10 18:08:20 2017
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	ELA
Top-level Entity Name	ELA
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	No
Total logic elements	523 / 68,416 (< 1 %)
Total combinational functions	522 / 68,416 (< 1 %)
Dedicated logic registers	267 / 68,416 (< 1 %)
Total registers	267
Total pins	20 / 622 (3 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

使用一個陣列將 input data 從陣列尾端放入，每個 cycle 都從尾端往前推一格，將 input data 放入陣列適當位置，利用相對位置做計算或直接將值取出。利用狀態機的概念，制定 4 個狀態，INIT、DIRECT、CALCULATE、SCAN，別處理不同狀態該做的事。INIT 狀態將 input data 循序從 data array 後端放入，並每個 cycle 在 data array 的最後一格取出 output data。DIRECT 狀態把 data array 的 data 位移推至適當位置，方便下一個 CALCULATE 狀態做計算。CALCULATE 狀態 每個 cycle 利用資料在陣列內的相對位置，依照 Homework

Introduction 給的(1)(2)演算法做內插計算，並將計算結果給 output data。
SCAN 狀態則將 data array 再位移至適當位置準備讓下一個 CALCULATE 狀態做計算。
狀態機: INIT->DIRECT->CALCULATE->SCAN-> CALCULATE->SCAN->….依此循環。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*