VLSI System Design (Graduate Level)

Fall 2024

HOMEWORK I

REPORT

Must do self-checking before submission:

◻ Compress all files described in the problem into one tar

◻ All SystemVerilog files can be compiled under SoC Lab environment

◻ All port declarations comply with I/O port specifications

◻ Organize files according to File Hierarchy Requirement

◻ No any waveform files in deliverables

Student name: \_\_\_\_\_\_\_\_\_\_\_

Student ID: \_\_\_\_\_\_\_\_\_\_