VLSI System Design (Graduate Level)

Fall 2024

HOMEWORK III

REPORT

Must do self-checking before submission:

Compress all files described in the problem into one tar

All SystemVerilog files can be compiled under SoC Lab environment

All port declarations comply with I/O port specifications

Organize files according to File Hierarchy Requirement

No any waveform files in deliverables

Student name: \_\_\_\_\_\_\_\_\_ , \_\_\_\_\_\_\_\_\_

Student ID: \_\_\_\_\_\_\_, \_\_\_\_\_\_\_

**Summary**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Hardware | | | | | | | | |
|  | | | | | | RTL | | synthesis |
| Top | CPU\_wrapper | | CPU | | |  | |  |
| New instructions | | |  | |  |
| SRAM\_wrapper (IM & DM) | | | | |  | |  |
| ROM\_wrapper | | | | |  | |  |
| DRAM\_wrapper | | | | |  | |  |
| AXI | | | | |  | |  |
| DMA | | | | |  | |  |
| Watch Dog Timer | | | | |  | |  |
| Synthesis result | | | | | | | | |
| Area | | | | | Clock cycle(ns) | | | |
|  | | | | |  | | | |
| Firmware & Software | | | | | | | | |
|  | | RTL pass | | syn pass | | | Execution time(ns) | |
| Booting | |  | |  | | | - | |
| Prog 0 | |  | |  | | |  | |
| Prog 1 | |  | |  | | |  | |
| Prog 2 | |  | |  | | |  | |
| Prog 3 | |  | |  | | |  | |
| Prog 4 | |  | |  | | |  | |
| Spyglass summary(number of inline messages) | | | | | | | | |
| Information | | Warning | | Error | | | Fatal | |
|  | |  | |  | | |  | |
| Superlint(number of inline messages) | | | | | | | | |
| Total lines | | Warning | | Error | | | coverage(%) | |
|  | |  | |  | | |  | |

**Contribution**

|  |  |
| --- | --- |
| XXX 50% | XXX 50% |
|  |  |

**Hardware Design Description**

* System Block Diagram
* Interrupt mechanism description and flow chart
* DRAM wrapper FSM chart
* WDT & CDC circuit description and diagram

**Software & Firmware design description**

* Prog 1
* Prog 2
* Booting

**Screen shot of wave forms and simulation results**

**Problems to answer**

1. What is the deference between mcycle and timer? When is mcycle used?
2. What is “Potential Qualifier” in Spyglass?

**Lesson learned**