pCT Scanner Phase II

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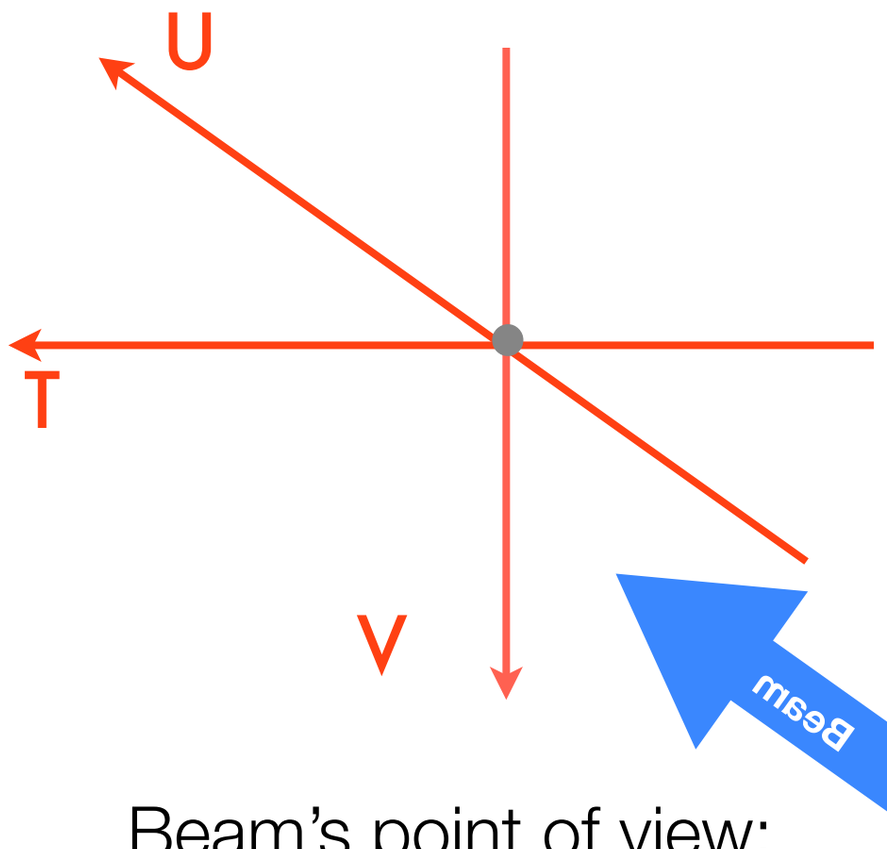
General warnings for the UTV frame of reference (f.o.r.)

- To avoid any mistakes we always refer to the UTV f.o.r. looking at the scanner from the beam's point of view
- The U axis is positive along the beam propagation direction
- The T Axis points from Right to Left, so a negative T means Right a positive T means Left
- The V Axis points from Up to Down, so a negative V means Top, a positive V means bottom



Beam's point of view:
the beam propagates along the U direction (reconstruction) or the Z direction (Geant4)

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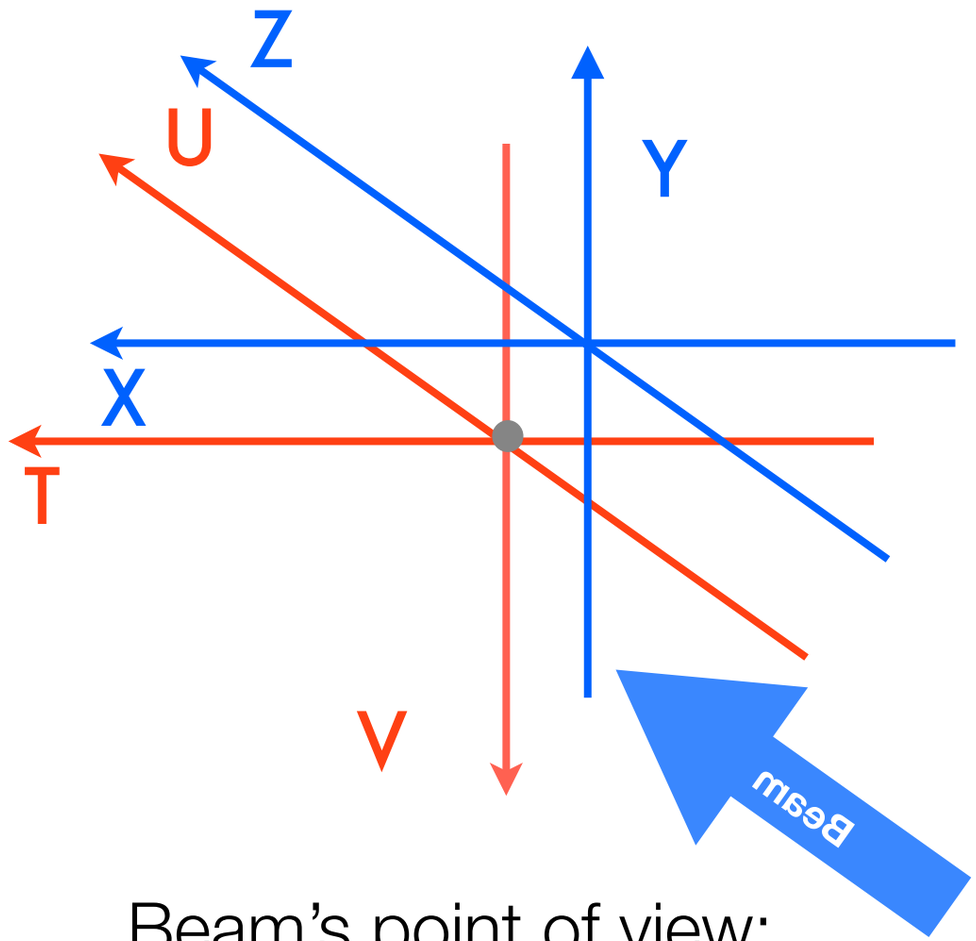
- In the Geant4 f.o.r. the Z and the X axes correspond, respectively, to the U and the T axes. The Y axis corresponds to the -V axis



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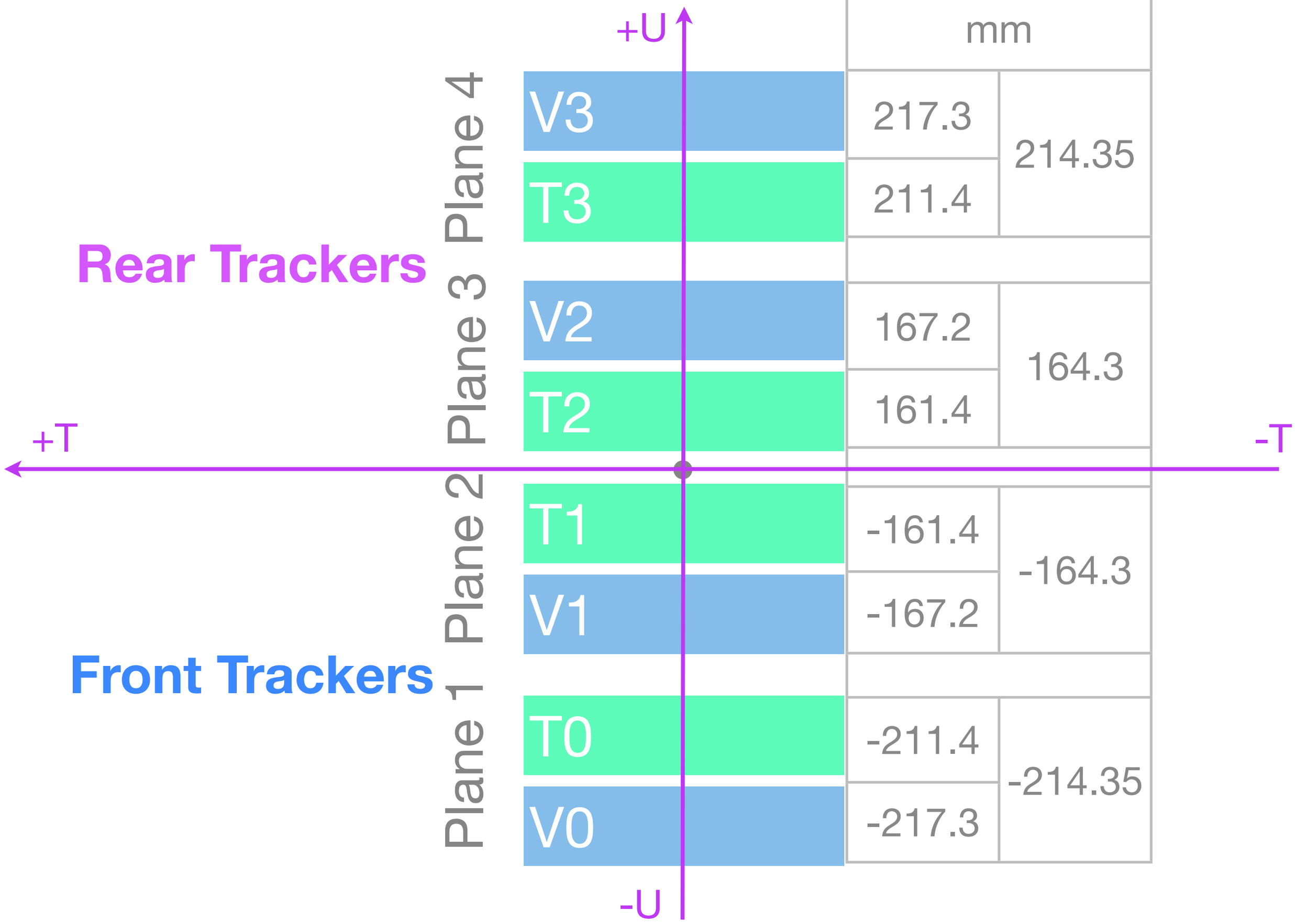
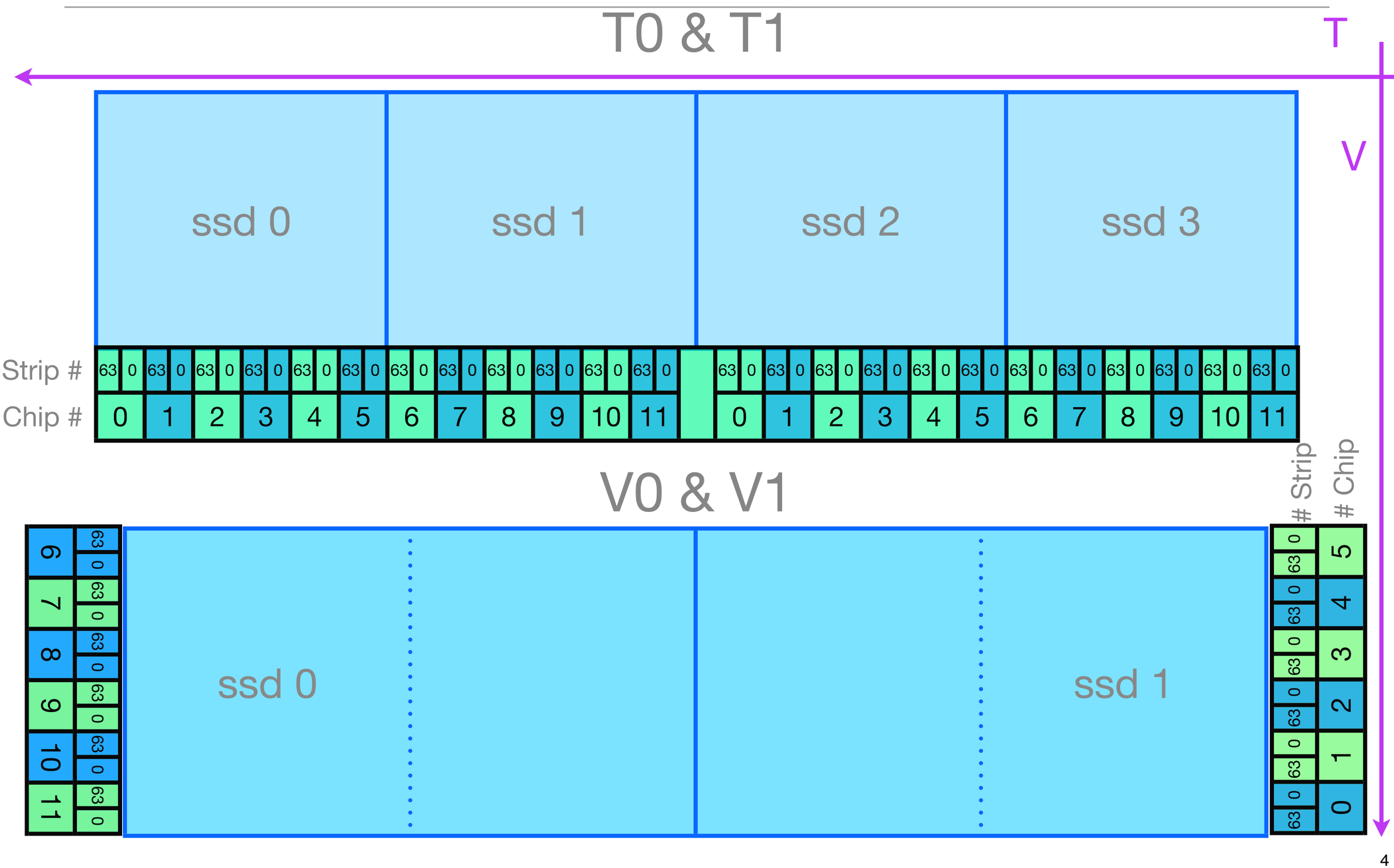
Rear Trackers

Front Trackers



U coordinates mm	
217.3	214.35
211.4	
167.2	164.3
161.4	
-161.4	-164.3
-167.2	
-211.4	-214.35
-217.3	

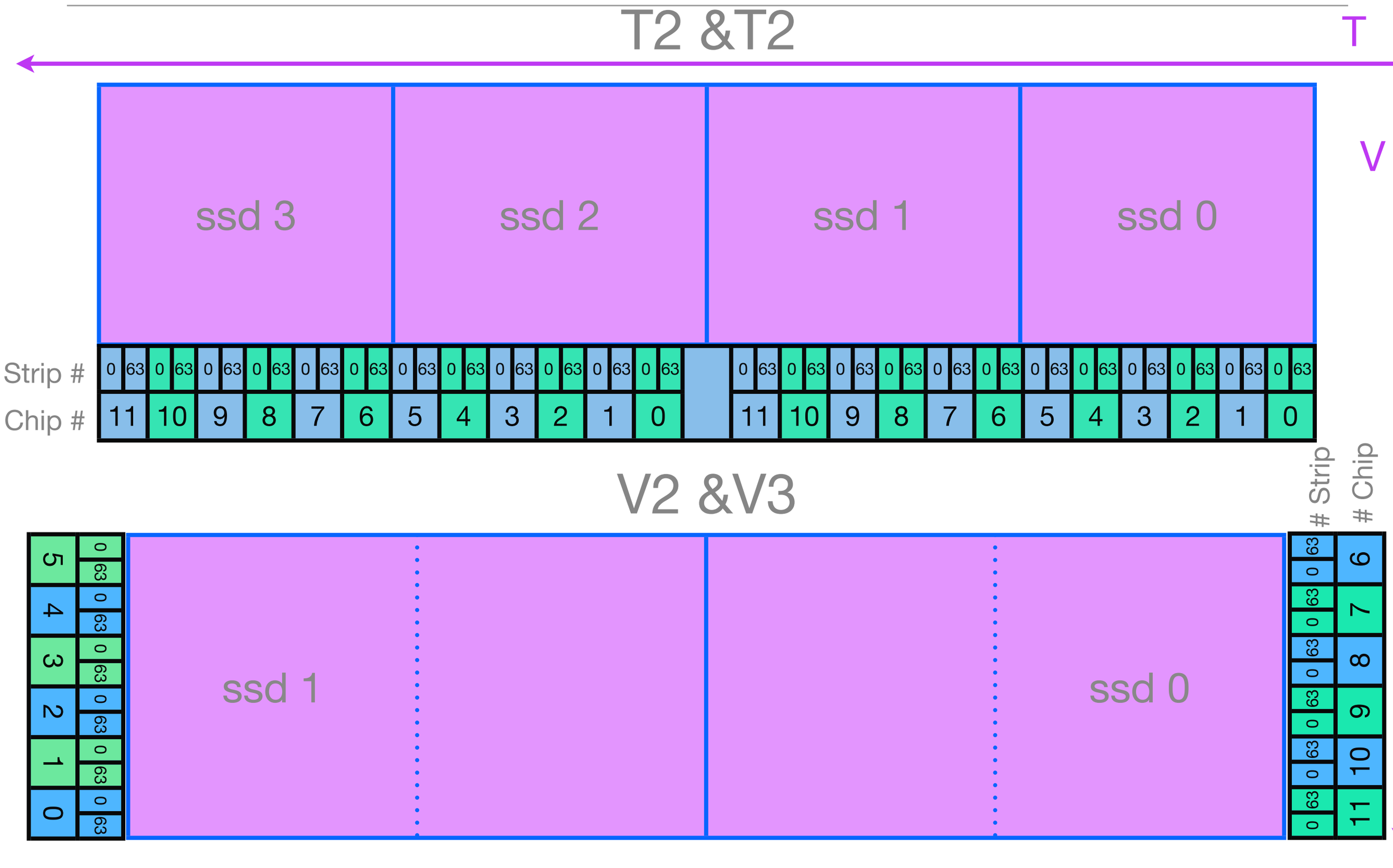
Chip and strip numbers - Front Trackers



Sensors and Gaps positioning - Front Trackers

FRONT	TRACKER																			
PLANE	PLANE #			x center		gap 0		x center		gap 1		x center		gap 2		x center				
V	0		total length	352.340																
x_center	2.3665	43.757	178.537	134.730	90.923	0.593	90.329	46.522	2.715	0.613	2.102	-41.705	-85.512	0.678	-86.190	-129.997	-173.804	height		
y_center	-0.055	-43.867		v1		x center gap		v1		x center gap		v0		x center gap		v0		87.624		
z center	-217.3		length	87.614		90.626	length	87.614		2.408	length	87.614		-85.851	length	87.614				
T	0																			
x_center	0.569	43.257	176.794	132.98	89.17	0.645	88.525	44.713	0.901	0.662	0.239	-43.57	-87.385	0.647	-88.032	-131.844	-175.656	height		
y_center	-0.55	-44.357		t0		x center gap		t1		x center gap		t2		x center gap		t3		87.614		
z center	-211.4		length	87.624		88.85	length	87.624		0.57	length	87.624		-87.71	length	87.624				
V	1		total length	352.274																
x_center	-1.4595	43.757	174.678	130.871	87.064	0.598	86.466	42.659	-1.149	0.616	-1.765	-45.572	-89.379	0.604	-89.983	-133.790	-177.597	height		
y_center	-0.055	-43.867		v1		x center gap		v1		x center gap		v0		x center gap		v0		87.624		
z center	-167.2		length	87.614		86.765	length	87.614		-1.457	length	87.614		-89.681	length	87.614				
T	1																			
x_center	-3.314	43.257	172.92	129.11	85.296	0.656	84.64	40.828	-2.984	0.653	-3.637	-47.45	-91.261	0.663	-91.924	-135.736	-179.548	height		
y_center	-0.55	-44.357		t0		x center gap		t1		x center gap		t2		x center gap		t3		87.614		
z center	-161.4		length	87.624		84.97	length	87.624		-3.31	length	87.624		-91.59	length	87.624				

Chip and strip numbers - Rear Trackers



Sensors and Gaps positioning - Rear Trackers

REAR	TRACKER																			
PLANE	PLANE #			x center		gap 0		x center		gap 1		x center		gap 2		x center				
T	2																			
x_center	11.539	43.257	187.793	143.98	100.169	0.715	99.454	55.642	11.83	0.652	11.178	-32.63	-76.446	0.645	-77.091	-120.903	-164.715		heigh	
y_center	-0.55	-44.357		t3		x center gap		t2		x center gap		t1		x center gap		t0			87.614	
z center	161.4		length	87.624		99.81	length	87.624		11.50	length	87.624		-76.77	length	87.624				
V	2		total length	352.251																
x_center	9.42875	43.757	185.554	141.747	97.940	0.571	97.369	53.562	9.755	0.636	9.119	-34.688	-78.495	0.588	-79.083	-122.890	-166.697		heigh	
y_center	-0.055	-43.867		v0		x center gap		v0		x center gap		v1		x center gap		v1			87.624	
z center	167.2		length	87.614		97.655	length	87.614		9.437	length	87.614		-78.789	length	87.614				
T	3																			
x_center	7.3985	43.257	183.605	139.79	95.981	0.636	95.345	51.53	7.721	0.635	7.086	-36.73	-80.538	0.646	-81.184	-125.00	-168.808		heigh	
y_center	-0.55	-44.357		t3		x center gap		t3		x center gap		t1		x center gap		t0			87.614	
z center	211.4		length	87.624		95.66	length	87.624		7.40	length	87.624		-80.86	length	87.624				
V	3		total length	352.308																
x_center	5.37675	43.757	181.531	137.724	93.917	0.611	93.306	49.499	5.692	0.630	5.062	-38.745	-82.552	0.611	-83.163	-126.970	-170.777		heigh	
y_center	-0.055	-43.867		v0		x center gap		v0		x center gap		v1		x center gap		v1			87.624	
z center	217.3		length	87.614		93.611	length	87.614		5.377	length	87.614		-82.858	length	87.614				

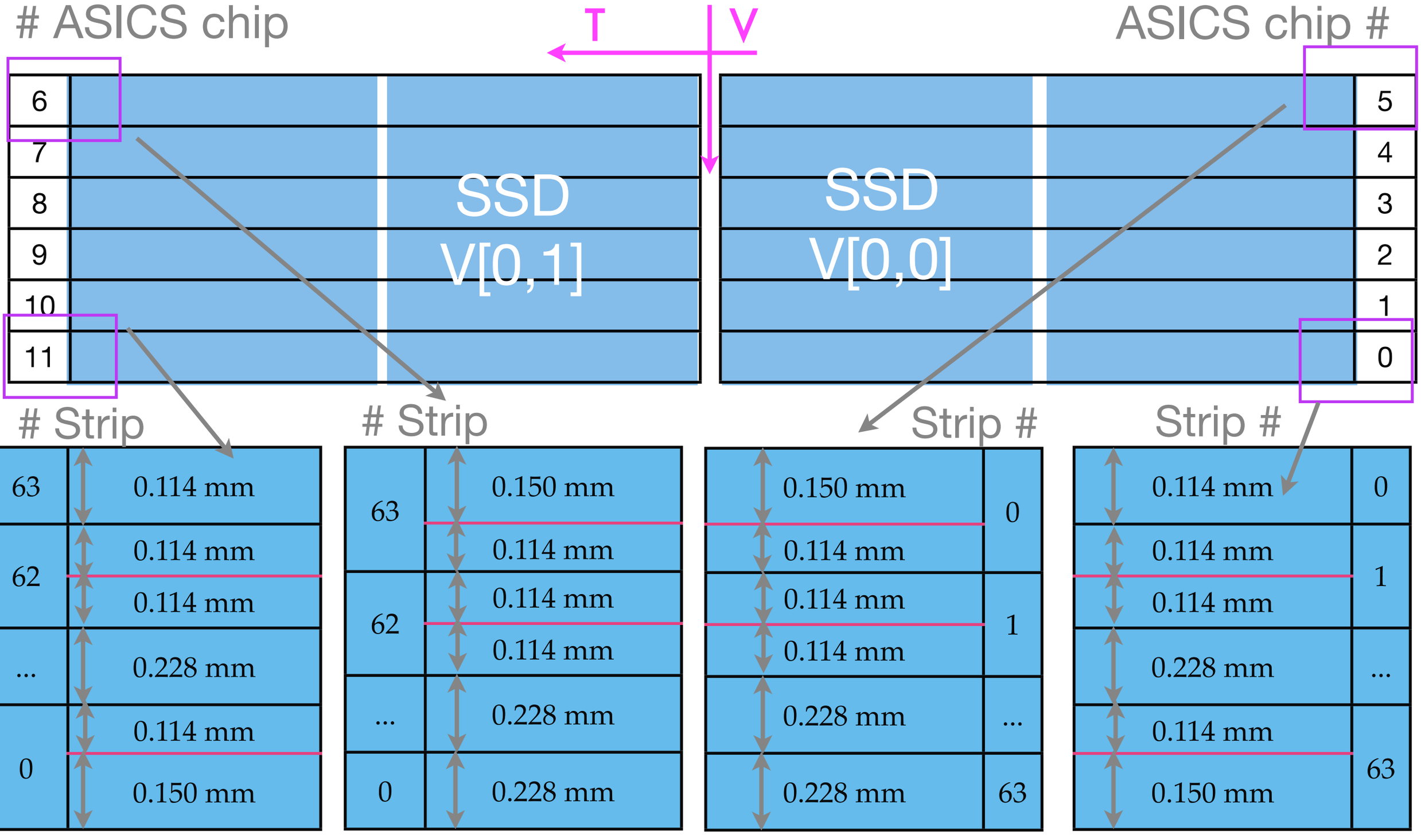
Real coordinate in the Lab f.o.r. for the strips

V plane	SSD #	Top strip	# strip	Bottom strip	# strip
V0	0	-43.72	0	43.607	383
	1	-43.72	0	43.607	383
V1	0	-43.72	0	43.607	383
	1	-43.72	0	43.607	383
V2	0	-43.72	0	43.607	383
	1	-43.72	0	43.607	383
V3	0	-43.72	0	43.607	383
	1	-43.72	0	43.607	383

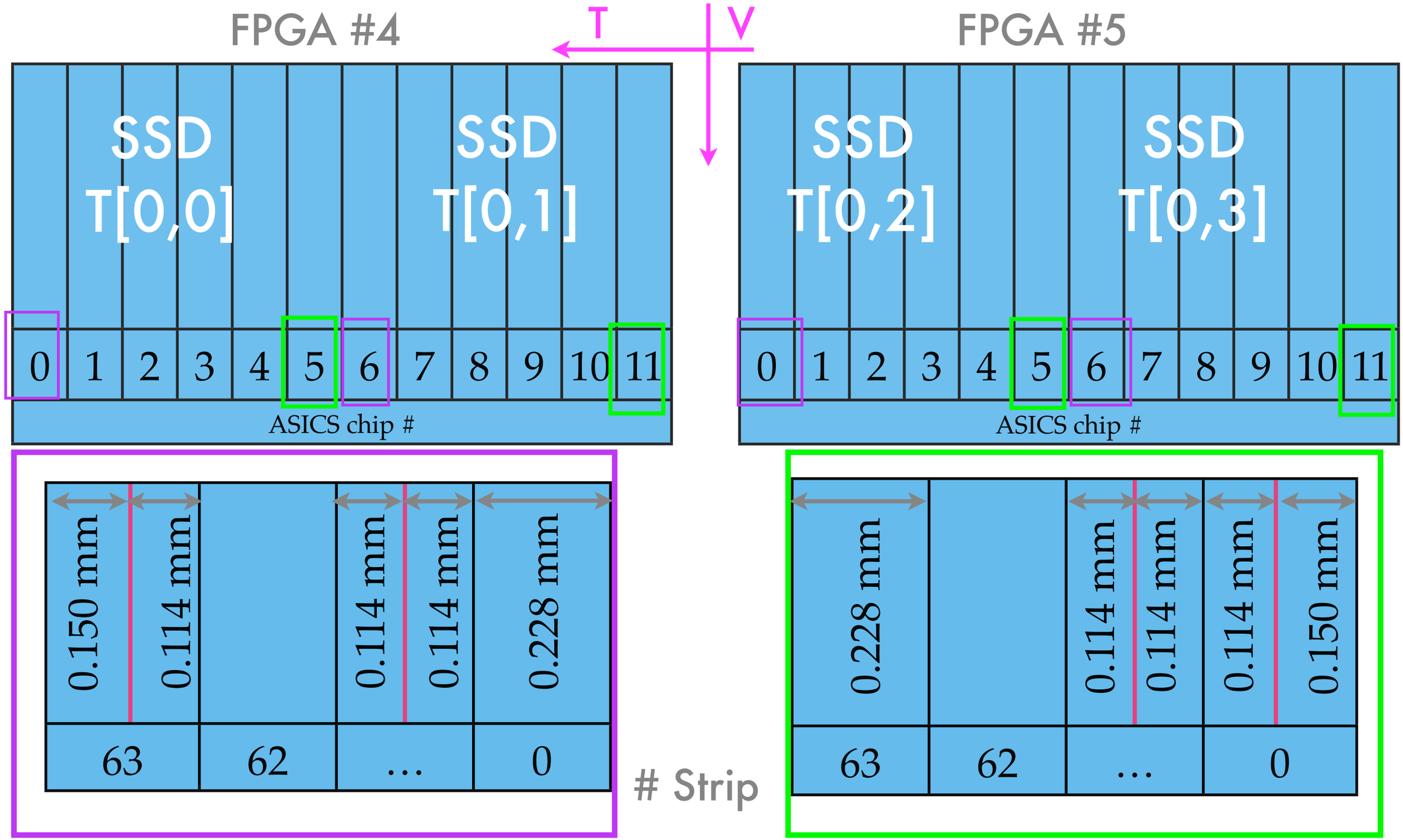
T plane	SSD #	Most Left strip	# strip	Most Right strip	# strip
T0	0	176.644	0	89.32	383
	1	88.375	384	1.051	767
	2	0.089	768	-87.235	1151
	3	-88.182	1152	-175.506	1535
T1	0	172.77	0	85.446	383
	1	84.49	384	-2.834	767
	2	-3.787	768	-91.111	1151
	3	-92.074	1152	-179.398	1535
T2	3	187.643	0	100.319	383
	2	99.304	384	11.98	767
	1	11.028	768	-76.296	1151
	0	-77.241	1152	-164.565	1535
T3	3	183.455	0	96.131	383
	2	95.195	384	7.871	767
	1	6.936	768	-80.388	1151
	0	-81.334	1152	-168.658	1535

Warning: the #strip is arbitrary, chosen to have a univocal strips numbering for each plane

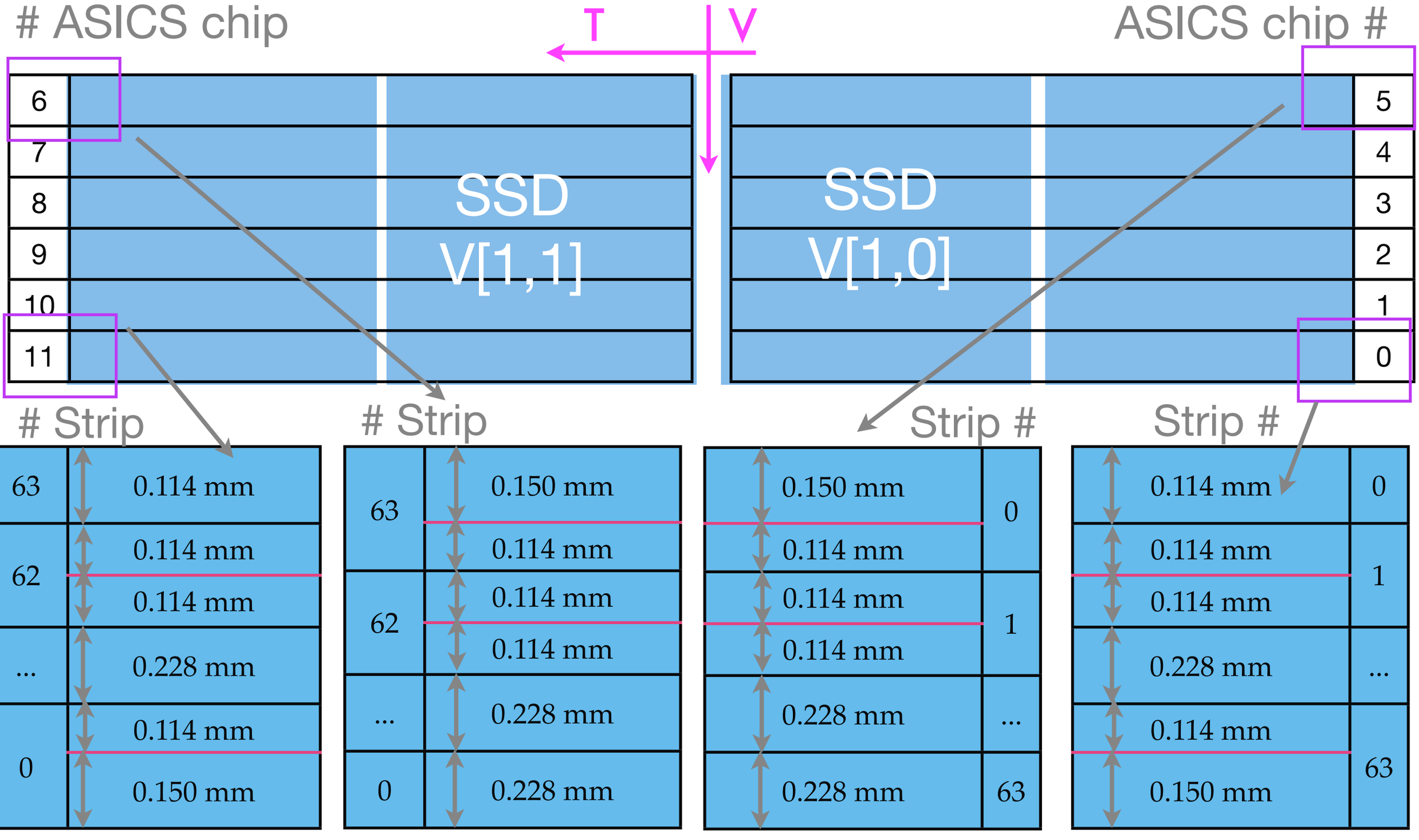
V-Tracker 0 - **FPGA #0**



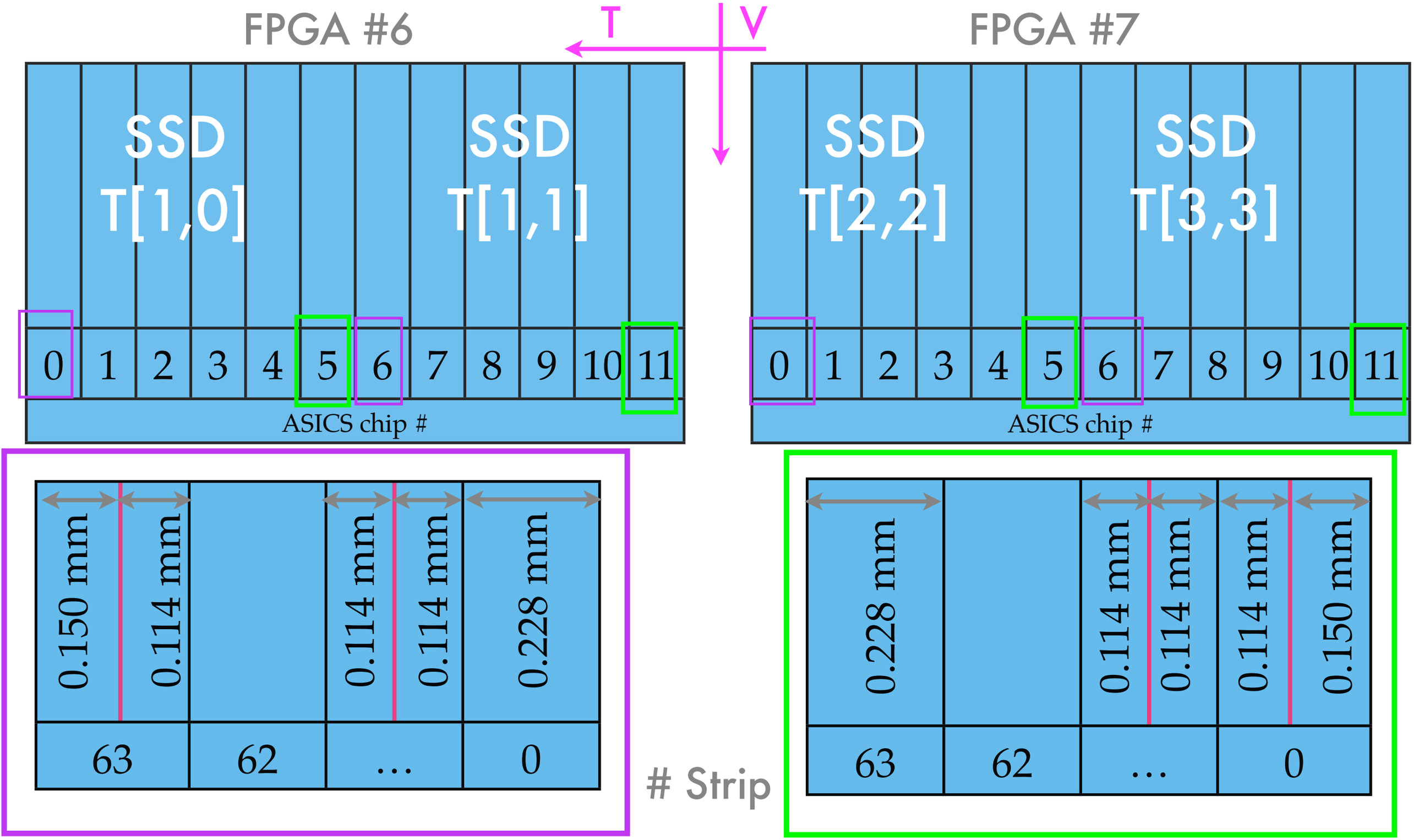
T-Tracker 0 - **FPGA #4 & #5**



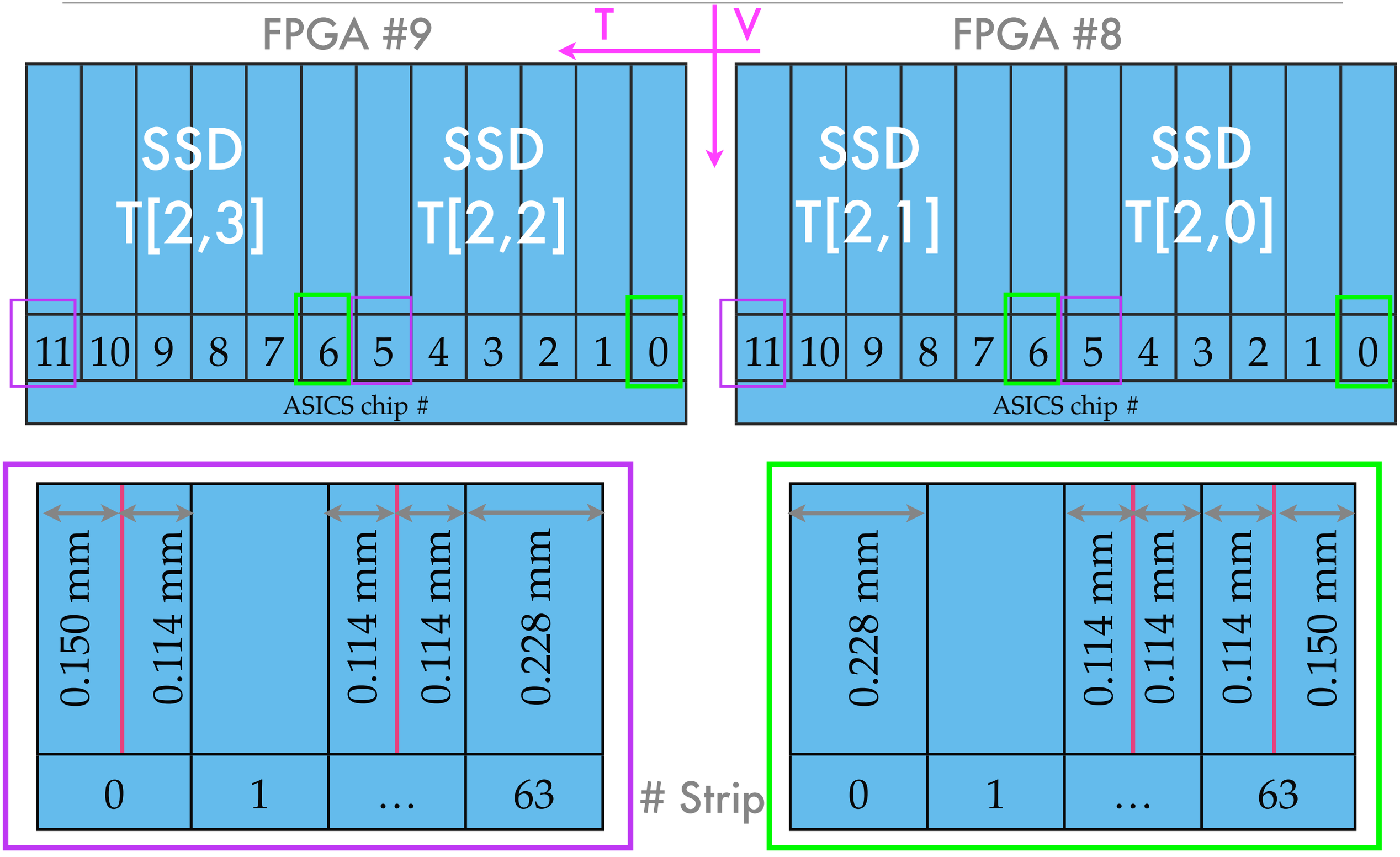
V-Tracker 1- **FPGA #1**



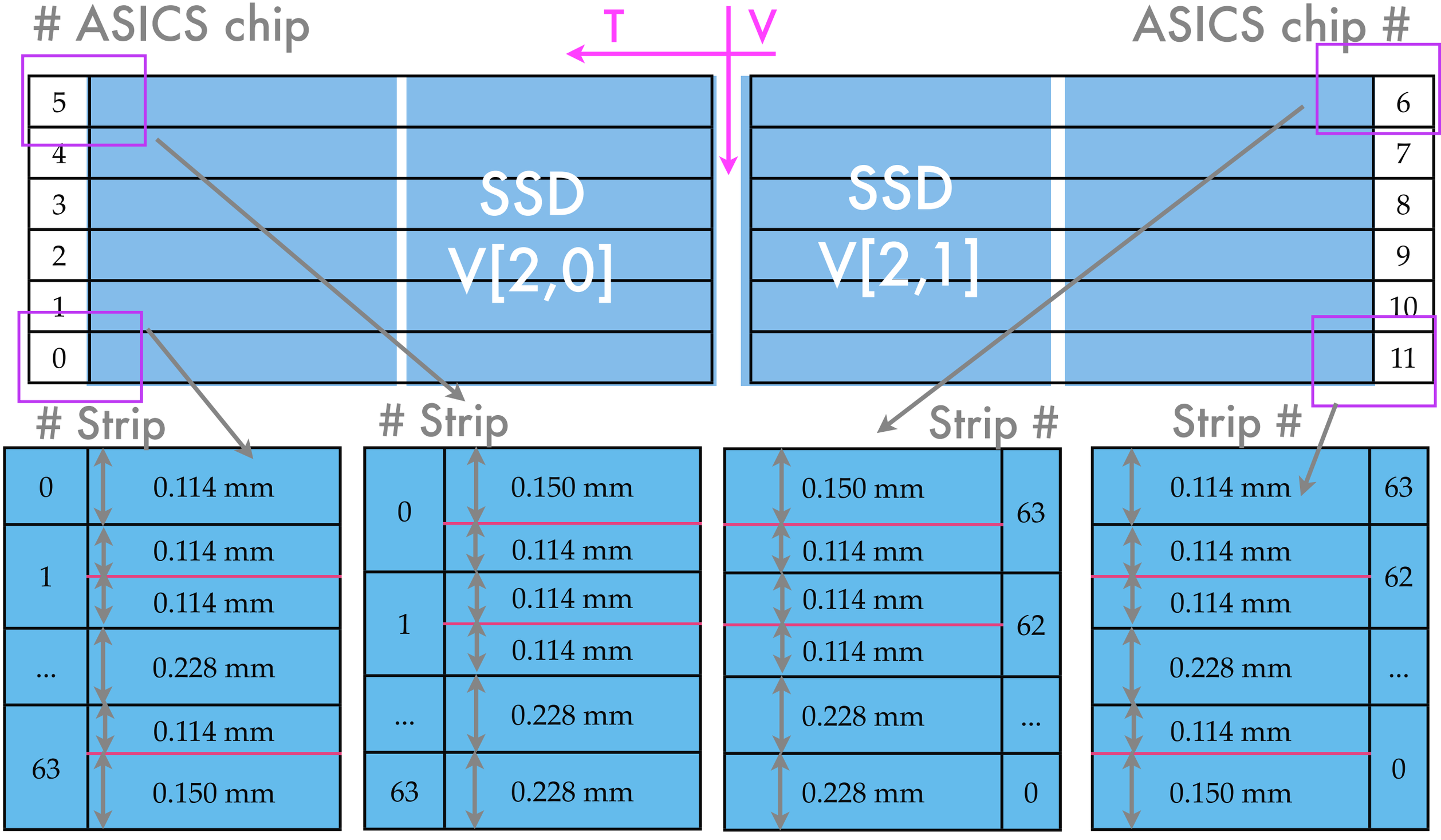
T-Tracker 1 - **FPGA #6 & #7**



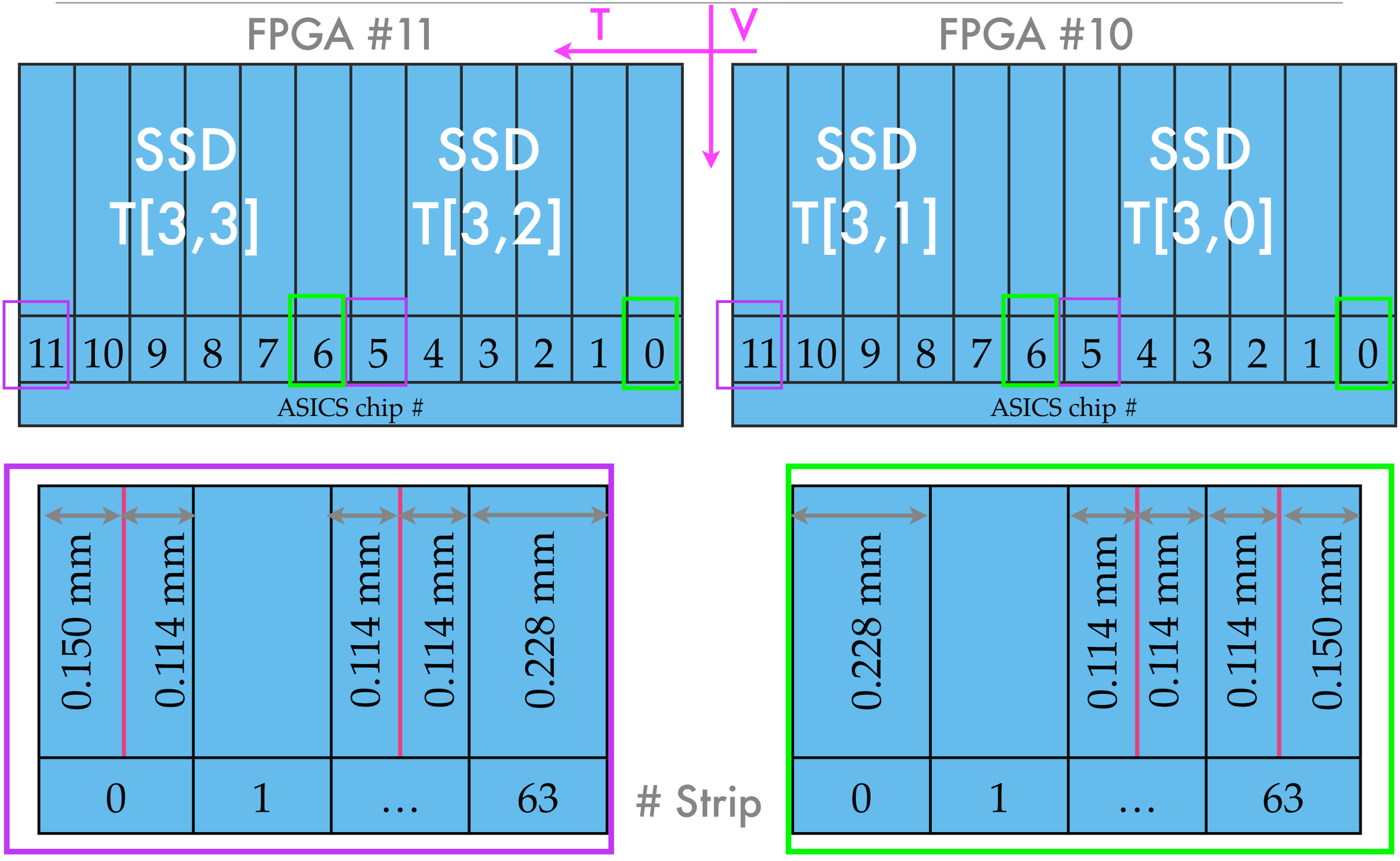
T-Tracker 2 - **FPGA #8 & #9**



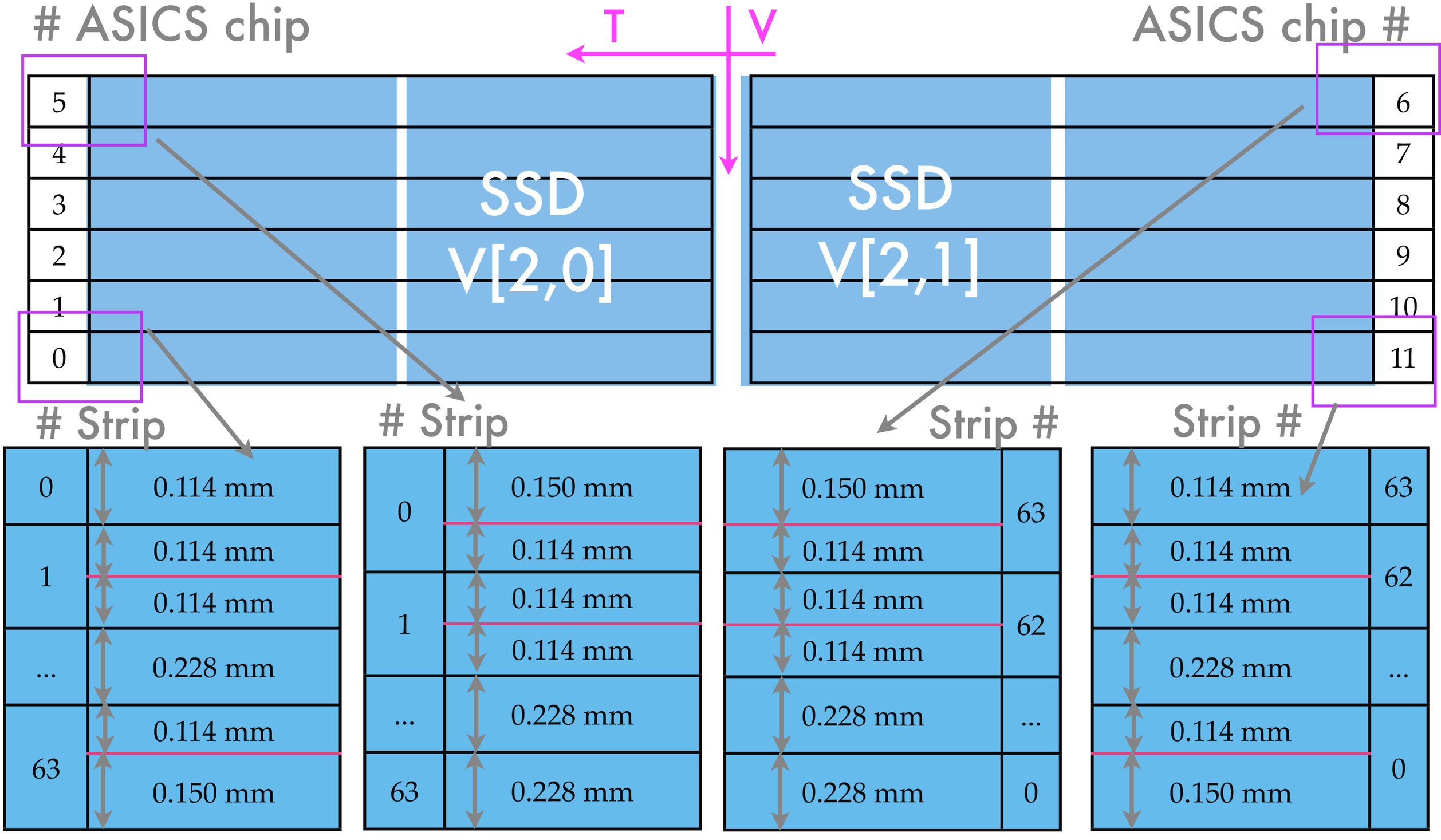
V-Tracker 2- **FPGA #2**



T-Tracker 3 - **FPGA #10 & #11**



V-Tracker 3- **FPGA #3**



pCT bit stream Output format

Warning: all the colored bold quantities are what we need the simulation to supply

pCT bit-stream

- 1 × Run Header

- #event ×

  Event Header

  - 12 × Tracker FPGA Headers

    if Nchip>0

    ➡ Nchip × Chip Headers

    if Ncluster>0

    ➡ Ncluster × Strip Headers

  - 2 × Energy detector FPGA Header

Run Header (13 Bytes)

★ 32-bit identifier

- byte 0: 0x0 `0000 0000`
- byte 1: 0xD2 `1101 0010`
- byte 2: 0x55 `0101 0101`
- byte 3: 0x4E `0100 1110 =1RUN(ASCII)`

★ 24-bit run number

★ 32-bit run start-time

★ 7 status bits, for now set to 0

★ 1 time tag bit

★ 8-bit program version number

★ 12-bit stage angle, in tenths of degree (**ProjDeg**)

Event Header

★ 24-bit beginning-of-event identifier
- byte 0: 0xF0 `1111 0000`
- byte 1: 0x43 `0100 0011`
- byte 3: 0x54 `0101 0100` `=1pCT(ASCII)`

★ 36-bit event time tag: 35-bit time tag + 1 time tag flag (inserted for time pix)

★ 12-bit time since the previous trigger, in clock cycles

★ 24-bit Event header:
- start bits: `10`
- error FLAGS:
  - Incorrect FPGA address received
  - tag mismatch error
  - CRC error
  - Chip error
- 18-bit event identifying number # (**Nevent**)

Tracker FPGA headers (12 bits)

- For each event at least a header for each Tracker FPGA is registered
  - 4-bit FPGA address :
    from `0000` **(FPGA #0)** to `1011` **(FPGA#11)**
  - 3-bit event tag: 1-bit tag clock counter + 2-bit ASIC trigger
  - 1-bit error flag (trigger tag mismatch)
  - 4-bit number of chips **(Nchip)** reporting cluster (strip) data, i.e. number of CHIP containing one or more hit strings.

- if **Nchip** is ≠ 0, #**Nchip** × CHIP headers are registered in the bit stream.

CHIP (ASIC) headers (12 bits)

- 1-bit cluster overflow
- 1 unused 0 bit
- 4-bit number of hit strips cluster (**Ncluster**)
- chip error bit
- parity error bit
- 4-bit CHIP address (**AddChip**)

#**Ncluster** × Strip headers are registered in the bit stream. (Ncluster is at least 1)

Strip headers (12 bits)

- 6-bit number of hit strips (**Nstrips**)
- 6-bit first hit strip address (**AddStrip**)

Warning: if Nstrip =0, just 1 strip has been hit and AddStrip correspond to the address of this hit strip. If Nstrip >0 Nstrip+1 strips have been hit and AddStrip represents the address of the first hit strip.

Energy Deposition FPGA header (12 bit)

★ 2-bit trigger tag
- 1-bit pedestal flag (**PedFlag**): `1` = included `0` = not included
- 1-bit additional trigger tag

★ 3-bit tag for the front-end buffer

★ 1-bit data type flag: `1` = samples `0` = reduced (in the latest beam tests is `0`)

★ 1-bit error flag

★ 2-bits number of channel (**Nch**) per FPGA: 3 for FPGA #12 (connected to 3 calorimeter stage) 2 for FPGA #13

Nch times the following:

★ (16) 24-bit energy deposition data (16 if PedFlag=0)
- if PedFlag =1 -> 8-bit pedestal (**PedValue**) [signed integer]
- 16-bit calorimeter response (sample sum) (**EnergyValue**) [signed integer]

★ if reduced data AND no pedestal AND Nch=2-> 4 unused 0 bits