BL0910
Ten-phase energy measurement chip
Datasheet

V1.0

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1、 PRODUCT DESCRIPTION

BL0910 is an on-chip clock multi-channel calibration-free energy measurement chip, which can achieve up to 10 phases of energy measurement. It can be used in multi-channel electric bicycle charging pile, multi Li intelligent socket / plug, Dali 2.0 intelligent lighting and other multi-channel power consumption measurement and fault detection, with high cost performance.

BL0910 integrates 11 high-precision Sigma-Delta ADCs, which can measure 11 signals (current or voltage) at the same time.

The 1U10I mode is which shares 1-channel voltage and 10-channel currents respectively to generate 10 energy measurement. You can also choose 5U5I mode, which uses 5-channel voltage and 5-channel current to generate 5-channel energy measurement. The 3U6U mode can also be selected. This mode shares three voltage UA / UB / UC, which is multiplied by IA / IB / IC and IA '/ IB' / IC ' to generate 6-channel energy measurement.

BL0910 can measure current and voltage rms, active power, active energy and other parameters, and can output fast current rms (used for fault detection such as leakage monitoring, overcurrent protection), temperature sensor, sampled waveform output and other functions, through UART or high-speed SPI interface outputs data, which can fully meet the needs of multi-channel power consumption data acquisition and monitoring of multi-channel charging pile and other IoT big data collection.

For the input waveform, BL0910 can also select different filters to obtain the full wave or fundamental rms value and power.

The measurement error of the BL0910 factory channel is calibrated to <1%. In the case of no calibration, the external use of 1% precision sampling resistance, the measurement error of the whole machine is less than 2%. If you need to meet the high-precision measurement requirements (the whole machine error <0.3%), you need to calibrate the whole machine.

2、 BASIC FEATURES

2.1 Main Feature

- ✓ 1U10I mode, 10 power metering modes, sharing 1 voltage, and 10 currents respectively, generating 10 power meters
- ✓ 5U5I mode, which uses 5-channel voltage and 5-channel current to generate 5-channel energy measurement.
- ✓ 3U6U mode, shares three voltage UA / UB / UC, which is multiplied by IA / IB / IC and IA '/ IB' / IC ' to generate 6-channel energy measurement.
- ✓ The active power measurement range is determined by the current input range, the current range (5mA~30A), and its measurement accuracy is as follows:

  Current range (50mA~30A), @ 1mohm sampling resistance @Gain=16, power measurement error <±0.3%;

  Current range (5mA~50mA), @ 1mohm sampling resistance @Gain=16, power measurement error <±1%
- ✓ The rms of voltage and current measurement range is determined by the current input range (5mA~30A), and its measurement accuracy is as follows:

  Current range (50mA~30A), @ 1mohm sampling resistance @Gain=16, rms measurement error <±0.6%;

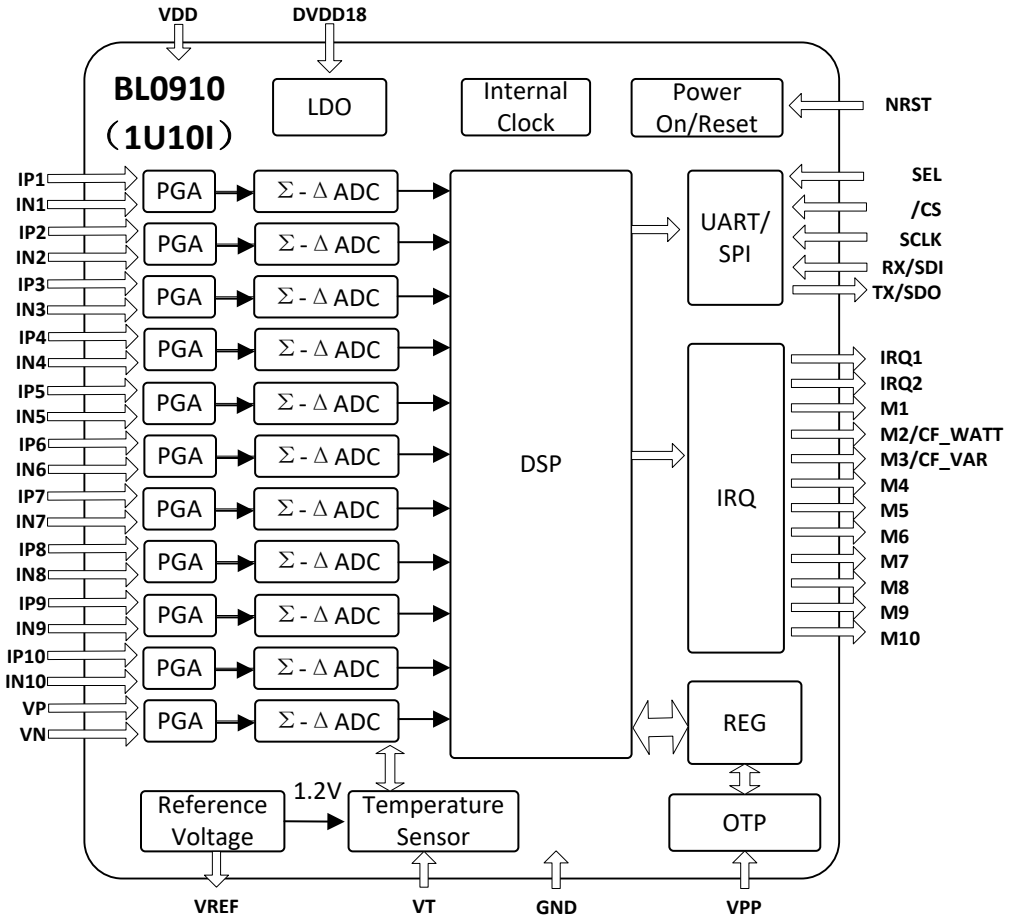
  Current range (5mA~50mA), @ 1mohm sampling resistance @Gain=16, rms measurement error <±5%
- ✓ For the input waveform, you can select different filters to obtain the full wave or fundamental rms and power
- ✓ The batch factory gain error is less than 1%, and the meter can be free of calibration (required for secondary meter)
- ✓ On-chip waveform register, can be used for waveform analysis
- ✓ Leakage monitoring function, can measure leakage current above 1mA, the fastest response time is 10mS, leakage monitoring threshold and response time can be set
- ✓ Each over-current output indication, over-current threshold can be set, response

time can be set

- ✓ On-chip temperature sensor, measuring range -40℃~85℃, measuring accuracy ±2℃, meeting the requirements of over-temperature monitoring and room temperature measurement of the product itself
- ✓ On-chip active, energy, current\voltage rms registers
- ✓ On-chip OTP, calibration parameters can be programed
- ✓ UART/ SPI output
- ✓ Anti-creeping design to ensure noise removal when there is no current
- ✓ Power failure monitoring, chip reset when lower than 2.7v
- ✓ On-chip 1.2v reference voltage source
- ✓ On-chip oscillation circuit, clock is about 8MHz
- ✓ Single working power supply 3.3V, low power consumption 30mW (typical value)
- ✓ LQFP48

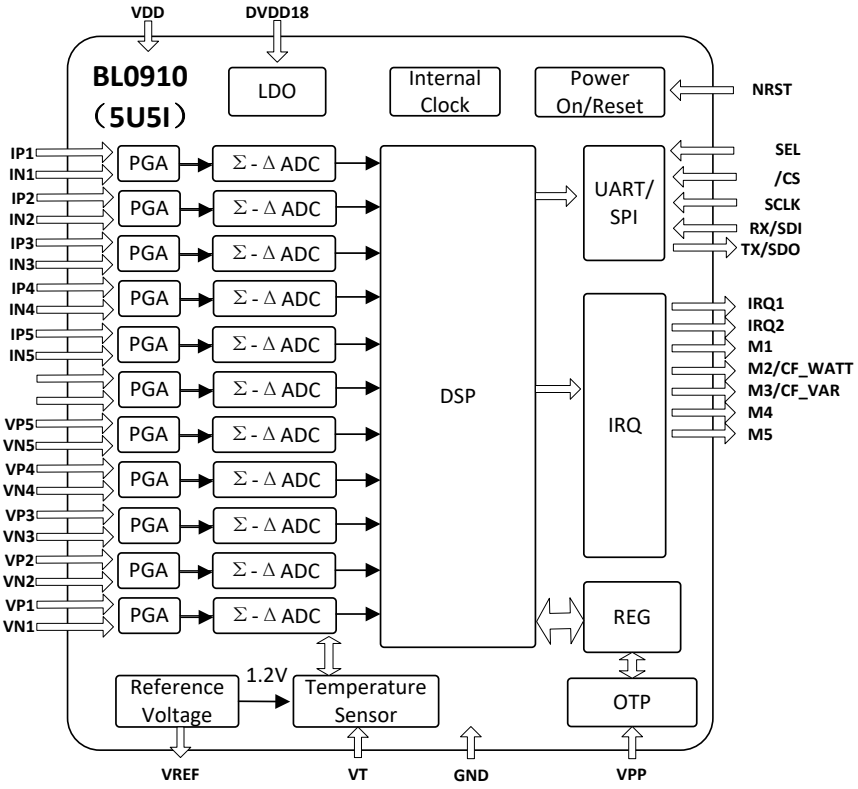
2.2 System Block Diagram

MODE1:1U10I

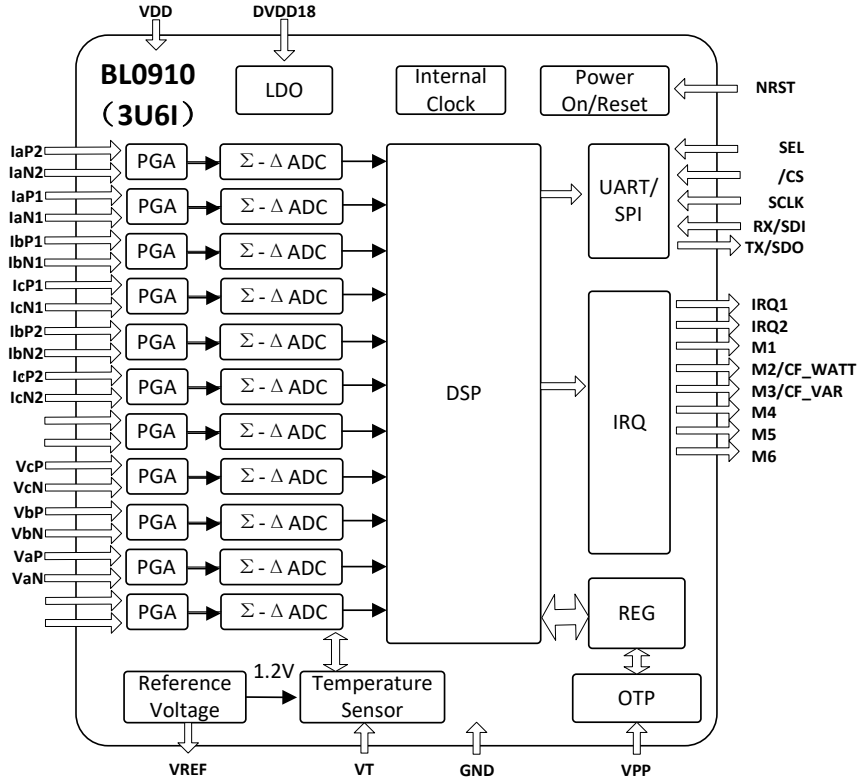


Bl0910 integrates 11 high-precision ADCs, which can measure 11 signals (current or voltage) at the same time. It has analog parts such as on-chip crystal oscillator, reference voltage, temperature measurement, etc. at the same time, the DSP part configures various internal filters according to different modes to calculate power and energy into registers. The digital part also includes optional UART or SPI, interrupt and various indication outputs.

MODE2:5U5I



MODE3:3U6I



2.3 Pin Arrangement (LQFP48)

Sort	Pin Function	I/O	Pin Description
1	VT	I	Temperature sensor terminal.
2	VREF	I/O	Reference voltage input and output, external 0.1uF filter capacitor.
3,4	IN6，IP6	I	#6_Current channel differential input. Gain x1/x2/x4/x16 adjustable. The maximum differential voltage of each pair of pins is ±0.7V.
5,6	IN7，IP7	I	#7_Current channel differential input. Gain x1/x2/x4/x16 adjustable. The maximum differential voltage of each pair of pins is ±0.7V.
7,8	IN8，IP8	I	#8_Current channel differential input. Gain x1/x2/x4/x16 is adjustable. The maximum differential voltage of each pair of pins is ±0.7V.
9,10	IN9，IP9	I	#9_Current channel differential input. The gain x1/x2/x4/x16 is adjustable. The maximum differential voltage of each pair of pins is ±0.7V.
11,12	IN10，IP10	I	#10_Current channel differential input. Gain x1/x2/x4/x16 is adjustable. The maximum differential voltage of each pair of pins is ±0.7V.
13,14	VN，VP	I	#11_Voltage channel differential input, maximum differential voltage ±0.7v.
15	/RST	I	Reset pin, active low.
16	AGND	I	Analog ground.
17	DGND	I	Digital ground.
18	CS	I	SPI chip select signal pin.
19	TX/SDO	O	SPI/UART communication pin, send.
20	RX/SDI	I	SPI/UART communication pin, accept.
21	SCLK	I	SPI communication clock.
22	/IRQ1	O	Interrupt output 1.
23	/IRQ2	O	Interrupt output 2.
24	VPP	I	Reserved, can be floating.

25	M1	O	Channel 1 overcurrent output.
26	M2/CF_watt	O	Channel 2 over current output or active power calibration meter pulse output.
27	M3/CF_var	O	Channel 3 over-current output or reactive power meter pulse output.
28	M4	O	Channel 4 overcurrent output.
29	M5	O	Channel 5 overcurrent output.
30	M6	O	Channel 6 over current output.
31	M7	O	Channel 7 overcurrent output.
32	M8	O	Channel 8 overcurrent output.
33	M9	O	Channel 9 over current output.
34	M10	O	Channel 10 overcurrent output.
35	DVDD18	I/O	1.8V voltage input and output, external 0.1uF filter capacitor.
36	SEL	I	SEL defaults to internal drop-down to select UART, when SEL=1, select SPI.
37	DVDD	I	Digital power input.
38	AVDD	I	Analog power input.
39,40	IN1，IP1	I	#1_Current channel differential input. The gain x1/x2/x4/x16 is adjustable. The maximum differential voltage of each pair of pins is ±0.7V.
41,42	IN2，IP2	I	#2_Current channel differential input. The gain x1/x2/x4/x16 is adjustable. The maximum differential voltage of each pair of pins is ±0.7V.
43,44	IN3，IP3	I	#3_Current channel differential input. The gain x1/x2/x4/x16 is adjustable. The maximum differential voltage of each pair of pins is ±0.7V.
45,46	IN4，IP4	I	#4_Current channel differential input. Gain x1/x2/x4/x16 adjustable. The maximum differential voltage of each pair of pins is ±0.7V.
47,48	IN5，IP5	I	#5_Current channel differential input. The gain x1/x2/x4/x16 is adjustable. The maximum differential voltage of each pair of pins is ±0.7V.

2.4 Performance

2.4.1 Electrical Parameter Performance Index

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active power measurement error	$watt_{err}$	5000:1 input DR		0.1		%
Reactive power measurement error	var_{err}	5000:1 input DR		0.1		%
Phase angle between channels causes measurement errors (PF=0.8 capacitive) (PF=0.5 inductive)	 $pf08c_{err}$ $pf05l_{err}$	 Phase lead 37° Phase lag 60°		 0.1 0.1		 % %
AC power supply suppression (Change in output frequency range) DC power supply suppression (Change in output frequency range)	ac_{psrr} dc_{psrr}	10-channel current input pin IP\IN@100mV, voltage channel input pin VP\VN=100mV		0.01 0.1		% %
Voltage rms measurement accuracy, relative error	$vrms_{err}$	3000:1 input DR		0.1		%
Current rms measurement accuracy, relative error	$irms_{err}$	3000:1 input DR		0.1		%
Analog input Input level (peak) input resistance		Differential input		 370	 700	 mV kΩ

Bandwidth (-3dB) Gain error Phase gain matching error		 External Vref=1.25V External Vref=1.25V		14 8 3		kHz % %
Internal voltage reference Baseline deviation Temperature Coefficient	Vref $Vref_{err}$ TempCoef			1.25 5 20		V mV ppm/℃
Logic input RX/SDI, SCLK, /CS Input high level Input low level		 DVDD=3.3V±2.5% DVDD=3.3V±2.5%	 2.6 	 	 0.8	 V V
Logic output TX/SDO, M1-M10, CF_watt, CF_var Output high level Output low level		 DVDD=3.3V±2.5% DVDD=3.3V±2.5%	 2.6 	 	 1	 V V
power supply AVDD, DVDD DVDD18 AIDD DIDD	 V_{avdd} V_{dvdd18} I_{avdd} I_{dvdd}	 DVDD18=1.8V AVDD=3.3 DVDD=3.3	 3 1.6 	 3.3 1.8 4 6	 3.6 2 8 10	 V V mA mA

2.4.2 Limit Range

（T = 25 ℃）

Project	Symbol	Extremum	Unit
Power supply voltage	AVDD, DVDD	-0.3 ~ +4	V
Digital power voltage	DVDD18	-0.3 ~ +2.5	V
Programming voltage	VPP	-0.3 ~ +7	V
Analog input voltage (relative to GND)	IN1-IN10、VN、IP1-IP10、VP、VT	-1 ~ +AVDD	V
Analog output voltage (relative to GND)	Vref	-0.3 ~ +AVDD	V

Digital input voltage (relative to GND)	SEL、/RST、RX/ SDI、SCLK、/CS	-0.3 ~ AVDD+0.3	V
Digital output voltage (relative to GND)	M1-M10、TX/SDO、/IRQ1、/IRQ2	-0.3 ~ AVDD+0.3	V
Operating temperature	Topr	-40 ~ +85	℃
Storage temperature	Tstr	-55 ~ +150	℃
Power consumption (LQFP48)	P	200	mW

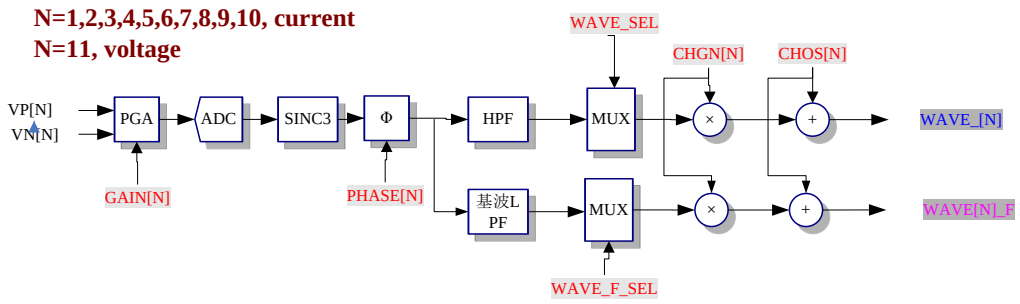
3、 PRINCIPLE OF OPERATION

3.1 Current and Voltage Mode Selection

There are 11 channels of high-precision ADC with the same structure, which adopt double terminal differential signal input. According to different modes, each channel is used for current input or voltage input. See the table below for details. In the following, the unified description is made according to 1U10I mode.

1U10Imode		5U5Imode		3U6Imode		output		
current	voltage	current	voltage	current	voltage	rms	power	M
1	11	1	11			rms01	watt01	m1
2	11	2	10	2	10	rms02	watt02	m2
3	11	3	9	3	9	rms03	watt03	m3
4	11	4	8	4	8	rms04	watt04	m4
5	11	5	7			rms05	watt05	m5
6	11					rms06	watt06	m6
7	11			1	10	rms07	watt07	m7
8	11			5	9	rms08	watt08	m8
9	11			6	8	rms09	watt09	m9
10	11					rms10	watt10	m10

3.2 Principle of Current and Voltage Waveform Generation



There are 11 waveform outputs, including 10 currents and 1 voltage. The positive and negative voltage signals input by the nth current channel are VP[N] and VN[N].

In the channel (the current and voltage are the same with the same circuit structure), the input signal is transmitted to the digital module through the analog module amplifier (PGA) and high-precision analog-to-digital conversion (ADC) to

obtain 1bit PDM code. The digital module is phase-calibrated and down-sampling filtering. After the module (SINC3), optional high-pass filter (HPF) or fundamental low-pass filter, through gain and offset correction modules, the required current waveform data and voltage waveform data (I[N]_WAVE,V_WAVE).

The PGA gain of 11 channels is adjustable (0000=1; 0001=2; 0010=8; 0011=16). For specific settings, see the description of the channel PGA gain adjustment register.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
60	GAIN1	R/W	R	24	0x000000	Channel PGA gain adjustment register.
61	GAIN2	R/W	R	20	0x00000	Channel PGA gain adjustment register.

3.2.1 Phase Compensation

At the ADC output position, a method for digital calibration of small phase errors is provided. It can introduce a small time delay or lead into the signal processing circuit to compensate for small phase errors. Because this compensation must be timely, this This method is only suitable for small phase errors of <0.6° range. Using time-shift technology to correct large phase errors will introduce significant phase errors in higher harmonics.

The phase calibration register PHASE[N] is a binary 8-bit register, and the data format of each register is as follows:

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
64	PHASE[1]/ PHASE[2]	R/W	R	16	0x0000	[15:8] Channel 1 phase correction register. [7:0] Channel 2 phase correction register.
65	PHASE[3]/ PHASE[4]	R/W	R	16	0x0000	[15:8] Channel 3 phase correction register. [7:0] Channel 4 phase correction register.
66	PHASE[5]/	R/W	R	16	0x0000	[15:8] Channel 5 phase correction

	PHASE[6]					register. [7:0] Channel 6 phase correction register.
67	PHASE[7]/ PHASE[8]	R/W	R	16	0x0000	[15:8] C channel 7 phase correction register. [7:0] Channel 8 phase correction register.
68	PHASE[9]/ PHASE[10]	R/W	R	16	0x0000	[15:8] Channel 9 phase correction register. [7:0] Channel 10 phase correction register.
69	PHASE[11]	R/W	R	8	0x00	[7:0] Voltage channel phase for correction register.

3.2.2 Channel Offset Correction

Contains 11 16-bit channel offset calibration registers CHOS[N], the default value is 0x0000.

These registers are placed in OTP and can be used for digital calibration or error pre-calibration before leaving the factory.

They use the data in the form of 2's complement to eliminate the deviation caused by the analog-to-digital conversion of the current channel and the voltage channel respectively. The deviation here may be caused by the input and the offset generated by the analog-to-digital conversion circuit itself. The deviation correction can be used in no load in this case, the waveform offset is 0.

The offset correction formula is detailed in the register description.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
AB	CHOS[1]	R/W	R	16	0x0000	Channel 1 offset adjustment register, complement.
AC	CHOS[2]	R/W	R	16	0x0000	Channel 2 offset adjustment register, complement.
AD	CHOS[3]	R/W	R	16	0x0000	Channel 3 offset adjustment register, complement.

AE	CHOS[4]	R/W	R	16	0x0000	Channel 4 offset adjustment register, complement.
AF	CHOS[5]	R/W	R	16	0x0000	Channel 5 offset adjustment register, complement.
B0	CHOS[6]	R/W	R	16	0x0000	Channel 6 offset adjustment register, complement.
B1	CHOS[7]	R/W	R	16	0x0000	Channel 7 offset adjustment register, complement.
B2	CHOS[8]	R/W	R	16	0x0000	Channel 8 offset adjustment register, complement.
B3	CHOS[9]	R/W	R	16	0x0000	Channel 9 offset adjustment register, complement.
B4	CHOS[10]	R/W	R	16	0x0000	Channel 10 offset adjustment register, complement.
B5	CHOS[11]	R/W	R	16	0x0000	Channel 11 offset adjustment register, complement.

3.2.3 Channel Gain Correction

Contains 11 16-bit channel gain calibration registers CHGN[N], the default value is 0x0000.

These registers are placed in OTP and can be used for digital calibration or error pre-calibration before leaving the factory.

They use 2's complement data to adjust the gain error caused by the analog-to-digital conversion of the current channel and the voltage channel. The error here may be caused by the input and the analog-to-digital conversion circuit itself. The gain correction can be made in the range of ±50% internal adjustment.

The correction formula is detailed in the register description.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
A0	CHGN[1]	R/W	R	16	0x0000	Channel 1 gain adjustment register, complement.
A1	CHGN[2]	R/W	R	16	0x0000	Channel 2 gain adjustment register, complement.

A2	CHGN[3]	R/W	R	16	0x0000	Channel 3 gain adjustment register, complement.
A3	CHGN[4]	R/W	R	16	0x0000	Channel 4 gain adjustment register, complement.
A4	CHGN[5]	R/W	R	16	0x0000	Channel 5 gain adjustment register, complement.
A5	CHGN[6]	R/W	R	16	0x0000	Channel 6 gain adjustment register, complement.
A6	CHGN[7]	R/W	R	16	0x0000	Channel 7 gain adjustment register, complement.
A7	CHGN[8]	R/W	R	16	0x0000	Channel 8 gain adjustment register, complement.
A8	CHGN[9]	R/W	R	16	0x0000	Channel 9 gain adjustment register, complement.
A9	CHGN[10]	R/W	R	16	0x0000	Channel 10 gain adjustment register, complement.
AA	CHGN[11]	R/W	R	16	0x0000	Channel 11 gain adjustment register, complement.

3.2.4 Current and Voltage Waveform Output

The current load current and voltage waveform data can be collected. The sampling current and voltage are updated at a rate of 15.625ksps, and 312.5 points can be sampled per cycle. Each sampled data is a 24bit signed number and stored in the waveform register (WAVE[N]). The SPI rate is about 1.5Mbps, and the waveform values of multiple channels can be read continuously.

The channels can be selected through HPF, fundamental LPF, and finally 11 channel waveforms are obtained (normal current and leakage current are optional).

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
1	WAVE[1]	R	W	24	0x000000	Channel 1 waveform register.
2	WAVE[2]	R	W	24	0x000000	Channel 2 waveform register.
3	WAVE[3]	R	W	24	0x000000	Channel 3 waveform register.

4	WAVE[4]	R	W	24	0x000000	Channel 4 waveform register.
5	WAVE[5]	R	W	24	0x000000	Channel 5 waveform register.
6	WAVE[6]	R	W	24	0x000000	Channel 6 waveform register.
7	WAVE[7]	R	W	24	0x000000	Channel 7 waveform register.
8	WAVE[8]	R	W	24	0x000000	Channel 8 waveform register.
9	WAVE[9]	R	W	24	0x000000	Channel 9 waveform register.
A	WAVE[10]	R	W	24	0x000000	Channel 10 waveform register.
B	WAVE[11]	R	W	24	0x000000	Channel 11 waveform register.

Wave output selection can be set by user mode register MODE1[23].

0x96	MODE1	Working mode register	
No.	Name	Defaults	Description
[23]	WAVE_REG_SEL	1'b0	Current wave waveform register output selection: default 0 selects the waveform of the normal current channel, and 1 selects the waveform output of the leakage channel.

The waveform is divided into full wave and fundamental wave. Through HPF is used to output the AC full wave waveform. The fundamental wave LPF is the fundamental wave measurement mode. This selection can be set by user mode register MODE2[21:0].

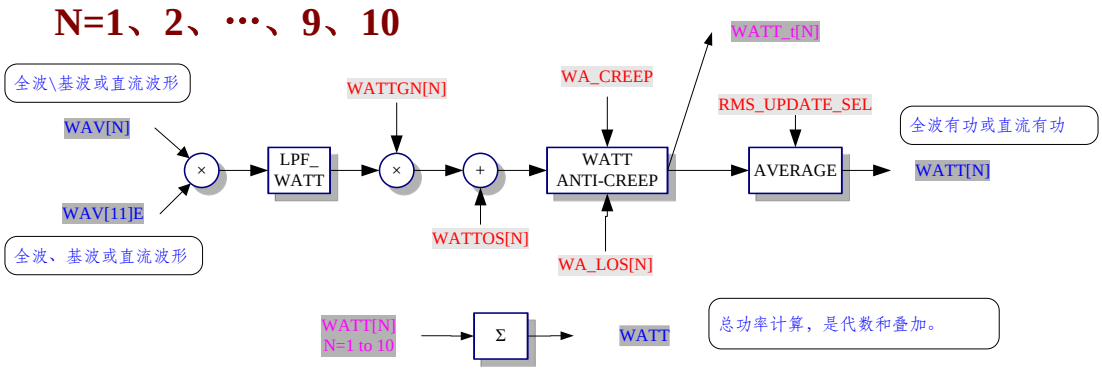
0x97	MODE2	Working mode register	
No.	Name	Defaults	Description
[21:0]	WAVE_RMS_SEL	11{2'b00}	RMS waveform selection: 00 - AC full wave (default), 01 - fundamental wave, 11 - full wave; [1:0]: 1 channel; [3:2]: 2 channel; [5:4]: 3 channel; [7:6]: 4 channel; [9:8]: 5 channel; [11:10]: 6 channel; [13:12]: 7 channel; [15:14]: 8 channel;

			[17:16]: 9 channel; [19:18]: 10 channel; [21:20]: 11 channel.

The waveform of leakage channel (for fast RMS calculation) is divided into full wave and AC full wave. Full wave waveform is not output through HPF. Through HPF for AC measurement mode, output full wave AC waveform. It can be set by user mode register MODE1[22].

0x96	MODE1	Working mode register	
No.	Name	Defaults	Description
[22]	L_F_SEL	1'b0	Leakage channel selection: 0 - not through HPF (default), 1 - through HPF.

3.3 Principle of Active Power Calculation



The current and voltage waveforms are digitally multiplied, and then the power signal can be obtained after low-pass filter, gain and deviation calibration, anti-creeping judgment and averaging processing in order.

3.3.1 Active Power Output

Corresponding to 10 currents are multiplied separately by 1 voltage to obtain 10 power signals WATT[N]. The active power register is a 24-bit signed number, complemented. Bit[23] is the sign bit, indicating positive active power and negative active power. The active power calculation formula is detailed in the register description.

Add.	Name	External	Internal	Bits	Defaults	Description

		R/W	R/W			
22	WATT[1]	R	W	24	0x000000	Channel 1 active power register.
23	WATT[2]	R	W	24	0x000000	Channel 2 active power register.
24	WATT[3]	R	W	24	0x000000	Channel 3 active power register.
25	WATTS [4]	R	W	24	0x000000	Channel 4 active power register.
26	WATTS [5]	R	W	24	0x000000	Channel 5 active power register.
27	WATTS [6]	R	W	24	0x000000	Channel 6 active power register.
28	WATTS [7]	R	W	24	0x000000	Channel 7 active power register.
29	WATTS [8]	R	W	24	0x000000	Channel 8 active power register.
2A	WATTS [9]	R	W	24	0x000000	Channel 9 active power register.
2B	WATTS [10]	R	W	24	0x000000	Channel 10 active power register.
2C	WATTS	R	W	24	0x000000	Total active power register.

It can be set by the add_sel register, and the total active power obtained is the absolute value addition or algebraic addition of the active power of each channel.

0x98	MODE3	Working mode register	
No.	Name	Defaults	Description
[8]	add_sel	1'b0	Watt conjoint sum addition method: 0- absolute value addition; 1- 1-algebraic sum addition.

3.3.2 Active Power Calibration

Contains 10 16-bit active power offset correction registers WATTOS[N] and 10

16-bit active power gain correction registers WATTGN[N], the default value is 0x0000.

These registers are placed in OTP and can be used for digital calibration or error pre-calibration before leaving the factory.

WATTOS is used to eliminate the offset deviation in the active power calculation, and WATTGN is used to eliminate the gain deviation in the active power calculation. The deviation here may be caused by the crosstalk between the two channels generated on the PCB board and the integrated circuit itself in the power calculation. It may also be the gain deviation of the ADC channel itself.

Deviation correction can make the value in the active power register close to 0 under no load.

For the correction of active power, see the detailed description of the register.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
B6	WATTGN[1]	R/W	R	16	0x0000	Channel 1 active power gain adjustment register, complement.
B7	WATTGN[2]	R/W	R	16	0x0000	Channel 2 active power gain adjustment register, complement.
B8	WATTGN[3]	R/W	R	16	0x0000	Channel 3 active power gain adjustment register, complement.
B9	WATTGN[4]	R/W	R	16	0x0000	Channel 4 active power gain adjustment register, complement.
BA	WATTGN[5]	R/W	R	16	0x0000	Channel 5 active power gain adjustment register, complement.
BB	WATTGN[6]	R/W	R	16	0x0000	Channel 6 active power gain adjustment register, complement.
BC	WATTGN[7]	R/W	R	16	0x0000	Channel 7 active power gain adjustment register, complement.

BD	WATTGN[8]	R/W	R	16	0x0000	Channel 8 active power gain adjustment register, complement.
BE	WATTGN[9]	R/W	R	16	0x0000	Channel 9 active power gain adjustment register, complement.
BF	WATTGN[10]	R/W	R	16	0x0000	Channel 10 active power gain adjustment register, complement.
C0	WATTOS[1]	R/W	R	16	0x0000	Channel 1 active power offset adjustment register, complement.
C1	WATTOS[2]	R/W	R	16	0x0000	Channel 2 active power offset adjustment register, complement.
C2	WATTOS[3]	R/W	R	16	0x0000	Channel 3 active power offset adjustment register, complement.
C3	WATTOS[4]	R/W	R	16	0x0000	Channel 4 active power offset adjustment register, complement.
C4	WATTOS[5]	R/W	R	16	0x0000	Channel 5 active power offset adjustment register, complement.
C5	WATTOS[6]	R/W	R	16	0x0000	Channel 6 active power offset adjustment register, complement.
C6	WATTOS[7]	R/W	R	16	0x0000	Channel 7 active power offset adjustment register, complement.
C7	WATTOS[8]	R/W	R	16	0x0000	Channel 8 active power offset adjustment register, complement.
C8	WATTOS[9]	R/W	R	16	0x0000	Channel 9 active power offset

						adjustment register, complement.
C9	WATTOS[10]	R/W	R	16	0x0000	Channel 10 active power offset adjustment register, complement.

3.3.3 Active Power Anti-Creeping

On-chip patented power anti-submarine function module to ensure that the power output is 0 when there is no-load.

The active anti-creep threshold register (WA_CREEP) is a 12-bit unsigned number, and the default is 0x04C. This value is internally expanded by 1 and compared with the absolute value of the input active power signal. When the absolute value of the input active power signal is less than this value, the output the active power is set to zero. This can make the value output to the active power register 0 under no-load conditions, even if there is a small noise signal.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
88	VAR_CREEP/ WA_CREEP	R/W	R	24	0x04C04C	[23:12] is the reactive power anti-creeping threshold register; [11:0] is the active power anti-creeping threshold register.
89	WA_CREEP2	R/W	R	12	0x000	[11:0] is the total active power anti-creeping threshold register.

You can set WA_CREEP according to the WATT value of the power register, and their corresponding relationship. The anti-submarine value generally takes 20 parts per million of the power full scale.

When the channel is in the anti-submarine state, the power of the channel below the threshold does not participate in the energy accumulation.

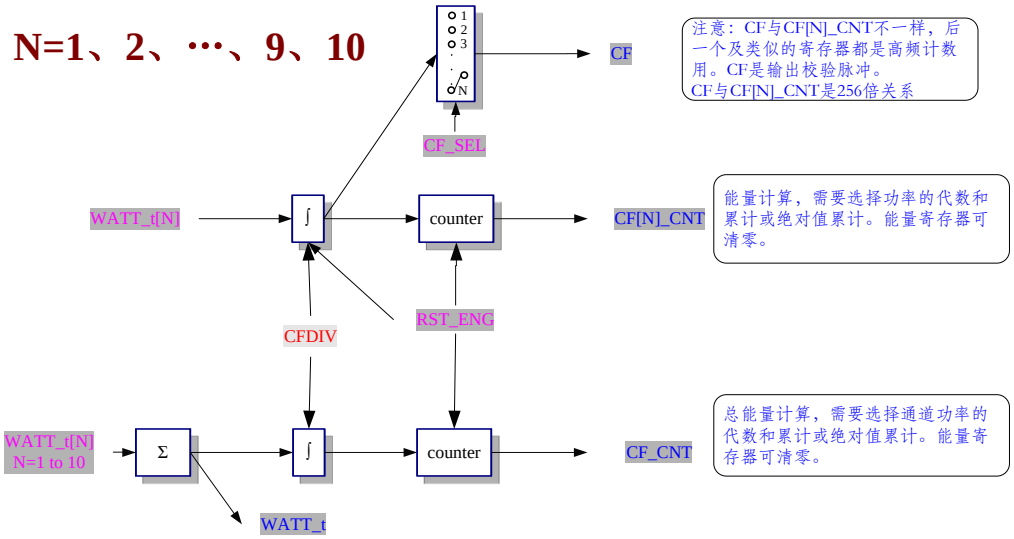
3.3.4 Active Power Small Signal Compensation

For the calculation of active power (fundamental wave and full wave), in order to reduce the noise error in the small signal section, it can be passed to the small signal compensation register to adjust the non-linear error of the small signal section.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
82	WA_LOS[1]/ WA_LOS[2]	R/W	R	24	0x000000	[23:12] Channel 1 active small signal compensation, complement. [11:0] Channel 2 active small signal compensation, complement.
83	WA_LOS[3]/ WA_LOS[4]	R/W	R	24	0x000000	[23:12] Channel 3 active small signal compensation, complement. [11:0] Channel 4 active small signal compensation, complement.
84	WA_LOS[5]/ WA_LOS[6]	R/W	R	24	0x000000	[23:12] Channel 5 active small signal compensation, complement. [11:0] Channel 6 active small signal compensation, complement.
85	WA_LOS[7]/ WA_LOS[8]	R/W	R	24	0x000000	[23:12] Channel 7 active small signal compensation, complement. [11:0] Channel 8 active small signal compensation, complement.
86	WA_LOS[9]/ WA_LOS[10]	R/W	R	24	0x000000	[23:12] Channel 9 active small signal compensation,

						complement. [11:0] Channel 10 active small signal compensation, complement.

3.4 Principle of Active Energy Measurement



Provide 10 channels of energy pulse accumulation. The principle is that the active power of each channel can be integrated for a period of time to obtain the functional energy during this period, and further convert the energy into the corresponding frequency check pulse CF, which uses more electricity and CF frequency just fast, less electricity, and slower CF frequency.

3.4.1 Active Energy Output

Counting CF pulses can obtain energy (power consumption), which is stored in the Nth phase energy accumulation register CF[N]_CNT. The total energy of ten phases is stored in the total energy register CF_CNT, as shown in the figure below.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
2F	CF[1]_CNT	R	W	24	0x000000	Channel 1 active pulse count register, unsigned.
30	CF[2]_CNT	R	W	24	0x000000	Channel 2 active pulse count register, unsigned.

31	CF[3]_CNT	R	W	24	0x000000	Channel 3 active pulse count register, unsigned.
32	CF[4]_CNT	R	W	24	0x000000	Channel 4 active pulse count register, unsigned.
33	CF[5]_CNT	R	W	24	0x000000	Channel 5 active pulse count register, unsigned.
34	CF[6]_CNT	R	W	24	0x000000	Channel 6 active pulse count register, unsigned.
35	CF[7]_CNT	R	W	24	0x000000	Channel 7 active pulse count register, unsigned.
36	CF[8]_CNT	R	W	24	0x000000	Channel 8 active pulse count register, unsigned.
37	CF[9]_CNT	R	W	24	0x000000	Channel 9 active pulse count register, unsigned.
38	CF[10]_CNT	R	W	24	0x000000	Channel 10 active pulse count register, unsigned.
39	CF_CNT	R	W	24	0x000000	Total active pulse count register, unsigned.

3.4.2 Function Output Selection

0x98	MODE3	Working mode register	
No.	Name	Default	Description
[9]	cf_enable	1'b0	0 - CF disable, default; 1 - CF enable.
[13:10]	CF_SEL	4'b0000	channel CF_watt output selection, 0000, CF is closed by default; 0001, channel 1 power CF; 0010, channel 2 power CF; 0011, channel 3 power CF; 0100, channel 4 power CF; 0101, channel 5 power CF; 0110, channel 6 power CF; 0111, channel 7 power CF; 1000, channel 8 power CF;

			1001, channel 9 power CF; 1010, channel 10 power CF; 1011, total active power CF; 1100, reactive power CF (channel optional); 1101, apparent power CF (channel optional); 1110, 1111, close CF; In addition, CF_var is always reactive power CF (channel optional), unchanged.
[15]	cf_add_sel	1'b0	Watt and VAR energy addition methods: 0-absolute value addition; 1-algebraic sum addition.

First set MODE3[9]=1 to select the CF pin to output energy pulses, configure to output CF_watt at M1 and CF_var at M2 respectively, then set CF_SEL to select the calibration pulse output of any channel for calibration.

The cf_add_sel can be used to set how the total energy is added, the algebraic sum or absolute value of each phase is added.

The count results of CF pulses are stored in the CF[N]_CNT register, and the number of pulses can also be directly counted from the CF pin through the I/O interrupt. When the cycle of CF is less than 180ms, it is a pulse with a 50% duty cycle, which is greater than when equal to 180ms, the fixed pulse width is 90ms.

The power conversion formula corresponding to 1 CF is detailed in the register description.

3.4.3 Active Power Output Ratio

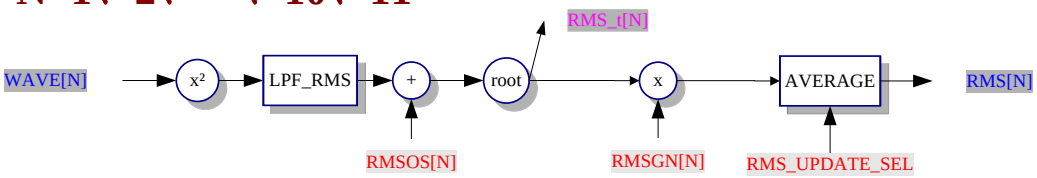
In the energy accumulation, the speed of energy accumulation can be set through the CF_DIV register, each gear is 2 times the relationship, a total of 12 gears. Used for coarse adjustment.

These registers are placed in OTP and can be used for digital calibration or error pre-calibration before leaving the factory.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
CE	CFDIV	R/W	R	12	0x010	CF scaling register.

3.5 The Calculation Principle of the RMS of Current and Voltage

N=1、2、…、10、11



The rms principle of the channel is shown in the figure above. The original waveform of each channel passes through the square circuit (X^2), the rms low-pass filter (LPF_RMS), and the root mean square (ROOT) to obtain the instantaneous value rms_t of the rms, and then average the average value of each channel is the values RMS[N].

3.5.1 RMS Output

The rms calculation result is output and summed to 11 registers. When the channel is in the anti-submarine state, the rms of the channel is not measured.

The conversion formula of voltage rms and current rms is detailed in the register description.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
C	RMS[1]	R	W	24	0x000000	Channel 1 rms register, unsigned.
D	RMS[2]	R	W	24	0x000000	Channel 2 rms register, unsigned.
E	RMS[3]	R	W	24	0x000000	Channel 3 rms register, unsigned.
F	RMS[4]	R	W	24	0x000000	Channel 4 rms register, unsigned.
10	RMS[5]	R	W	24	0x000000	Channel 5 rms register, unsigned.
11	RMS[6]	R	W	24	0x000000	Channel 6 rms register, unsigned.
12	RMS[7]	R	W	24	0x000000	Channel 7 rms register, unsigned.
13	RMS[8]	R	W	24	0x000000	Channel 8 rms register, unsigned.
14	RMS[9]	R	W	24	0x000000	Channel 9 rms register, unsigned.
15	RMS[10]	R	W	24	0x000000	Channel 10 rms register, unsigned.
16	RMS[11]	R	W	24	0x000000	Channel 11 rms register, unsigned.

3.5.2 Setting of RMS Input Signal

Set WAVE_RMS_SEL of MODE2[21:0], you can choose the waveforms for calculating RMS, include full wave, AC full wave and fundamental wave. Full wave waveform is not output through HPF. Through HPF for AC measurement mode, output full wave AC waveform. Through the fundamental LPF as the fundamental wave measurement mode, the fundamental wave waveform is output. Each channel can be set separately.

0x97	MODE2	Working mode register	
No.	Name	Defaults	Description
[21:0]	WAVE_RMS_SEL	11{2'b00}	RMS waveform selection: 00 - AC full wave (default), 01 - fundamental wave, 11 - full wave; [1:0]: 1 channel; [3:2]: 2 channel; [5:4]: 3 channel; [7:6]: 4 channel; [9:8]: 5 channel; [11:10]: 6 channel; [13:12]: 7 channel; [15:14]: 8 channel; [17:16]: 9 channel; [19:18]: 10 channel; [21:20]: 11 channel.

3.5.3 Valid Value Refresh Rate Setting

Set RMS_UPDATE_SEL of MODE2[22], you can choose the rms average refresh time is 525ms or 1.05s, the default is 525ms.

0x97	MODE2	Working mode register	
No.	Name	Defaults	Description
[22]	RMS_UPDATE_SEL	1'b0	Slow rms register update speed selection: 1- 1.05s; 0- 525ms (default).

3.5.4 Current and Voltage RMS Calibration

Contains 11 24-bit rms offset correction registers RMSOS[N] and 11 16-bit rms

gain correction registers RMSGN[N], the default value is 0x0000.

They use the data in the form of 2's complement to calibrate the deviation in the rms calculation. This deviation may come from input noise, because there is a step of square operation in the rms calculation, which may introduce a DC offset caused by noise. Gain and offset correction can make the value in the rms register close to 0 under no load.

The calibration formula is detailed in the register description.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
6C	RMSGN[1]	R/W	R	16	0x0000	Channel 1 rms gain adjustment register.
6D	RMSGN[2]	R/W	R	16	0x0000	Channel 2 rms gain adjustment register.
6E	RMSGN[3]	R/W	R	16	0x0000	Channel 3 rms gain adjustment register.
6F	RMSGN[4]	R/W	R	16	0x0000	Channel 4 rms gain adjustment register.
70	RMSGN[5]	R/W	R	16	0x0000	Channel 5 rms gain adjustment register.
71	RMSGN[6]	R/W	R	16	0x0000	Channel 6 rms gain adjustment register.
72	RMSGN[7]	R/W	R	16	0x0000	Channel 7 rms gain adjustment register.
73	RMSGN[8]	R/W	R	16	0x0000	Channel 8 rms gain adjustment register.
74	RMSGN[9]	R/W	R	16	0x0000	Channel 9 rms gain adjustment register.
75	RMSGN[10]	R/W	R	16	0x0000	Channel 10 rms gain adjustment register.
76	RMSGN[11]	R/W	R	16	0x0000	Channel 11 rms gain adjustment register.
77	RMSOS[1]	R/W	R	24	0x000000	Channel 1 rms offset correction register.

78	RMSOS[2]	R/W	R	24	0x000000	Channel 2 rms offset correction register.
79	RMSOS[3]	R/W	R	24	0x000000	Channel 3 rms offset correction register.
7A	RMSOS[4]	R/W	R	24	0x000000	Channel 4 rms offset correction register.
7B	RMSOS[5]	R/W	R	24	0x000000	Channel 5 rms offset correction register.
7C	RMSOS[6]	R/W	R	24	0x000000	Channel 6 rms offset correction register.
7D	RMSOS[7]	R/W	R	24	0x000000	Channel 7 rms offset correction register.
7E	RMSOS[8]	R/W	R	24	0x000000	Channel 8 rms offset correction register.
7F	RMSOS[9]	R/W	R	24	0x000000	Channel 9 rms offset correction register.
80	RMSOS[10]	R/W	R	24	0x000000	Channel 10 rms offset correction register.
81	RMSOS[11]	R/W	R	24	0x000000	Channel 11 rms offset correction register.

3.5.5 RMS of Anti-Creeping

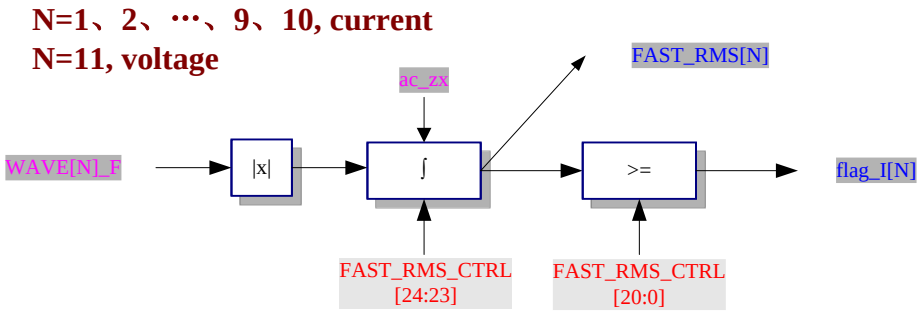
It has a patented rms anti-submarine function to ensure that the rms output is 0 when there is no current input.

The rms anti-creep threshold register (RMS_CREEP) is a 12bit unsigned number, and the default is 0x200. This value is internally expanded by 2 and compared with the absolute value of the input rms signal. When the input rms signal is less than this value, the output is set to zero. This can make the value output to the rms register 0 under no load, even if there is a small noise signal.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
8A	RMS_CREEP	R/W	R	12	0x200	[11:0] is the rms small signal threshold register.

3.6 Principle of Fast Leakage and Overcurrent Detection

The principle of fast rms calculation is shown in the figure below.



11 channels have fast rms registers, which can detect half cycle or cycle rms. This function can be used for leakage or overcurrent detection.

The input waveform is obtained by taking the absolute value and then integrating within the specified time to obtain a fast rms. This value can be compared with a preset threshold, and a flag can be given if it exceeds.

3.6.1 Fast RMS Output

The 11-channel fast rms output register is shown in the figure below.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
17	FAST_RMS[1]	R	W	24	0x000000	Channel 1 fast (leakage current) rms register, unsigned.
18	FAST_RMS[2]	R	W	24	0x000000	Channel 2 fast (leakage current) rms register, unsigned.
19	FAST_RMS[3]	R	W	24	0x000000	Channel 3 fast (leakage current) rms register, unsigned.
1A	FAST_RMS[4]	R	W	24	0x000000	Channel 4 fast (leakage current) rms register, unsigned.
1B	FAST_RMS[5]	R	W	24	0x000000	Channel 5 fast (leakage current) rms register,

						unsigned.
1C	FAST_RMS[6]	R	W	24	0x000000	Channel 6 fast (leakage current) rms register, unsigned.
1D	FAST_RMS[7]	R	W	24	0x000000	Channel 7 fast (leakage current) rms register, unsigned.
1E	FAST_RMS[8]	R	W	24	0x000000	Channel 8 fast (leakage current) rms register, unsigned.
1F	FAST_RMS[9]	R	W	24	0x000000	Channel 9 fast (leakage current) rms register, unsigned.
20	FAST_RMS[10]	R	W	24	0x000000	Channel 10 fast (leakage current) rms register, unsigned.
21	FAST_RMS[11]	R	W	24	0x000000	Channel 11 fast rms register, unsigned.

3.6.2 Fast RMS Input Selection

For the source of the waveform, please refer to the channel waveform block diagram. You can choose to pass HPF or not to pass HPF, the default is not to pass HPF, get WAVE[N]_F. It can also be selected by channel I_f_sel.

0x96	MODE1	Working mode register	
No.	Name	Default	Description
[22]	I_f_sel	1'b0	HPF selection: 0-not use HPF; 1- use HPF.

3.6.3 Fast RMS Accumulation Time and Threshold

To calculate the fast rms, first take the absolute value, and then integrate according to the set cumulative time. Generally, it is an integer multiple of half cycle and cycle time.

Add.	Name	External	Internal	Bits	Defaults	Description

		R/W	R/W			
8B	FAST_RMS_CTRL	R/W	R	24	0x20FFFF	[23:21] Channel fast rms register refresh time, half cycle and N cycle can be selected, the default is one cycle; [20:0] channel fast rms threshold register.

Select the accumulated time by FAST_RMS_CTRL[23:21], which is divided into six types: 000-10ms, 001-20ms, 010-40ms, 011-80ms, 100-160ms, 101-320ms. By default, the cycle cumulative response time is 20ms, and the cumulative time is selected. The longer the accumulated time, the smaller the jump errors.

FAST_RMS_CTRL[20:0] is used to set the fast rms over-limit threshold. Once exceeded, the output FLAG[N] is 1. The flag bit is connected to the output (M1~M10), and the leakage current overcurrent output indicator pin can be pulled directly high.

3.6.4 Grid Frequency Selection

The AC_FREQ_SEL register can distinguish between 50Hz and 60Hz grid applications.

0x97	MODE2	Working mode register	
No.	Name	Default	Description
[23]	AC_FREQ_SEL	1'b0	AC frequency selection, 1- 60Hz, 0- 50Hz (default).

3.6.5 Fast Data Saving of RMS Exceeding Limit

In order to record the amplitude of the fast overload signal, the fast rms exceeding the limit has a save function, and certain setting operations are required to clear the related register FAST_RMS_H[N]. The specific registers are shown in the following table:

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
46	FAST_RMS_H[1]	R	W	24	0x000000	Channel 1 fast (leakage

						current) RMS register, unsigned, hold.
47	FAST_RMS_H[2]	R	W	24	0x000000	Channel 2 fast (leakage current) rms register, unsigned, hold.
48	FAST_RMS_H[3]	R	W	24	0x000000	Channel 3 fast (leakage current) rms register, unsigned, hold.
49	FAST_RMS_H[4]	R	W	24	0x000000	Channel 4 fast (leakage current) rms register, unsigned, hold.
57	FAST_RMS_H[5]	R	W	24	0x000000	Channel 5 fast (leakage current) rms register, unsigned, hold.
58	FAST_RMS_H[6]	R	W	24	0x000000	Channel 6 fast (leakage current) rms register, unsigned, hold.
59	FAST_RMS_H[7]	R	W	24	0x000000	Channel 7 fast (leakage current) rms register, unsigned, hold.
5A	FAST_RMS_H[8]	R	W	24	0x000000	Channel 8 fast (leakage current) rms register, unsigned, hold.
5B	FAST_RMS_H[9]	R	W	24	0x000000	Channel 9 fast (leakage current) rms register, unsigned, hold.
5C	FAST_RMS_H[10]	R	W	24	0x000000	Channel 10 fast (leakage current) rms register, unsigned, hold.

3.6.6 Overcurrent Indication

The overcurrent indication can be controlled by the following registers:

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
91	FLAG_CTRL1	R/W	R	24	0x000000	Overcurrent indication control register 1. [23:10] Disconnect delay timing, 0.1ms/LSB; [9:0] indication control, M10-M1:0-output real-time interrupt; 1-output delay control.
92	FLAG_CTRL2	R/W	R	24	0x000000	Overcurrent indication control register 2. [23:10] Closing delay timer, 0.1ms/LSB; [9:0] Closing control, M10-M1:0-close, 1-open.

3.6.7 Relay Control

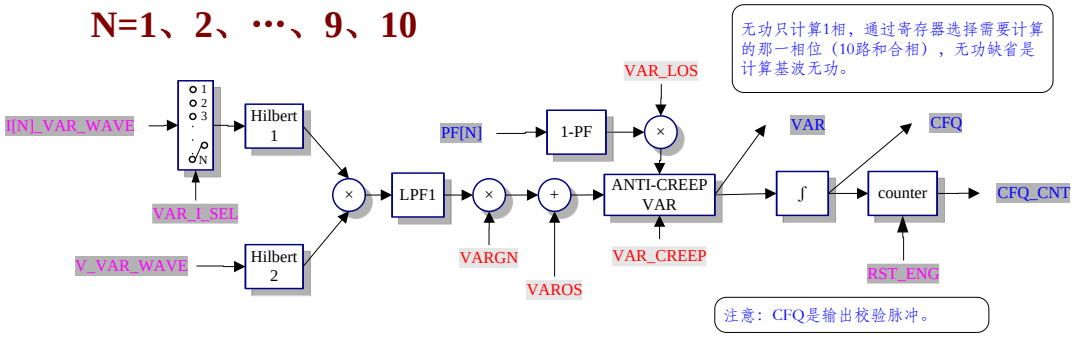
You can also directly control the output level of M1~M10 pins by directly writing the register FLAG_CTRL for relay control:

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
90	FLAG_CTRL	R/W	R	24	0x000000	Overcurrent indication control register. The main control directly controls the level state of M10~M1 output.

Bit[9:0] is the level control of M10~M1 output;

Bit[21:12] is the control priority of M10~M1 output. When the corresponding position is 1, the output level of M10~M1 can be directly controlled by the corresponding bit state of bit[9:0]. Priority to FLAG_CTRL1 and FLAG_CTRL2, FLAG_CTRL has a higher level.

3.7 Principle of Reactive Power Calculation



The principle of reactive power calculation is shown in the figure above. After the current and voltage waveforms pass through the Hilbert filter, digital multiplication is performed, and then the reactive power signal can be obtained after the low-pass filter, gain and deviation calibration, anti-creeping judgment and averaging processing in order. After integration, the amount of pulse accumulation is obtained.

3.7.1 Reactive Power Calculation Input Selection

The input can be multiplied by one of 10 currents and voltages through the VAR_I_SEL register

0x98	MODE3	Working mode register	
No.	Name	Defaults	Description
[3:0]	VAR_I_SEL	4'b000	Select reactive current metering channel, select 1 from 10, default 0000. 0000-channel 1; 0001-channel 2; 0010-channel 3; 0011-channel 4; 0100-channel 5; 0101-channel 6; 0110-channel 7; 0111-channel 8; 1000-channel 9; 1001-channel 10.

3.7.2 Reactive Power Output

The output is only 1 optional channel of reactive power.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
2D	FVAR	R	W	24	0x000000	Optional channel reactive power

						register (fundamental wave).
5D	VAR	R	W	24	0x000000	Optional channel reactive power register (full wave).

3.7.3 Reactive Power Calibration

Contains a 16-bit reactive power offset correction register VAROS and a 16-bit reactive power gain correction register VARGN, the default value is 0x0000.

These registers are placed in OTP and can be used for digital calibration or error pre-calibration before leaving the factory.

They use data in the form of 2's complement to calibrate the deviation in the reactive power calculation. This deviation may come from input noise or phase difference, which may introduce offset and gain errors caused by noise. Gain and deviation correction can be correct the reactive power measurement curve.

Refer to the detailed description of the register for the correction of reactive power.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
CA	VARGN	R/W	R	16	0x0000	Corresponding channel reactive power gain adjustment register, complement.
CB	VAROS	R/W	R	16	0x0000	Corresponding channel reactive power offset adjustment register, complement.

3.7.4 Anti-Creeping of Reactive Power

It has a patented power anti-submarine function to ensure that the power output is 0 when there is no-load.

The reactive power anti-creep threshold register (VAR_CREEP) is a 12-bit unsigned number, and the default is 0x04C. This value is internally expanded by 1 and compared with the absolute value of the input reactive power signal. When the absolute value of the input reactive power signal is less than this value, the output reactive power is set to zero. This can make the value of the output to the reactive power register 0 in the case of reactive power measurement, even if there is a small

noise signal.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
88	VAR_CREEP/ WA_CREEP	R/W	R	24	0x04C04C	[23:12] is the reactive power anti-creeping threshold register ; [11:0] is the active power anti-creeping threshold register.

VAR_CREEP can be set according to the VAR value of the power register, and their corresponding relationship. The anti-submarine value generally takes 20 parts per million to 200 parts per million of the full scale of reactive power.

When the channel is in the anti-submarine state, the power of the channel below the threshold does not participate in the energy accumulation.

3.7.5 Reactive Power Small Signal Compensation

For the calculation of reactive power, in order to reduce the noise error in the small signal section, the small signal compensation register can be passed to the small signal compensation register to adjust the nonlinear error of the small signal section.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
87	FVAR_LOS/ VAR_LOS	R/W	R	24	0x000000	[23:12]is the reactive power small signal compensation register, complement (fundamental wave); [11:0] is the reactive power small signal compensation register, complement (full wave).

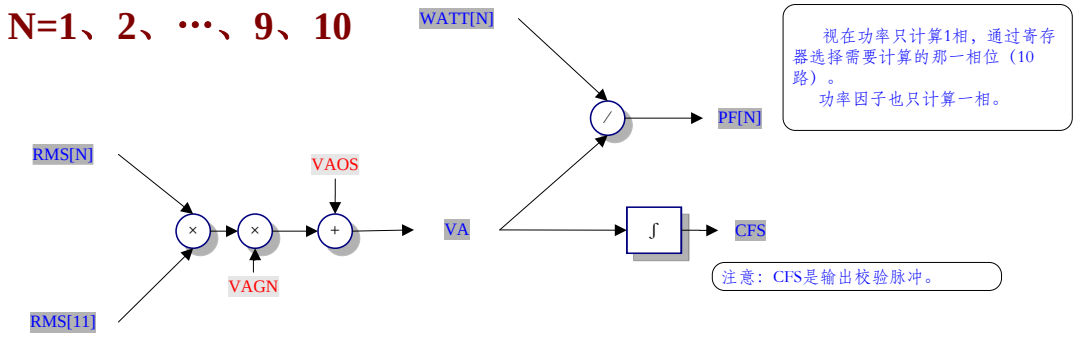
3.7.6 Reactive Energy Output

Reactive energy can be obtained by counting reactive CF pulses, which is stored

in the reactive energy accumulation register CFQ_CNT, as shown in the figure below.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
3A	CFQ_CNT	R	W	24	0x000000	Optional channel reactive pulse count register, unsigned (fundamental wave).

3.8 Principle of Apparent and Power Factor Calculation



See the figure above for the apparent calculation principle. The rms of current and voltage are digitally multiplied, and then the gain and deviation calibration are performed in order to obtain the reactive power signal. After integration, the reactive energy pulse accumulation is obtained. The active power is divided by the apparent power to obtain the power factor.

3.8.1 Apparent Power and Energy Output

The output has only 1 optional channel of apparent power and energy, which is selected by the VAR_I_SEL register, that is, which channel is selected for reactive power and which channel is also selected for apparent power.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
2E	VA	R	W	24	0x000000	Optional channel apparent power register.
3B	CFS_CNT	R	W	24	0x000000	Optional channel apparent pulse count register, unsigned.

3.8.2 Apparent Power Calibration

Contains a 16-bit apparent offset correction register VAOS and a 16-bit apparent gain correction register VAGN, the default value is 0x0000.

These registers are placed in OTP and can be used for digital calibration or error pre-calibration before leaving the factory.

They use 2's complement data to calibrate the deviation in the apparent calculation. This deviation may come from the previous stage, which may introduce offset and gain errors. Gain and deviation correction can correct the apparent measurement curve. The apparent power calibration is detailed in the register description.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
CC	VAGN	R/W	R	16	0x0000	Corresponding channel apparent power gain adjustment register, complement.
CD	VAOS	R/W	R	16	0x0000	Corresponding channel apparent power offset adjustment register, complement.

3.8.3 Power Factor

The output has only 1 optional channel of power factor, which needs to be selected by the VAR_I_SEL register, that is, which channel is selected for reactive power and which channel is selected for power factor.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
4A	PF	R	W	24	0x000000	Optional channel power factor register.

3.9 Temperature Measurement

Provide internal temperature measurement and external temperature measurement. The external and internal temperature measurement readings are

stored in two registers, TPS1 and TPS2, respectively. For the temperature measurement formula, see the detailed description of the register.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
5E	TPS1	R	W	10	0x000000	Internal temperature register.
5F	TPS2	R	W	10	0x000000	External temperature register.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
94	TPS_CTRL	R/W	R	16	0x07FF	Temperature sensor control register. [15] Temperature measurement switch, 1 - temperature measurement is off, 0 - turned on (default); [14] External temperature measurement alarm release switch, 1 - alarm is turned off, 0 - alarm is turned on (default); [13:12] Temperature measurement selection, 00 (default), 01 - selects automatic temperature measurement, 10 - selects internal temperature measurement, 11 - selects external temperature measurement; [11:10] Time interval selection for temperature measurement, 00 - 50ms, 01 - 100ms (default), 10 - 200ms, 11 - 400ms; [9:0] External temperature measurement alarm threshold

						setting, the default setting is 0x3ff.
95	TPS2_A/ TPS2_B	R/W	R	24	0x000000	[23:12]: External temperature sensor coefficient a register; [11:0]: External temperature sensor coefficient b register.

3.10 Electric Parameter Measurement

3.10.1 Line Cycle Measurement

The line cycle energy accumulation calculator includes active and reactive power.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
4B	LINE_ WATTHR	R	W	24	0x000000	Line cycle cumulative active energy register.
4C	LINE_ VARHR	R	W	24	0x000000	Line cycle cumulative reactive energy register.

The number of line cycles can be selected through the LINECYC register.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
8F	SAGLVL/ LINECYC	R/W	R	24	0x100009	[11: 0) Line energy accumulation cycle number register LINECYC, default 0x009, representing 10 cycles.

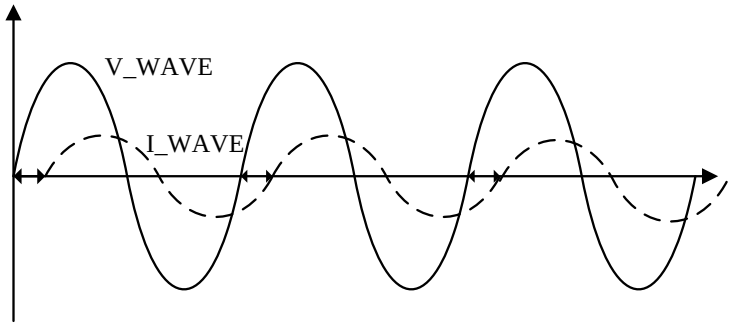
3.10.2 Line Frequency Measurement

Grid frequency detection according to the voltage input channel signal.

The count of the line period recorded in the PERIOD register, if the input signal deviates from 50Hz/60Hz, the corresponding count value will change.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
4E	PERIOD	R	W	20	0x00000	Line voltage frequency register.

3.10.3 Phase Angle Calculation



Phase angle measurement principle, see the figure above. The phase difference is obtained by calculating the time difference between the positive zero-crossing of the current and the voltage, and the corresponding time value is updated to the register ANGLE[N], and each register is a 16-bit unsigned number.

The phase angle conversion formula is detailed in the register description.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
3C	ANGLE[1]	R	W	16	0x0000	Channel 1 current and voltage phase angle register.
3D	ANGLE[2]	R	W	16	0x0000	Channel 2 current and voltage phase angle register.
3E	ANGLE[3]	R	W	16	0x0000	Channel 3 current and voltage phase angle register.
3F	ANGLE[4]	R	W	16	0x0000	Channel 4 current and voltage phase angle register.
40	ANGLE[5]	R	W	16	0x0000	Channel 5 current and voltage phase angle register.
41	ANGLE[6]	R	W	16	0x0000	Channel 6 current and voltage phase angle register.
42	ANGLE[7]	R	W	16	0x0000	Channel 7 current and voltage phase angle register.
43	ANGLE[8]	R	W	16	0x0000	Channel 8 current and voltage phase angle register.
44	ANGLE[9]	R	W	16	0x0000	Channel 9 current and voltage

						phase angle register.
45	ANGLE[10]	R	W	16	0x0000	Channel 10 current and voltage phase angle register.

3.10.4 Power Sign Bit

For each channel power pulse CF output, there is a sign bit register indicating the direction of each CF. This direction indicates the direction of the corresponding accumulated energy (electricity or power supply) from the last CF to the current CF pulse.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
4D	SIGN	R	W	24	0x000000	Power sign bit. Corresponds to the sign bit of the current energy pulse count, refreshed when the CF pulse is output.

SIGN[0] to SIGN[12] correspond to the following CF.

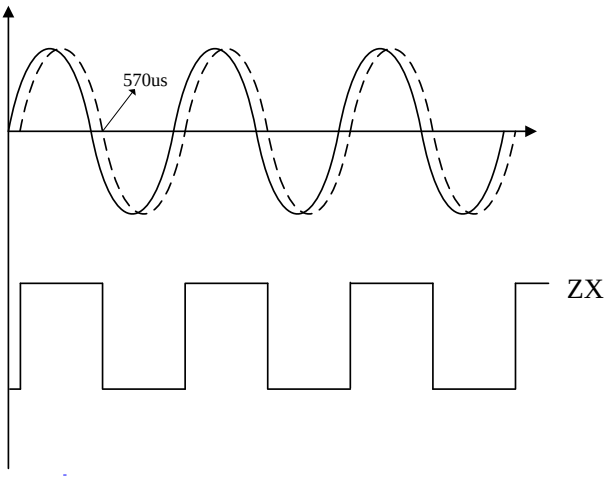
0x4D	SIGN		
position	name	count	description
0	SIGN[0]	CF[1]_CNT	Channel 1 active power pulse CF sign bit.
1	SIGN[1]	CF[2]_CNT	Channel 2 active power pulse CF sign bit.
2	SIGN[2]	CF[3]_CNT	Channel 3 active power pulse CF sign bit.
3	SIGN[3]	CF[4]_CNT	Channel 4 active power pulse CF sign bit.
4	SIGN[4]	CF[5]_CNT	Channel 5 active power pulse CF sign bit.
5	SIGN[5]	CF[6]_CNT	Channel 6 active power pulse CF sign bit.
6	SIGN[6]	CF[7]_CNT	Channel 7 active power pulse CF sign bit.
7	SIGN[7]	CF[8]_CNT	Channel 8 active power pulse CF sign bit.
8	SIGN[8]	CF[9]_CNT	Channel 9 active power pulse CF sign bit.
9	SIGN[9]	CF[10]_CNT	Channel 10 active power pulse CF sign bit.
10	SIGN[10]	CF_CNT	Total active power pulse CF sign bit.
11	SIGN[11]	CFQ_CNT	Optional reactive power pulse CFQ sign bit.
12	SIGN[12]	CFS_CNT	Optional apparent power pulse CFS sign bit.

3.11 Fault Detection

3.11.1 Zero-crossing Detection

Provide voltage zero-crossing detection. The zero-crossing signal is directly output from the pin ZX. ZX is zero to indicate the positive half cycle of the waveform, and ZX is 1 to indicate the negative half cycle of the waveform. The delay from the actual input signal is about 570us.

The output zero-crossing signal mainly assists in turning off the relay at the zero-crossing point to reduce relay adhesion.



3.11.2 Peak Overrun

The threshold value of the rms of current and voltage can be set by programming, which is set by the peak threshold register (I_PKLVL, V_PKLVL).

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
8C	I_PKLVL/ V_PKLVL	R/W	R	24	0xFFFFFF	[23:12] Current peak value threshold register; [11:0] Voltage peak value threshold register.

For example, when the fast rms of channel 1 current is greater than the threshold set by the current peak threshold register (I_PKLVL), the current overload indication PK01 is given. If the corresponding PK01 enable position in the interrupt mask register (MASK1) is logic 1, then the /IRQ logic output becomes active low.

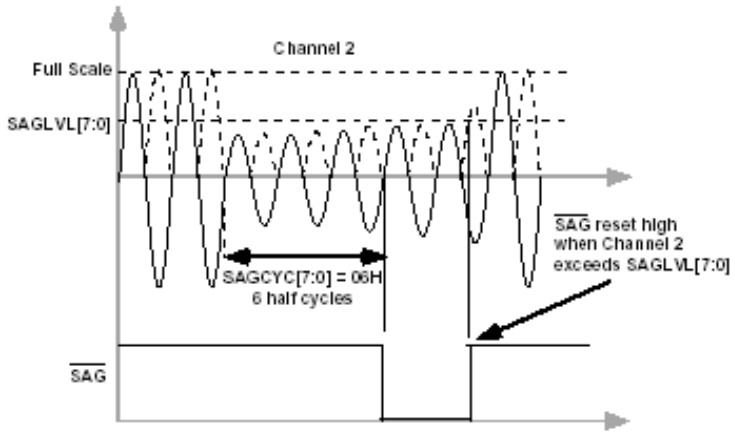
Similarly, when the fast rms of channel 2~10 current is greater than the threshold set by the current peak threshold register (I_PKLVL), the current overload indication PK02~PK10 is given, if any of the corresponding PK02~PK10 in the interrupt mask register (MASK1) is enabled the position is logic 1, then the /IRQ logic output becomes active low.

Similarly, when the voltage fast rms is greater than the threshold set by the voltage peak threshold register (V_PKLVL), a voltage overload indication is given. If the corresponding PKV enable position in the interrupt mask register (MASK1) is logic 1, then the /IRQ logic output becomes active low.

0x96	STATUS1		
position	Interrupt flag	Defaults	description
13	PK01	0	Channel 1 overcurrent signal
14	PK02	0	Channel 2 overcurrent signal
15	PK03	0	Channel 3 overcurrent signal
16	PK04	0	Channel 4 overcurrent signal
17	PK05	0	Channel 5 overcurrent signal
18	PK06	0	Channel 6 overcurrent signal
19	PK07	0	Channel 7 overcurrent signal
20	PK08	0	Channel 8 overcurrent signal
21	PK09	0	Channel 9 overcurrent signal
22	PK10	0	Channel 10 overcurrent signal
23	PKV	0	Overvoltage signal

3.11.3 Line Voltage Drop

It can be indicated by programming. When the rms of the line voltage is lower than a certain peak value for more than a certain number of half cycles, an indication of the line voltage drop is given.



As shown in the figure above, when the rms of the voltage is less than the threshold set in the drop voltage threshold register (SAGLVL) and the drop time exceeds the set time in the drop line cycle register (SAGCYC) (the figure shows that after the sixth half cycle is exceeded, SAGCYC[11:0] = 06h), the line voltage drop event is recorded by setting the /SAG flag bit in the interrupt status STATUS1 register.

0x96	STATUS1		
position	Interrupt flag	Defaults	description
0	/SAG	0	Line voltage drop

If the corresponding /SAG enable position in the interrupt mask register (MASK1) is logic 1, the /IRQ logic output becomes active low.

The drop voltage threshold register (SAGLVL) can be written or read by the user, and the initial value is 04H. The drop line period register (SAGCYC) can also be written or read by the user, and the initial value is 100H. The resolution of this register is 10ms/LSB, the maximum delay time of such an interrupt is limited to 2.55s.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
8E	SAGCYC/ ZXTOUT	R/W	R	24	0x04FFFF	[23:16] Drop line period register SAGCYC, default 04h.
8F	SAGLVL/ LINECYC	R/W	R	24	0x100009	[23:12] Drop voltage threshold register SAGLVL, the voltage channel input is continuously lower than the value of this register for more than the time in SAGCYC, a line voltage

						drop interrupt will be generated, default 100h, about 1/16 full amplitude voltage input.

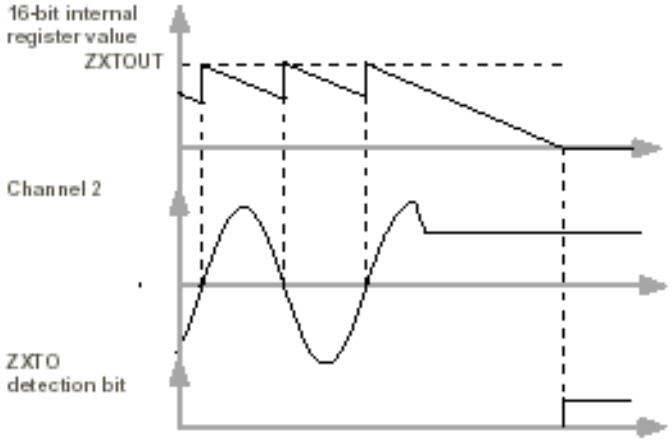
3.11.4 Zero-crossing Timeout

The zero-crossing detection circuit is also connected to a register ZXTOUT that detects the zero-crossing signal timeout, and ZXTOUT is set to the initial value whenever there is a zero-crossing signal in the detection voltage channel. If there is no zero-crossing signal, it will decrement. When the zero-crossing signal is output, the value in this register will become 0. At this time, the corresponding bit ZXTO in the interrupt status register is set to 1. If the corresponding enable bit ZXTO in the interrupt mask register is also 1, the zero-crossing signal timeout events are also reflected on the interrupt pin /IRQ. Regardless of whether the corresponding enable bit in the interrupt register is set or not, the ZXTO flag bit in the interrupt status register (MASK) is always set to be valid when the ZXTOUT register is reduced to 0.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
8E	SAGCYC/ ZXTOUT	R/W	R	24	0x04FFFF	[15:0] Zero-crossing timeout register ZXTOUT, if there is no zero-crossing signal within the time indicated by this register, a zero-crossing timeout interrupt will be generated, default FFFFH.

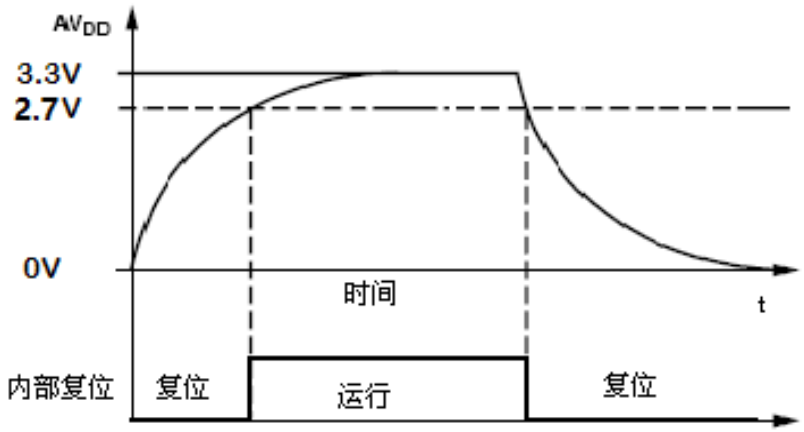
The zero-crossing timeout register ZXTOUT can be written or read by the user, the initial value is FFFFH. The resolution of this register is 70.5us/LSB, so the maximum delay time of an interrupt is limited to 4.369s.

The following figure shows the mechanism of detecting zero-crossing timeout when the line voltage is always a fixed DC signal:



3.11.5 Power Supply Indication

Contain an on-chip power monitor circuit that can continuously detect analog power (AVDD). If the power supply voltage is less than 2.7v±5%, the entire circuit is not activated (not working), that is to say, when the power supply voltage is less than 2.7v, it is not performed Energy accumulation. This approach can ensure that the device maintains correct operation when the power is powered on. This power monitoring circuit has a hysteresis and filtering mechanism, which can eliminate false triggers caused by noise to a large extent. Generally, the power supply The decoupling part of the power supply should ensure that the ripple on AVDD does not exceed 3.3v ± 5%.



片内电源供电监视

4、 REGISTERS

4.1 Electrical Parameter Register (Internal Write)

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
Electrical parameter register (Internal writing)						
1	WAVE[1]	R	W	24	0x000000	Channel 1 waveform register (normal current and leakage current are optional).
2	WAVE[2]	R	W	24	0x000000	Channel 2 waveform register (normal current and leakage current optional).
3	WAVE[3]	R	W	24	0x000000	Channel 3 waveform register (normal current and leakage current optional).
4	WAVE[4]	R	W	24	0x000000	Channel 4 waveform register (normal current and leakage current optional).
5	WAVE[5]	R	W	24	0x000000	Channel 5 waveform register (normal current and leakage current are optional).
6	WAVE[6]	R	W	24	0x000000	Channel 6 waveform register (normal current and leakage current optional).
7	WAVE[7]	R	W	24	0x000000	Channel 7 waveform register (normal current and leakage current optional).

8	WAVE[8]	R	W	24	0x000000	Channel 8 waveform register (normal current and leakage current optional).
9	WAVE[9]	R	W	24	0x000000	Channel 9 waveform register (normal current and leakage current optional).
A	WAVE[10]	R	W	24	0x000000	Channel 10 waveform register (normal current and leakage current optional).
B	WAVE[11]	R	W	24	0x000000	Channel 11 waveform register.
C	RMS[1]	R	W	24	0x000000	Channel 1 rms register, unsigned.
D	RMS[2]	R	W	24	0x000000	Channel 2 rms register, unsigned.
E	RMS[3]	R	W	24	0x000000	Channel 3 rms register, unsigned.
F	RMS[4]	R	W	24	0x000000	Channel 4 rms register, unsigned.
10	RMS[5]	R	W	24	0x000000	Channel 5 rms register, unsigned.
11	RMS[6]	R	W	24	0x000000	Channel 6 rms register, unsigned.
12	RMS[7]	R	W	24	0x000000	Channel 7 rms register, unsigned.
13	RMS[8]	R	W	24	0x000000	Channel 8 rms register, unsigned.
14	RMS[9]	R	W	24	0x000000	Channel 9 rms register, unsigned.
15	RMS[10]	R	W	24	0x000000	Channel 10 rms register, unsigned.

16	RMS[11]	R	W	24	0x000000	Channel 11 rms register, unsigned.
17	FAST_RMS[1]	R	W	24	0x000000	Channel 1 fast (leakage current) rms register, unsigned.
18	FAST_RMS[2]	R	W	24	0x000000	Channel 2 fast (leakage current) rms register, unsigned.
19	FAST_RMS[3]	R	W	24	0x000000	Channel 3 fast (leakage current) rms register, unsigned.
1A	FAST_RMS[4]	R	W	24	0x000000	Channel 4 fast (leakage current) rms register, unsigned.
1B	FAST_RMS[5]	R	W	24	0x000000	Channel 5 fast (leakage current) rms register, unsigned.
1C	FAST_RMS[6]	R	W	24	0x000000	Channel 6 fast (leakage current) rms register, unsigned.
1D	FAST_RMS[7]	R	W	24	0x000000	Channel 7 fast (leakage current) rms register, unsigned.
1E	FAST_RMS[8]	R	W	24	0x000000	Channel 8 fast (leakage current) rms register, unsigned.
1F	FAST_RMS[9]	R	W	24	0x000000	Channel 9 fast (leakage current) rms register, unsigned.
20	FAST_RMS[10]	R	W	24	0x000000	Channel 10 fast (leakage current) rms register, unsigned.
21	FAST_RMS[11]	R	W	24	0x000000	Channel 11 fast (leakage current) rms register,

						unsigned.
22	WATT[1]	R	W	24	0x000000	Channel 1 active power register.
23	WATT[2]	R	W	24	0x000000	Channel 2 active power register.
24	WATT[3]	R	W	24	0x000000	Channel 3 active power register.
25	WATT [4]	R	W	24	0x000000	Channel 4 active power register.
26	WATT [5]	R	W	24	0x000000	Channel 5 active power register.
27	WATT [6]	R	W	24	0x000000	Channel 6 active power register.
28	WATT [7]	R	W	24	0x000000	Channel 7 active power register.
29	WATT [8]	R	W	24	0x000000	Channel 8 active power register.
2A	WATT [9]	R	W	24	0x000000	Channel 9 active power register.
2B	WATT [10]	R	W	24	0x000000	Channel 10 active power register.
2C	WATT	R	W	24	0x000000	Total active power register.
2D	VAR	R	W	24	0x000000	Optional channel reactive power register (fundamental wave).
2E	VA	R	W	24	0x000000	Optional channel apparent power register.
2F	CF[1]_CNT	R	W	24	0x000000	Channel 1 active pulse count register, unsigned.
30	CF[2]_CNT	R	W	24	0x000000	Channel 2 active pulse count register, unsigned.
31	CF[3]_CNT	R	W	24	0x000000	Channel 3 active pulse count register, unsigned.

32	CF[4]_CNT	R	W	24	0x000000	Channel 4 active pulse count register, unsigned.
33	CF[5]_CNT	R	W	24	0x000000	Channel 5 active pulse count register, unsigned.
34	CF[6]_CNT	R	W	24	0x000000	Channel 6 active pulse count register, unsigned.
35	CF[7]_CNT	R	W	24	0x000000	Channel 7 active pulse count register, unsigned.
36	CF[8]_CNT	R	W	24	0x000000	Channel 8 active pulse count register, unsigned.
37	CF[9]_CNT	R	W	24	0x000000	Channel 9 active pulse count register, unsigned.
38	CF[10]_CNT	R	W	24	0x000000	Channel 10 active pulse count register, unsigned.
39	CF_CNT	R	W	24	0x000000	Total active pulse count register, unsigned.
3A	CFQ_CNT	R	W	24	0x000000	Optional channel reactive pulse count register, unsigned (fundamental wave).
3B	CFS_CNT	R	W	24	0x000000	Optional channel apparent pulse count register, unsigned.
3C	ANGLE[1]	R	W	16	0x0000	Channel 1 current and voltage phase angle register.
3D	ANGLE[2]	R	W	16	0x0000	Channel 2 current and voltage phase angle register.
3E	ANGLE[3]	R	W	16	0x0000	Channel 3 current and voltage phase angle register.
3F	ANGLE[4]	R	W	16	0x0000	Channel 4 current and voltage phase angle

						register.
40	ANGLE[5]	R	W	16	0x0000	Channel 5 current and voltage phase angle register.
41	ANGLE[6]	R	W	16	0x0000	Channel 6 current and voltage phase angle register.
42	ANGLE[7]	R	W	16	0x0000	Channel 7 current and voltage phase angle register.
43	ANGLE[8]	R	W	16	0x0000	Channel 8 current and voltage phase angle register.
44	ANGLE[9]	R	W	16	0x0000	Channel 9 current and voltage phase angle register.
45	ANGLE[10]	R	W	16	0x0000	Channel 10 current and voltage phase angle register.
46	FAST_RMS_H[1]	R	W	24	0x000000	Channel 1 fast (leakage current) rms register, unsigned, hold.
47	FAST_RMS_H[2]	R	W	24	0x000000	Channel 2 fast (leakage current) rms register, unsigned, hold.
48	FAST_RMS_H[3]	R	W	24	0x000000	Channel 3 fast (leakage current) rms register, unsigned, hold.
49	FAST_RMS_H[4]	R	W	24	0x000000	Channel 4 fast (leakage current) rms register, unsigned, hold.
4A	PF	R	W	24	0x000000	Optional channel power factor register.
4B	LINE_ WATTHR	R	W	24	0x000000	Line cycle cumulative

						active energy register.
4C	LINE_ VARHR	R	W	24	0x000000	Line cycle cumulative reactive energy register.
4D	SIGN	R	W	24	0x000000	Power sign bit register. Corresponds to the sign bit of the current energy pulse count, refreshed when the CF pulse is output.
4E	PERIOD	R	W	20	0x000000	Line voltage frequency register.
54	STATUS1	R	W	24	0x000000	Interrupt status register 1, unsigned.
56	STATUS3	R	W	10	0x000	M status register, unsigned.
57	FAST_RMS_H[5]	R	W	24	0x000000	Channel 5 fast (leakage current) rms register, unsigned, hold.
58	FAST_RMS_H[6]	R	W	24	0x000000	Channel 6 fast (leakage current) rms register, unsigned, hold.
59	FAST_RMS_H[7]	R	W	24	0x000000	Channel 7 fast (leakage current) rms register, unsigned, hold.
5A	FAST_RMS_H[8]	R	W	24	0x000000	Channel 8 fast (leakage current) rms register, unsigned, hold.
5B	FAST_RMS_H[9]	R	W	24	0x000000	Channel 9 fast (leakage current) rms register, unsigned, hold.
5C	FAST_RMS_H[10]	R	W	24	0x000000	Channel 10 fast (leakage current) rms register, unsigned, hold.
5D	VAR	R	W	24	0x000000	Optional channel (full

						wave) reactive power register.
5E	TPS1	R	W	10	0x000000	Internal temperature value register.
5F	TPS2	R	W	10	0x000000	External temperature value register.

4.2 Calibration Register (External Write)

User operation register (External write)						
Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
60	GAIN1	R/W	R	24	0x000000	Channel PGA gain adjustment register, 0000=1； 0001=2； 0010=8； 0011=16.
61	GAIN2	R/W	R	20	0x00000	Channel PGA gain adjustment register, 0000=1； 0001=2； 0010=8； 0011=16.
64	PHASE[1]/ PHASE[2]	R/W	R	16	0x0000	[15:8] Channel 1 phase correction register. [7:0] Channel 2 phase correction register.
65	PHASE[3]/ PHASE[4]	R/W	R	16	0x0000	[15:8] Channel 3 phase correction register. [7:0] Channel 4 phase correction register.
66	PHASE[5]/ PHASE[6]	R/W	R	16	0x0000	[15:8] Channel 5 phase correction register. [7:0] Channel 6 phase correction register.
67	PHASE[7]/ PHASE[8]	R/W	R	16	0x0000	[15:8] Channel 7 phase correction register.

						[7:0] Channel 8 phase correction register.
68	PHASE[9]/ PHASE[10]	R/W	R	16	0x0000	[15:8] Channel 9 phase correction register. [7:0] Channel 10 phase correction register.
69	PHASE[11]	R/W	R	8	0x00	[7:0] Voltage channel phase correction register.
6A	VAR_ PHCAL_I	R/W	R	5	0x0000	Current channel reactive phase correction register.
6B	VAR_ PHCAL_V	R/W	R	5	0x0000	Voltage channel reactive phase correction register.
6C	RMSGN[1]	R/W	R	16	0x0000	Channel 1 rms gain adjustment register.
6D	RMSGN[2]	R/W	R	16	0x0000	Channel 2 rms gain adjustment register.
6E	RMSGN[3]	R/W	R	16	0x0000	Channel 3 rms gain adjustment register.
6F	RMSGN[4]	R/W	R	16	0x0000	Channel 4 rms gain adjustment register.
70	RMSGN[5]	R/W	R	16	0x0000	Channel 5 rms gain adjustment register.
71	RMSGN[6]	R/W	R	16	0x0000	Channel 6 rms gain adjustment register.
72	RMSGN[7]	R/W	R	16	0x0000	Channel 7 rms gain adjustment register.
73	RMSGN[8]	R/W	R	16	0x0000	Channel 8 rms gain adjustment register.
74	RMSGN[9]	R/W	R	16	0x0000	Channel 9 rms gain adjustment register.
75	RMSGN[10]	R/W	R	16	0x0000	Channel 10 rms gain adjustment register.
76	RMSGN[11]	R/W	R	16	0x0000	Channel 11 rms gain adjustment register.

77	RMSOS[1]	R/W	R	24	0x000000	Channel 1 rms offset correction register.
78	RMSOS[2]	R/W	R	24	0x000000	Channel 2 rms offset correction register.
79	RMSOS[3]	R/W	R	24	0x000000	Channel 3 rms offset correction register.
7A	RMSOS[4]	R/W	R	24	0x000000	Channel 4 rms offset correction register.
7B	RMSOS[5]	R/W	R	24	0x000000	Channel 5 rms offset correction register.
7C	RMSOS[6]	R/W	R	24	0x000000	Channel 6 rms offset correction register.
7D	RMSOS[7]	R/W	R	24	0x000000	Channel 7 rms offset correction register.
7E	RMSOS[8]	R/W	R	24	0x000000	Channel 8 rms offset correction register.
7F	RMSOS[9]	R/W	R	24	0x000000	Channel 9 rms offset correction register.
80	RMSOS[10]	R/W	R	24	0x000000	Channel 10 rms offset correction register.
81	RMSOS[11]	R/W	R	24	0x000000	Channel 11 rms offset correction register.
82	WA_LOS[1]/ WA_LOS[2]	R/W	R	24	0x000000	[23:12] Channel 1 active small signal compensation register, complement. [11:0] Channel 2 active small signal compensation register, complement.
83	WA_LOS[3]/ WA_LOS[4]	R/W	R	24	0x000000	[23:12] Channel 3 active small signal compensation register, complement. [11:0] Channel 4 active small signal compensation register, complement.

84	WA_LOS[5]/ WA_LOS[6]	R/W	R	24	0x000000	[23:12] Channel 5 active small signal compensation register, complement. [11:0] Channel 6 active small signal compensation register, complement.
85	WA_LOS[7]/ WA_LOS[8]	R/W	R	24	0x000000	[23:12] Channel 7 active small signal compensation register, complement. [11:0] Channel 8 active small signal compensation register, complement.
86	WA_LOS[9]/ WA_LOS[10]	R/W	R	24	0x000000	[23:12] Channel 9 active small signal compensation register, complement. [11:0] Channel 10 active small signal compensation register, complement.
87	FVAR_LOS/ VAR_LOS	R/W	R	24	0x000000	[23:12]is the reactive power small signal compensation register, complement (fundamental wave); [11:0] is the reactive power small signal compensation register, complement (full wave).
88	VAR_CREEP/ WA_CREEP	R/W	R	24	0x04C04C	[23:12] is the reactive power anti-creeping threshold register; [11:0] is the active power anti-creeping threshold register.
89	WA_CREEP2	R/W	R	12	0x000	[11:0] Total active anti-creep threshold register.

8A	RMS_CREEP	R/W	R	12	0x200	[11:0] is the rms small signal threshold register.
8B	FAST_RMS _CTRL	R/W	R	24	0x20FFFF	[23:21] Channel fast rms register refresh time, half cycle and N cycle can be selected, the default is one cycle; [20:0] channel fast rms threshold register.
8C	I_PKLVL/ V_PKLVL	R/W	R	24	0xFFFFFF	[23:12] Current peak value threshold register; [11:0] Voltage peak value threshold register.
8E	SAGCYC/ ZXTOUT	R/W	R	24	0x04FFFF	[23:16] Fall line period register SAGCYC, default 04h; [15:0] Zero-crossing timeout register ZXTOUT, if there is no zero-crossing signal within the time indicated by this register, a zero-crossing timeout interrupt will be generated, default FFFFh.
8F	SAGLVL/ LINECYC	R/W	R	24	0x100009	[23:12] Drop voltage threshold register SAGLVL, the voltage channel input is continuously lower than the value of this register for more than the time in SAGCYC, a line voltage drop interrupt will be generated, default 100h, about 1/16 full amplitude voltage input; [11: 0) Line energy accumulation cycle number

						register LINECYC, default 009h, representing 10 cycles.
90	FLAG_CTRL	R/W	R	24	0x000000	Overcurrent indication control register. The main control directly controls the level state of M10~M1 output.
91	FLAG_CTRL1	R/W	R	24	0x000000	Overcurrent indication control register 1. [23:10] Disconnect delay timing, 0.1msslsb; [9:0] indication control, M10-M1:0-output real-time interrupt; 1-output delay control.
92	FLAG_CTRL2	R/W	R	24	0x000000	Overcurrent indication control register 2. [23:10] Closing delay timer, 0.1msslsb; [9:0] Closing control, M10-M1:0-close, 1-open.
93	ADC_PD	R/W	R	11	0x000	Enable control of 11 channels ADC register. ADC_PD<0> controls the voltage channel; ADC_PD<10:1> controls the corresponding current channel 10 to current channel 1.
94	TPS_CTRL	R/W	R	16	0x07FF	Temperature sensor control register. [15] Temperature measurement switch, 1 - temperature measurement is off, 0 - turned on (default); [14] External temperature

						measurement alarm release switch, 1 - alarm is turned off, 0 - alarm is turned on (default); [13:12] Temperature measurement selection, 00 (default), 01 - selects automatic temperature measurement, 10 - selects internal temperature measurement, 11 - selects external temperature measurement; [11:10] Time interval selection for temperature measurement, 00 - 50ms, 01 - 100ms (default), 10 - 200ms, 11 - 400ms; [9:0] External temperature measurement alarm threshold setting, the default setting is 0x3ff.
95	TPS2_A/ TPS2_B	R/W	R	24	0x000000	[23:12]: External temperature sensor coefficient a register; [11:0]: External temperature sensor coefficient b register.
96	MODE1	R/W	R	24	0x000000	User mode selection register 1.
97	MODE2	R/W	R	24	0x000000	User mode selection register 2.
98	MODE3	R/W	R	24	0x000000	User mode selection register 3.
9A	MASK1	R/W	R	24	0x000000	Interrupt mask register 1, which controls whether an

						interrupt generates a valid /IRQ1 output, see "Interrupt Mask Register" description for details.
9B	MASK2	R/W	R	24	0x000000	Interrupt mask register 2, which controls whether an interrupt generates a valid /IRQ2 output, see "Interrupt Mask Register" description for details.
9D	RST_ENG	R/W	R	24	0x000000	Clear the setting register after reading the energy pulse.
9E	WRPROT	R/W	R	16	0x0000	User write protection setting register, when 5555H is written, it means that the user register can be operated from reg60 to reg9d and rega0 to regd0.
9F	SOFT _RESET	R/W	R	24	0x000000	When the input is 5A5A5A, the system is reset, only the state machine and registers of the digital part are reset! When the input is 55AA55, the user read and write registers are reset. Reset: reg60 to reg9f and rega0 to regd0.

4.3 OTP Register

Calibration register (write externally, save internal OTP)						
Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
A0	CHGN[1]	R/W	R	16	0x0000	Channel 1 gain adjustment register, complement.

A1	CHGN[2]	R/W	R	16	0x0000	Channel 2 gain adjustment register, complement.
A2	CHGN[3]	R/W	R	16	0x0000	Channel 3 gain adjustment register, complement.
A3	CHGN[4]	R/W	R	16	0x0000	Channel 4 gain adjustment register, complement.
A4	CHGN[5]	R/W	R	16	0x0000	Channel 5 gain adjustment register, complement.
A5	CHGN[6]	R/W	R	16	0x0000	Channel 6 gain adjustment register, complement.
A6	CHGN[7]	R/W	R	16	0x0000	Channel 7 gain adjustment register, complement.
A7	CHGN[8]	R/W	R	16	0x0000	Channel 8 gain adjustment register, complement.
A8	CHGN[9]	R/W	R	16	0x0000	Channel 9 gain adjustment register, complement.
A9	CHGN[10]	R/W	R	16	0x0000	Channel 10 gain adjustment register, complement.
AA	CHGN[11]	R/W	R	16	0x0000	Channel 11 gain adjustment register, complement.
AB	CHOS[1]	R/W	R	16	0x0000	Channel 1 offset adjustment register, complement.
AC	CHOS[2]	R/W	R	16	0x0000	Channel 2 offset adjustment register, complement.
AD	CHOS[3]	R/W	R	16	0x0000	Channel 3 offset adjustment register, complement.
AE	CHOS[4]	R/W	R	16	0x0000	Channel 4 offset adjustment register, complement.
AF	CHOS[5]	R/W	R	16	0x0000	Channel 5 offset adjustment register, complement.
B0	CHOS[6]	R/W	R	16	0x0000	Channel 6 offset adjustment register, complement.
B1	CHOS[7]	R/W	R	16	0x0000	Channel 7 offset adjustment register, complement.

B2	CHOS[8]	R/W	R	16	0x0000	Channel 8 offset adjustment register, complement.
B3	CHOS[9]	R/W	R	16	0x0000	Channel 9 offset adjustment register, complement.
B4	CHOS[10]	R/W	R	16	0x0000	Channel 10 offset adjustment register, complement.
B5	CHOS[11]	R/W	R	16	0x0000	Channel 11 offset adjustment register, complement.
B6	WATTGN[1]	R/W	R	16	0x0000	Channel 1 active power gain adjustment register, complement.
B7	WATTGN[2]	R/W	R	16	0x0000	Channel 2 active power gain adjustment register, complement.
B8	WATTGN[3]	R/W	R	16	0x0000	Channel 3 active power gain adjustment register, complement.
B9	WATTGN[4]	R/W	R	16	0x0000	Channel 4 active power gain adjustment register, complement.
BA	WATTGN[5]	R/W	R	16	0x0000	Channel 5 active power gain adjustment register, complement.
BB	WATTGN[6]	R/W	R	16	0x0000	Channel 6 active power gain adjustment register, complement.
BC	WATTGN[7]	R/W	R	16	0x0000	Channel 7 active power gain adjustment register, complement.
BD	WATTGN[8]	R/W	R	16	0x0000	Channel 8 active power gain adjustment register, complement.
BE	WATTGN[9]	R/W	R	16	0x0000	Channel 9 active power gain adjustment register,

						complement.
BF	WATTGN[10]	R/W	R	16	0x0000	Channel 10 active power gain adjustment register, complement.
C0	WATTOS[1]	R/W	R	16	0x0000	Channel 1 active power offset adjustment register, complement.
C1	WATTOS[2]	R/W	R	16	0x0000	Channel 2 active power offset adjustment register, complement.
C2	WATTOS[3]	R/W	R	16	0x0000	Channel 3 active power offset adjustment register, complement.
C3	WATTOS[4]	R/W	R	16	0x0000	Channel 4 active power offset adjustment register, complement.
C4	WATTOS[5]	R/W	R	16	0x0000	Channel 5 active power offset adjustment register, complement.
C5	WATTOS[6]	R/W	R	16	0x0000	Channel 6 active power offset adjustment register, complement.
C6	WATTOS[7]	R/W	R	16	0x0000	Channel 7 active power offset adjustment register, complement.
C7	WATTOS[8]	R/W	R	16	0x0000	Channel 8 active power offset adjustment register, complement.
C8	WATTOS[9]	R/W	R	16	0x0000	Channel 9 active power offset adjustment register, complement.
C9	WATTOS[10]	R/W	R	16	0x0000	Channel 10 active power offset adjustment register, complement.

CA	VARGN	R/W	R	16	0x0000	Corresponding channel reactive power gain adjustment register, complement.
CB	VAROS	R/W	R	16	0x0000	Corresponding channel reactive power offset adjustment register, complement.
CC	VAGN	R/W	R	16	0x0000	Corresponding channel apparent power gain adjustment register, complement.
CD	VAOS	R/W	R	16	0x0000	Corresponding channel apparent power offset adjustment register, complement.
CE	CFDIV	R/W	R	16	0x0010	CF scaling register [11:0], reserved [15:12].
CF	RESERVE0	R/W	R	16	0x0000	Keep.
D0	OTP checksum1	R/W	R	16	0x0000	OTP register checksum, checksum1 has a problem and restores to 0 to rega0 to regd0.

4.4 Mode Register

4.4.1 Mode Register 1 (MODE1)

0x96	MODE1	Working mode register	
No.	Name	Defaults	Description
[21:0]	RESERVE		
[22]	L_F_SEL	1'b0	Leakage selection through high pass, the default is 0 to select no high pass, and 1 to select high pass.

[23]	WAVE_REG_SEL	1'b0	Current wave waveform register output selection, default 0 selects the waveform of the normal current channel, and 1 selects the waveform output of the leakage channel.

4.4.2 Mode Register 2 (MODE2)

0x97	MODE2	Working mode register	
No.	Name	Defaults	Description
[21:0]	WAVE_RMS_SEL	11{2'b00}	RMS waveform selection, 00-high pass, 01-select fundamental wave, 11-select full wave.
[22]	RMS_UPDATE_SEL	1'b0	Slow rms register update speed selection, 1 - 1.05s, 0 - 525ms (default).
[23]	AC_FREQ_SEL	1'b0	AC frequency selection, 1 - 60Hz, 0 - 50Hz (default).

4.4.3 Mode Register 3 (MODE3)

0x98	MODE3	Working mode register	
No.	Name	Defaults	Description
[3:0]	VAR_I_SEL	4'b000	Select reactive current metering channel, select 1 from 10, default 0000. 0000，channel 1；0001，channel 2 0010，channel 3；0011，channel 4 0100，channel 5；0101，channel 6 0110，channel 7；0111，channel 8 1000，channel 9；1001，channel 10
[8]	add_sel	1'b0	Watt sum addition method: 0- absolute value addition; 1- algebraic sum addition.
[9]	CF_enable	1'b0	0- CF disable, default; 1- CF enable and output at M2 and M3.
[13:10]	CF_SEL	4'b0000	channel CF_watt output selection, 0000, CF is closed by default;

			0001, channel 1 power CF; 0010, channel 2 power CF; 0011, channel 3 power CF; 0100, channel 4 power CF; 0101, channel 5 power CF; 0110, channel 6 power CF; 0111, channel 7 power CF; 1000, channel 8 power CF; 1001, channel 9 power CF; 1010, channel 10 power CF; 1011, total active power CF; 1100, reactive power CF (channel optional); 1101, apparent power CF (channel optional); 1110, 1111, close CF; In addition, CF_var is always reactive power CF (channel optional), unchanged.
[14]	hpf_sel	1'b0	HPF selection: 0- use HPF; 1- not use HPF.
[15]	CF_add_sel	1'b0	Watt and VAR energy addition methods: 0- absolute value addition; 1- algebraic sum addition.
[16]	var_sel	1'b0	VAR energy selection: 0- fundamental wave; 1- full wave.
[19]	mode_sel	1'b0	Mode selection: 0- 1U10I mode; 1- 3U6I/5U5I mode.

4.5 Interrupt Status Register (Status1/Status2)

4.5.1 Status1 Register

Position	Interrupt Flag	Defaults	Description
0	SAG	0	Line voltage drop.
1	ZXTO	0	Zero-crossing overrun.
2	ZX01	0	Channel 1 zero-crossing signal.

3	ZX02	0	Channel 2 zero-crossing signal.
4	ZX03	0	Channel 3 zero-crossing signal.
5	ZX04	0	Channel 4 zero-crossing signal.
6	ZX05	0	Channel 5 zero-crossing signal.
7	ZX06	0	Channel 6 zero-crossing signal.
8	ZX07	0	Channel 7 zero-crossing signal.
9	ZX08	0	Channel 8 zero-crossing signal.
10	ZX09	0	Channel 9 zero-crossing signal.
11	ZX10	0	Channel 10 zero-crossing signal.
12	ZX11	0	Channel 11 zero-crossing signal.
13	PK01	0	Channel 1 overcurrent signal.
14	PK02	0	Channel 2 overcurrent signal.
15	PK03	0	Channel 3 overcurrent signal.
16	PK04	0	Channel 4 overcurrent signal.
17	PK05	0	Channel 5 overcurrent signal.
18	PK06	0	Channel 6 overcurrent signal.
19	PK07	0	Channel 7 overcurrent signal.
20	PK08	0	Channel 8 overcurrent signal.
21	PK09	0	Channel 9 overcurrent signal.
22	PK10	0	Channel 10 overcurrent signal.
23	PKV	0	Overvoltage signal.

4.5.2 Status3 Register

Position	Interrupt Flag	Defaults	Description
0	FLAG01	0	Channel 1 flag.
1	FLAG02	0	Channel 2 flag.
2	FLAG03	0	Channel 3 flag.
3	FLAG04	0	Channel 4 flag.
4	FLAG05	0	Channel 5 flag.
5	FLAG06	0	Channel 6 flag.
6	FLAG07	0	Channel 7 flag.
7	FLAG08	0	Channel 8 flag.

8	FLAG09	0	Channel 9 flag.
9	FLAG10	0	Channel 10 flag.

4.6 Detailed Description of Calibration Register

4.6.1 Channel PGA Gain Adjustment Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
60	GAIN1	R/W	R	24	0x000000	Channel PGA gain adjustment register.
61	GAIN2	R/W	R	20	0x00000	Channel PGA gain adjustment register.

It is used to set the PGA amplification parameters of the analog input channel, which can be set (0000=1 times; 0001=2 times; 0010=8 times; 0011=16 times); one channel is set per 4bit.

GAIN1	Bit[23:20]	Bit[19:16]	Bit[15:12]	Bit[11:8]	Bit[7:4]	Bit[3:0]
	Current channel 5	Current channel 4	Current channel 3	Current channel 2	Current channel 1	Voltage channel

GAIN2		Bit[19:16]	Bit[15:12]	Bit[11:8]	Bit[7:4]	Bit[3:0]
		Current channel 10	Current channel 9	Current channel 8	Current channel 7	Current channel 6

It should be noted that after the gain is set for the corresponding channel, the maximum allowable input signal of the channel should be reduced accordingly!

4.6.2 Phase Correction Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
64	PHASE[1]/ PHASE[2]	R/W	R	16	0x0000	[15:8] Channel 1 phase correction. [7:0] Channel 2 phase correction.
65	PHASE[3]/ PHASE[4]	R/W	R	16	0x0000	[15:8] Channel 3 phase correction. [7:0] Channel 4 phase correction.
66	PHASE[5]/	R/W	R	16	0x0000	[15:8] Channel 5 phase correction.

	PHASE[6]					[7:0] Channel 6 phase correction.
67	PHASE[7]/ PHASE[8]	R/W	R	16	0x0000	[15:8] Channel 7 phase correction. [7:0] Channel 8 phase correction.
68	PHASE[9]/ PHASE[10]	R/W	R	16	0x0000	[15:8] Channel 9 phase correction. [7:0] Channel 10 phase correction.
69	PHASE[11]	R/W	R	8	0x00	[7:0] Voltage channel phase for correction.

The minimum adjustment delay time is 250nS, corresponding to 0.0045°/LSB, and the corresponding error ≈1.732*Sin (0.0045°) =0.0136%.

The maximum adjustment is about 0.574°, and the maximum adjustment error is about 1.734%.

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
6A	VAR_PHCAL_I	R/W	R	4	0x0	Current channel reactive phase correction register (fine adjustment).
6B	VAR_PHCAL_V	R/W	R	4	0x0	Voltage channel reactive phase correction register (fine adjustment).

Used to specify the channel phase fine adjustment of the reactive power measurement, 0.009°/LSB, the corresponding error ≈0.0245%.

4.6.3 RMS Gain Adjustment Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
6C	RMSGN[1]	R/W	R	16	0x0000	Channel 1 rms gain adjustment register.
6D	RMSGN[2]	R/W	R	16	0x0000	Channel 2 rms gain adjustment register.
6E	RMSGN[3]	R/W	R	16	0x0000	Channel 3 rms gain adjustment register.
6F	RMSGN[4]	R/W	R	16	0x0000	Channel 4 rms gain adjustment

						register.
70	RMSGN[5]	R/W	R	16	0x0000	Channel 5 rms gain adjustment register.
71	RMSGN[6]	R/W	R	16	0x0000	Channel 6 rms gain adjustment register.
72	RMSGN[7]	R/W	R	16	0x0000	Channel 7 rms gain adjustment register.
73	RMSGN[8]	R/W	R	16	0x0000	Channel 8 rms gain adjustment register.
74	RMSGN[9]	R/W	R	16	0x0000	Channel 9 rms gain adjustment register.
75	RMSGN[10]	R/W	R	16	0x0000	Channel 10 rms gain adjustment register.
76	RMSGN[11]	R/W	R	16	0x0000	Channel 11 rms gain adjustment register.

Complement code, the highest bit is the sign bit, used for gain correction of the rms, the adjustment range is ±50%.

$$I[N]\_RMS = I[N]\_RMS0 * (1 + \frac{RMSGN[N]}{2^{16}})$$

Among them, I[N]_RMS0 is the measured value of the nth channel, RMSGN[N] is the gain correction value, and I[N]_RMS is the corresponding calibration output value.

4.6.4 RMS Offset Correction Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
77	RMSOS[1]	R/W	R	24	0x000000	Channel 1 rms offset correction register.
78	RMSOS[2]	R/W	R	24	0x000000	Channel 2 rms offset correction register.
79	RMSOS[3]	R/W	R	24	0x000000	Channel 3 rms offset correction register.

7A	RMSOS[4]	R/W	R	24	0x000000	Channel 4 rms offset correction register.
7B	RMSOS[5]	R/W	R	24	0x000000	Channel 5 rms offset correction register.
7C	RMSOS[6]	R/W	R	24	0x000000	Channel 6 rms offset correction register.
7D	RMSOS[7]	R/W	R	24	0x000000	Channel 7 rms offset correction register.
7E	RMSOS[8]	R/W	R	24	0x000000	Channel 8 rms offset correction register.
7F	RMSOS[9]	R/W	R	24	0x000000	Channel 9 rms offset correction register.
80	RMSOS[10]	R/W	R	24	0x000000	Channel 10 rms offset correction register.
81	RMSOS[11]	R/W	R	24	0x000000	Channel 11 rms offset correction register.

Complement, the sign bit of the highest bit. It is used to eliminate the deviation caused by input noise in the rms calculation, and can make the rms register value close to 0 under no load.

$$I[N]\_RMS = \sqrt{I[N]\_RMS0^2 + RMSOS[N] * 256}$$

Among them, I[N]_RMS0 is the measured value of the nth channel, RMSOS[N] is the gain correction value, and I[N]_RMS is the corresponding calibration output value.

4.6.5 Active Small Signal Compensation Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
82	WA_LOS[1]/ WA_LOS[2]	R/W	R	24	0x000000	[23:12] Channel 1 active small signal compensation, complement. [11:0] Channel 2 active small signal compensation,

						complement.
83	WA_LOS[3]/ WA_LOS[4]	R/W	R	24	0x000000	[23:12] Channel 3 active small signal compensation, complement. [11:0] Channel 4 active small signal compensation, complement.
84	WA_LOS[5]/ WA_LOS[6]	R/W	R	24	0x000000	[23:12] Channel 5 active small-signal compensation, complement. [11:0] Channel 6 active small-signal compensation, complement.
85	WA_LOS[7]/ WA_LOS[8]	R/W	R	24	0x000000	[23:12] Channel 7 active small signal compensation, complement. [11:0] Channel 8 active small signal compensation, complement.
86	WA_LOS[9]/ WA_LOS[10]	R/W	R	24	0x000000	[23:12] Channel 9 active small signal compensation, complement. [11:0] Channel 10 active small signal compensation, complement.

It is used to compensate the small signal deviation of active power caused by DC bias,

$$WATT[N] = WATT0[N] + WA\_LOS[N] * 2$$

Among them, WATT0[N] is the measured value of the nth channel, WA_LOS[N] is the offset correction value, and WATT[N] is the calibration output value of the corresponding channel.

Note that WA_LOS[N] is a signed number, complement, and the correction range of the active power register is ±4094.

4.6.6 Reactive Small Signal Compensation Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
87	FVAR_LOS/ VAR_LOS	R/W	R	24	0x000000	[23:12]is the reactive power small signal compensation register, complement (fundamental wave); [11:0] is the reactive power small signal compensation register, complement (full wave).

$$VAR = VAR0 + VAR\_LOS * 2$$

Among them, VAR0 is the measured value of reactive power, VAR_LOS is the offset correction value, and VAR is the calibration output value.

Note that VAR_LOS is a signed number, complemented, and the correction range of the reactive power register is ±4094.

The FVAR_LOS formula is similar.

4.6.7 Anti-Creep Threshold Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
88	VAR_CREEP/ WA_CREEP	R/W	R	24	0x04C04C	[23:12] is the reactive power anti-creeping threshold register; [11:0] is the active power anti-creeping threshold register.

The active power anti-creep and reactive power anti-creep is setting for each

channel. When a channel is in the anti-submarine state, the power below the threshold does not participate in the energy accumulation.

When the absolute value of the input power signal is less than this value, the output power register value is set to zero. This can make the value of the output to the active power register 0 under no-load conditions, even if there is a small noise signal.

$$Corresponding\ to\ CREEP\ value\ = \frac{Corresponding\ power\ register\ value}{2}$$

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
89	WA_CREEP2	R/W	R	12	0x000	[11:0] is the total active power anti-creeping threshold register.

The anti-creep threshold setting of the total active power of 10 channels, if the Reg88 register has been set, this register does not need to be set.

$$WA\_CREEP2 = \frac{WATT\ register\ value}{2}$$

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
8A	RMS_CREEP	R/W	R	12	0x200	[11:0] is the rms anti-creeping threshold register.

It can be made that under no load, even if there is a small noise signal, the value output to the rms register is 0.

$$RMS\_CREEP = I[N]\_RMS$$

4.6.8 Fast RMS Related Setting Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
8B	FAST_RMS _CTRL	R/W	R	24	0x20FFFF	[23:21] Channel fast rms register refresh time, half cycle

						and N cycle can be selected, the default is one cycle; [20:0] channel fast rms threshold register.

Select the cumulative time by FAST_RMS_CTRL[23:21], divided into six types: 10ms(000), 20ms(001), 40ms(010), 80ms(011), 160ms(100), 320ms(101), default (001) selection the cumulative response time of the cycle is 20ms, and the longer the cumulative time, the smaller the jump.

FAST_RMS_CTRL[20:0] is used to set the fast rms threshold. Once exceeded, the output flag FLAG[N] is 1. The flag is connected to the output (M1~M10), and the leakage current overcurrent output indicator pin can be pulled directly high.

$$FAST\_RMS\_CTRL[20:0] = \frac{I[N]\_FAST\_RMS}{8}$$

4.6.9 Overcurrent Alarm and Control

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
90	FLAG_CTRL	R/W	R	24	0x000000	Overcurrent indication control register. The main control directly controls the level state of M10~M1 output.
91	FLAG_CTRL1	R/W	R	24	0x000000	Overcurrent indication control register 1. [23:10] Disconnect delay timing, 0.1ms/LSB; [9:0] indication control, M10-M1: 0- output real-time interrupt; 1- 1-output delay control.
92	FLAG_CTRL2	R/W	R	24	0x000000	Overcurrent indication control register 2. [23:10] Closing delay timer, 0.1ms/LSB;

						[9:0] Closing control, M10-M1:0-close, 1-open.

flag_ctrl register

Bit[9:0] is the level control of M10~M1 output;

Bit[21:12] is the control priority of M10~M1 output. When the corresponding position is 1, the output level of M10~M1 can be directly controlled by the corresponding bit state of Bit[9:0]. Priority to FLAG_CTRL1 and FLAG_CTRL2, FLAG_CTRL has a higher level.

Real-time alarm output

The alarm high level of the corresponding channel is output in real time through the M10~M1 pins. Only the overcurrent (leakage) threshold register Reg8B (FAST_RMS_CTRL) is set, and the fast rms threshold between the fast rms refresh time;

Logic description of delay control

1） Set the Reg8B register, the fast rms threshold between the fast rms refresh time;

2） Set Reg91 register, Bit[23:10] delay output high level time T1, Bit[9:0] enable the delay control of the corresponding channel;

3） Set Reg92 register, Bit[23:10] delay output low time T2, Bit[9:0]=0;

---------- While running the process---------- ----------

4） If the channel N has a fast rms overrun event, the FAST_RMS_H[N] register retains the fast rms when the limit is exceeded; then T1 seconds, the corresponding M[N] pin is pulled high, and the corresponding indication status bit of the Reg56 register is 1;

----------After troubleshooting of fast rms exceeding limit ----------

5） MCU writes the delayed output low level time T2 to the Reg92 register, the corresponding channel [N] position of Bit[9:0] is 1; the M[N] pin is pulled low after a delay of T2, and the Reg56 state is cleared;

6） The MCU writes to the Reg92 register, Bit[23:10]=T2 delay time, the corresponding channel [N] position of Bit[9:0] is 0, and the corresponding FAST_RMS_H[N] register value is cleared.

4.6.10 ADC Enable Control

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
93	ADC_PD	R/W	R	11	0x000	Enable control of 11 channels ADC register. ADC_PD<0> controls the voltage channel; ADC_PD<10:1> controls the corresponding current channel 10 to current channel 1.

You can reduce power consumption by turning off unused channels.

4.6.11 Clear Setting Register after Energy Read

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
9D	RST_ENG	R/W	R	13	0x0000	Clear setting after reading the energy pulse count register.

When Bit[12:0] is set to 1, the energy-related registers Reg3B~2F are set to be cleared after reading. It can be set individually.

4.6.12 User Write Protection Setting Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
9E	WRPROT	R/W	R	16	0x0000	User write protection setting register, when 0x5555 is written, it means that the user register can be operated from reg60 to reg9d and rega0 to regd0.

BL0910 has a strict protection mechanism for register writing. You must write 0x5555 to the write protection setting register before writing to other registers.

4.6.13 Soft Reset Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
9F	SOFT_RESET	R/W	R	24	0x000000	When the input is 5a5a5a, the system is reset-only the state machine and registers of the digital part are reset! When the input is 55AA55, the user read and write registers are reset-Reset: reg60 to reg9f and rega0 to regd0.

4.6.14 Channel Gain Adjustment Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
A0	CHGN[1]	R/W	R	16	0x0000	Channel 1 gain adjustment register, complement.
A1	CHGN[2]	R/W	R	16	0x0000	Channel 2 gain adjustment register, complement.
A2	CHGN[3]	R/W	R	16	0x0000	Channel 3 gain adjustment register, complement.
A3	CHGN[4]	R/W	R	16	0x0000	Channel 4 gain adjustment register, complement.
A4	CHGN[5]	R/W	R	16	0x0000	Channel 5 gain adjustment register, complement.
A5	CHGN[6]	R/W	R	16	0x0000	Channel 6 gain adjustment register, complement.
A6	CHGN[7]	R/W	R	16	0x0000	Channel 7 gain adjustment register, complement.
A7	CHGN[8]	R/W	R	16	0x0000	Channel 8 gain adjustment register, complement.
A8	CHGN[9]	R/W	R	16	0x0000	Channel 9 gain adjustment register, complement.

A9	CHGN[10]	R/W	R	16	0x0000	Channel 10 gain adjustment register, complement.
AA	CHGN[11]	R/W	R	16	0x0000	Channel 11 gain adjustment register, complement.

16-bit signed number, adjust the gain of the ad sampling waveform of the corresponding channel in the form of 2's complement, the adjustable range is ±50%.

$$WAVE[N] = WAVE0[N] * (1 + \frac{CHGN[N]}{2^{16}})$$

Among them, WAVE0[N] is the measured value of the nth channel, CHGN[N] is the gain calibration value, and WAVE[N] is the calibration output value.

4.6.15 Channel Offset Adjustment Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
AB	CHOS[1]	R/W	R	16	0x0000	Channel 1 offset adjustment register, complement.
AC	CHOS[2]	R/W	R	16	0x0000	Channel 2 offset adjustment register, complement.
AD	CHOS[3]	R/W	R	16	0x0000	Channel 3 offset adjustment register, complement.
AE	CHOS[4]	R/W	R	16	0x0000	Channel 4 offset adjustment register, complement.
AF	CHOS[5]	R/W	R	16	0x0000	Channel 5 offset adjustment register, complement.
B0	CHOS[6]	R/W	R	16	0x0000	Channel 6 offset adjustment register, complement.
B1	CHOS[7]	R/W	R	16	0x0000	Channel 7 offset adjustment register, complement.
B2	CHOS[8]	R/W	R	16	0x0000	Channel 8 offset adjustment register, complement.
B3	CHOS[9]	R/W	R	16	0x0000	Channel 9 offset adjustment register, complement.
B4	CHOS[10]	R/W	R	16	0x0000	Channel 10 offset adjustment

						register, complement.
B5	CHOS[11]	R/W	R	16	0x0000	Channel 11 offset adjustment register, complement.

The data in the form of 2's complement is used to eliminate the deviation caused by the current channel and the voltage channel analog-to-digital conversion. The deviation here may be caused by the input and the offset generated by the analog-to-digital conversion circuit itself. The deviation correction can be used in no-load conditions the lower waveform offset is 0.

$$\mathrm{WAVE[N]} = \mathrm{WAVE0[N]} + \mathrm{CHOS[N]}*2$$

Where WAVE0[N] is the measured value of the nth channel, CHOS[N] is the calibration value, and WAVE[N] is the output value after calibration.

4.6.16 Active Power Gain Adjustment Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
B6	WATTGN[1]	R/W	R	16	0x0000	Channel 1 active power gain adjustment register, complement.
B7	WATTGN[2]	R/W	R	16	0x0000	Channel 2 active power gain adjustment register, complement.
B8	WATTGN[3]	R/W	R	16	0x0000	Channel 3 active power gain adjustment register, complement.
B9	WATTGN[4]	R/W	R	16	0x0000	Channel 4 active power gain adjustment register, complement.
BA	WATTGN[5]	R/W	R	16	0x0000	Channel 5 active power gain adjustment register, complement.
BB	WATTGN[6]	R/W	R	16	0x0000	Channel 6 active power gain adjustment register,

						complement.
BC	WATTGN[7]	R/W	R	16	0x0000	Channel 7 active power gain adjustment register, complement.
BD	WATTGN[8]	R/W	R	16	0x0000	Channel 8 active power gain adjustment register, complement.
BE	WATTGN[9]	R/W	R	16	0x0000	Channel 9 active power gain adjustment register, complement.
BF	WATTGN[10]	R/W	R	16	0x0000	Channel 10 active power gain adjustment register, complement.

$$\mathrm{WATTS[N]} = \mathrm{WATT0[N]} * (1 + \frac{WATTGN[N]}{2^{16}})$$

Among them, WATT[N] is the active power after the nth correction, and WATT0[N] is the active power before the nth correction. The adjustment range is ±50%.

4.6.17 Active Power Bias Adjustment Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
C0	WATTOS[1]	R/W	R	16	0x0000	Channel 1 active power offset adjustment register, complement.
C1	WATTOS[2]	R/W	R	16	0x0000	Channel 2 active power offset adjustment register, complement.
C2	WATTOS[3]	R/W	R	16	0x0000	Channel 3 active power offset adjustment register, complement.
C3	WATTOS[4]	R/W	R	16	0x0000	Channel 4 active power offset adjustment register,

						complement.
C4	WATTOS[5]	R/W	R	16	0x0000	Channel 5 active power offset adjustment register, complement.
C5	WATTOS[6]	R/W	R	16	0x0000	Channel 6 active power offset adjustment register, complement.
C6	WATTOS[7]	R/W	R	16	0x0000	Channel 7 active power offset adjustment register, complement.
C7	WATTOS[8]	R/W	R	16	0x0000	Channel 8 active power offset adjustment register, complement.
C8	WATTOS[9]	R/W	R	16	0x0000	Channel 9 active power offset adjustment register, complement.
C9	WATTOS[10]	R/W	R	16	0x0000	Channel 10 active power offset adjustment register, complement.

Complement code, sign bit of the highest bit. Used to eliminate the deviation of active power caused by board-level noise.

$$WATT[N] = WATT0[N] + \frac{WATTOS[N]}{2}$$

Among them, WATT0[N] is the measured value of the nth channel, WATTOS[N] is the offset correction value, and WATT[N] is the corresponding calibration output value.

4.6.18 Reactive Power Apparent Power Gain Adjustment Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
CA	VARGN	R/W	R	16	0x0000	Corresponding channel reactive power gain adjustment register, complement.

CC	VAGN	R/W	R	16	0x0000	Corresponding channel apparent power gain adjustment register, complement.

The adjustment formula is similar to the active power gain adjustment.

4.6.19 Reactive Power Apparent Power Bias Adjustment Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
CB	VAROS	R/W	R	16	0x0000	Corresponding channel reactive power offset adjustment register, complement.
CD	VAOS	R/W	R	16	0x0000	Corresponding channel apparent power offset adjustment register, complement.

The adjustment formula is similar to the active power offset adjustment.

4.6.20 CF Scaling Register

Used to control the accumulation speed of the energy pulse count, the default setting of BL0910 is 0x10

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
CE	CFDIV	R/W	R	12	0x010	CF scaling register[11:0].

Take the frequency of energy pulse counting when CFDIV=0x10 as the standard frequency, and the multiples of energy pulse counting in other settings are as follows:

CFDIV	Counting Magnification	CFDIV	Counting Magnification
0x00	0.03125	0x40	4
0x01	0.0625	0x80	8
0x02	0.125	0x100	16
0x04	0.25	0x200	32
0x08	0.5	0x400	64
0x10	1	0x800	256

0x20	2	Other value	1

4.7 Detailed Description of Electrical Parameter Register

4.7.1 Wave Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
1	WAVE[1]	R	W	24	0x000000	Channel 1 waveform register (normal current and leakage current are optional).
2	WAVE[2]	R	W	24	0x000000	Channel 2 waveform register (normal current and leakage current optional).
3	WAVE[3]	R	W	24	0x000000	Channel 3 waveform register (normal current and leakage current optional).
4	WAVE[4]	R	W	24	0x000000	Channel 4 waveform register (normal current and leakage current optional).
5	WAVE[5]	R	W	24	0x000000	Channel 5 waveform register (normal current and leakage current are optional).
6	WAVE[6]	R	W	24	0x000000	Channel 6 waveform register (normal current and leakage current optional).
7	WAVE[7]	R	W	24	0x000000	Channel 7 waveform register (normal current and leakage current optional).
8	WAVE[8]	R	W	24	0x000000	Channel 8 waveform register (normal current and leakage current optional).
9	WAVE[9]	R	W	24	0x000000	Channel 9 waveform register (normal current and leakage current optional).

A	WAVE[10]	R	W	24	0x000000	Channel 10 waveform register (normal current and leakage current optional).
B	WAVE[11]	R	W	24	0x000000	Channel 11 Waveform register.

Waveform data of real-time sampling points, sampling clock is 4MHz, then 4MH/256/50=312.5, so about 312 sampling points per cycle.

4.7.2 RMS Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
C	RMS[1]	R	W	24	0x000000	Channel 1 rms register, unsigned.
D	RMS[2]	R	W	24	0x000000	Channel 2 rms register, unsigned.
E	RMS[3]	R	W	24	0x000000	Channel 3 rms register, unsigned.
F	RMS[4]	R	W	24	0x000000	Channel 4 rms register, unsigned.
10	RMS[5]	R	W	24	0x000000	Channel 5 rms register, unsigned.
11	RMS[6]	R	W	24	0x000000	Channel 6 rms register, unsigned.
12	RMS[7]	R	W	24	0x000000	Channel 7 rms register, unsigned.
13	RMS[8]	R	W	24	0x000000	Channel 8 rms register, unsigned.
14	RMS[9]	R	W	24	0x000000	Channel 9 rms register, unsigned.
15	RMS[10]	R	W	24	0x000000	Channel 10 rms register, unsigned.
16	RMS[11]	R	W	24	0x000000	Channel 11 rms register, unsigned.

By setting the RMS_UPDATE_SEL of MODE2[22], the average refresh time of the rms can be selected to be 525ms or 1.05s, and the default is 525ms.

4.7.3 Fast Valid Value Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
17	FAST_RMS[1]	R	W	24	0x000000	Channel 1 fast (leakage current) rms register,

						unsigned.
18	FAST_RMS[2]	R	W	24	0x000000	Channel 2 fast (leakage current) rms register, unsigned.
19	FAST_RMS[3]	R	W	24	0x000000	Channel 3 fast (leakage current) rms register, unsigned.
1A	FAST_RMS[4]	R	W	24	0x000000	Channel 4 fast (leakage current) rms register, unsigned.
1B	FAST_RMS[5]	R	W	24	0x000000	Channel 5 fast (leakage current) rms register, unsigned.
1C	FAST_RMS[6]	R	W	24	0x000000	Channel 6 fast (leakage current) rms register, unsigned.
1D	FAST_RMS[7]	R	W	24	0x000000	Channel 7 fast (leakage current) rms register, unsigned.
1E	FAST_RMS[8]	R	W	24	0x000000	Channel 8 fast (leakage current) rms register, unsigned.
1F	FAST_RMS[9]	R	W	24	0x000000	Channel 9 fast (leakage current) rms register, unsigned.
20	FAST_RMS[10]	R	W	24	0x000000	Channel 10 fast (leakage current) rms register, unsigned.
21	FAST_RMS[11]	R	W	24	0x000000	Channel 11 fast rms register, unsigned.

For over-current or leakage detection, the detection cycle can be set by the FAST_RMS_CTRL register. It should be noted that the smaller the detection cycle, the greater the jump in the register value.

$$I[N]\_FAST\_RMS \approx I[N]\_RMS * 0.55$$

4.7.4 Active Power Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
22	WATT[1]	R	W	24	0x000000	Channel 1 active power register.
23	WATT[2]	R	W	24	0x000000	Channel 2 active power register.
24	WATT[3]	R	W	24	0x000000	Channel 3 active power register.
25	WATTS[4]	R	W	24	0x000000	Channel 4 active power register.
26	WATTS[5]	R	W	24	0x000000	Channel 5 active power register.
27	WATTS[6]	R	W	24	0x000000	Channel 6 active power register.
28	WATTS[7]	R	W	24	0x000000	Channel 7 active power register.
29	WATTS[8]	R	W	24	0x000000	Channel 8 active power register.
2A	WATTS[9]	R	W	24	0x000000	Channel 9 active power register.
2B	WATTS[10]	R	W	24	0x000000	Channel 10 active power register.
2C	WATTS	R	W	24	0x000000	Total active power register.

The active power register is signed 24-bit data, complemented. The highest bit is the sign bit, Bit[23]=1, indicating that the current power is negative power.

$$WATT = \frac{SUM(WATT[N])}{16}$$

4.7.5 Reactive Power Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
2D	FVAR	R	W	24	0x000000	Optional channel reactive power register (fundamental wave).
5D	VAR	R	W	24	0x000000	Optional channel (full wave)

						reactive power register.

Signed 24-bit data, complement. Bit[23] is the sign bit, =1, indicating that the current power is negative; MODE3[3:0] is used to select the reactive power measurement channel.

4.7.6 Apparent Power Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
2E	VA	R	W	24	0x000000	Optional channel apparent power register.

4.7.7 Energy Pulse Count Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
2F	CF[1]_CNT	R	W	24	0x000000	Channel 1 active pulse count register, unsigned.
30	CF[2]_CNT	R	W	24	0x000000	Channel 2 active pulse count register, unsigned.
31	CF[3]_CNT	R	W	24	0x000000	Channel 3 active pulse count register, unsigned.
32	CF[4]_CNT	R	W	24	0x000000	Channel 4 active pulse count register, unsigned.
33	CF[5]_CNT	R	W	24	0x000000	Channel 5 active pulse count register, unsigned.
34	CF[6]_CNT	R	W	24	0x000000	Channel 6 active pulse count register, unsigned.
35	CF[7]_CNT	R	W	24	0x000000	Channel 7 active pulse count register, unsigned.
36	CF[8]_CNT	R	W	24	0x000000	Channel 8 active pulse count register, unsigned.
37	CF[9]_CNT	R	W	24	0x000000	Channel 9 active pulse count register, unsigned.

38	CF[10]_CNT	R	W	24	0x000000	Channel 10 active pulse count register, unsigned.
39	CF_CNT	R	W	24	0x000000	Total active pulse count register, unsigned.
3A	CFQ_CNT	R	W	24	0x000000	Optional channel reactive pulse count register, unsigned (fundamental wave).
3B	CFS_CNT	R	W	24	0x000000	Optional channel apparent pulse count register, unsigned.

The energy pulse count is related to the CFDIV register. The larger the CFDIV register setting value, the faster the pulse count.

MODE3[15] is used to set the accumulation method of electric energy pulse counting: algebraic sum and absolute value method;

The RST_ENG register is used to set whether the energy pulse count register is cleared after reading;

$$CF\_CNT = \frac{SUM\ （CF[N])}{16}$$

4.7.8 Waveform Angle Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
3C	ANGLE[1]	R	W	16	0x000000	Channel 1 current and voltage phase angle register.
3D	ANGLE[2]	R	W	16	0x000000	Channel 2 current and voltage phase angle register.
3E	ANGLE[3]	R	W	16	0x000000	Channel 3 current and voltage phase angle register.
3F	ANGLE[4]	R	W	16	0x000000	Channel 4 current and voltage phase angle register.
40	ANGLE[5]	R	W	16	0x000000	Channel 5 current and voltage phase angle register.
41	ANGLE[6]	R	W	16	0x000000	Channel 6 current and voltage

						phase angle register.
42	ANGLE[7]	R	W	16	0x000000	Channel 7 current and voltage phase angle register.
43	ANGLE[8]	R	W	16	0x000000	Channel 8 current and voltage phase angle register.
44	ANGLE[9]	R	W	16	0x000000	Channel 9 current and voltage phase angle register.
45	ANGLE[10]	R	W	16	0x000000	Channel 10 current and voltage phase angle register.

It should be noted that when the current is less than a certain value, the angle register stops working.

$$Included\ angle(°) = \frac{360 * ANGLE[N] * f_c}{500000}$$

f_c is the measurement frequency of the AC signal source, the default is 50Hz.

4.7.9 Fast Valid Value Holding Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
46	FAST_RMS_H[1]	R	W	24	0x000000	Channel 1 fast (leakage current) rms register, hold.
47	FAST_RMS_H[2]	R	W	24	0x000000	Channel 2 fast (leakage current) rms register, hold.
48	FAST_RMS_H[3]	R	W	24	0x000000	Channel 3 fast (leakage current) rms register, hold.
49	FAST_RMS_H[4]	R	W	24	0x000000	Channel 4 fast (leakage current) rms register, hold.
57	FAST_RMS_H[5]	R	W	24	0x000000	Channel 5 fast (leakage current) rms register, hold.
58	FAST_RMS_H[6]	R	W	24	0x000000	Channel 6 fast (leakage current) rms register, hold.
59	FAST_RMS_H[7]	R	W	24	0x000000	Channel 7 fast (leakage current) rms register, hold.

5A	FAST_RMS_H[8]	R	W	24	0x000000	Channel 8 fast (leakage current) rms register, hold.
5B	FAST_RMS_H[9]	R	W	24	0x000000	Channel 9 fast (leakage current) rms register, hold.
5C	FAST_RMS_H[10]	R	W	24	0x000000	Channel 10 fast (leakage current) rms register, hold.

The data that exceeds the fast rms threshold is stored in the corresponding FAST_RMS_H[N] register, and can be cleared after setting operations.

1） The corresponding bit of flag_ctrl2[9:0] is set to 1;

2） The corresponding bit of flag_ctrl2[9:0] is set to 0; the corresponding FAST_RMS_H register value is cleared;

4.7.10 Power Factor Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
4A	PF	R	W	24	0x000000	Optional channel power factor register.

It is selected by the VAR_I_SEL register, that is, which channel is selected for reactive power and which channel is selected for power factor.

24-bit signed number, complement. Bit[23] is the sign bit,

$$Power\ factor\ = \frac{PF}{2^{23}}$$

4.7.11 Line Voltage Frequency Register

Add.	Name	External R/W	Internal R/W	Bits	Defaults	Description
4E	PERIOD	R	W	20	0x000000	Line voltage frequency register.

Measure the frequency of the sine wave signal of the voltage channel.

$$Line\ voltage\ frequency\ = \frac{10000000}{PERIOD}\ \text{Hz}$$

5、 COMMUNICATION INTERFACE

Register data are all sent in 3 bytes (24bit), register data less than 3 bytes, unused bits are filled with 0, and 3 bytes are sent together.

Select by pin SEL, when SEL=1, it is SPI, when SEL=0, it is UART.

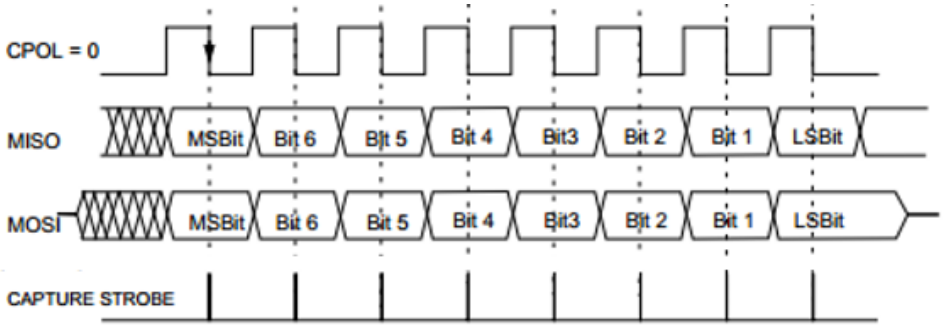
5.1 SPI

5.1.1 Overview

- ✓ Slave mode, half-duplex communication, maximum communication speed 1.5M
- ✓ 8-bit data transmission, MSB first, LSB behind
- ✓ Fix a clock polarity phase (CPOL=0, CPHA=1)

5.1.2 Operating Mode

The master device works in Mode1: CPOL=0, CPHA=1, that is, in the idle state, SCLK is at low level, and the data transmission is on the first edge, that is, the transition of SCLK from low to high, so Data sampling is on the falling edge, and data transmission is on the rising edge.



5.1.3 Frame Structure

In the communication mode, first send the 8bit identification byte (0x81) or (0x82), (0x82) is the read identification byte, (0x81) is the write identification byte, and then the register address byte is sent to determine the address of the access register (Please refer to the list of BL0910 registers). The following figure shows the data transfer sequence of read and write operations. One frame of data transfer is completed, and BL0910 re-enters the communication mode. The number of SCLK pulses required for each read and write operation both are 48 bits.

There are two types of frame structures, which are explained as follows:

1） Write register

Cmd: {0x81}+ Addr+Data_H+Data_M+Data_L+SUM

{0x81} is the frame identification byte of the write operation;

Addr is the internal register address of BL0910 corresponding to the write operation;

The checksum byte CHECKSUM is (((0x81)+ ADDR+ DATA_H+ DATA_M+ DATA_L)& 0xFF) and then inverted by bit.

写操作帧	0x81	ADDR[7:0]	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

2） Read register

Cmd:{0x82}+Addr

Returns: Data_H+Data_M+Data_L+SUM

{0x82} is the frame identification byte of the read operation;

Addr is the internal register address of BL0910 corresponding to the read operation (0x00-0xff);

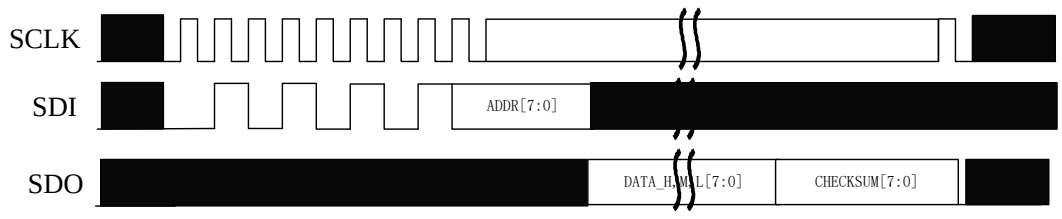
The checksum byte CHECKSUM is (((0x82)+ ADDR+ DATA_H+ DATA_M+ DATA_L)& 0xFF) and then inverted by bit.

读命令帧	0x82	ADDR[7:0]

读数据帧	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

5.1.4 Read Timing

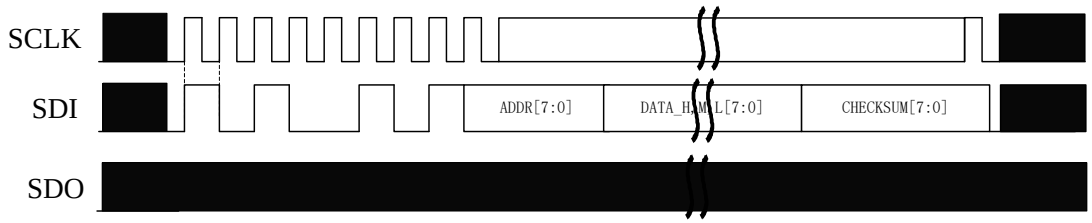
During the data read operation of BL0910, at the rising edge of SCLK, BL0910 shifts the corresponding data out to the DOUT logic output pin. During the next time when SCLK is 1, the DOUT value remains unchanged, that is, at the next at the falling edge, the external device can sample the DOUT value. Like the data write operation, the MCU must first send the identification byte and address byte before the data read operation.



When BL0910 is in communication mode, the frame identification byte {0x82} indicates that the next data transfer operation is to read. Then the byte immediately following is the address of the target register to be read. BL0910 starts to move out of the register at the rising edge of SCLK all the remaining bits of the register data are shifted out on the subsequent rising edge of SCLK. Therefore, on the falling edge, the external device can sample the output data of the SPI. Once the read operation is over, the serial interface will re-enter the communication mode at this time, the DOUT logic output enters a high impedance state on the falling edge of the last SCLK signal.

5.1.5 Write Timing

The serial write sequence is performed in the following manner. The frame identification byte {0x81} indicates that it is written during data transfer operations. The MCU will prepare the data bits that need to be written to BL0910 before the lower edge of SCLK, and at this clock of SCLK the lower edge of the SCLK starts to shift in the register data. All the remaining bits of the register data are also shifted left on the lower edge of the SCLK.



5.1.6 Fault Tolerance Mechanism of SPI Interface

1) If the frame recognition byte is wrong or the sum byte is wrong, the frame data is abandoned.

2) SPI module reset: send 6 bytes of 0xFF through the SPI interface, and the SPI interface can be reset separately;

3) _CS is pulled high to reset.

5.2 UART

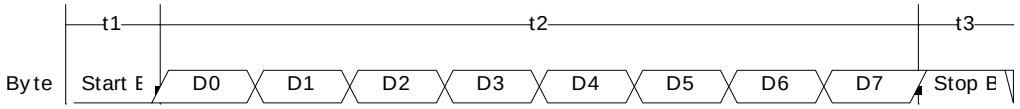
5.2.1 Overview

- ✓ Select by pin SEL, when SEL=1, it is SPI, when SEL=0, it is UART
- ✓ The communication baud rate is 4800bps/9600bps/19200bps/38400bps, no parity, stop bit 1;
- ✓ In UART mode, CS and SCLK pins are used as baud rate setting pins.

Baud rate setting	4800	9600	19200	38400
CS PIN	0	0	1	1
SCLK PIN	0	1	0	1

5.2.2 Byte Format

Take 4800bps as an example:

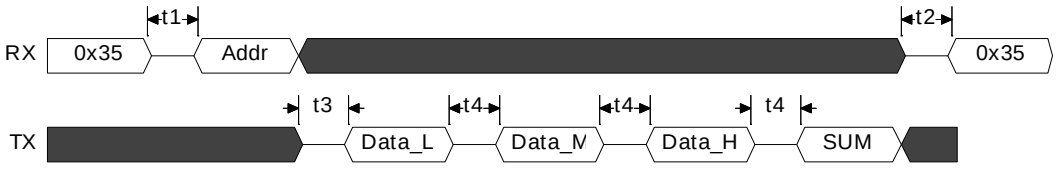


Start bit low level duration t1=208us (4800bps);

The valid data bit time lasts t2=208*8=1664us(4800bps);

Stop bit high level duration t3=208u(4800bps)s;

5.2.3 Read Timing



The host UART read data sequence is shown in the figure below. The host first sends the command byte (0x35), then the address byte (ADDR) that needs to be read, then BL0910 sends the data byte in turn, and finally the checksum byte.

{0x35} is the frame identification byte of the read operation;

Addr is the internal register address of BL0910 corresponding to the read operation;

The SUM byte is (Addr+Data_L+Data_M+Data_H)&0xFF reverse;

	Description	Min	Type	Max	Unit
t1	The interval between MCU sending bytes	0		20	mS
t2	Frame interval	0.5			uS

t3	The interval time from the end of MCU sending register address to Bl050 sending byte during read operation		110		uS
t4	The interval between sending bytes		1		bit

5.2.4 Write Timing

The host UART writes data sequence is shown in the figure below. The host first sends the command byte (0xCA), then the write address byte (ADDR), then sends the data byte in turn, and finally the checksum byte.

{0xCA} is the frame identification byte of the write operation;

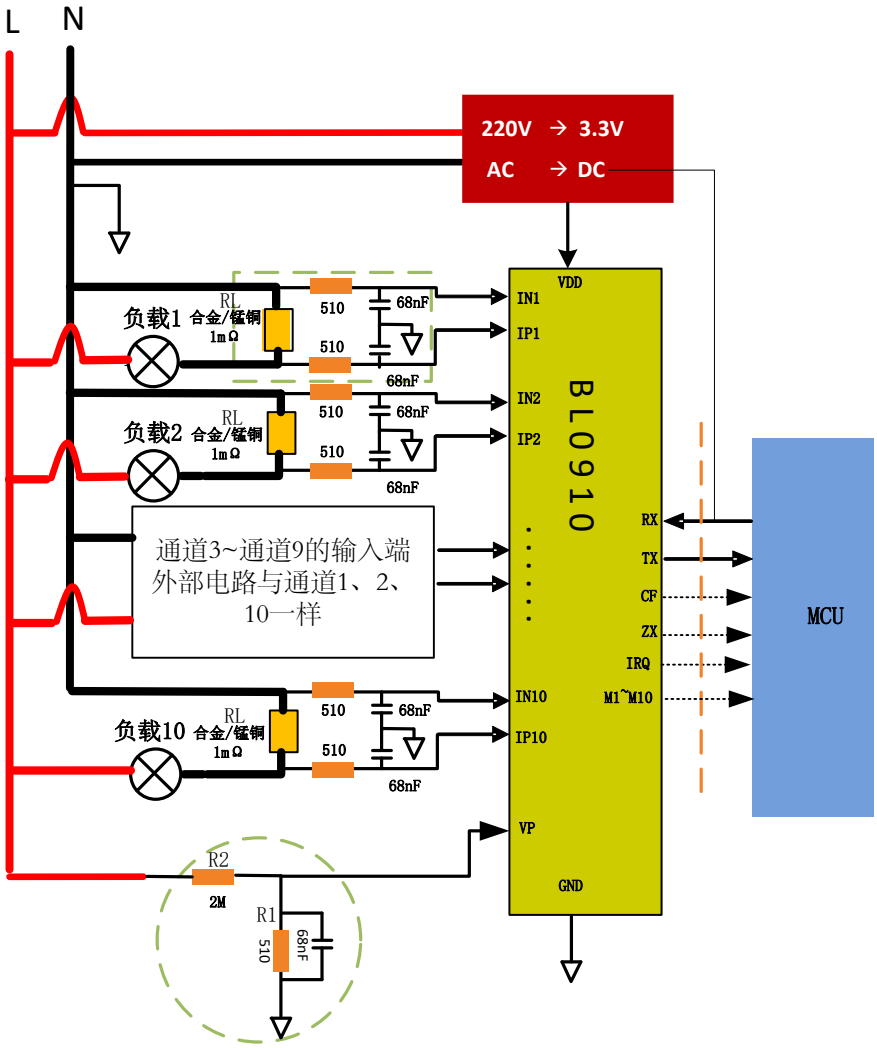
Addr is the internal register address of BL0910 corresponding to the write operation;

The CHECKSUM byte is ((ADDR+Data_L+Data_M+Data_H)& 0xFF) and then inverted by bit.

5.2.5 Protection Mechanism of UART Interface

1) The UART communication of BL0910 provides a timeout protection mechanism. If the interval time between bytes exceeds 18.5mS, the UART interface will automatically reset.
2) If the frame recognition byte is wrong or the checksum byte is wrong, the frame data is abandoned.
3) UART module reset: The RX pin is pulled high after the low level exceeds 32 bps (6.67ms at 4800 bps), and the UART module is reset.

6、 TYPICAL APPLICATION DIAGRAM



For 1U10I applications, the external circuit diagram of each current channel is the same, and the voltage channel requires signal division.

7、 PACKAGE INFORMATION

7.1 Package Information

BL0910 LQFP48 PACKAGE

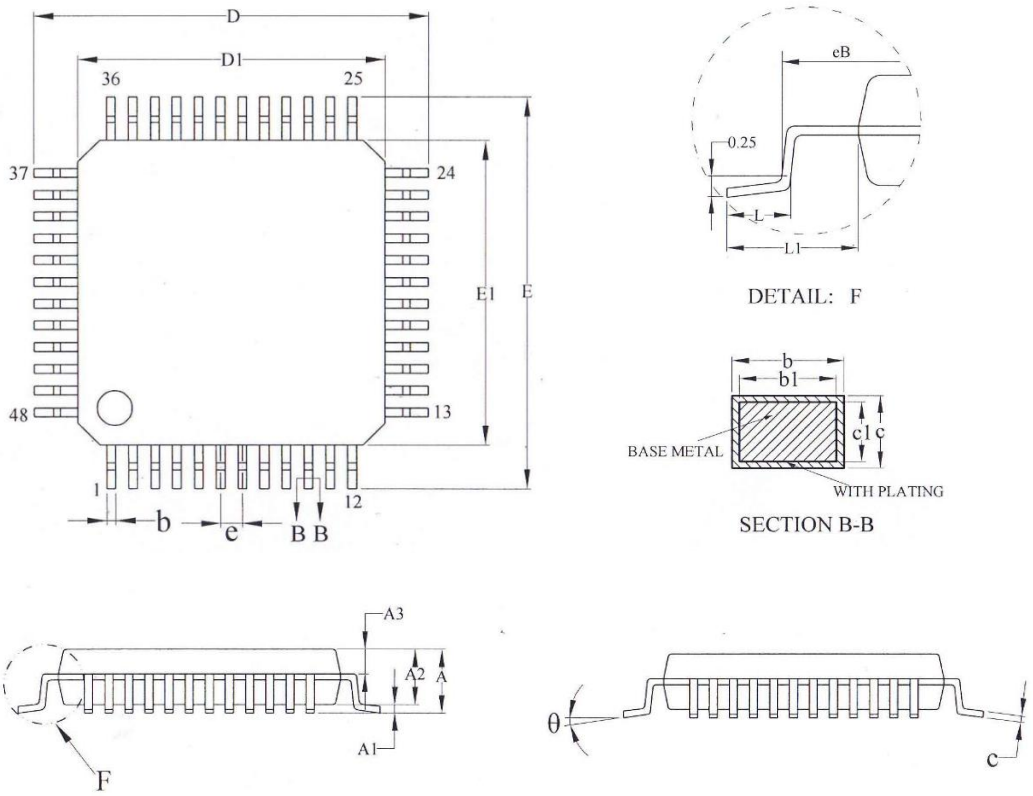
7.2 Order Information

Moisture sensitivity level MSL 3

Warranty Two years

Packing Plate mount

7.3 Appearance Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.50BSC		
L	0.40	—	0.65
L1	1.00REF		
θ	0	—	7°