



Jose Rizal University
College of Computer Studies Engineering
Computer Engineering Department

W2 - Webinar Report

CPE C409 – SEMINARS AND FIELDTRIPS

Submitted by:

Exiquiel John A. Pines

Submitted to:

Mrs. Monette Loy-A

Date Submitted:

September 9, 2023

Hosting Institution: **Jose Rizal University**

Seminar Title: **Field Programmable Gate Array (FPGA) Implementation of Digital Design**

Speaker: **Engr. Jesse Dela Cruz**

Seminar Date and Time: **August 31, 2023 / 12:30 AM**

Seminar Venue: **Jose Rizal University / H-306**

Engr. Jesse Dela Cruz is currently working part time as professor in Jose Rizal University and handling computer engineering related subjects. He also worked with various companies not only in the Philippines but also from different countries. Knowing that the speaker is a professional and has great experience in the field, I was intrigued about what he will be teaching us at the seminar.

Engr. Jesse Dela Cruz started with the introduction of what are Field Programmable Gate Array or FPGA, FPGAs are digital integrated circuits (ICs) that contain configurable (programmable) blocks of logic along with configurable interconnects between these blocks. FPGAs are configured by design engineers to perform a tremendous variety of tasks. FPGAs are devices that can be configured to perform different digital functions. They have reconfigurable logic blocks and interconnects, which can be programmed using a hardware description language (HDL) such as Verilog or VHDL.

To be programmable, a silicon chip must have a mechanism that allows us to configure it, or program it, to perform different tasks. There are four main techniques for programming silicon chips: **Fuse-based programming** uses fuses to create connections between different parts of the chip. Once a fuse is blown, it cannot be reversed. This makes fuse-based programming a one-time process. **Anti-fuse-based programming** is similar to fuse-based programming, but the anti-fuses can be programmed multiple times. This makes anti-fuse-based programming more flexible than fuse-based programming. **Flash technology** uses floating gate transistors to store the configuration data. The configuration data can be erased and rewritten multiple times, making flash technology a very flexible programming technique. **SRAM-based programming** uses static random-access memory (SRAM) cells to store the configuration data. SRAM cells are volatile, which means that the configuration data is lost when the power is turned off. This makes SRAM-based programming a less permanent programming technique than the other techniques.

He then instructed us to install a software call Quartus II which is a software used for designing and programming FPGAs. He also brought an Altera DE2 Board which is a development board used to learn about and experiment about FPGAs. He walked us through the process of programming in Quartus II such as writing the Verilog code, assigning input and output of the pins, and verifying and debugging of the code. We were able to create a simple XOR program that will use the board's switches as input and the LEDs as output.

In this seminar, Engr. Jesse Dela Cruz provided an overview of the advantages of FPGAs and the FPGA design flow. FPGAs are a powerful tool for digital design. They offer a number of advantages over other digital design technologies, and they can be used to implement a wide variety of systems. He also discussed some of the challenges of FPGA design. I found this seminar to be very informative and helpful. I learned a lot about the capabilities of FPGAs and how they can be used to implement digital designs. I am now more confident in my ability to use FPGAs for my own projects.

Hands-On Activity





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W2 - Webinar Evaluation

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Seminar Evaluation Form

Topic : Field Programmable Gate Array (FPGA) Implementation of Digital Design

Speaker : Engr. Jesse Dela Cruz

Date : August 31, 2023

Time : 12:30 pm

exiqueiljohn.pines@my.jru.edu [Switch account](#)

Draft saved

* Indicates required question

Email *

Record exiqueiljohn.pines@my.jru.edu as the email to be included with my response

Name *

Exiquiel John A. Pines

I. CONTENT

Relevance of the topic discussed *

1

2

3

4

5

Poor

Excellent



Scope of the topics covered *



Usefulness of activities *



Clarity of the presentation *



The presentation was well organized *



Did you find the content practical and applicable to your interest? *

- Yes
 No

Did the content provide you with new insights or knowledge? *

Did the content provide you with new insights or knowledge? *

Yes

No

Which specific topics or areas of the content did you find most valuable? *

Uses of FPGA

II. RESOURCE PERSON

Mastery of the topic *

1 2 3 4 5

Poor Excellent

Effectiveness of the speaker *

1 2 3 4 5

Poor Excellent

How well did the speaker engage with the audience (e.g., Q&A, discussions)? *

1 2 3 4 5

Poor Excellent



The speaker's presentation was clear and engaging *

1 2 3 4 5

Poor

Excellent

Did the speaker engage the audience and maintain your interest? *

Yes

No

What aspects of the speaker's presentation did you find particularly effective or *
valuable?

Hands-On

III. OVERALL SATISFACTION

How satisfied are you with the overall seminar event? *

1 2 3 4 5

Very Dissatisfied

Very Satisfied

List any suggestions you have for improving the presentation

Your answer



A copy of your responses will be emailed to exiqueiljohn.pines@my.jru.edu.



Seminar Evaluation Form

Your response has been recorded.

This form was created inside of Jose Rizal University. [Report Abuse](#)

Google Forms



JOSÉ RIZAL UNIVERSITY

CERTIFICATE

OF APPRECIATION

IS HEREBY GIVEN TO

Exequiel John A. Pines

In recognition of your active participation and engagement in the seminar entitled:
"Field Programmable Gate Array (FPGA) Implementation of Digital Design".

Your commitment to learning and your enthusiastic involvement in the seminar session have contributed to its success. You have demonstrated a keen interest in expanding your knowledge in the field of web development. We commend your dedication and hope that the skills and insights gained during this seminar propel you towards greater achievements in your professional journey.

Given this 1st day of September in the year of the Lord, 2023.

aloya
ENGR. MONETTE LOY-A

Course Adviser