Improved Balancing And Sensing of Sub-module Capacitor Voltages In Modular Multi-level Converters

Shamkant D. Joshi
Dept. of Electrical Eng.
IIT Bombay
Mumbai, India
shamkant@ee.iitb.ac.in

Mukul C. Chandorkar
Dept. of Electrical Eng.
IIT Bombay
Mumbai, India
mukul@ee.iitb.ac.in

Anshuman Shukla
Dept. of Electrical Eng.
IIT Bombay
Mumbai, India
ashukla@ee.iitb.ac.in

***Abstract*—Capacitor voltage balancing is necessary in Modular Multilevel Converters. Voltage controlled oscillator is used for capacitor voltage measurement in reported literature where voltage sensor is required to be calibrated. In the present work, a voltage sensing method that does not need calibration of individual voltage sensors is used for capacitor voltage measurement. Open loop phase shifted carrier pulse width modulation (PSCPWM) method is used and sorting algorithm is employed for capacitor voltage balance. A method of sorting capacitor voltages that selects the modules to be inserted directly based on logic equations is used as compared to the conventional methods of arranging them in ascending or descending order. This facilitates use of Field Programmable Gate Array for sorting. Fairly good capacitor voltage balance is obtained.**

***Index Terms*—Sensing of capacitor voltages in Modular Multilevel Converters, Balancing of capacitor voltages in Modular Multilevel Converters.**

I. Introduction

Modular Multilevel Converter (MMC) has emerged as the preferred configuration of multilevel converter for high voltage high power applications because of scalability and modularity considerations. MMC mathematical analysis, modeling, modulation, control, capacitor voltage balancing topologies, fault protection and pre-charging have been studied extensively. Due to several modules connected in series per arm of MMC, the capacitor voltage in MMC needs to be continuously balanced. The capacitor voltage must be measured for this purpose. Presently two methods are reported in literature. They are by using a) analog to digital converter (ADC)[1] or b) voltage controlled oscillator (VCO)[2]. When the number of capacitors is large, interface between the measurement systems with the control circuit is complex while using ADC [3] and therefore measurement by VCO is preferred. While using VCO, the range of frequency is a function of voltage variation. The measurement of voltage is based on the count of the number of pulses at the output of the VCO. Therefore calibration of each capacitor voltage sensing circuit is done as a function of voltage [4]. The present work proposes a new method of measuring capacitor voltages, that does not require calibration of individual modules.

Two methods are used for capacitor voltage balancing, a) averaging and balancing control and b) sorting [5]. In the averaging and balancing control of MMC method [6] [7], capacitor voltage control loops are added for each submodule, and therefore, all references for pulse generation are different. The major disadvantage of this control method is that it uses a centralized controller for the voltage balancing. This fact reduces significantly the response time of a balancing action [8].

For the Sorting and Selection approach, there is no capacitor voltage control loop. The voltage reference is the same for all modules in one arm. The generated pulses are reassigned to modules according to the sorting results of the capacitor voltage and arm current direction [9] [10] [11]. This approach does not require tuning of control parameters. It usually has faster response compared with the individual control loop approach. As this approach is applied after pulse generation, both the pulse generation and voltage balancing control (VBC) are usually implemented in the field-programmable gate array (FPGA)[11]. The difficulty is in the FPGA implementation since the conventional methods need to sort the capacitor voltages in ascending or descending order and reassign the pulses according to the sorting result [8]. The present work suggests a new method for selecting the modules to be inserted and bypassed employing FPGA without arranging the capacitor voltages in ascending or descending order.

Section II explains the module capacitor pre-charging used; section III describes the capacitor voltage sensing method used; section IV presents in detail the sorting method that uses logic based selection of modules to be inserted or bypassed for balancing the capacitor voltages; section V shows the experimental results for three phase seven level MMC during continuous running and complete pre-charging and section VI concludes.

II. Pre-charging of MMC in open loop

Pre-charging in MMC can be done from the AC side when used in rectifier mode or from the DC side when used in inverter mode [12]. Pre-charging in inverter mode is presented

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here. With reference to single phase MMC circuit with N number of modules per arm as shown in Fig. 1, all modules M_1 *to* M_{2N} are identical full bridge modules. The module M_1 is shown in detail. Before charging directly from the dc bus, initially the module capacitors are in a completely discharged state. Pre-charging is done in two stages a) uncontrolled and b) controlled. While starting MMC directly from the dc bus initially the switches Sc are open. When the input DC voltage was switched on by closing the switches S_u and S_l, each module capacitor got charged to Vdc/2N through the diode D1, capacitor C and diode D2f of each module of the top and the bottom arms, the arm inductors L and the limiting resistors R_c during the uncontrolled pre-charging process. The resistors R_c in series limit the initial current to a safe level. When each of the capacitors in all the modules in both upper and lower arm is charged to Vdc/2N, uncontrolled pre-charging is over.

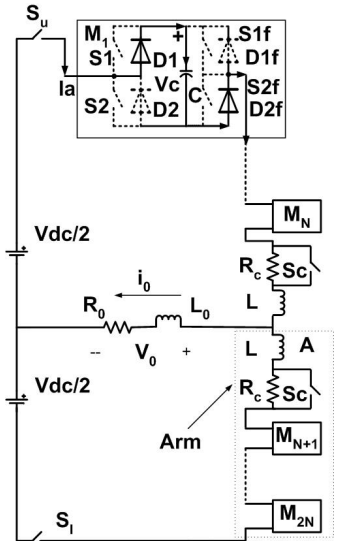

Fig. 1. Single phase full bridge MMC with (N) modules per arm

It is necessary to charge each of the capacitors to Vdc/N for proper operation of MMC [9]. This was achieved by controlled pre-charging. The switches Sc were closed bypassing the resistors R_C. All the modules were run in PWM mode of operation. The PWM mode of operation is explained by the equivalent circuits Fig. 2 and Fig. 3. Module inserting and bypass is illustrated by the details of the switch positions of the module M_1. In Fig. 2 the module M_1 is bypassed by closing the switch S2 and the path of current flow through the module M_1 is shown by the bold line. The current Ia flows through the switch S2 and diode D2f bypassing the capacitor.

All modules that are bypassed operate in the same manner. When any of the modules are bypassed energy is stored in the arm inductors L as the current Ia increases. The switch S2 is then opened and the module M_1 is inserted. Corresponding flow of current Ia is shown by the bold lines in the module M_1 as shown in Fig. 3. The current Ia now charges the capacitor C through D1, C, D2f inside the module M_1. All module

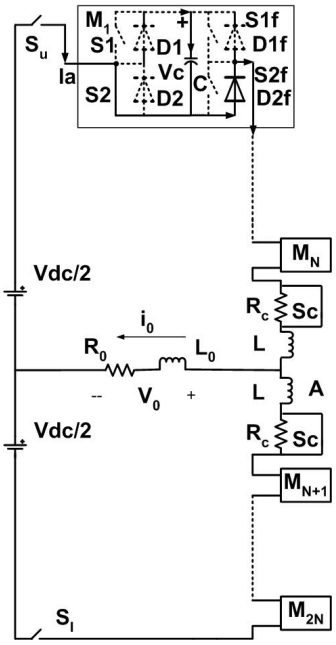

Fig. 2. MMC controlled pre-charging module bypass

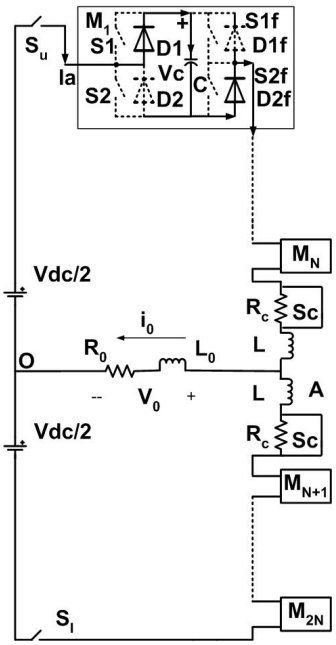

Fig. 3. MMC controlled pre-charging module insert

capacitors that are inserted get charged in the same manner.

The program for controlled pre-charging was loaded in FPGA. The controlled pre-charging of the module capacitors is explained with the help of Fig. 4. Two counters were set-up in software and were reset to zero after 250 μs. The reset of the two were separated by 125 μs. Thus the two saw tooth waves were separated by 125 μs as shown in Fig. 4. Immediately after the uncontrolled pre-charging was over, the module capacitors were charged from Vdc/2N to Vdc/N. The

duty cycle of the switch S1 of all the modules in a leg of Fig. 1 was 100% at start. In order to double the capacitor voltage to Vdc/N it should be gradually reduced to 50 %. For minimizing circulating current the average DC input voltage presented by a leg should be equal to Vdc.

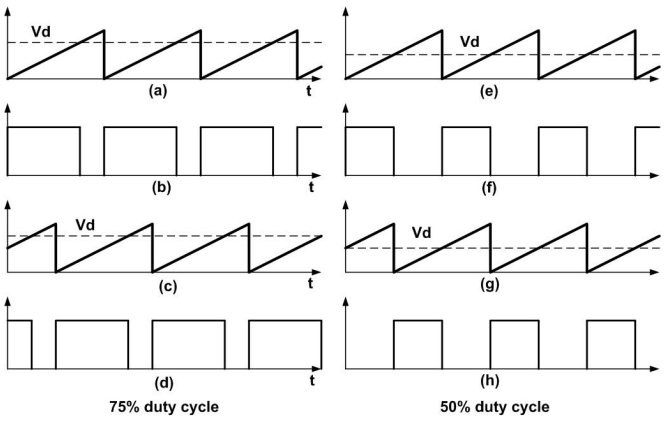

Fig. 4. Controlled pre-charging by duty cycle change

In Fig. 4, saw tooth waves of Fig. 4(a)(e) are shifted by half a cycle from those of Fig. 4(c)(g). The duty cycle of the output pulses applied to switches S1 was changed by reducing the level of Vd from 100% to 50%. The signal Vd is compared with the saw tooth wave to obtain PWM waveforms in Fig.4 (b) and (f). In Fig. 4(a)(b)(c)(d), the signal Vd and the duty cycle are at 75%. In Fig. 4(e)(f)(g)(h) Vd and the duty cycle are at 50%. At 50% duty cycle pulses at (f) are applied to half the modules and pulses at (h) are applied to the remaining half of the modules of each arm. This ensures that at 50% duty cycle only half the numbers of modules are inserted at any instant and total voltage presented by a leg to the DC supply is Vdc. When duty cycle of 50% was reached, controlled pre-charging was complete and sorting algorithm was introduced.

III. Proposed Capacitor Voltage Sensing Method

Capacitor voltage balancing is necessary in MMC and accurate voltage measurement of capacitor voltage is required. As mentioned in section I, measurement by using VCO is preferred in conventional method. While using VCO, the range of frequency as a function of voltage varies. Therefore calibration of each capacitor voltage sensing circuit is required [4]. In the present work a new voltage sensing method has been developed that does not need calibration of each individual voltage sensing module. The capacitor voltage sensing functional diagram is shown in Fig. 5. A saw tooth wave with voltage variation of 0-5 V is compared with capacitor voltage by reducing the the voltage at comparison level by a potential divider as shown in Fig. 5. The saw tooth waveform frequency across the modules varies between 25-30 kHz. A variable duty cycle that is proportional to the capacitor voltage is produced at the comparator output. The power supply used for the sawtooth generator and the comparator is the same for sensing one capacitor voltage. A separate isolated 9 V supply has been used for each capacitor voltage sensing circuit in the present case. When a separate isolated 9 V supply is not desired it should be derived from the module capacitor of each submodule. The same is discussed in detail in [13] and [14].

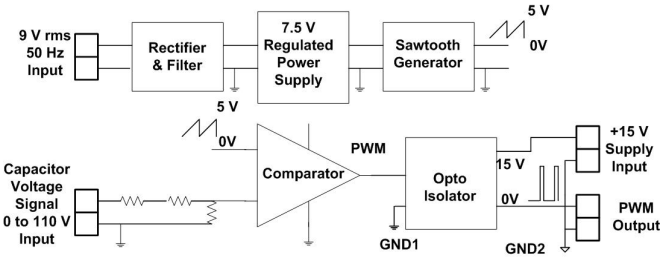

Fig. 5. Capacitor voltage sensing functional diagram

In the present method, the duty cycle represents the capacitor voltage and is measured by FPGA. Since the voltage pulses at 25-30 kHz are at a low voltage level of 3.3 volts, when connected to FPGA, they are prone to error and noise. Therefore, a fixed averaging window was used to filter and get a better voltage calculation. A counter counts the total time period for which it is high for a window of 250 μs and another counter counts for the total time for which it is low. After the end of this window, the high time counter was compared with the total time i.e. 250 μs. The counters were reset and the ON counter value was saved in V_{C1} as capacitor voltage for the first module. The capacitor voltages were measured for all capacitors and voltage V_{Ci} was assigned to the i^{th} capacitor accordingly by just saving the time for which the signal was high. In 7 level MMC with (N+1) modulation, six modules are used per arm. No calibration of individual modules was required.

IV. Logic Based Selection Of Capacitors For Voltage Balancing

Although all the module capacitors are at the required voltage level immediately after the controlled pre-charging is over, control is required for maintaining the voltage levels. Otherwise the capacitor voltages start diverging. Sorting algorithm was used for balancing the capacitor voltages. Phase shifted carrier (PSCPWM)[15] modulation strategy was used. There should be some current flow in the arm to achieve balancing. Hence the balancing operation was coupled with obtaining sine wave modulated PWM (SPWM) output.

For obtaining SPWM output the number of modules to be inserted at any instant is determined by the output voltage desired at that instant. The SPWM pattern for each module was generated by a common digital signal controller per phase.

A. Digital Signal Controller (DSC) Algorithm

The PWM waveform generated by DSC is shown in Fig. 6. The algorithm that was used for three phase MMC control is explained below. Digital Signal Controller (DSC) was used for generating switching pattern for 3-level, 5-level and 7-level three phase MMC. One sinusoidal voltage per phase was

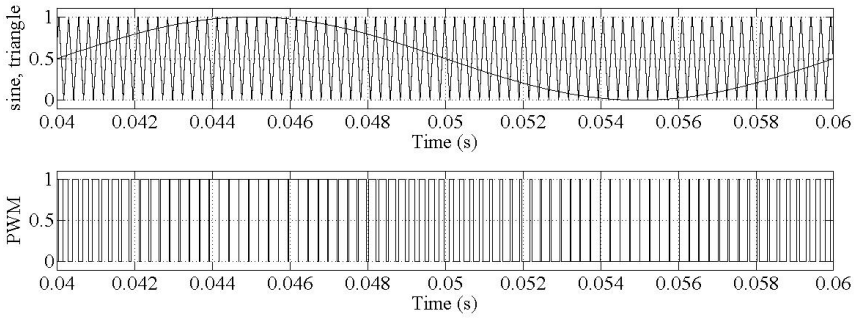

Fig. 6. PWM waveform generation in epwm module of DSC

generated at 50 Hz frequency by numerical integration of the following Quadrature Oscillator equations:

$$\frac{dx}{dt} = \omega y, \quad \frac{dy}{dt} = -\omega x \tag{1}$$

Phase shifted carrier based PWM (PSCPWM) was chosen for modulation. The phase-shifted carrier can be utilized to achieve the necessary voltage balancing. The control of MMC can be achieved with multicarrier modulation techniques. In order to generate the ideal output, the corresponding PWM waveform is required to be generated by comparing sine wave and triangle wave. A module available in the DSC for generating the sine-triangle modulated switching pattern for every module of an MMC arm was used. The equations were solved using Forward Euler method at a time step of 50 μs. The ePWM module was used to generate a triangular waveform at 4 kHz. At every zero crossing of triangular wave, a new compare value computed from the current sine amplitude was loaded into the compare register. One PWM pattern is generated for every module in upper arm.

Thus if there are N number of modules per arm, N number of triangle waves are generated per phase. The triangle waves are phase shifted from each other by 360/N degrees. Each triangle wave was compared with the same sine wave to generate N number of different PWM patterns. These were fed to the FPGA.

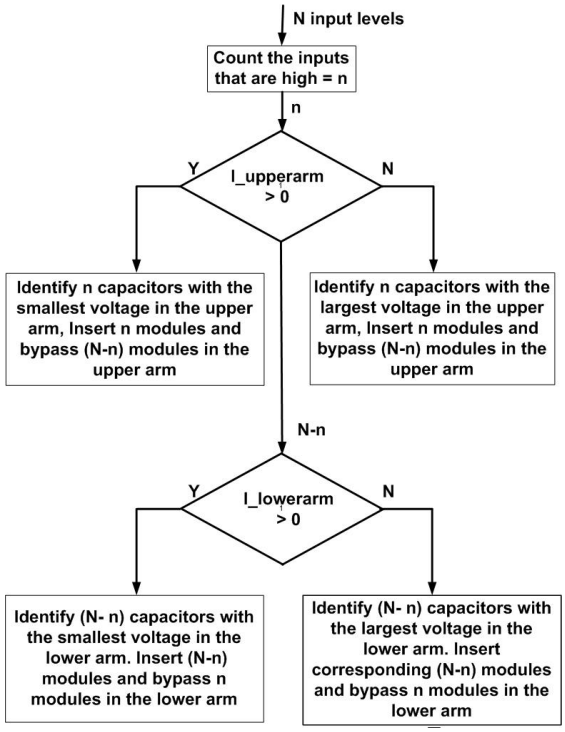

Fig. 7. Flowchart for sorting algorithm

B. Sorting of Capacitor Voltages Using FPGA

Fig. 7 shows the flow chart used for sorting of capacitor voltages. The directions of the arm currents were sensed. All the capacitor voltages in each phase were measured and the number of modules to be inserted, 'n' in the upper arm was estimated from the PWM waveforms as shown in Fig. 6. If the current direction was positive then 'n' number of the modules with the lowest voltages were inserted, while if the arm current was negative then 'n' number of modules with the highest voltages value were inserted in the upper arm. In the same manner (N-n) numbers of modules were inserted in the lower arm. In order to get a sinusoidal output voltage, the voltages of the top and the bottom arms are required to be in opposite phase. The flow chart for sorting the capacitors and corresponding insertion and bypassing of the modules is given in Fig. 7.

The capacitor voltages of all the modules have to be balanced. Hence the logic followed was:

If the number of modules to be inserted in the upper arm is 'n', it is required to identify 'n' number of capacitors with smallest voltage when the arm current is positive and 'n' number of capacitors with the largest voltage when the arm current is negative. In conventional methods, sorting is done by arranging the capacitor voltages in ascending or descending order [8]. Since sorting has been done using FPGA, a different technique was used to identify the modules to be inserted. If there were 'N' number of modules per arm and 'n' number of modules were to be inserted, for positive arm current, 'n' number of module capacitor voltages must be smaller

than (N-n) number module capacitor voltages. Hence the voltage of each of these modules must be smaller than at least (N-n) capacitor voltages. If one of these modules say i^{th} module was selected; it must be smaller than at least one set of (N-n) modules out of all the combinations of (N-1) remaining modules. There will be ${}^{(N-1)}C_{N-n}$ combinations. The number of combinations 'm' is given by:

$$m = {}^{(N-1)}\, C_{N-n} = (\frac{(N-1)!}{(n-1)!\,(N-n)!}) \tag{2}$$

If i^{th} module is inserted then $M_i = 1$ and if i^{th} module is bypassed then $M_i = 0$ and If V_{ci} and V_{cj} represent the capacitor voltages of the i^{th} and j^{th} modules respectively then if V_{ci} is less than V_{Cj} then $C_iC_j = 1$ and $C_jC_i = 0$, else $C_iC_j = 0$ and $C_jC_i = 1$.
If n = 0, all 'N' modules in the upper arm are bypassed.

$$M_{i|(i=1toN)} = 0 \tag{3}$$

If n = N, all 'N' modules in the upper arm are inserted.

$$M_{i|(i=1toN)} = 1 \tag{4}$$

If n = 1 to (N-1) and the arm current is positive,

$$M_{i|(i=1\ to\ N)} = (\sum^{m\ terms} \Pi_{i\neq j}^{(N-n)variables} C_iC_j) \tag{5}$$

If n = 1 to (N-1) and the arm current is negative,

$$M_{i|(i=1\ to\ N)} = (\sum^{m\ terms} \Pi_{i\neq j}^{(N-n)variables} C_jC_i) \tag{6}$$

Maximum 'N' number of modules per leg are inserted for (N+1) modulation scheme at any instant. There will be 'N' number of equations per arm, for $M_1, M_2, - - -M_N$, 'n' number of equations will have value equal to '1' and (N-n) number of equations will have value '0'. Each equation will be a sum of 'm' number of terms and each term will be a product of 'n' variables.

Consider a case of 7 levels MMC with (N+1) modulation. Therefore N=6. In order to obtain a sinusoidal output, the number of modules to be inserted in the upper arm varies between 0 to 6 over one cycle of the sine waveform. The table I shows the number of terms of summation and the number of variables in each product term of equation (5) and (6) for each case. If the number of modules to be inserted is n=3, then m = 10 from equation (2). If the direction of current is positive each capacitor voltage must be less than or equal to at the most three other capacitor voltages. Hence each product term must have 3 variables and there will be total 10 terms. Using table I and equation (5), the value of the fourth module will be simple AND/OR logic as shown in equation (7).

TABLE I
THE NUMBER OF TERMS OF SUMMATION AND THE NUMBER OF VARIABLES IN EACH PRODUCT TERM IN EQUATIONS (5) AND (6) FOR THE UPPER ARM IN 7 LEVEL MMC

No. of Modules to be inserted (n) in the upper arm	No. of Terms of summation (m)	No. of Variables in the product terms (N-n)
–	–	–
1	1	5
2	5	4
3	10	3
4	10	2
5	5	1

$$\begin{aligned} M_4 = {} & (C_4C_1)(C_4C_2)(C_4C_3) + (C_4C_1)(C_4C_2)(C_4C_5) \\ & + (C_4C_1)(C_4C_2)(C_4C_6) + (C_4C_1)(C_4C_3)(C_4C_5) \\ & + (C_4C_1)(C_4C_3)(C_4C_6) + (C_4C_1)(C_4C_5)(C_4C_6) \\ & + (C_4C_2)(C_4C_3)(C_4C_5) + (C_4C_2)(C_4C_3)(C_4C_6) \\ & + (C_4C_2)(C_4C_5)(C_4C_6) + (C_4C_3)(C_4C_5)(C_4C_6) \end{aligned} \tag{7}$$

If $M_4 = 1$ the fourth module is inserted else it is bypassed.

If the number of modules to be inserted is $n = 2$ and the direction of current is negative (discharging) then using table I and equation (6), the value of the fourth module will be simple AND/OR logic as shown in equation (8).

$$\begin{aligned} M_4 = {} & (C_1C_4)(C_2C_4)(C_3C_4)(C_5C_4) \\ & + (C_1C_4)(C_2C_4)(C_3C_4)(C_6C_4) \\ & + (C_1C_4)(C_2C_4)(C_5C_4)(C_6C_4) \\ & + (C_1C_4)(C_3C_4)(C_5C_4)(C_6C_4) \\ & + (C_2C_4)(C_3C_4)(C_5C_4)(C_6C_4) \end{aligned} \tag{8}$$

Logical equations for $M_1\ to\ M_6$ can be written using Table I and equations (3) to (6).

If 'n' number of modules are inserted in the upper arm (N-n) number of modules are inserted for the lower arm for (N+1) modulation scheme.

If there were 'N' number of modules in the lower arm and $n' = (N-n)$ number of modules were to be inserted, for positive arm current, (n') number of module voltages must be smaller than the remaining 'n' number modules. Hence the voltage of each of these (n') modules must be smaller than at least 'n' capacitor voltages. If one of these modules say i^{th} module was selected; it must be smaller than at least one set of 'n' modules out of all the combinations of (N-1) remaining modules. There will be ${}^{(N-1)}C_n$ combinations. The number of combinations m' is given by:

$$m' = {}^{(N-1)}\, C_n = (\frac{(N-1)!}{(n)!\,(N-n-1)!}) \tag{9}$$

If i^{th} module is inserted then $M_i = 1$ and if i^{th} module is bypassed then $M_i = 0$ and If V_{ci} and V_{cj} represent the capacitor voltages of the i^{th} and j^{th} modules respectively then if V_{Ci} is less than V_{Cj} then $C_iC_j = 1$ and $C_jC_i = 0$, else $C_iC_j = 0$ and $C_jC_i = 1$.
If n' = 0, all 'N' modules in the lower arm are bypassed.

$$M_{i|(i=(N+1)\ to\ 2N)} = 0 \tag{10}$$

If n' = N, all 'N' modules in the lower arm are inserted.

$$M_{i|(i=(N+1)\ to\ 2N)} = 1 \tag{11}$$

If n' = 1 to (N-1) and the arm current is positive,

$$M_{i|(i=(N+1)\ to\ 2N)} = (\sum^{m'\ terms} \Pi_{i\neq j}^{n\ variables} C_i C_j) \quad (12)$$

If n' = 1 to (N-1) and the arm current is negative,

$$M_{i|(i=(N+1)\ to\ 2N)} = (\sum^{m'\ terms} \Pi_{i\neq j}^{n\ variables} C_j C_i) \quad (13)$$

There will be 'N' number of equations for the lower arm, for $M_{N+1}, M_{N+2}, ---M_{2N}$, $n' = (N-n)$ number of equations will have value equal to '1' and (n) number of equations will have value '0'. Each equation will be a sum of (m') number of terms and each term will be a product of (n) variables.

In case of 7 level MMC with (N+1) modulation, in order to obtain a sinusoidal output, the number of modules to be inserted in the lower arm varies between 0 to 6 over one cycle of the sine waveform. The table II shows the number of terms of summation and the number of variables in each product term of equations (12) and (13) for each case.

TABLE II
THE NUMBER OF TERMS OF SUMMATION AND THE NUMBER OF VARIABLES IN EACH PRODUCT TERM IN EQUATIONS (12) AND (13) FOR THE LOWER ARM IN 7 LEVEL MMC

No. of Modules to be inserted (n) in the upper arm	No. of Modules to be inserted (n') in the lower arm	No. of Terms of summation (m')	No. of Variables in each product term (n)
1	5	5	1
2	4	10	2
3	3	10	3
4	2	5	4
5	1	1	5

Consider the case when the number of modules to be insereted in the upper arm $n = 2$ the number of modules to be inserted in the lower arm will be $n' = (N - n) = 4$. The number of terms (m') from equation (12) and table II will be $m' = 10$. The number of variables in each product term will be $n = 2$. If the direction of current in the lower arm is positive, using table II and equation (12) the value of the module number 10, M_{10} will be simple AND/OR logic as shown in equation (14).

$$\begin{aligned} M_{10} = {} & (C_{10}C_7)(C_{10}C_8) + (C_{10}C_7)(C_{10}C_9) \\ & + (C_{10}C_7)(C_{10}C_{11}) + (C_{10}C_7)(C_{10}C_{12}) \\ & + (C_{10}C_8)(C_{10}C_9) + (C_{10}C_8)(C_{10}C_{11}) \\ & + (C_{10}C_8)(C_{10}C_{12}) + (C_{10}C_9)(C_{10}C_{11}) \\ & + (C_{10}C_9)(C_{10}C_{12}) + (C_{10}C_{11})(C_{10}C_{12}); \end{aligned} \quad (14)$$

If $M_{10} = 1$, the tenth module is inserted else it is bypassed. Logical equations for $M_7\ to\ M_{12}$ can be written using Table II and equations (10) to (13). Thus if any of the modules $M_1\ to\ M_{12}$ have a value equal to 1 they are inserted and those that have a value equal to 0 are bypassed. Single phase and three phase MMC was tested using the above sensing and sorting method. The next section discusses the results.

V. EXPERIMENTAL VALIDATION USING SEVEN LEVEL MMC

A. Single Phase MMC

The seven levels MMC system was run as 3 , 5 and 7 levels MMC to evaluate the capacitor voltage balancing. The results are listed in the table III. It is seen that the capacitor voltages are balanced within close tolerance of $\pm$ 1.5 V of the average value. The capacitor voltages were measured by averaging method. The sorting algorithm with logic based selection of modules to be inserted or bypassed for balancing capacitor voltages was used.

TABLE III
KEY RESULTS FOR SINGLE PHASE, 3, 5 AND 7 LEVEL MMC STEADY STATE OPERATION

No. of levels -	Vdc Bus Vdc	Cap Volt Vdc	o/p volt Vrms	o/p Amp Arms
3 level	150 V	71 $\pm$1.5 V	48 V	3.3 A
5 level	250 V	60 $\pm$1.5 V	75 V	3.5 A
7 level	550 V	88 $\pm$1.5 V	172 V	5.2 A

Seven level MMC has number of modules per arm, $N = 6$. Fig. 8 shows steady state waveforms for 7 level MMC with RL load. The four waveforms show the capacitor voltages across four of the twelve capacitors, two from each arm.

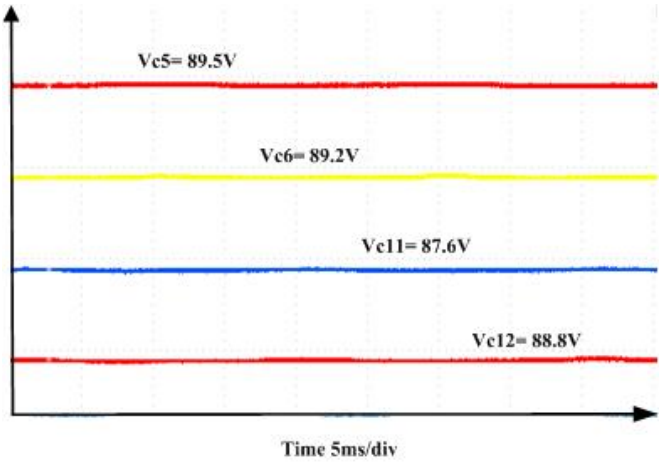

Fig. 8. Four module capacitor voltages during 7 level steady state

Fig. 9 shows waveforms for single phase seven level MMC that include uncontrolled pre-charging, controlled pre-charging and sine pulse width modulated output of 7 level MMC. With reference to Fig.1, the upper arm has modules $M_1\ to\ M_6$ and the lower arm has modules $M_7\ to\ M_{12}$. The DC voltage was set at 300 V. The switches S_u and S_l were closed at the instant t1 as shown in Fig. 9. It shows output filtered voltage, output unfiltered voltage, one capacitor voltage and output current. Each module capacitor got first pre-charged to $V_{dc}/(2N) = V_{dc}/12$ exponentially in uncontrolled mode at the instants t1 through the current limiting resistors R_c.

In Fig. 9, the upper half shows the output filtered voltage in the first waveform, the output unfiltered voltage in the

second waveform, one module capacitor voltage in the third waveform, and output current in the fourth waveform.

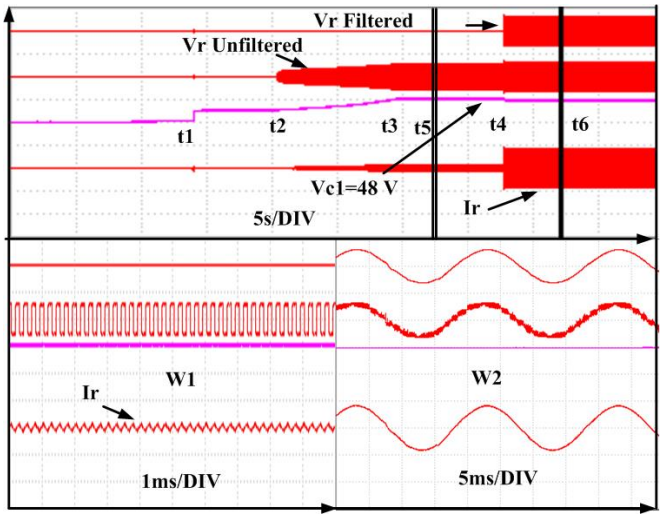

Fig. 9. Output filtered voltage, output unfiltered voltage, one capacitor voltage and output current during single phase 7 level starting

When the uncontrolled pre-charging through the resistors R_c was over the switches Sc were closed between the instants t1 and t2 to bypass the resistors R_c. Controlled pre-charging was enabled at t2 to charge the capacitors to V_{dc}/6, by open loop control. This was achieved by changing the duty cycle of the switches S1 of the modules M_1 *to* M_{12} from 1 to 0.5 and the duty cycle of the switches S2 of the modules M_7 *to* M_{12} from 0 to 0.5. After the controlled pre-charging process was complete at t3, sinusoidal PWM pulses were enabled at the instant t4, to produce modulated output waveforms. The waveforms at the time t5, immediately after the pre-charging is over, are expanded on time scale in window W1. The waveforms at t6 after the sine wave PWM was introduced, are expanded on time scale in window W2. The window W1 shows a small upper arm current which must be present to supply the circuit losses and the average voltage at the output is zero as desired. The module capacitor voltage rose to the required level and was able to support the sine wave output.

B. Three Phase MMC

Fig. 10 shows 3 phase 7 level full bridge circuit diagram of MMC that has total 36 full bridge MMC modules.

Fig. 11 shows the complete hardware setup for 3 phase MMC power and control with different parts labeled. Three racks are assembled for three phases. The three phase power circuit is arranged in three vertical racks. Positions of the two power stacks, the incoming switch, voltage sensing assembly, control power supplies, arm inductors, control circuit and control pcs are shown.

Fig. 12 shows the output PWM voltages of the three phases.

The first three waveforms show the three phase seven level sine wave modulated PWM output unfiltered waveforms. The fourth waveform shows module capacitor voltage of one of

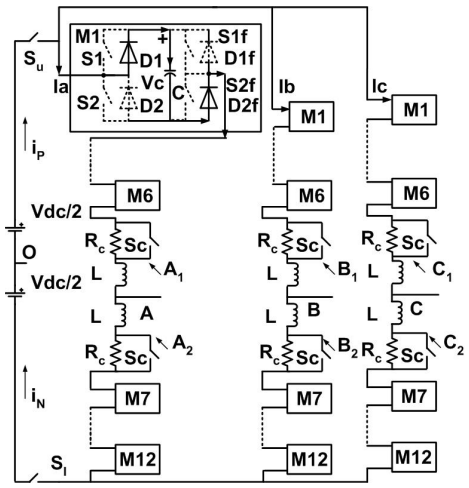

Fig. 10. 3 phase 7 level full bridge mmc power circuit diagram

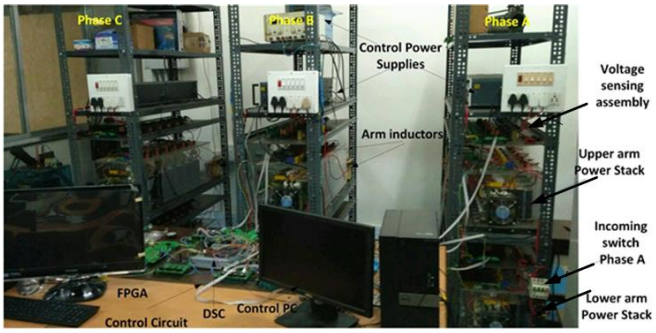

Fig. 11. 3 phase MMC power and control setup

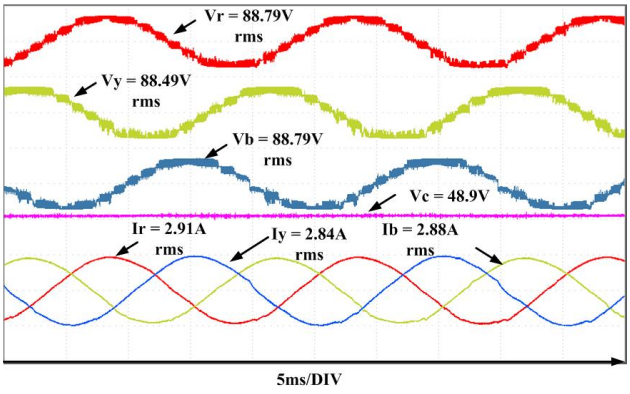

Fig. 12. 3 ph 7 level unfiltered output voltages, capacitor voltage and output currents

the 36 capacitors. The fifth waveform shows the three phase output current waveforms.

With reference to Fig. 13, the first waveform shows filtered three output voltages, the second waveform shows unfiltered 7 level output voltage, third waveform shows one of the 36 capacitor voltages, and the fourth waveform shows unfiltered output currents. The top half shows waveforms at a slow time

scale to see the overall pre-charging process and the bottom half shows two windows with expanded time scale.

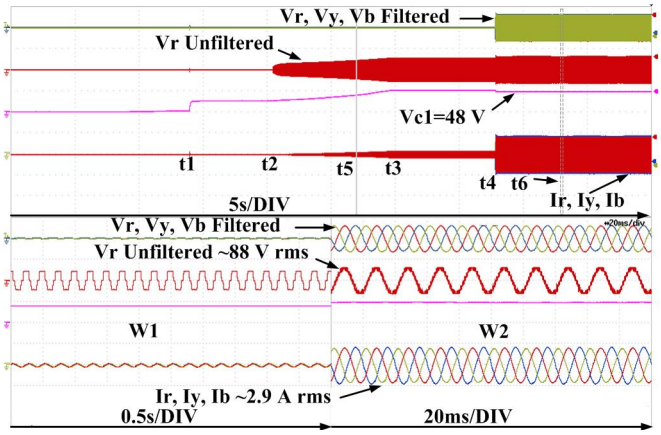

Fig. 13. 3 ph 7 level filtered output voltages, capacitor voltage and 3 ph output currents during starting

With reference to Fig. 10 and Fig. 13, the DC input voltage Vdc was set at $300V$. The input power switches S_u and S_l were closed at t1 resulting in charging of the capacitors exponentially to Vdc/12 through the current limiting resistors R_c. The uncontrolled pre-charging was over in a short time after t1. The resistors R_c in all the six arms were bypassed by closing switches Sc between the instants t1 and t2. At t2 controlled pre-charging of all the module capacitors in all the three phases was started from the master control switch on one of the FPGAs. The capacitor got charged to double the voltage to Vdc/6 by the time t3. The principle used for controlled pre-charging is explained in section II. At t4 sine wave PWM pulses were introduced simultaneously in all three phases by controlling a switch on the master FPGA controller. The 3 phase output appeared. At t5 and t6, all the waveforms are shown in two windows W1 and W2 on expanded time scale. The capacitor is seen to be partially charged in W1 and fully charged in W2. Sine wave output is seen in W2. At the window W2, the output voltages and currents are seen to be balanced.

VI. Conclusion

The new method of measurement of capacitor voltages sensing by averaging along with new method of sorting by logic based selection of the modules to be inserted is presented. In this method it is not necessary to arrange the capacitor voltages in ascending or descending order. It results in proper capacitor voltage balancing in open loop. The method of balancing presented enables easy use of FPGA for capacitor voltage balancing. Finally three phase seven level output with sine wave PWM modulation is obtained. Experimental waveforms for the complete process of MMC starting with uncontrolled and controlled pre-charging followed by sine wave PWM output waveforms are obtained as desired.

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