FABRICATION AND MEASUREMENTS OF AN INDIVIDUALLY ADDRESSABLE MICRO-PROBE ELECTRODE ARRAY USING SILICON THROUGH-GLASS VIA

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ABSTRACT

In this study, a micro-probe electrode array with independent interconnections through the substrate has been developed using LRS(Low Resistance Silicon) via and glass reflow process. The silicon vias have electrical resistance less than 2 Ω because the boron ion in the borosilicate glass wafer can diffuse into the LRS pillars during glass reflow process. The LRS wafer was etched with double DRIE (Deep Reactive Ion Etching) and RIE (Reactive Ion Etching) process to form 70 μm-height and 190 μm-pitch silicon micro-probe structures. To connect to silicon via, Cr/Au was deposited and patterned on micro-probe array structures. The Parylene-C film was deposited and patterned for insulating layer. To verify electrochemical characteristics of individually addressable micro-probe electrode array, the CV (Cyclic Voltammetry) measurement method was performed.

INTRODUCTION

In the past decade, the micromachining technology has been drastically growing in many research fields. With this growth of technology, many micro-probe type electrodes have been demonstrated using micromachining fabrication method. In biological applications, 3D micro electrode arrays (3D MEAs) are utilized in stimulating and recording applications by penetrating tissues or cell membranes [1-3]. Moreover, various types of micro-probe structures have been studied as neural probe electrodes for neurophysiological measurements. Many techniques have been employed to implement 3D micro-probe arrays, including a neural recording probe with built-in load sensors [4], using glass reflow process [5], flexible micro-probe array using parylene-C and PDMS(polydimethyl siloxane) [6, 7], using thermal drawing method [8], and magnetization-induced self-assembly method [9]. To detect local response or electrochemical reaction with higher electrical signal output, each micro-probe electrode should be individually addressed and isolated from other electrodes with spatial resolution in the chip level. In many of the previous studies, the electrical line was patterned and connected to each electrode on the surface for the individual addressing of the 3D electrodes, which limits the number of electrodes in the array and affects the detection signal from the probe electrodes. In this paper, a vertical out-of-plane silicon-based micro-probe electrode array with independent interconnections through the substrate has been demonstrated using silicon bulk micromachining technology and glass reflow process. Figure 1 shows the schematic view of the proposed conductive micro-probe electrode array using silicon through glass vias (TGVs). The conductive part of a probe electrode was exposed at the tip end, and the other areas electrically insulated. In addition, each micro-probe electrode was connected to the backside through the silicon TGVs and isolated using reflowed glass between silicon vias.

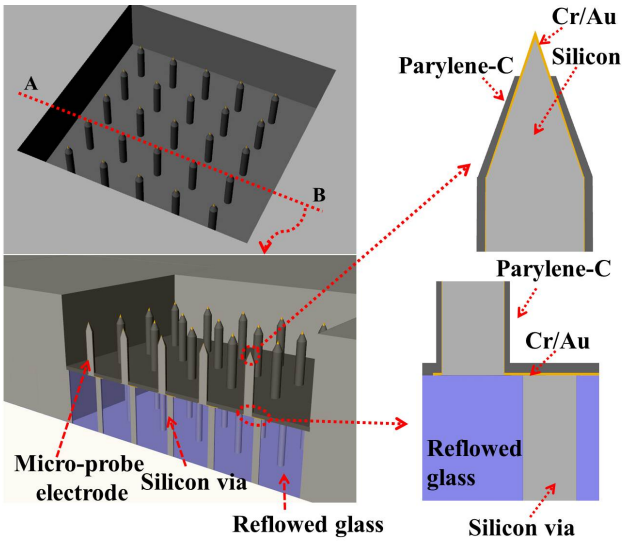


Figure 1. Schematic view of the proposed micro-probe electrode array

FABRICATION PROCESS AND RESULTS

The Fabrication process is shown in figure 2. Firstly, the SiO_2 etch mask for the silicon etching is deposited, using the plasma enhanced chemical vapor deposition (PECVD) process. A photoresist AZ4330 is used to pattern for silicon pillars. After patterning SiO_2 etch mask, the LRS was etched with DRIE process to form 250 μm-height silicon pillars. Residual photoresist and polymer from DRIE process are removed by O_2 plasma cleaning process. The SiO_2 etch mask is also removed by hydrofluoric (HF) etching process. Then, the borosilicate glass wafer is anodically bonded to the etched silicon wafer prior to the glass reflow process. For the reflowed glass to fill up completely between pillars, the vacuum pressure during bonding was kept 10^{-3} Torr. During glass reflow process in a furnace at 1030 ˚C for 5 hours, the boron ion in the glass wafer can diffuse into the LRS pillars, which makes the silicon vias have electrical resistance less than 2 Ω [10]. After CMP process of the reflowed glass surface, the SiO_2 etch mask is deposited by PECVD at the other side of the silicon wafer. After photolithography and

SiO_2 etch process, the LRS was etched with double DRIE and RIE process to form 70 μm-height silicon micro-probe structures. This fabrication method was composed of first DRIE, first RIE, second DRIE and second RIE process. The DRIE and RIE process conditions are summarized in table 1. In the first and second RIE process, the cylindrical silicon pillars are sharpened to form a tip shape. After second RIE process, the SiO_2 etch mask is blown, during the cleaning process. Cr/Au layer was deposited and patterned on the micro-probe structure to be connected to the silicon vias. A photoresist AZ 5214 is used to pattern the individual Cr/Au electrode. The parylene-C film was deposited for the insulating layer. For patterning the Parylene-C at only the tip end, the whole surface of micro-probe array with conducting and insulating layers was entirely coated with viscous photoresist AZ4620 in the spin coating process. The thickness of the photoresist at the tip end was very thin due to the micro-probe shape. As shown in figure 3 (a), the thickness of photoresist is very thin at the tip-end. After photoresist coating process, the isotropic etch process is performed for parylene-C etch at the tip-end. In the Parylene-C etching process with low selectivity, the photoresist at the tip ends is removed first and then, insulating layer, enabling the exposure of conducting layer only at the tip ends. The isotropic etch process were performed at RF power of 200 W with gas flow rates of 100 sccm O_2 and 5 sccm Ar. The process pressure was adjusted to 100 mTorr [11]. As shown in the magnified image of the probe tip (figure 3 (b)), the parylene-C is selectively etched at the tip-end. Finally, the photoresist is removed by cleaning process. Figure 3 (c) shows SEM images of the fabricated micro-probe electrode. The height and pitch of the micro-probe were measured to be approximately 70 μm and 190 μm, respectively.

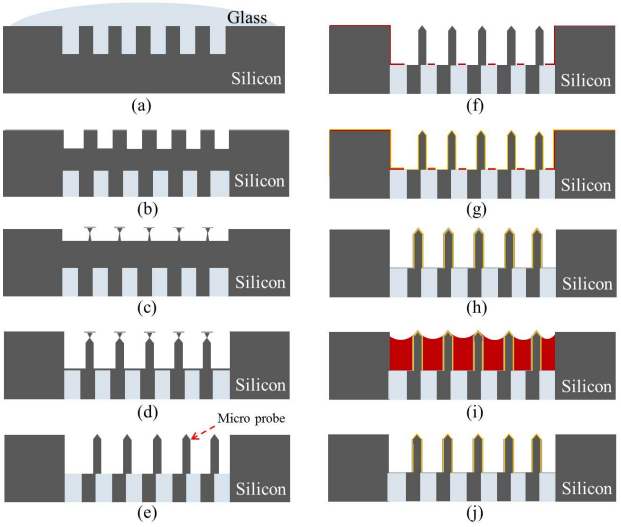
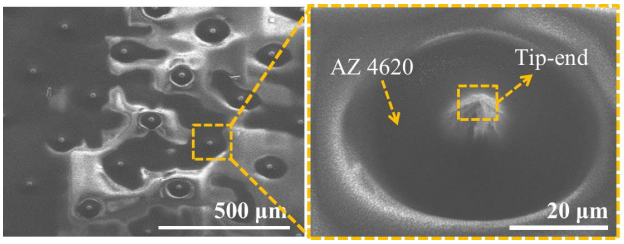


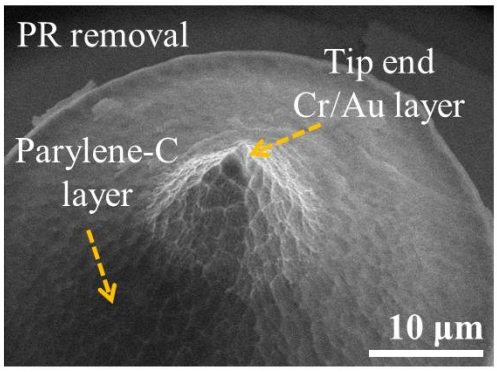
Figure 2. Fabrication steps of the micro-probe electrode array. (a) DRIE & Glass reflow; (b) Backside 1st DRIE; (c) 1st RIE; (d) 2nd DRIE; (e) 2nd RIE; (f) AZ5214 patterning; (g) Cr/Au deposition; (h) Lift-off process & Parylene-C deposition; (i) AZ4620 spin coating; (j) Parylene-C etching & PR removal.

Table 1. Etching condition for the DRIE & RIE process.

DRIE & RIE				
	Power (W)	**Pressure (mTorr)**	**Time (s)**	**Gas flow (sccm)**
Polymer deposition	825	22	5	C_4F_8 100 SF_6 0.5 Ar 30
Polymer etch	825	23	3	C_4F_8 0.5 SF_6 50 Ar 30
Silicon etch	825	23	5	C_4F_8 0.5 SF_6 100 Ar 30
Silicon etch (RIE)	825	23		C_4F_8 0.5 SF_6 100 Ar 30



(a)



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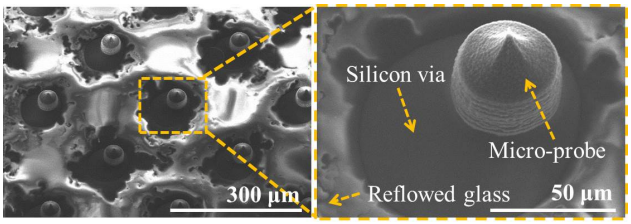
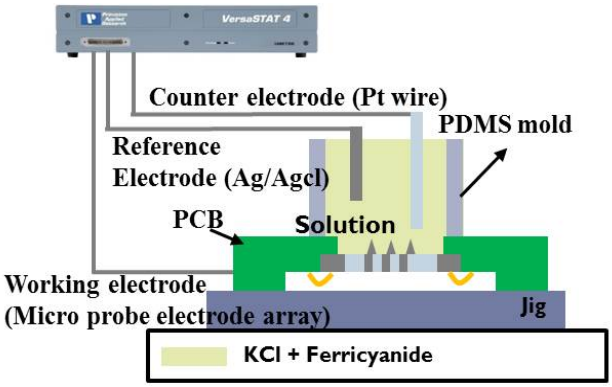


(c)

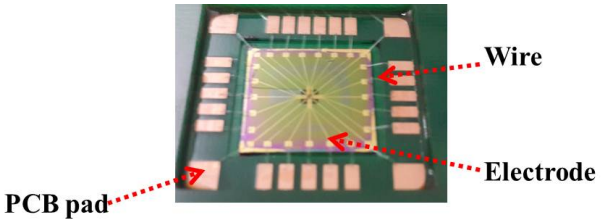
Figure 3. SEM images of the fabrication results: (a) AZ4620 photoresist coating; (b) Exposure of electrode at the tip end; (c) Fabricated micro electrode array

MEASUREMENT

The proposed micro-probe electrode array has been verified with the electrochemical reaction measurements with CV experiment. For the measurements of independent micro-probe electrodes, each electrode was individually wire-bonded to PCB board. The CV was measured in a 0.1M Fe[(CN)6]4- and 0.1M KCL solution in a three-electrode measurement setup shown in figure 4 (a). The micro-probe tip-end electrode was used as a working electrode and then Pt wire and Ag/AgCl were used as a counter electrode and a reference electrode, respectively. The CV was measured at a 50 mV/s scan rate with the voltage range of -0.7 V to 1.4 V. The measurement results are shown in figure 5. The measured current was proportional as increasing the number of tips which are connected individually to the potentiostat through the silicon TGVs with bonded wires. As the above results, the micro-probe array exhibits independent measurement with individual addressing. To analyze the CV results, the micro-probe array was estimated by current limiting equation based on conical electrode theory [12]. The measured peak current value with different numbers of micro-probe arrays were compared with the estimated values based on limiting current equation. As shown in table 2, the measured peak current was found to be in good agreement with the estimated values.



(a)



(b)

Figure 4. Cyclic voltammetry measurement: (a) Experimental setup for CV measurements (b) Wire bonded interconnections on the backside of the sample

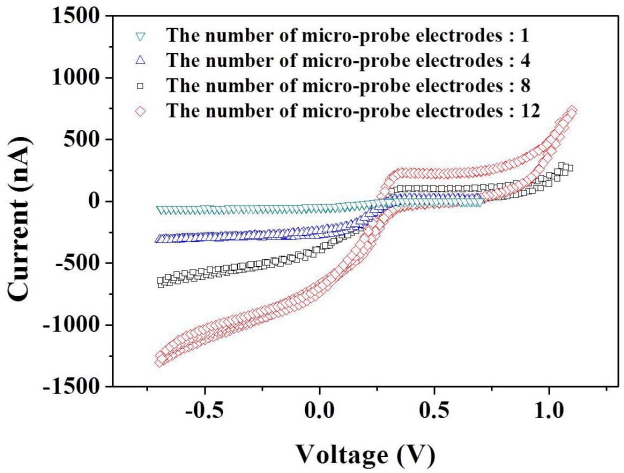


Figure 5. Cyclic voltammetry measurement results as increasing the number of micro-probe electrodes connected to the potentiostat individually through the silicon vias.

Table 2. Comparisons of the measured current with the estimated values.

Number of tips	Current (μA)		
	Estimated value	Measured value	Error (%)
1	84 nA	90 nA	7.00 %
4	337 nA	350 nA	3.86 %
8	674 nA	650 nA	3.56 %
12	1011 nA	1250 nA	23.6 %

CONCLUSION

In this study, a micro-probe electrode array with independent interconnections through the substrate was presented. The micro-probe was fabricated by multi DRIE and RIE process. The silicon via for electrical connection through reflowed glass substrate has low resistance value because the boron ion in the glass wafer can diffuse into the LRS pillars during glass reflow process. The electrochemical characterization of the fabricated micro-probe electrode array was verified with CV measurement method.

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