HIGH-YIELD INDIUM-BASED WAFER BONDING FOR LARGE-AREA MULTI-PIXEL OPTOELECTRONIC PROBES FOR NEUROSCIENCE

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ABSTRACT

This paper reports on the yield optimization of a wafer-level indium (In)-based bonding process for joining 4-inch sapphire and silicon (Si) wafers. The process allows to realize neural probes with integrated micro light-emitting diodes (µLED) for optogenetic applications. The sapphire substrates comprise 6-µm-thick gallium nitride (GaN)-based µLEDs with lateral dimensions down to 50×50 µm², which are transferred by the In-based bonding process onto gold pads on a Si wafer with interconnecting leads. Challenges that needed to be addressed in this context were the patterning of In on top of the GaN structures and thermomechanical stress limiting the overall bonding yield. The first challenge was met using a bilayer lift-off process; the yield was optimized by using an analytical model supported by an experimental study systematically varying the bond metal thickness t_{In} and the normalized bond area $A_{norm} = A_{pads}/A_{wafer}$, where A_{pads} and A_{wafer} denote the total area of all bond pads on the wafer and the wafer area, respectively. The stress-induced rupture of bond interfaces is completely suppressed when $t_{In} \geq 3$ µm and $A_{norm} \geq 15\%$. The optimized In-based bonding process was successfully applied to realize 2D µLED arrays with high yield.

INTRODUCTION

Optogenetics describes the interaction between neural tissue and light mediated by light-sensitive molecules [1] called opsins, such as Channelrhodopsin-2 (ChR2). These opsins are introduced into the cell membrane by viral transfection [2]. The cell-type specific stimulation and inhibition of neural activity using various opsins sensitive at different wavelengths represents a new approach in neuroscience. With a peak sensitivity of ChR2 at a wavelengh of 470 nm [3], neuronal tissue can be efficiently stimulated using GaN-based LEDs.

Various approaches have been conceived to realize neural implants with integrated GaN-based µLEDs [3]. In one approach, such devices are obtained by starting with a GaN-LED layer stack grown on a sapphire substrate [4]. For this purpose, the GaN layer is first patterned by dry etching to define the µLEDs. Thereafter a sapphire etch process allows to delimit the probe shafts. However, this latter process is challenging for the lack of an appropriate anisotropic sapphire etching technique.

Alternatively, the GaN-LED layer stack can be directly deposited onto a silicon wafer, thereby simplifying the 3D patterning of the probe shafts [5]. However, this approach leaves room for improvement as far as the internal quantum efficiency of the µLEDs is concerned. A third approach aims at combining the particular advantages of the aforementioned techniques: the GaN LED layer stack is grown on a sapphire substrate to achieve an optimized internal quantum efficiency. The µLEDs are subsequently transferred to a Si wafer using wafer-level In-based metal bonding and laser lift-off processes [6]. The Si wafer can easily be patterned into probe shafts using standard MEMS fabrication techniques. However, due to the difference in the thermal expansion coefficients of sapphire and silicon, considerable residual stress builds up at the bond interface after In bonding. This strongly affects the bond yield by the potential fracture of bond interfaces.

This work investigates the In-based wafer-bonding process for joining sapphire substrates comprising µLED structures with silicon wafers destined to carry the µLEDs. The focus of this process optimization study is on the one hand on the In layer thickness t_{In} and on the other hand on the normalized bond area A_{norm}. The goal is to ensure a high-quality bond formation across the entire wafer sandwich.

ANALYTICAL MODEL

In a first step we applied an analytical model to describe the influence of A_{norm} and t_{In} on the shear stress in the In bond layer [7]. The model is based on a three-layer system, as shown in Fig. 1, where layers #1 to #3 represent the sapphire wafer, the In bond layer and the Si substrate, respectively. In this model, all exerting forces are defined for the three-layer system.

Due to differences in the coefficients of thermal expansion of the applied materials (Si: $\alpha_{th,Si} = 2.6\times10^{-6}$ K^{-1}; In: $\alpha_{th,In} = 56\times10^{-6}$ K^{-1}; sapphire: $\alpha_{th,sapphire} = 5.6\times10^{-6}$ K^{-1}) an inner force F_n (n = 1,..,3) develops within the layers as a

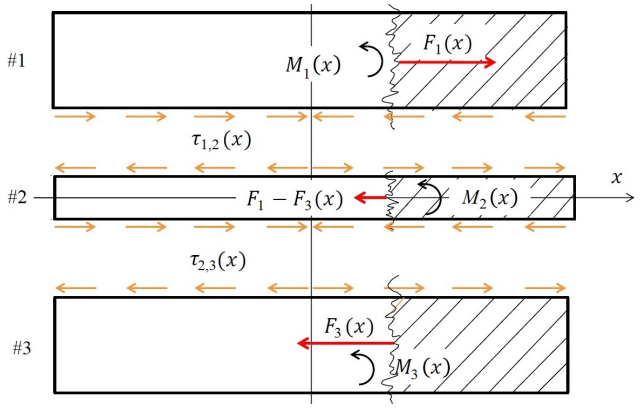

Figure 1: Model of the three layer system to calculate the inner forces F_n and moment M_n in layer #n (n = 1,...,3) and the respective shear stress $\tau_{n,m}$ between different layers n and m.

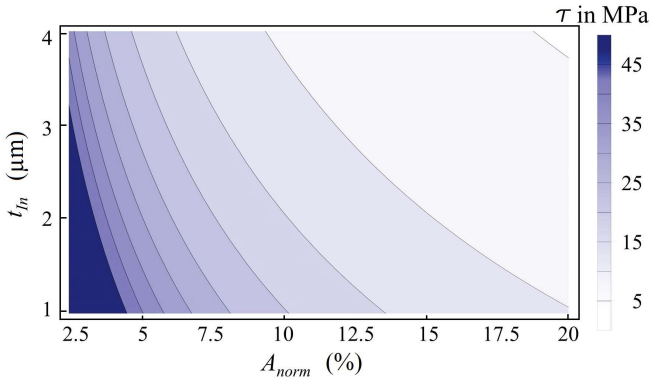

Figure 2: Calculated shear stress in the In bond layer as a function of bond layer thickness t_{In} and normalized bond area A_{norm} for joining 4-inch sapphire and silicon wafers by In-based wafer bonding at 140 °C.

result of cooling down from the bonding temperature T_B. As a result of cooling, the interface between Si and In is stretched since $\alpha_{th,Si} < \alpha_{th,sapphire}$. In contrast, the sapphire compresses the In-sapphire interface. Because Si and sapphire are bonded by the In layer, both wafers experience bending moments M_n (n = 1,..,3), which are also taken into account in the calculation. The combined effects result in shear stress at both material interfaces between the In layer and the two wafers. As the shear stress on both sides of the bond metal are pointing in opposite directions, they need to be added to determine the residual stress in the bond layer, which is crucial for a successful bond.

The calculated residual shear stress obtained when 4-inch silicon and sapphire wafers are bonded with t_{In} and A_{norm} varied between 1 µm and 4 µm, and between 2.5% and 20%, respectively, is shown in Fig. 2. Obviously, the shear stress in the bond layer can be reduced by increasing both t_{In} and A_{norm}. The shear strength of In being in the range of 5 to 10 MPa [8], it is obvious that the wafer bond will not likely achieve a high yield for $A_{norm} < 10\%$ and $t_{In} < 2$ µm. Taking the lower limit of the In shear strength of 5 MPa, values of $A_{norm} = 20\%$ and $t_{In} = 4$ µm seem recommendable when aiming for stable bond interfaces.

FABRICATION

In order to support the conclusions of the analytical model, test structures with different A_{norm} and t_{In} values were fabricated. The test structures comprise up to 4-µm-thick In layers on top of 6-µm-high µLED structures. The photolithography required a lift-off photoresist with a thickness of at least 14 µm. The precise definition of the undercut length for a well-controlled metal lift-off is mandatory: on the one hand an insufficient undercut causes metal deposition on the resist sidewalls, thus prohibiting a clean metal lift-off, while large undercut lengths degrade the lateral resolution of the process.

Figure 3 illustrates the main steps of the lithography and bonding processes. The bilayer resist {Fig. 3(a)} comprises a photo-insensitive resist (LOR 30B, Microresist Technology, Berlin, Germany) and a standard positive resist (AZ 4533,

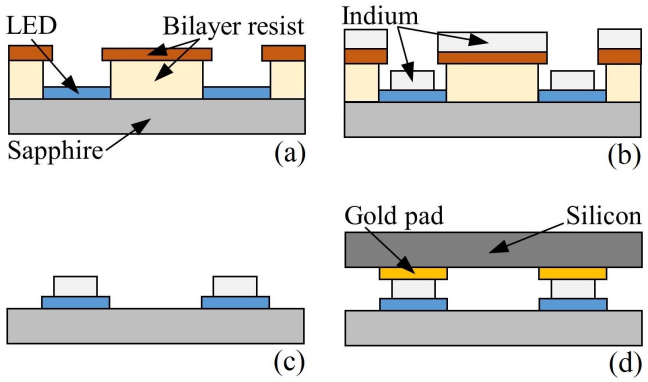

Figure 3: Schematic of bilayer resist lift-off technique and subsequent wafer bonding. (a) Lithographic patterning of a 15-µm-thick bilayer resist on µLEDs; (b) Thermal evaporation of a 4-µm-thick In bond layer; (c) Lift-off of resist and surplus In; (d) Wafer-level bonding of silicon to sapphire.

MicroChemicals, Ulm, Germany). The LOR 30B resist is deposited by two-step spin-coating. The first layer serves to planarize the recesses between the µLED structures. The second layer is then deposited to a thickness of at least 120% of the planned In height. After exposure of the AZ 4533 resist, it is developed using a standard developer (AZ 726, MicroChemicals) that simultaneously removes the LOR 30B layer underneath. The development rate of the LOR 30B resist is adjusted by the soft bake temperature. As shown in Fig. 4, undercuts from 1 µm to 20 µm, as determined by optical microscopy, are reliably achieved.

Because the LOR 30B resist dissolves isotropically, the achievable lateral resolution is correlated with the resist height. This is documented in Fig. 5 showing the line and space resolution of the bilayer resist process. For a 5-µm-thick LOR 30B resist a distance of at least 10 µm is required between the structures to guarantee a successful patterning of laterally separated In bond pads.

The In used for thermal evaporation {Fig. 3(b)} is

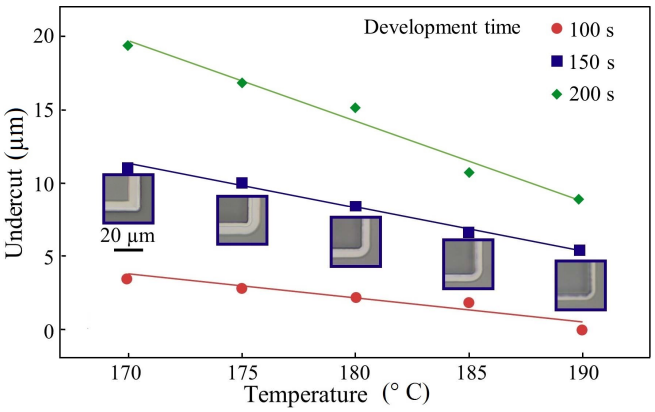

Figure 4: Undercut of bilayer resist as a function of soft bake temperature and development time. The inset photographs show the undercut around the edge of a bond pad at a development time of 150 s. The dissolution rate is determined by the soft bake temperature while the total undercut is adjusted by the development time.

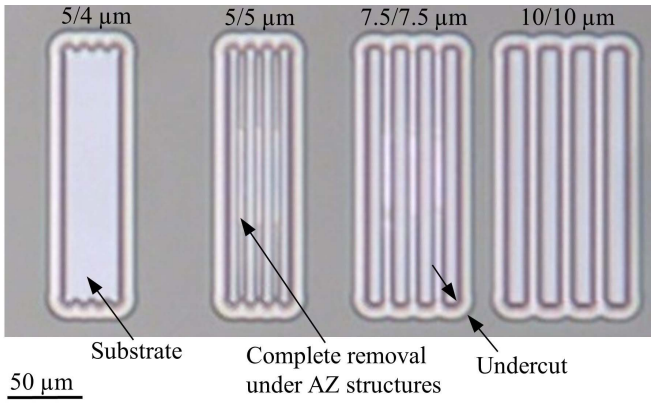

Figure 5: Line and space resolution of LOR30B. Structure with 5 µm/4 µm line and space could not be resolved, while 5 µm and 7.5 µm patterns exhibit a local complete removal of the LOR 30B resist from under the AZ structures, as indicated by brighter areas. 10 µm/10 µm structures show the desired result.

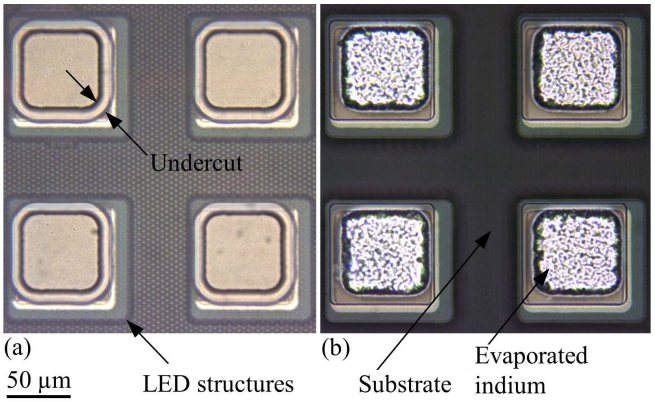

Figure 6: (a) µLED structures with developed bilayer resist on top. The undercut is clearly visible as two parallel lines surrounding the pad. The inner line corresponds to AZ4533, while the outer line to the LOR30B; (b) µLED with 4-µm-high patterned In on top, deposited by thermal evaporation and structured with the bilayer lift-off process.

melted into nuggets of ca. 2 g. After removal of the natural In oxide on the nugget surface in 10 vol% hydrochloric acid, the nuggets are directly transferred into the evaporation chamber, which has to be evacuated without delay to prevent any re-oxidation. Indium is then thermally evaporated at a deposition rate of 1-2 nm/s. The metal lift-off {Fig. 3(c)} is performed by immersing the wafers in dimethyl sulfoxide (DMSO) at 80 °C for 30 min under ultrasonic agitation and cleaning them in isopropanol at room temperature.

Figures 6(a) and (b) show an exemplary bilayer resist structure and In bond pads with lateral dimensions of 50×50 µm^2 after resist lift-off and removal of surplus In, respectively. The resulting sapphire wafers with In pads are then bonded to silicon carrier wafers comprising corresponding gold (Au) bond pads with a thickness of 300 nm. The Au-In interdiffusion bonding was carried out at a bond temperature of 140 °C. For bonding {Fig. 4(d)}, the wafers are aligned (mask aligner MA/BA6, SÜSS, Germany) and transferred to the bonding chamber (SB6, SÜSS). A pressure of 80 kPa is applied while the wafers are heated to a bond temperature of 140 °C, kept there for 30 min, and cooled back down to room temperature. The constant pressure prevents the bond contact to rupture during the cooling phase. At room temperature the wafer sandwich shows the expected concave bow {cf. Fig. 7}.

EXPERIMENTAL RESULTS

The wafer bow measurement was used as a first indicator for the bond quality. As shown in Fig. 7, three different regimes can be identified. Wafer bonds with low bond yield and large un-bonded area exhibit a wafer bow below 50 µm, which indicates an effective stress relaxation by bond rupture {Fig. 7, red dashed curve}. Wafers with an improved but still insufficient yield exhibit bond failures mostly at the wafer edges as expected from the analytical model {Fig. 7, yellow dotted curve}. In contrast, fully bonded wafers show a homogeneous bow across the entire wafer with a total height difference of up to 500 µm {Fig. 7, green solid curve}. Bonded wafer pairs with a bow of similar magnitude show no ruptured bond interfaces.

Figure 8 summarizes the bond yield results of the parameter study. It shows the fraction of successfully bonded area normalized to the wafer area as a function of t_{In} and A_{norm}. The numbers were obtained by observing Newton's rings between the sapphire and Si wafers. Unbonded regions are indicated by the mobility of Newton's rings under load, whereas Newton's rings in successfully bonded areas are stationary.

The red area in Fig. 8 represents wafer sandwiches so unstable (bond yield ≤ 13%) they could not be processed further. Wafer sandwiches in the yellow region (bond yield 60% to 85%) still contained areas lending themselves for further processing, since the bond rupture is localized along the wafer rim. Fully bonded wafer pairs were achieved using bond parameters from the green, rupture-free region. Distinct trends are apparent in Fig. 8 regarding the influence of the

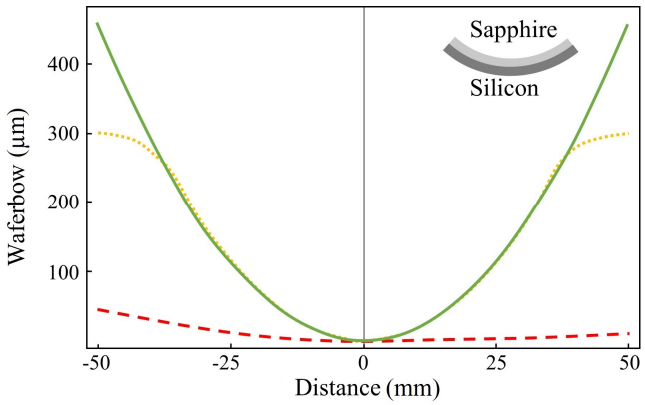

Figure 7: Wafer bow across the whole wafer indicating the quality of the performed bond process. The red dashed curve shows a wafer with low bond yield while. The yellow dotted curve indicates stress relaxation towards the wafer edges due to bond rupture. The green solid is from a successfully bonded silicon-sapphire wafer pair.

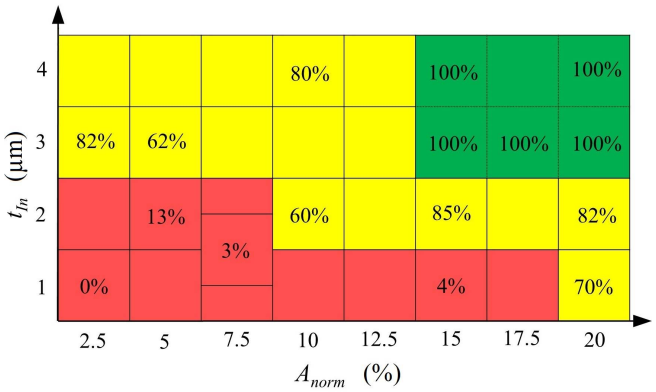

Figure 8: Experimental outcome of the wafer bond test as a function of A_{norm} and t_{In}. Colors are consistent with the wafer bow results in Fig. 7. Percentages highlight the successfully bonded wafer area fraction. The expected bond regimes of intermediate parameter sets, without a percentage given, were interpolated.

varied parameters. An increase of both t_{In} and A_{norm} enhances the bond quality leading to higher bond yield, in agreement with the analytical model.

After bonding sapphire and silicon wafers using the optimized parameters, we continued processing them as described previously [6]. Thereby the sapphire wafer is released using laser lift-off and the Si substrate is separated into optical probes with integrated µLED arrays using the etching before grinding technology [9]. As an example, Fig. 9 shows a 12×12 arrays of 50×50-µm²-sized µLEDs arranged at a pitch of 100 µm.

CONCLUSION

This paper reports on the optimization of an In-based bond process for joining 4-inch sapphire wafers carrying GaN-based µLEDs with Si carrier wafers with interconnecting leads needed for realizing multi-pixel optoelectronic probes for neuroscience. An analytical model used to extract the mechanical stress between the sapphire and Si wafers was validated by a technological parameter study.

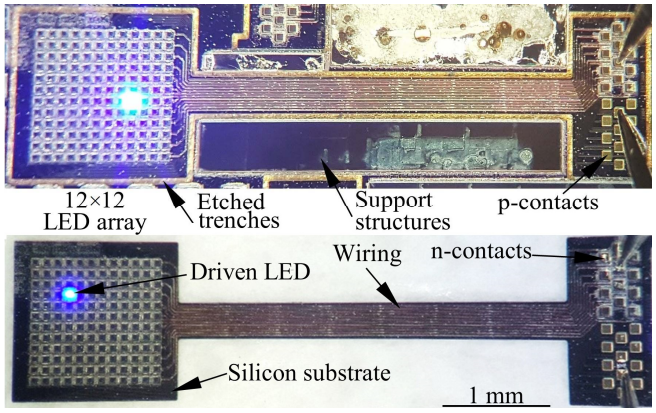

Figure 9: 12×12 µLED-array for optogenetic research: (a) Probe on Si wafer before release by grinding the backside and (b) released device; LED size: 50×50 µm², LED pitch: 100 µm.

The optimized bonding process takes advantage of a bi-layer resist enabling up to 4-µm-thick In layers. Successful full area wafer bonding was achieved using optimized parameters of $t_{\mathrm{In}} \geq 3$ µm and $A_{norm} \geq 15\%$.

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