ULTRA HIGH ASPECT-RATIO AND THICK DEEP SILICON ETCHING (UDRIE)

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ABSTRACT

We report an advanced deep-reactive-ion-etching (DRIE) process developed specifically for etching ultra-deep structures in thick (>500µm) silicon wafers with high aspect-ratio and straight sidewalls across a wide range of feature sizes and patterns. This is achieved by ramping critical process parameters throughout the etching duration. 600-800µm deep trenches with widths as small as 20-40µm are etched in 1mm-thick silicon wafer, and are expected to be etched through a 1mm wafer with thicker and/or higher selectivity masking materials. We have produced holes >500µm deep with hole diameters as small as 25µm, and potentially with 10-15µm diameter holes. This ultra-deep silicon etching process will benefit both IC integration and emerging MEMS applications at micrometer and millimeter scale that demand high-resolution deep DRIE.

Index Terms—*deep reactive ion etching; DRIE; ultra-high aspect-ratio; through wafer DRIE; DRIE with ramped recipe parameters; through silicon via (TSV)*

INTRODUCTION

Deep reactive ion etching (DRIE) has been widely adopted by the MEMS community in fabricating high aspect-ratio MEMS devices [1]. Reported plasma-based DRIE techniques are time-multiplexed processes based on a sequential recipe alternating between a passivation step and an etching step to achieve anisotropic etching [1-5]. The most prevalent DRIE process is known as the Bosch process [2]. During the passivation step a polymer layer is deposited isotropically on the bottom and sidewall of the region that is being etched. In the next sub-cycle, the passivation polymer layer at the bottom of the etch region is removed while the sidewall passivation remains intact due to the directionality of plasma bombardment. The underlying silicon is now exposed and is etched, resulting in an anisotropic etch. Bosch DRIE has the ability to etch very precise, deep, narrow, and vertical structures.

DRIE is applied to a wide range of applications from micrometer-scale high-resolution high aspect-ratio features [1-2, 6-7] to millimeter-scale ultra-deep high aspect-ratio structures [8-10]. However, DRIE technologies confront several issues for ultra-deep, well-controlled, high aspect ratio (HAR) features (Figure 1). Standard BOSCH DRIE recipes utilize fixed process parameters and suffer from aspect-ratio dependent etch (ARDE) and DRIE lag. Etch rate and profile are also pattern-dependent: trenches with the same width as the diameter of circular holes etch faster. In addition, one of the current trends for through-silicon via (TSV) fabrication is to increase the aspect-ratio with the same diameter (i.e. to increase the via depth) to address thermal dissipation and warp issue [11-12]. It will also assist subsequent passivation and via plating steps. All these issues are observed even when the depth of silicon DRIE is limited to <500µm [6-7]. For some emerging applications, millimeter-scale deep structures are needed in which the issues mentioned above get more challenging to overcome.

In this paper we report an advanced DRIE process to address these shortcomings for ultra-high aspect-ratio ultra-deep etching of silicon structures (Figure 1). 600-800µm deep trenches with trench width as small as 10-20µm, and as large as 100µm in 1mm thick silicon wafers are etched with effectively suppressed ARDE effect. The sidewall profiles indicate the etching recipe has not reached its limits and greater etch depth approaching or exceeding 1mm is feasible. In addition, etching of narrow trenches (2-3µm wide) is demonstrated with aspect ratio exceeding 90:1 with reduced undercut. Sidewall slopes of narrower trenches (<10µm) are slightly positive (>89.50°) whereas those of wider trenches are readily tuned by adjusting process parameters to achieve either positive or negative slopes. Furthermore, circular holes with various diameters as small as 25-35µm can be etched all the way through 550µm thick silicon wafers with slight positive sidewalls.

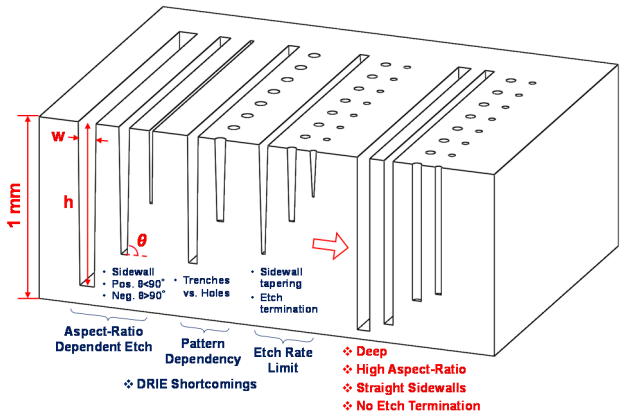

Figure 1: Ultra-deep ultra-high aspect ratio etching of thick silicon wafers (≥1mm) with high aspect ratio and straight sidewalls across a wide range of feature sizes and patterns using the novel etching process with ramped DRIE parameters.

This ultra-deep silicon etching process will benefit both IC integration and immerging MEMS transducer applications at micrometer and millimeter scale.

DESCRIPTION OF THE NEW METHOD

To overcome the DRIE shortcomings in Figure 1, we introduce a method for improving the achievable aspect-ratio as well as reducing ARDE for ultra-deep DRIE by dynamically ramping the process parameters including the 380 kHz bias power during etch step, the step times, and the chamber pressure. We also compare the new recipe

with the standard fixed-parameter recipe for deep etch in order to demonstrate its advantages.

Standard Fixed Parameter Process

The experiments reported are conducted using a SPTS Pegasus 4 inductively coupled plasma (ICP) etcher. Standard DRIE recipes have fixed process parameters throughout the etch. For etching relatively small (1-100µm) features with a vertical, smooth sidewall and minimal undercut, the etcher is conditioned to operate at an ICP power level of 2800W and a RF bias power at 60W. At 30mTorr chamber pressure, C_4F_8 and SF_6 are alternated between the passivation and etching steps.

2-5µm wide trenches (>1000µm in length) are patterned and etched for 150min with the fixed-parameter DRIE process. The widths of the trenches for all the feature sizes narrow toward the bottom of the trenches as shown in Figure 2. This standard recipe provides an average etch rate of <1.5µm/min for 2µm wide trenches and <2µm/min for 5 µm features. The 5 µm trench closes at a depth of <290µm.

Holes with different diameters ranging from 15–35µm are also etched with the standard fixed-parameter recipe. As shown in Figure 3, 15µm diameter holes <400µm were etched within 210min. The apparent etch rate is similar to that of 5µm trenches at ~2µm/min while 35µm holes are etched through. Tapering of sidewalls and closing of features are observed toward the bottom of the holes. Since the sidewalls converge to points at the very bottom, sharp points are not observed by cleaving the silicon wafers as in the deep trenches shown in Figure 2.

This standard fixed-parameter recipe is used as a baseline recipe to develop and tune the dynamic recipe with ramped process parameters.

Advanced DRIE with Ramped Process Parameters

Modern plasma etching tools allow two or more sequential recipes back-to-back to be used to address aspect-ratio dependent plasma etch and create desired structure. For example, one can perform an anisotropic RIE etch, an isotropic etch and a Bosch DRIE one after another by programming the sequence.

Continuous adjustment of process parameters has also been proposed to address aspect-ratio dependent plasma etch. Teixeira et. al. [13] proposed programming a governing function with initial parameters that determines how the parameters are to be transitioned.

In this work, DRIE etch parameters are gradually and continuously varied to compensate for DRIE shortcomings (ARDE effects, sidewall profile tapering and etch depth for both limitations for small and large features). Thus the etch is better optimized at each etch depth as the etch proceeds.

We ramp three parameters of the DRIE etch cycle: 380kHz RF platen bias power, etch step duration, and chamber pressure. Reduced etch rate in deep high aspect-ratio structures is compensated by enhancing the etching agents effect, this includes increasing the 380kHz bias power during etch step from 60W to 140W, increasing the etch step time from 2s to 2.6s, decreasing the passivation step time from 2s to 3.5s, ramping the passivation step chamber pressure from 24mTorr to 34mTorr, and ramping the etch step chamber pressure from 30mTorr to 15mTorr.

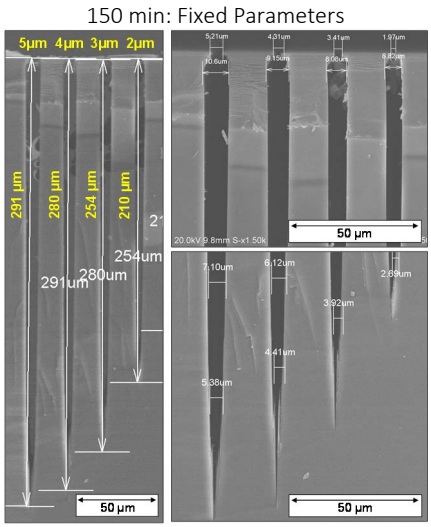

Figure 2: 2-5µm wide trenches etched for 150min using fixed-parameter DRIE process. DRIE lag and aspect-ratio dependent etching (ARDE) effects are observed.

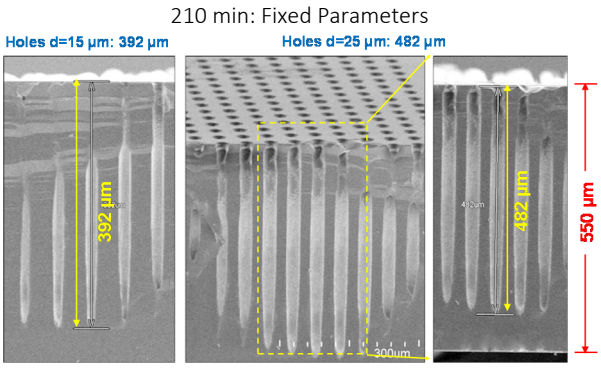

Figure 3: 15µm and 25µm diameter holes etched by the fixed-parameter DRIE process for 210min.

Microfabrication Process

For characterization of the ramped-parameter silicon DRIE process, experiments were carried out on 4-inch-diameter lightly doped p-type (10-20 Ω-cm) silicon wafers of <100> orientation. The silicon wafers are patterned with a wide range of patterns and feature sizes: trenches (long lines) with width ranging from 1µm to 100µm; and circular holes with 10, 15, 25, 35µm diameters.

1mm thick silicon wafers are used to characterize the etch of wider width trenches while 550µm thick wafers are used to characterize narrower width trenches and holes.

Thick oxide hard mask in addition to thick photoresist is needed to preserve sufficient DRIE masking material toward the end of long silicon DRIE with ramped-up RF bias power and etch step time since mask erosion rate increases throughout the process when dynamic process control is employed. In addition, lithography resolution will limit how precise the small-feature patterns can be transferred to a thick masking layer, whether it is thick oxide or thick photoresist. In the future, deep etch of relatively larger features (>10µm) may take advantage of new developments in ultra-thick PR to achieve a larger etch depth [14].

For >150min DRIE with the ramped-parameter process, 4µm thick LPCVD SiO_2 layer along with 10µm SPR220(7.0) photoresist layer is used as masking materials for feature sizes of >10µm, and 4µm LPCVD SiO_2 along with ~3µm SPR220(7.0) photoresist as masking materials for feature sizes of 1-10µm.

1µm wide trench patterns need to be precisely transferred to the oxide mask with vertical sidewalls, thus they are patterned using a GCA AS200 AutoStepper with 5:1 reduction and etched using SPTS APS Dielectric Etcher for high sidewall verticality.

EXPERIMENTAL RESULTS

Since real-time in-situ process monitoring tool is not available in the SPTS Pegasus Etcher, cross-sectional SEMs are used to characterize the DRIE profile and etch rate.

Deep HAR Trenches

DRIE of narrow trenches (2-10µm wide and >1000µm in length) in 500µm thick silicon wafers using the advanced ramped-parameter recipe for 150min is demonstrated in Figure 4 with increased etch rate, reduced undercut, suppressed ARDE, and aspect-ratios exceeding 90:1 compared to Figure 2.

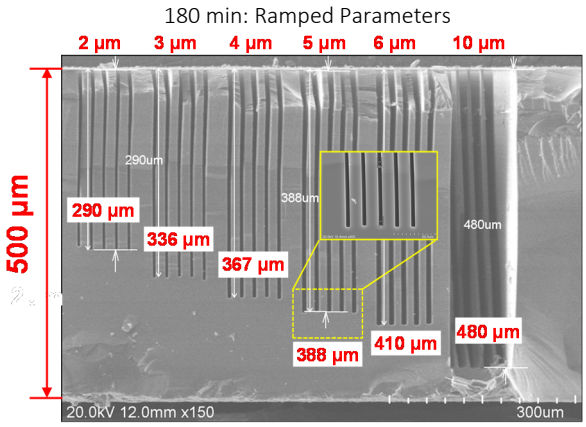

Figure 4: 150min DRIE of 2-10µm wide trenches using the ramped-parameter DRIE recipe. The etch rate is increased, the DRIE ARDE, lag effect and undercut is reduced and aspect-ratios exceeding 90:1 is obtained.

In contrast to the 150min DRIE using fixed-parameter process with tapered sidewall and converged trench bottom shown in Figure 2, the ramped-parameter process results in flat trench bottom even after 180min (3 hours) etch (Figure 5). The widths at the bottom of the trenches are reduced by only 10-15% from the original feature sizes on the mask. The overall etch rate is increased by >25% for all feature sizes when using the ramped process compared to the fixed-parameter process.

In another test, 10-100µm wide and >1000µm long trenches are patterned on a 1mm thick silicon wafer and etched for >130min (Figure 6). The sidewall slopes are slightly positive ($89.50° < \theta < 90°$) for relatively narrow trenches (1-10µm and 10-25µm), and slightly negative ($\theta > 90°$) for wider trenches (>25-100µm). We plot trench depth vs. trench width in Figure 7 and show that ARDE is effectively suppressed for trenches >20-25µm wide and are easily etched to more than 600µm deep. The flat trench bottom and nearly vertical sidewall profiles indicate the etch has not been tested to its limit and can go through 1mm with additional time.

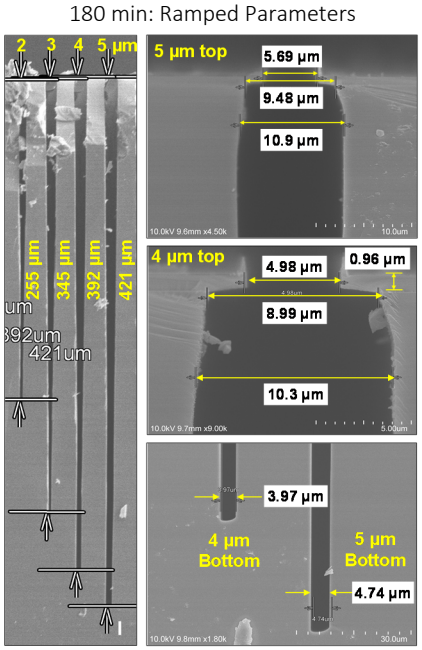

Figure 5: 2-5µm wide trenches etched for 180min with ramped-parameter DRIE process: nearly vertical sidewalls ($89.50° < \theta < 90°$) and flat trench bottom with suppressed ARDE and reduced DRIE lag effect.

Deep HAR Circular Holes

Circular holes with various diameters from 15-25µm are also tested. In contrast to the converged bottoms of trenches, the ramped-parameter process creates flat bottoms with increased etch rate (Figure 8). 25µm diameter holes are etched >500µm within 150min with the ramped process, whereas only being etched <400µm deep within 210min by the fixed-parameter process.

Comparison of trench and circular hole etch indicate that the in-plane aspect-ratio (length /width, L/W) of the features being etched play an important role on the etch depth and etch rate. 15µm wide trenches reach a depth of more than 520µm whereas the 15µm diameter circular holes only reach a depth of >400µm etched with the same 150min ramped-parameter process. Another rectangular trench (8µm × 50µm) is also etched deeper than 15µm diameter circular holes. This confirms that etch rate is dependent on the in-plane aspect-ratio (W/L): long lines etch considerably faster than circular holes of the same width, or of even larger width.

CONCLUSION

We report an advanced customized BOSHC DRIE process with dynamically ramped process parameters to compensate for DRIE aspect-ratio dependent etching (ARDE) and DRIE lag effect. Reduced etch rate in deep high aspect-ratio structures is compensated by gradually and continuously enhancing the etching agents by ramping the 380kHz RF platen bias power, etch sub-cycle duration, and chamber pressure throughout the DRIE process. We demonstrated ultra-high aspect-ratio ultra-deep etching in 1mm thick silicon substrate for a wide range of feature sizes from <10µm to 100µm, and for both trench and circular hole patterns.

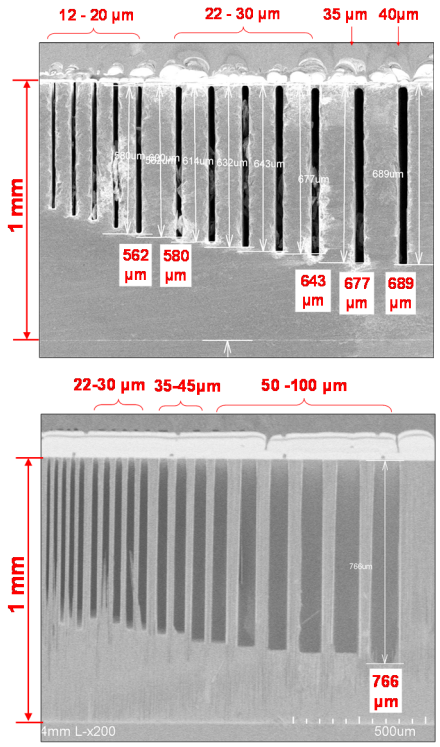

Figure 6: Ultra-deep DRIE characterization for 10–100µm wide trenches in 1mm thick silicon wafer etched by the ramped-parameter DRIE recipe for >130min.

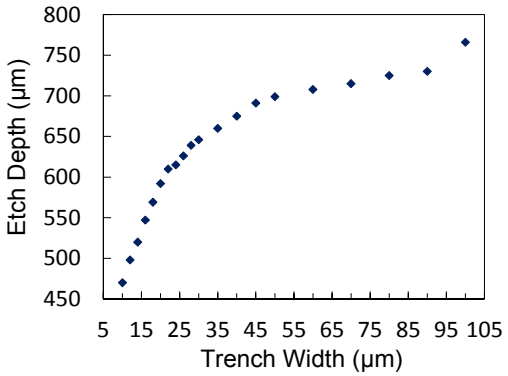

Figure 7: Trench etch depth vs. trench width for deep ultra-high aspect-ratio DRIE results of 10-100µm wide trenches.

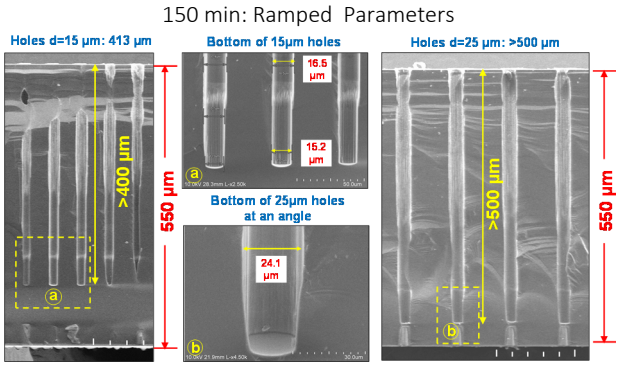

Figure 8: 15µm and 25µm diameter holes etched by ramped-parameter DRIE process recipes after 150 min: increased etch rate and flat hole bottom.

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