SILICON NANOWIRE ARRAYS THERMOELECTRIC POWER HARVESTER

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ABSTRACT

This study aims to investigate the performance of Silicon Nanowire Arrays (SiNWAs) and bulk Si material as thermoelectric power harvesters. SiNWAs were developed using a two-step metal-assisted chemical etching technique. The fabricated thermoelectric devices of 1 x 1 cm p- and n-type SiNWAs each have a diameter of 70-100 nm, and an approximate nanowire length of 6 µm. Bulk Si devices were also tested as a benchmark for the SiNWAs thermoelectric devices. The heat flow across the SiNWAs devices exhibits a higher temperature difference, ΔT, between hot and cold junctions, compared to bulk silicon devices. This reveals that the heat capacity, C, of silicon is reduced significantly by the presence of nanowires. Consequently, a reduction in C also reduces the thermal conductivity of silicon, which is favourable for a good thermoelectric material. Compared to bulk silicon, SiNWAs thermoelectric devices also demonstrate higher Seebeck voltage, V_{oc}, and Seebeck coefficient, S. The voltage rises as the ΔT between two junctions increases. An increase in V_{oc} and S in the SiNWAs thermoelectric device aids to improve the figure-of-merit and the efficiency of the thermoelectric device. Experimental characterization of all fabricated thermoelectric devices suggest that the p-SiNWAs device possesses the highest ΔT of 17ºC at 40 sec; V_{oc} = ~35 mV and S = ~8 mV/K.

INTRODUCTION

A thermoelectric device is a low cost power harvester that converts ambient, human body or unused heat into electrical energy. This device has no moving parts, which makes it easily scalable and noiseless. Moreover, it has no emissions, which thus leads to a healthier environment [1]. A thermoelectric power harvester is currently applied in several applications, including wrist watches [2], biomedical monitoring systems [3], biometric sensors [4], and autonomous wireless sensors for body area networks [5]. The thermoelectric devices that are available in today's market are commonly composed of a bismuth-tellurium compound that has proven to be highly efficient with a figure-of-merit (ZT) of more than one [6].

However, these materials are costly due to the limited sources and toxicity. Alternatively, silicon, a semiconductor material which is widely used in microelectronic devices, may be a prominent material for application in thermoelectric devices. However, bulk Si has a relatively high thermal conductivity of around ~150 $Wm^{-1}K^{-1}$ at room temperature, contributing a ZT of 0.01 at 300 K. On the other hand, nanostructured Si can be used to enhance thermoelectric efficiency.

Numerous studies in the literature report the hundredfold reduction of thermal conductivity in silicon nanowires as a result of suppressed phonon distribution [7-9], which helps to improve the ZT of thermoelectric devices. Although many studies on thermoelectric materials have been reported, there are gaps that need further investigation, including the heat flow in SiNWAs thermoelectric devices.

This paper reports a comprehensive study of SiNWAs and bulk Si material as a thermoelectric power harvester. The effects of etching time to the length of nanowires that are formed by using step metal-assisted chemical etching (MACE) technique are investigated. Besides, the amount of heat flow across the devices that affects ΔT across hot and cold junctions, and thermal conductivity of the material, is examined. Additionally, the voltage generated from the device is measured, and the S of SiNWAs thermoelectric devices are calculated.

DEVICE WORKING PRINCIPLE

The theory underlying thermoelectricity involves the movement of the majority carriers (holes and electrons) that exist in a semiconductor. When a semiconductor material is heated from one side and cooled from the other to create a temperature gradient, a potential difference between two ends, known as Seebeck voltage, V_{oc}, is developed, as illustrated in Figure 1(a). What really occurs inside a heated semiconductor is that majority carriers on the hot side gain more energy. This causes the carriers on the hot side to accelerate faster than the carriers on the cold side. The majority carriers diffuse towards the cold end, leaving behind low density minority carriers on the hot end. Eventually, the net diffusion of carriers stops when the electric field is built up between the two ends.

Similarly in this work, heat is applied on the fabricated thermoelectric devices to produce T between two Cu sheets, as shown in Figure 1(b). Eventually, V_{oc} is generated, which is measured between the two Cu sheets.

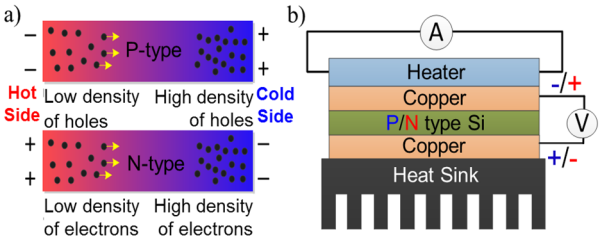

Figure 1: SiNWAs thermoelectric power harvester. (a) Working principle in thermoelectricity. (b) Experimental set-up.

DESIGN AND FABRICATION

In this work, four types of thermoelectric devices (i.e. p-Si bulk, n-Si bulk, p-SiNWAs and n-SiNWAs) are prepared by using Si wafer with a resistivity of 1 to 10 Ω-cm, and (100) orientation. The size of all devices is fixed at 1 x 1 cm, and the length of SiNWAs, approximately 6 µm. Bulk silicon thermoelectric devices are also tested in this experiment as a benchmark for SiNWAs thermoelectric devices. The nanowires are fabricated using

a two-step MACE technique, as illustrated in Figure 2. The MACE technique is employed in this work because the process is simple, and almost all of its processes can be performed in a laboratory without any expensive equipment [10].

In the MACE technique, the types of noble metal particles, concentration of etchant used, wafer orientation, wafer resistivity, type of dopants in Si wafer, and etching temperature are important parameters that need to be considered. The variation of these parameters affect the formation of nanowires, e.g., the various concentrations of etchant will form different structure of nanowires (cone-shaped, cylindrical-shaped, etc.). The different types of noble metal particles also influence the etching rate. Noble metal particles (e.g. Au, Pt, Ag, etc.) or in this work, Ag particles are deposited on top of the Si substrate surface, which act as catalysts that speed up the etching process of the Si substrate. The Si substrate beneath Ag particles will etch more rapidly compared to the area that is not covered with Ag particles, thus creating vertical nanowires (Figure 2).

To fabricate SiNWAs, Ag particles are first deposited by immersing a 1 x 1 cm silicon wafer in 0.06 M $AgNO_3$ and 49% HF aqueous solution for 15 minutes. Next, it is etched using 0.6 M H_2O_2 and 49% HF solution for several minutes to obtain the desired nanowire length. The length of SiNWAs are then characterized by using a Field Emission Scanning Electron Microscope (FESEM).

The Si substrate with SiNWAs is then sandwiched between two Cu sheets for electrical contact, as shown in Figure 3. Cu is used as a contact probe due to its high electrical and thermal conductivity. Each Cu sheet is connected to the test lead of a digital multimeter (34410A, Keysight, USA) for voltage measurement. A resistive heating element composed of a single-sided Cu clad polyimide is placed on top of the device to provide heat to the hot junction. A heat sink is placed at the bottom, helping to preserve the temperature at the cold junction. The temperature of the heat junction is increased by supplying current to the heater attached to the hot junction, while keeping the cold junction almost at room temperature.

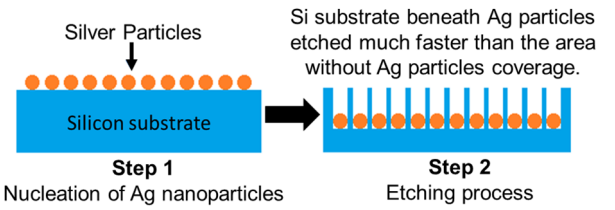

Figure 2: Two-steps MACE technique.

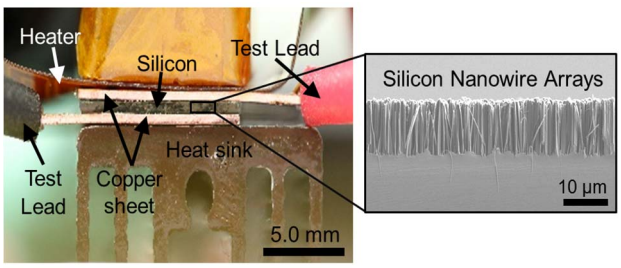

Figure 3: Fabricated device with copper sheets attached (left); and close-up FESEM image of SiNWAs (right).

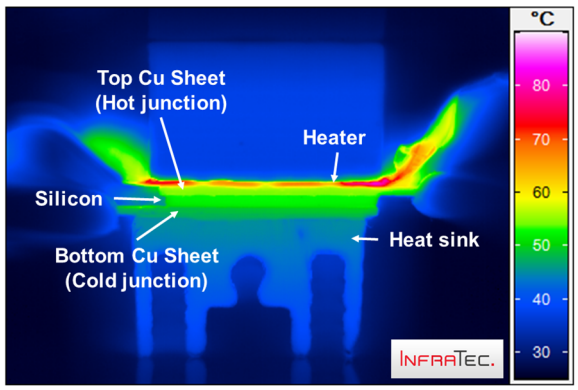

Figure 4: Thermal image of experimental set-up.

Furthermore, a small load is applied on top of the device to improve thermal and electrical contact between Cu sheets and the fabricated SiNWAs. The temperature at the hot and cold junctions is measured by using an Infrared (IR) camera (VarioCAM® HD, InfraTec, Germany), as shown in Figure 4. The experiment is conducted in a controlled environment at room temperature, with no forced air flow.

RESULTS AND DISCUSSION

Figure 5 illustrates the length of the fabricated nanowires which were formed by using the MACE technique as the time of etching increases. The diameter of the SiNWAs remains unchanged as the length increases, which is approximately measured at 70 to 100 nm. Based on the graph, the etch rate of p-type Si is ~0.2303 µm/min is slightly higher than the n-type Si which is measured to be ~0.1861 µm/min. This is due to the low internal resistivity [11] in the p-type Si compared to the n-type Si.

An experiment on heat flow in the thermoelectric device is conducted with the aim of observing the amount of heat being transferred from the hot junction to the cold one. Figure 6 shows the ΔT and heat flow, Q, across the thermoelectric device from the hot junction to the cold one, that passes from the top Cu sheet, where a heater is attached, to the SiNWAs and Si substrate, and then finally to the bottom Cu sheet. The highest ΔT was measured at p-type SiNWAs, with ΔT = 17°C in 40 sec, followed by n-type SiNWAs, with ΔT = 9 °C. Meanwhile, p- and n-type bulk Si yielded a ΔT of 7 °C and 5 °C respectively.

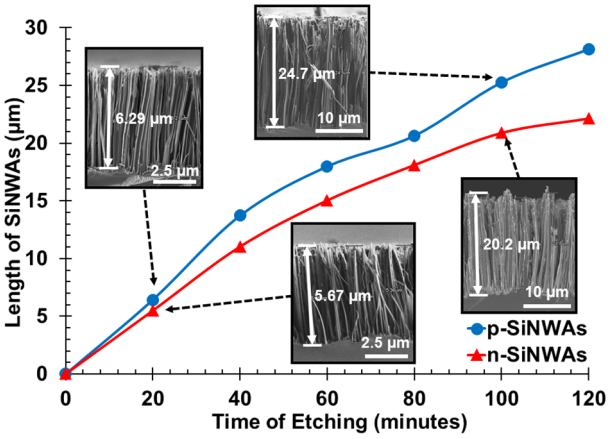

Figure 5: Increasing length of nanowires as the etching time increases.

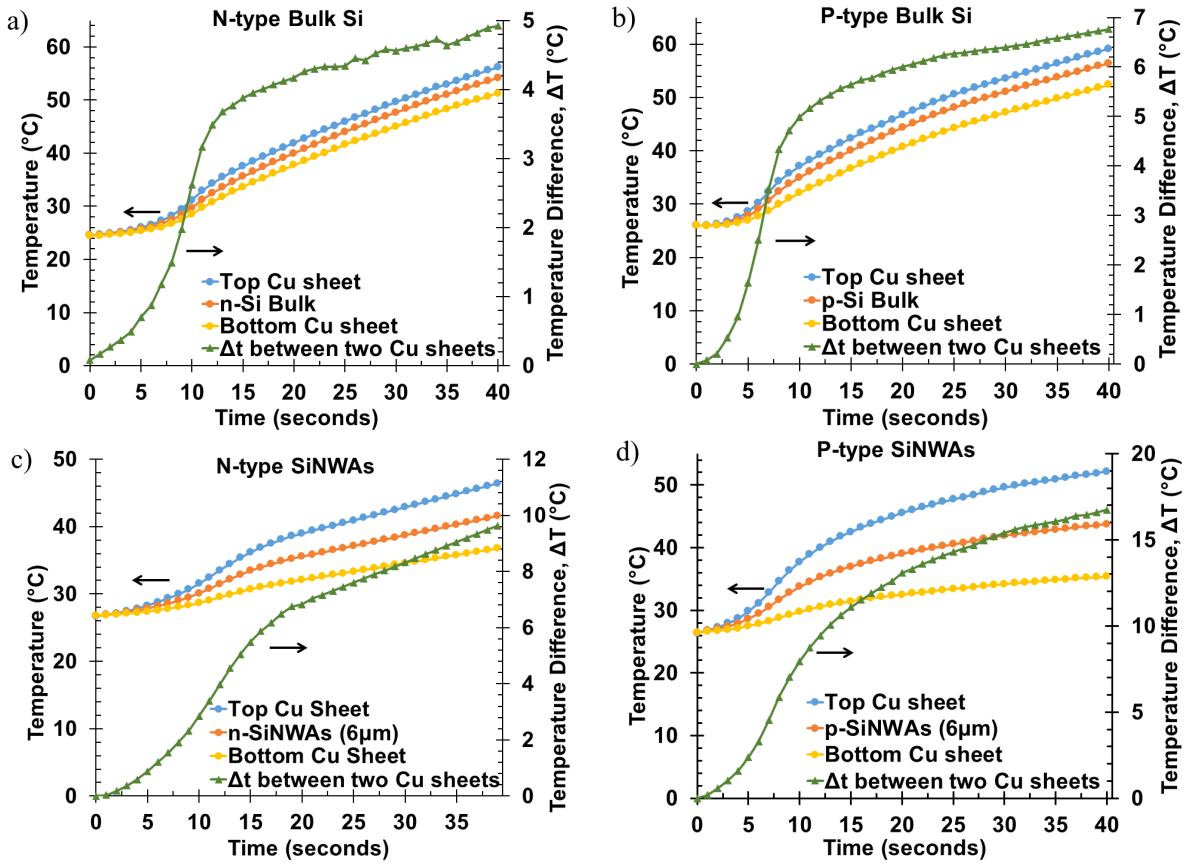

Figure 6: Temperature between hot and cold junctions, and temperature difference of thermoelectric device for; (a) n-Si bulk, (b) p-Si bulk, (c) n-SiNWAs and (d) p-SiNWAs.

Based on the results, it is seen that ΔT for SiNWAs is much higher than bulk-Si for both n- and p-type, which contributes to a higher output voltage. In nanowires, heat capacity, C, of Si is reduced significantly, causing increased ΔT between two Cu sheets, as given in Equation (1). A reduction in C also reduces the thermal conductivity of Si, which might lead to an improvement in the thermoelectric efficiency up to four folds [12].

$$C = \frac{Q}{\Delta T} \tag{1}$$

Si is a semiconductor that has a bandgap energy of 1.1 eV at 300 K. A small amount of energy is required to excite more majority carriers (i.e. electrons and holes in doped Si) from valence band into conduction band [13]. This condition will make Si more conductive where current is allowed to flow through the material. In this experiment, Si becomes more conductive when heat is applied to the material, allowing current to flow, thus developing the potential difference shown in Figure 7.

Figure 7 shows the measured V_{oc} for both p- and n-type bulk Si and SiNWAs thermoelectric devices. V_{oc} is obtained directly by using a multimeter without connecting the device to any load. The value of V_{oc} increases as ΔT between the hot and cold junctions increases. The highest V_{oc} measured at p-type SiNWAs, which yielded ~35 mV at ΔT = 5 °C, followed by n-type SiNWAs, with ~16 mV at the same ΔT. The bulk Si device of both p- and n-type shows V_{oc} of 4 mV and 8 mV, respectively, at ΔT of 4°C.

The V_{oc} values obtained were used to calculate the S based on Equation (2), as plotted in Figure 8. The p-type SiNWAs thermoelectric device has the highest S compared to others, with S = ~8 mV/K, followed by n-type SiNWAs, with S = ~4 mV/K. Bulk Si for both p- and n-type obtained the lowest S of ~2 mV/K and ~3 mV/K, respectively. However, there is a slight reduction in S as ΔT is greater than 2 °C across all types of devices.

$$|S| = \frac{V}{\Delta T} \tag{2}$$

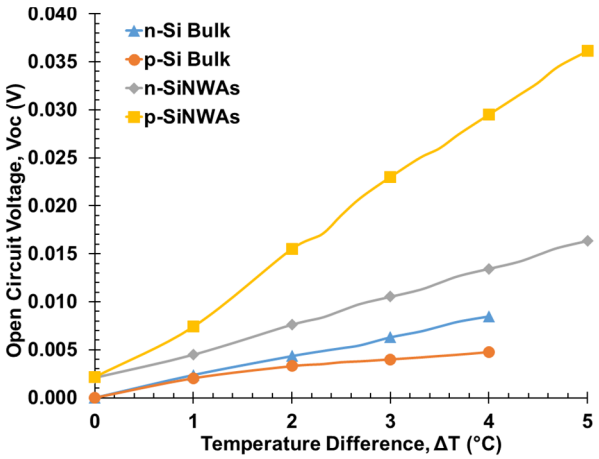

Figure 7: Measured Seebeck voltage, V_{oc} with temperature difference.

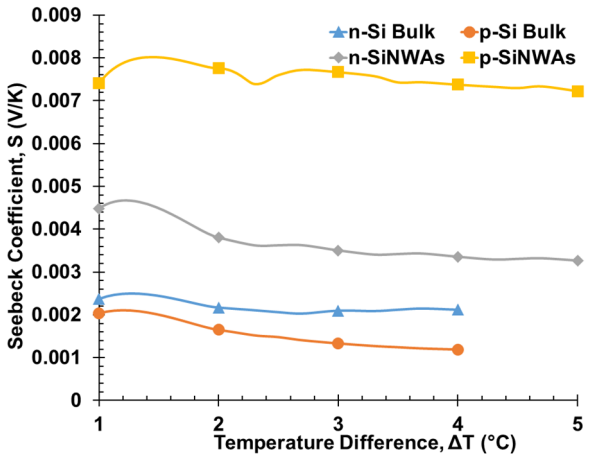

Figure 8: Seebeck coefficient of bulk Si and SiNWAs thermoelectric device against temperature difference.

Based on the presented results, SiNWAs thermoelectric devices show an improvement in heat flow across devices, V_{oc} and S compared to bulk Si. The introduction of a nanoscale component in Si will lead to a quantum confinement effect [14]. The movement of free electrons are restricted, while the large number of interfaces in nanostructured material (e.g. nanowires) scatter a wide range of phonons that carry heat in the material [15]. A larger interface density will introduce more phonon scattering, which narrows the distribution of heat and carrier transport. Consequently, phonons in nanowires will encounter more thermal resistance, thus causing a reduction in thermal conductivity compared to bulk Si.

CONCLUSION

SiNWAs as thermoelectric material have been investigated. A fabrication process based on a wet etching MACE technique was applied in this experiment to develop nanowires. Compared to bulk Si, heat flow across SiNWAs devices exhibits a higher ΔT between the hot and cold junctions. Moreover, the fabricated device of both p- and n-type SiNWAs thermoelectric device shows a higher V_{oc} and S than bulk Si. The voltage rises as the ΔT between the junctions increases. It is shown that the value of S for p-type SiNWAs is increased by a factor of four while n-type SiNWAs show a slight increase of 33.3 % compared to p- and n- type bulk Si, respectively. High V_{oc} and improvement of ΔT and S in SiNWAs thermoelectric devices help to improve ZT, which responsible for the overall efficiency of the thermoelectric power harvester.

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