VERTICAL INTEGRATION OF CAPACITIVE AND PIEZO-RESISTIVE SENSING UNITS TO ENLARGE THE SENSING RANGE OF CMOS-MEMS TACTILE SENSOR

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ABSTRACT

This study presents a tactile sensor design to enlarge the sensing range by vertically integrated capacitive and piezo-resistive sensing units. The lower stiffness membrane with high sensitivity capacitance sensing electrodes is used to detect small force. To avoid the saturation of capacitive sensing, the higher stiffness cantilevers with piezo-resistive sensors are employed to detect larger force. Thus, sensing range of CMOS-MEMS tactile sensor is improved by the proposed two-stage sensing device. The presented design is implemented by the TSMC 0.18μm 1P6M standard CMOS process and in-house post-CMOS releasing. Measurement results indicate the capacitive sensing could detect loads ranging 0~0.03N (sensitivity is 1.8fF/mN) and the piezo-resistive sensing could detect loads ranging 0.05~0.5N (sensitivity is 9mV/N with 2V input voltage).

INTRODUCTION

With the fast development of robot recently, various related sensors such as tactile and image sensors have received attention. The tactile sensors could enable the robot to realize the contact conditions which are critical to many applications. In addition to a single sensing unit, the array type tactile sensors to detect force distribution or improve spatial resolution are also required [1]. Thus, various design issues need to be considered. For instance, the integration of sensing structures and signal processing circuits is an important issue for the array type sensors. In this regards, the CMOS-MEMS processes is a promising platform which has the advantage to monolithically integrate the sensing structures and circuits for tactile sensor using the standard CMOS processes.

The capacitive type [2-3] and piezo-resistive type [1][4] CMOS-MEMS tactile sensors using foundry available processes have been demonstrated. Generally, the capacitive and piezo-resistive sensing approaches could respectively offer the advantages of higher sensitivity [2] and larger sensing range [5]. However, the structure stiffness which is a key parameter to influence the sensing range is limited by the thickness of thin films for the standard CMOS process. Therefore, CMOS-MEMS tactile sensors are usually employed to detect small loads. However, a wide sensing range would be required for the robot applications. For example, a larger force sensing is needed for the robot in hospital service to carry patient.

Many novel approaches have been reported to improve the sensing range of tactile sensors by filling with polymer or ER-fluid [2-3][6]. In general, the existing approaches have the tradeoff issue for the sensitivity and the sensing range. In

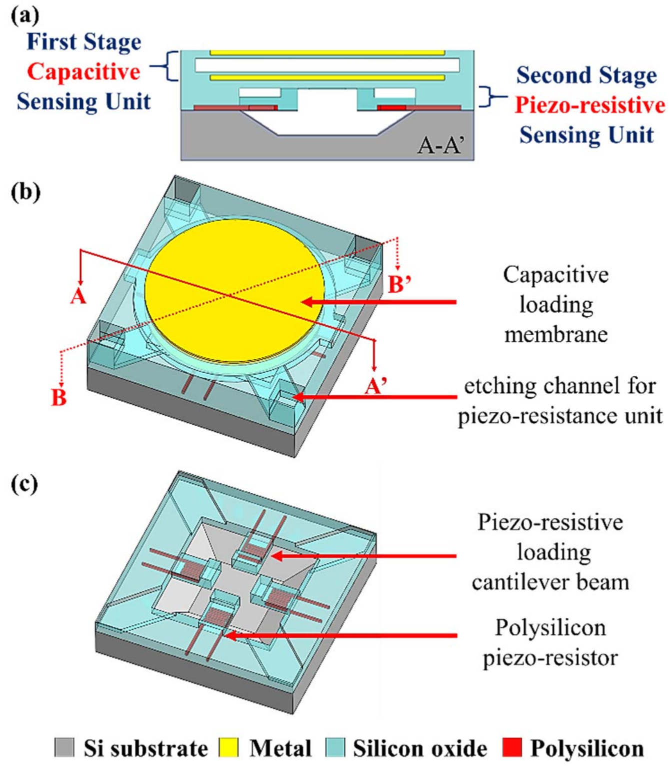

Figure 1: The design concept of tactile sensor, (a) cross-section schema； (b)first-stage and (c) second-stage 3D overview.

short, the filler could increase the stiffness to enlarge the sensing range at the cost of reducing sensitivity. Thus, this study exploits the CMOS multilayer structure to realize a tactile sensor by vertically integrating two sensing units of different sensing mechanisms to enlarge the sensing range without sacrificing the sensitivity.

DESIGN CONCEPT

This study exploits the metal layers and poly-Si in standard CMOS process to fabricate and vertically integrate the capacitive and piezo-resistive sensing units to enlarge the sensing-range of tactile sensor. Fig.1a illustrates the schematic design of the proposed tactile sensor with a two-stage sensing structure. Note that the sensor will be implemented by the TSMC 0.18μm 1P6M CMOS process, and thus has to meet the design rules and available materials. The first capacitive sensing stage is designed with a pair of 180μm diameter deformable electrode membranes. The second piezo-resistive sensing stage with relatively stiff structure is designed with four cantilever beams above a 100

×100 μm^2 cavity. The piezo-resistors at second stage are designed with a Wheatstone bridge circuit to decrease the temperature influence. Fig.1b-c further indicate the designed structure of capacitive and piezo-resistive sensing units, respectively. The design exploits the standard CMOS layers to form the capacitance sensing electrodes by metal-layers, piezo-resistors by poly-Si, deformable membrane and supporting cantilevers by dielectric-layers. Moreover, a cavity is fabricated on the silicon substrate after the bulk silicon etching.

Fig.2 shows the sensing mechanism of two stage sensing units. As in Fig.2a, the smaller loads are detected by the relatively sensitive capacitive sensing unit with deformable electrode of lower stiffness. As the load exceeding a threshold, the deformable electrode will contact the reference electrode and causes the saturation of capacitive sensing. Meanwhile, the force will transmit to the supporting structure of piezo-resistive sensors. The larger loads are then detected by the piezo-resistive sensing unit attached to a relatively stiff supporting structure as illustrated in Fig.2b. Thus, the sensing range of tactile sensor is improved by piezo-resistive sensing unit, yet the good sensitivity for small load detection remains available by capacitive sensing unit.

FABRICATION

This tactile sensor was implemented by the TSMC 0.18μm 1P6M CMOS process with the in-house post-CMOS releasing. Fig.3 shows the fabrication processes for the cross-sections of A-A' (along capacitive sensing unit releasing channel) and B-B' (along piezo-resistive sensing unit releasing channel) indicated in Fig.1b. Fig.3a presented the layer stacking and patterning fabricated by TSMC 0.18μm 1P6M process. In Fig.3b, removed Al metal/tungsten-via by H_2SO_4/H_2O_2 [7] to define the sensing gap, sensing membrane for capacitive sensing structure and the cantilever beams, inlet channels for piezo-resistive sensing structure. The inlet channels for piezo-resistive sensing unit defined by the metal routings are used as the path for TMAH etching. Fig.3c shows the piezo-resistive sensing structures were suspended after TMAH Si etching. Due to the good selectivity for TMAH silicon anisotropic etching, this study employed the dielectric-layer as protection mask to define the cavity shape. In Fig.3d, reactive ion etching (RIE) was used to remove passivation layer to open bonding pads. After the in-house post-CMOS fabrication processes, the chip was wire-bonded on PCB for the subsequent measurements.

The SEM micrographs in Fig.4 show typical fabricated tactile sensor and etching holes to release structure. It can be clearly observed that the CMOS layers stacking and releasing channel are well defined, as displayed in the zoom-in micrographs. Micrographs in Fig.5a-b respectively show the

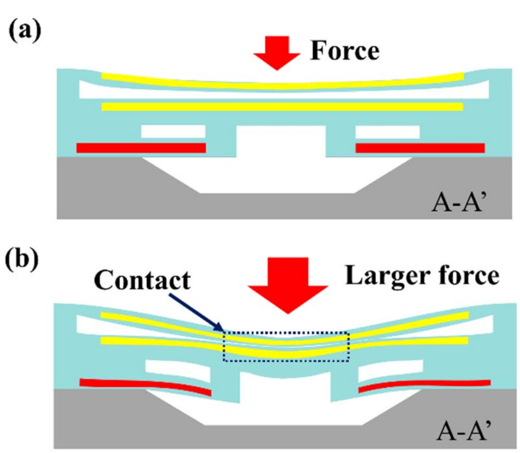

Figure 2: sensing principle (a) smaller force detected by capacitance stage ; (b) larger force detected by piezo-resistance stage.

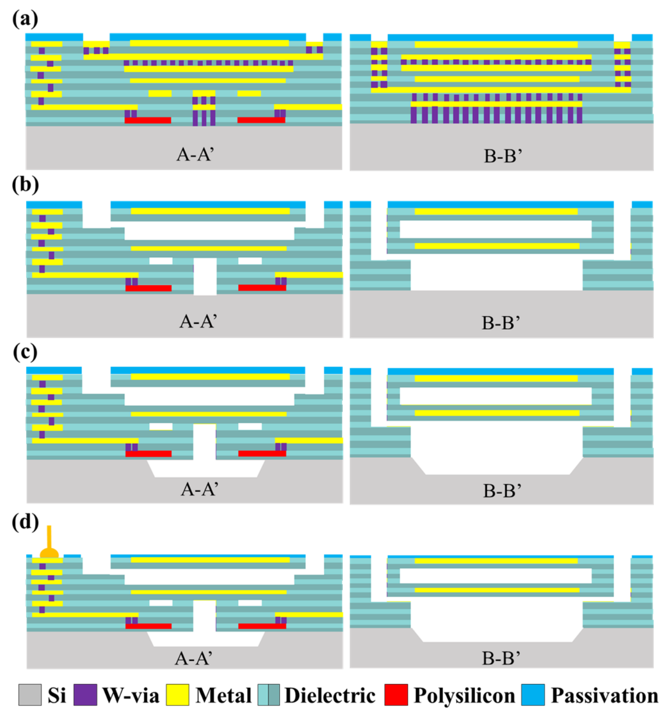

Figure 3: Fabrication process of tactile sensor, (a) chip prepared by TSMC ; (b) H_2SO_4 metal wet-etch ; (c) TMAH silicon etch ; (d) RIE open bonding pad and wire bond.

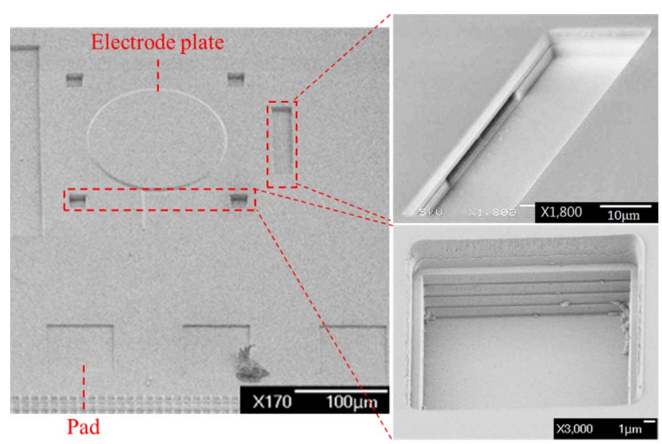

Figure 4: SEM micrographs of tactile sensor, (a) fabrication result, and zoom-in micrographs of etching hole (b) for capacitance unit ; (c) for piezo-resistance unit.

capacitive sensing membrane, and the piezo-resistive sensing cantilevers above cavity. Fig.5a depicts the capacitance unit etching channels to release the membrane, and the membrane is well defined after metal etching releasing. The micrograph in Fig.5b was observed from a test-key unit. No metal electrode was covered on the membrane of the test-key. Thus, the transparent silicon oxide membrane enables the monitoring of the cantilever beams, cavity, etching channels, and polysilicon piezo-resistors underneath. Fig.5c depicts the surface morphology of membrane measured by optical interferometer. The result indicates that there is only small deformation (0.7μm at center) of capacitive sensing membrane (180μm in diameter) by residual stresses of CMOS films after releasing.

MEASUREMENT RESULTS

This study performed various tests to evaluate the performance of tactile sensors. The major tests are small force measurements using capacitive sensing unit, and large force measurements using piezo-resistive sensing unit. In addition, the sensing signal drift of piezo-resistors with temperature is also characterized. Fig.6a-b show the measurement setup and results for capacitance sensing tests. Measurements indicate the capacitive sensing unit can measure tactile forces ranging 0~0.03N with a sensitivity of 1.8fF/mN. The sensing capacitance is saturated as tactile load exceeding 0.03N. The minimum detectable load of the tactile sensor is 0.01N. Note that the above result is limited by the resolution of the commercial force gauge. The exact resolution of the tactile sensor is smaller than 0.01N. Fig.7a illustrates the measurement setup for piezo-resistive sensing and the signal is measured with Wheatstone bridge circuit. Measurements in Fig.7b show the decrease of temperature influence on piezo-resistor by Wheatstone bridge. The resistance and voltage signal are the measurement result before/after Wheatstone bridge circuit transform. The result indicates Wheatstone bridge circuit can decrease the thermal drift of sensing signals from 8% to 2% when temperature changed from 30 to 60°C. Due to the process tolerance, the four piezo-resistors are not perfectly symmetric and thus 2% signal drift is still left. Measurements in Fig.7c depict the variation of piezo-resistance with tactile loads. The result shows that the signal has good linearity as compare with the signal of capacitance, and the sensing range is 0.05~0.5N which is larger than the capacitive sensing. The electrostatic force between the two capacitance sensing electrodes may lead to the structure deformations and further cause the sensing signal drift. More tests are required for detail investigations and design improvements.

CONCLUSIONS

In summary, this study has demonstrated a novel tactile sensor design with vertical integrated capacitive and piezo-resistive sensing units to enlarge the sensing range. The capacitive sensing unit can measure tactile forces ranging 0~0.03N with a sensitivity of 1.8fF/mN. The piezo-resistive sensing unit can measure tactile forces ranging 0.05~0.5N with a sensitivity of 9mV/N. Moreover, the piezo-resistor with Wheatstone bridge circuit could decrease the thermal drift of signals from 8% to 2% as temperature changed from

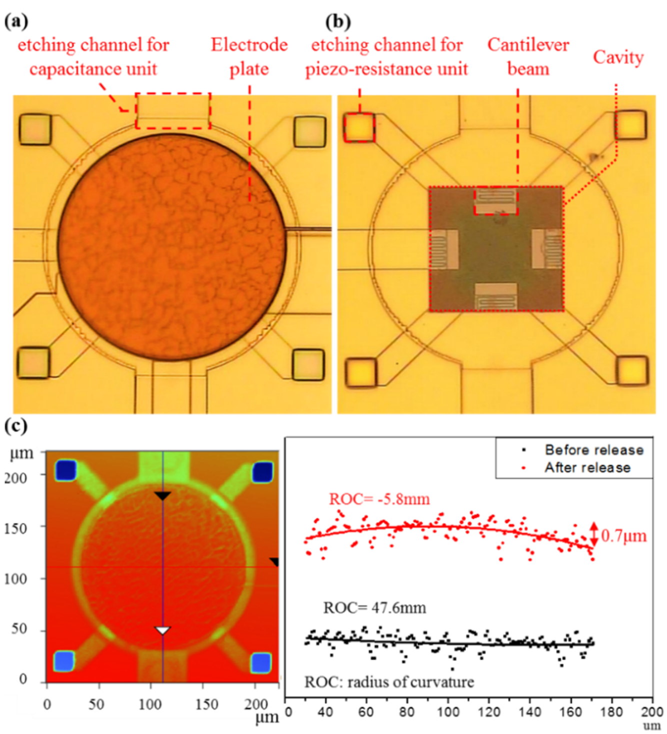

Figure 5: Micrographs of (a) electrode plate and (b) cantilevers; (c) the capacitance membrane deformation.

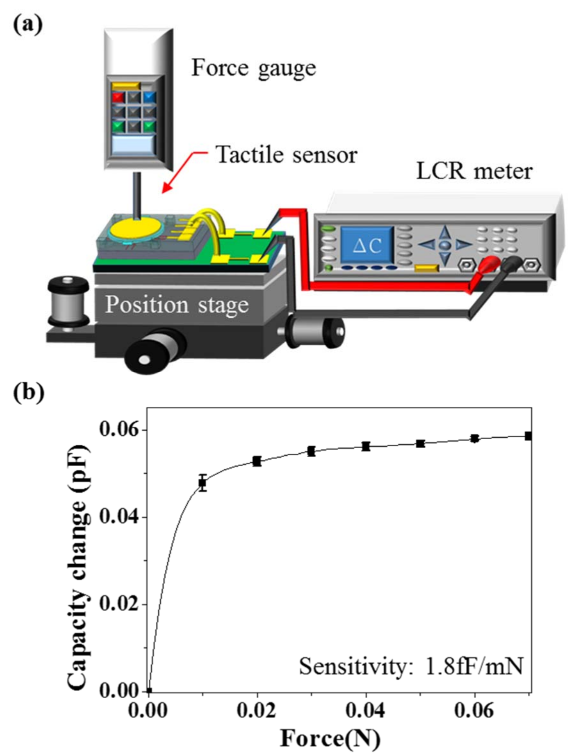

Figure 6: (a) the schema of capacitance measurement setup; (b) measured output capacitance change versus force.

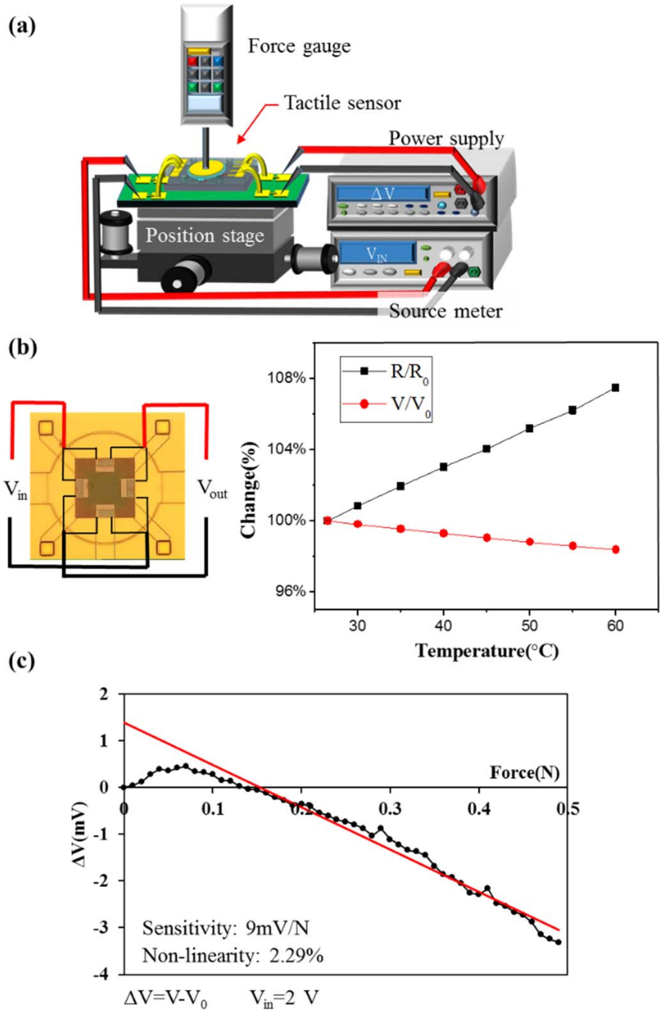

Figure 7: (a) the schema of piezo-resistance measurement setup; (b) measured piezo-resistance signal change versus temperature; (c) measured output voltage change versus force.

30 to 60°C. On-going design improvement is performed to cover the range of 0.03~0.05N. Note that the polymer or ER-fluid fill-in in [1-2] can be employed to further improve the sensing range of this CMOS-MEMS tactile sensor.

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