A LOW TEMPERATURE INKJET PRINTING AND FILLING PROCESS FOR LOW RESISTIVE SILVER TSV FABRICATION IN A SU-8 SUBSTRATE

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ABSTRACT

The paper presents a low temperature (with 60 °C) inkjet printing and filling process to realize low resistive Ag TSV (Through Substrate Vias) with the aspect ratio of via depth vs. diameter from 2 to 5 in a SU-8 substrate potential for flexible microsystem packaging applications. Combining humidity control and layer-by-layer Ag mirror reaction, the proposed process technology can accomplish a fully filled TSV with the lowest electrical resistivity of ~450 μΩ•cm in comparison with the prior printing and filling technologies.

INTRODUCTION

Through Substrate Via (TSV) is a critical interconnect structure for signal transmission with high density, speed, and flexibility in microsystems [1]. As compared to traditional planar interconnect lines on an electronic packaging or device substrate, the electrical wire devised directly through the substrate can be regarded as the most expeditious signal transmission way for the chip-to-chip communication in a 3D manner. The state-of-the-arts TSV technology has been successfully developed to facilitate the integration of heterogeneous chips, which can enhance the connectivity, power transfer, circuit density, flexibility, and faster signal transmission of the chip system without increasing manufacture complexity. Nevertheless, how to realize TSVs in a flexible substrate is still a critical research topic in the fabrication of flexible microsystems owing to the increase of the demand in internet of things (IOT) technologies for various applications such as smart grid [2], food safety monitor [3], body sensor network [4] etc. that require numerous distinct sensors in a microsystem.

The main body of the TSVs is a fully filled electrically conductive trench embedded with free ends on both sides of a substrate. Conventional processes to fill the TSVs include metal-electroplating, paste-filling or physical metal vapor deposition, etc. Recent studies also explored the feasibility of inkjet printing and filling process for TSV fabrication due to the superior characteristics of less chemical waste, processing time, and process temperature applicable for different TSV substrates [5-7]. Besides, unlike the conventional IC and MEMS fabrication requiring an expensive and heavy energy-consuming clean-room facility, maskless inkjet printing process is more cost-effective, easy accessible, timely for fast prototyping in the development of organic electronics. Since Sirringhaus et al. successfully demonstrated the first inkjet-printed inorganic integrated circuit in 2000 [8], inkjet printing has opened a new era as one of the semiconductor manufacture technologies. As a result, in this work, we will develop a low temperature inkjet printing and filling process to facilitate the TSV fabrication in flexible electronics.

Inkjet-printed structures are typically accompanied with a non-uniformity issue resulting from the solute redistribution in the ink droplets, which is called "coffee-ring effect" [9]. An outward liquid flow resulting from the replenishment of evaporated liquid in the edge of a drying liquid droplet will drag interior solute to the contact line formed and then pined in between the air and substrate. The solute redistribution accounts for the stains with high perimeter concentration, i.e. called "coffee-ring", also cause the process liability problem in filling TSV by the inkjet printing. The liability problem can also result from the aspect ratio of via depth vs. diameter. While the aspect ratio is too high whereas the via diameter is too small, the solute particles will segregate to jam the opening of the via after the evaporation of solvent. Fig. 1 shows incomplete via filling where Ag nanoparticles either condensed less inside the vias resulting from the coffee ring effect (Fig. 1(a)) or quickly dried out and left on the via surface (Fig. 1(b)). In addition to

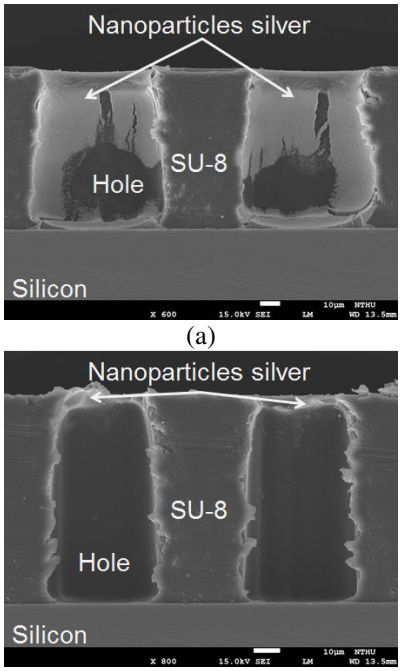


Figure 1: Incomplete via filling (a) less Ag condensation is formed inside the via resulting from coffee ring effect and (b) Ag ink is drying out and left on the surface before flowing into the vias.

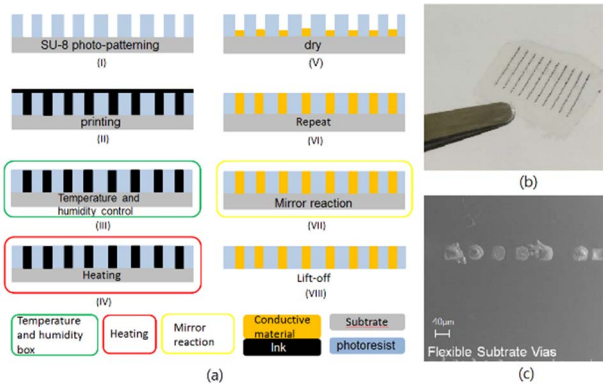


Figure 2: (a) The scheme of process flow: (I) SU-8 phot-patterning, (II) inkjet printing and filling Ag ink into the vias, (III) holding @ 30 °C and 80 % relative humidity, (IV) substrate heating up to 60 °C, (V) ink drying out, (VI) repeated printing, filling and drying, (VII) completing the via filling, and (VIII) substrate detachment, (b) the micrograph of a flexible SU-8 substrate with filled TSV, and (c)enlarged view on the vias with a 40 μm pitch.

incomplete filling, the inkjet printing and filling could also result in poor electrical performance of TSVs due to inevitable high resistivity typically larger than several hundreds of μΩ•cm that requires a high temperature sintering process for further reduction.

Fukuda et al. recently presented that a high ambient humidity can effectively suppress the evaporation speed difference of solvent whereby the printed film shape can be easily controlled from being concave to convex shape [9]. Our group previously introduced the mirror reaction to deposit Ag atoms onto an Ag substrate via the self-redox reaction in a Tollen solution [10], so the loosely packed Ag microstructure can become denser with less porosity whereby the resistance of the printed Ag interconnect can be effectively reduced. Since the electrical reduction scheme is reaction and diffusion rate dependent, we plan to combine humidity control and layer-by-layer Ag mirror reaction in the inkjet printing and filling process for not only resolving the predicament but also facilitating the TSV fabrication in flexible electronics.

EXPERIMENTAL METHODS

Figure 2 shows the process flow and as-fabricated SU-8 substrate with Ag TSV array. The process begins with 120 μm thick SU-8 coating and via patterning with a 40 μm pitch on a Kapton film followed by inkjet printing droplets with 60 μm diameter in the vias at 30 °C. The substrate is kept in a controlled chamber @ 30 °C and 80 % relative humidity for 5 minutes and then heated up to 60 °C for drying out the ink. The prior filling steps are then repeated until the via is fully filled. The substrate with fully filled vias is placed in the previously developed mirror reaction solution for 30 minutes. Finally, the SU-8 substrate with TSVs is formed by detaching itself from the bottom substrate using scotch tape. For the layer-by-layer mirror reaction process, the vias must go through the mirror reaction once the ink inside is dried out every time.

RESULTS AND DISCUSSION

Figure 3 shows the cross sectional SEM micrographs of fully filled Ag vias with the aspect ratio of 2 to ~5 where the via depth is about 120 μm. For electrical characterization of the TSVs, we design and fabricate a daisy chain structure comprising of eight vias to measure the resistivity of the Ag TSV. Figure 4 shows the daisy chains (Fig. 4(a)) with corresponding I-V measurement where the voltage value has been divided by eight and the via is about 40 μm in diameter and 80 μm in depth. Figure 4(b) shows small resistance difference between the samples before and after with one time mirror reaction. The resistivity of the Ag TSV is ~7 Ω•cm. As aforementioned, the mirror reaction is a chemical reaction in liquid phase employed to deposit Ag atoms onto a loosely packed Ag microstructure for electrical resistance reduction. As a result, the incidence of the reaction will be restricted and limited by the penetration of the solution into the inkjet printed Ag vias. Figure 5 shows a diced cross sectional view on the Ag-filled via after with one-time mirror reaction where the enlarged SEM micrographs on the via surface and the regions 10 and 15 μm below the surface, respectively. It shows the mirror reaction can only take place on the top part of via to make the Ag microstructure denser with less porosity.

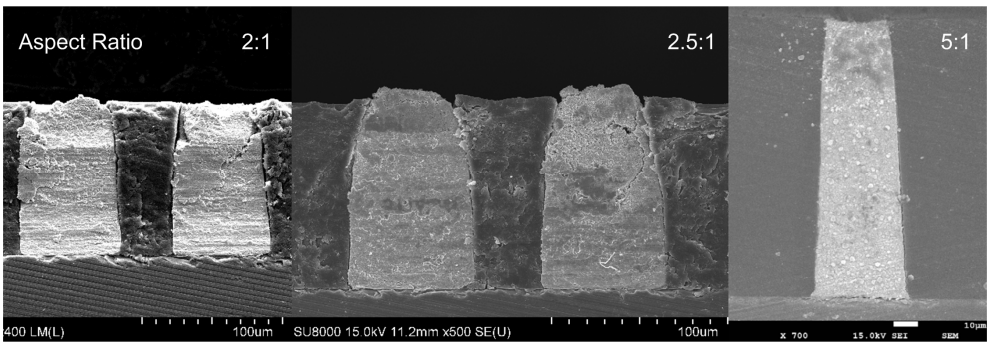
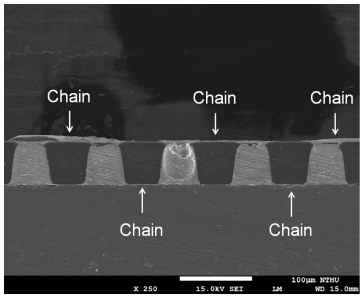
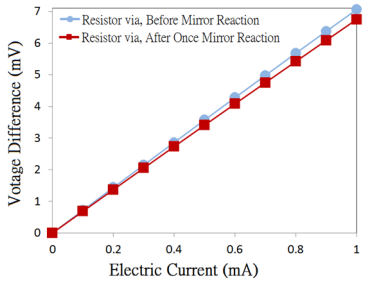


Figure 3: The TSV with the aspect ratio of about 2:1, 2.5:1, and 5:1, i.e. via depth vs. diameter, filled using the inkjet printing and filling process where the via depth is about 120 μm.



(a)



(b)

Figure 4: (a) Cross sectional SEM micrograph of the as-fabricated daisy chain on a silicon substrate and (b) I-V measurement of the samples with/without one time mirror reaction.

For the silver mirror reaction process used in this work, the concentration of ammonia and glucose in the Tollen solution have been adjusted for controlling the precipitation rate of Ag atoms whereby these atoms can only be deposited onto the printed Ag vias. Therefore, the solution cannot supply enough reactants to the bottom of the vias that will cease the further precipitation of Ag and still keep the bottom side of the vias with a loosely packed structure once the perforations of the top printed Ag vias are fully sealed by the mirror reaction. From Fig. 5, it is observed the infiltration of

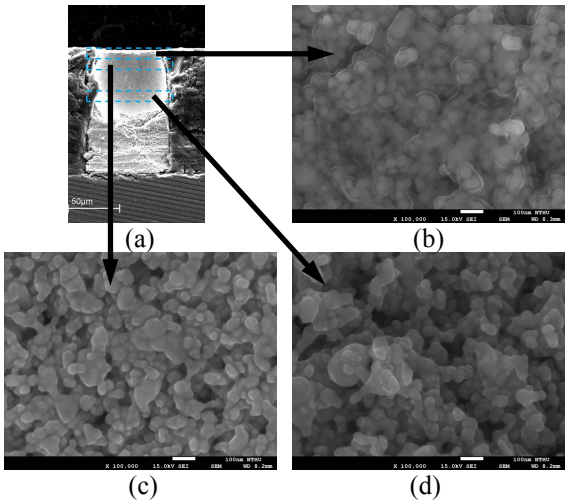
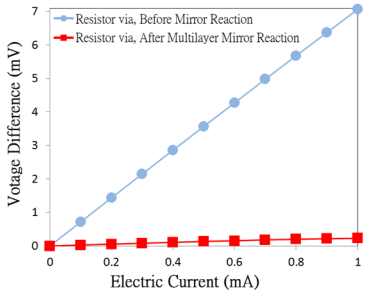
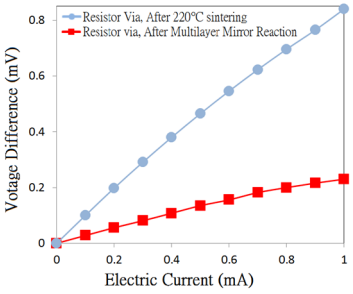


Figure 5: SEM micrographs on a diced via treated with one-time mirror reaction. (a) the overall via, (b) the top surface region (c)10 μm from the top, and (d)15 μm from the top.



(a)



(b)

Figure 6: Comparisons of the measured I-V characteristics of the samples treated with/without layer-by-layer mirror reaction, as well as and with 220 ℃

the mirror reaction only takes place within 10 μm from the top of the printed vias surface indicating the layer-by-layer mirror reaction is required to perform for further electric conductivity improvement of the printed TSV.

Figure 6 shows the measured *I-V* characteristics of a single via fabricated with/without the layer-by-layer mirror reaction. The electrical resistivity of the printed vias can be further reduced to ~450 μΩ•cm. In comparison with the Ag TSV sintered @ 220 °C whose resistivity is ~1.4 mΩ•cm, the low temperature printing and filling process has shown its potential to accomplish the TSV with a lower resistivity for flexible microelectronics fabrication. Referring to our previous research result where an inkjet printed 10 μm wide and 0.5 μm thick Ag interconnect line treated with the mirror reaction can exhibit an electrical resistivity as low as 7.7 μΩ•cm [9], the electrical characteristic of the printed vias can be improved with further process optimization

Via filling is a time-consuming process [1]. In the conventional electroplating via process, there exists competition between ionic diffusion and deposition mechanisms during the via filling, which requires process optimization to accomplish super filling. Otherwise, the vias could be sealed before fully filled as a result of void formation inside the vias to raise reliability problem. In contrast, the competition existing in the inkjet printing and filling process is the solute reflowing and solvent drying mechanisms that also require process optimization. For the printing process, the evaporation rate of the ink solvent, which is temperature and humidity dependent would determine the overall process time for the accomplishment of via filling due to the requirement of process repetition. Since the substrate heating temperature cannot be too high to

Table 1: Comparisons between prior inkjet printing and filling processes and this work.

	Khorramdel et al. [5]	Quack et al. [6]	Mäntysalo et al. [7]	This Work
Substrate	Silicon	Silicon	Silicon	SU-8
Substrate temperature (℃)	40-60	140	60	30
Sintering temperature (℃)	220	250	220	60
Aspect ratio of Via	2:1	2:1	2:1	Up to 5:1
Via diameter (μm)	85	60	85	25
Resistivity (μΩ•cm)	N.A.	<200 (Au)	<20000 (Ag)	<450 (Ag)

provide enough time for the solute nanoparticles flowing into the vias as aforementioned, the printing process has a difficulty to realize deep vias with a reasonable processing time. So far, this technique took about 4 hrs to accomplish the vias with the aspect ratio of ~5, which is comparable with the current electroplating process.

Khorramdel et al. inkjet printed silver nano-particles to fill ~115 μm deep silicon vias with the outer diameter of 80 μm at 60 °C and sintered the vias at 220°C for achieving moderate resistance [5]. Quack et al. filled the silicon vias, i.e. 50 μm in diameter and 50 μm in depth, with inkjet printed Au nanoparticles at 140 °C and then sintered them at 250 °C for about 60 minutes [6]. According to their four point probe measurement, the extracted TSV resistance is about 50 mΩ indicating less than 200 μ •cm resisitivty of the filled Au stub can be obtained that is 2 times lower than our work. Mäntysalo et al. demonstrated an inkjet printing and filling process to make the Si vias with the outer diameter of ~85 μm and ~115 μm in diameter at 60°C using Ag ink [7] and then sintering these vias at 220 °C for 60 minutes. The resistance measurement showed the resistance of a single void free via could be less than 4 Ω, which means the electrical resisitivty of the filled Ag via could be as high as 20 m •cm. As compared with these prior arts summarized in Table 1, the proposed inkjet printing and filling TSV technology has shown a great potential not only for flexible microsystem but also 3D-IC and MEMS applications in terms of the characteristics of higher via aspect ratio and lower processing temperature and electrical resisitivty, especially the via resistivity should be lower than the expected since it also includes the contribution from thin film resistivity based on the daisy chain design.

CONCLUSION

In summary, a new inkjet printing and filling technology combining humidity control and layer-by-layer Ag mirror reaction has been successfully developed for TSV fabrication in a flexible substrate. Based on a thick film lithography process using SU-8 and the inkjet printing and filling process, a low cost flexible substrate with the TSVs with the aspect ratio of via depth vs. diameter from 2 to 5 can be fabricated to foster the advancement of flexible microsystems in various IOT applications.

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