FABRICATION OF NANOSCALE STRUCTURES WITH NANOMETER RESOLUTION AND SURFACE UNIFORMITY

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ABSTRACT

We integrated bottom-up and top-down techniques to develop a platform for the fabrication of structures with nanometer resolution and sub-nanometer surface uniformity, to serve as building-blocks of functional nanoscale devices and systems. By engineering surfaces and interfaces, chemically-synthesized gold (Au) nanoplates, with <1 nm surface roughness, are assembled to form nanogaps as small as ~10 nm in width. Interconnects and contact pads are added using top-down lithography to introduce electrical functionality to the assembled nanogaps. A planarization technique is employed to eliminate nanometer-scale height variations across the gap due to the thickness inhomogeneity inherent to synthesized Au nanoplates. This is achieved by peeling the Au nanoplate electrodes as a uniform layer off the original substrate using an adhesive receiving surface, revealing the coplanar side originally in contact with the substrate. The peeling also eliminates edge defects and minimizes the surface roughness inherent to features formed through lithography. An extension of this technique demonstrates <5 nm vertical resolution in controlling the height variations between neighboring structures. Overall, the proposed technique provides a versatile platform to achieve nanometer resolution and surface uniformity essential in developing nanodevices for applications such as nanoelectromechanical systems, plasmonics, and molecular electronics.

INTRODUCTION

Miniaturization to the nanoscale leads to the emergence of phenomena that can be used to develop unique device designs. Implementing these concepts requires unprecedented resolution and precision in the fabrication of nanoscale structures void of imperfections. Structures of particular importance are electrodes separated by nanometer-thin gaps. To overcome resolution and precision limitations of conventional top-down techniques, various alternative approaches have been proposed, including focused ion-beam milling, stiction-assisted lithography, adhesion lithography and atomic layer lithography [1-4]. However, when considering device dimensions on the order of a few nanometers, these techniques largely lack the desired surface uniformity, resulting in irregularities on the order of device critical dimensions, thus inhibiting the desired functions. Furthermore, some techniques suffer from inefficient scalability to larger areas and lack versatility in the choice of compatible substrates.

Bottom-up techniques, on the other hand, promise to achieve nanometer precision, resolution and uniformity beyond the limits feasible through top-down approaches. Importantly, they are well suited for large area processing with minimal limitations on the choice of substrate or the nanomaterials employed [5]. However, the resulting structures often lack the infrastructure needed to function as independent electrically-controlled entities, a feature required for many device applications.

To overcome the limitations of bottom-up assembly while leveraging their benefits, here we propose a hybrid approach in which bottom-up and top-down techniques are integrated. As a result, a platform is developed to fabricate structures with nanometer resolution and uniformity to serve as components of nanodevices.

DESIGN PRINCIPLES

Our fabrication methodology relies on three main thrusts. First, bottom-up assembly is used to promote controlled formation of well-defined nanogaps using chemically-synthesized single-crystalline Au nanoplates shown in Figure 1. With average roughness <1 nm, these Au nanoplates have surface uniformity significantly better than Au thin films formed through thermal evaporation, a commonly used deposition technique (Figure 1d). Second, top-down lithography is utilized to integrate interconnects with the nanogaps such that they can be electrically-driven. Third, a technique is implemented to planarize the step height across the nanogap, introduced by the non-uniform thicknesses of the nanoplates. The planarization also helps eliminate the edge imperfections and reduce surface roughness of the lithographically patterned electrical connections.

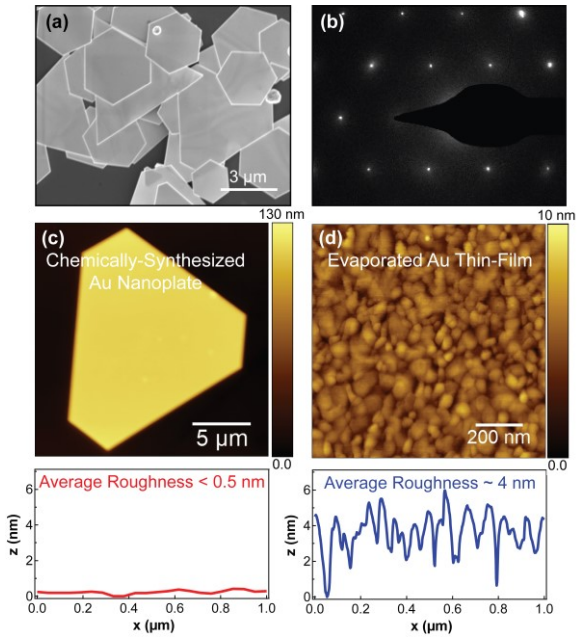

Figure 1: Chemically-synthesized Au nanoplates (a) exhibit uniform crystallinity (b) with sub-1 nm roughness, much smaller than ~4 nm roughness of an evaporated Au film, shown through atomic force micrographs (AFM) of (c) and (d).

FABRICATION

The fabrication scheme is shown in Figure 2. Au nanoplates are synthesized by reducing $HAuCl_4$ with ethylene glycol in presence of aniline and using polyvinylpyrrolidone (PVP) as the capping agent [6]. Their self-assembly is driven by engineering the surface interactions between the plates such that they come together to achieve an equilibrium state corresponding to the nanogaps (Figure 2b). The as-synthesized Au nanoplates are functionalized with octadecanethiol to assume a hydrophobic surface, and then are phase transferred into chloroform. A ~20 µL droplet of the functionalized Au nanoplates is then dispensed on a thin layer of deionized water coating a SiO_2 substrate of about 1 cm^2. Chloroform is immiscible in water. The hydrophobic surfaces of the Au plates prevent them from entering the hydrophilic phase, allowing them to be suspended at the water-chloroform interface. Chloroform having a higher density than water exerts a downward force on the plates to stabilize them at the interface. As the solvents evaporate, a force is exerted laterally to bring the Au plates together to form nanogaps adhered to the substrate.

Upon assembly, the substrate containing the nanogaps is briefly sonicated in ethanol to remove undesired aggregated Au nanoplates and spherical Au particles formed as byproducts of the synthesis. To remove the residual PVP and octadecanethiol molecules, the substrate is rinsed in a piranha solution. Once cleaned, interconnects and contact pads are added to the nanogaps using electron-beam lithography and a lift-off process based on thermally evaporated Au.

At this point, electrically accessible well-defined nanogaps are achieved. However, due to non-uniformities in the thicknesses of the Au nanoplates, a step height across the nanogap may be present. If a planarized profile is required, the height variation must be eliminated. This is achieved through peeling the Au nanoplates and the electrical contacts using a receiving surface covered with an adhesive layer. The peeling reveals the coplanar side of the plates originally in contact with the substrate. To do so, first, the substrate surface is functionalized with a layer of trichloro(1H,1H,2H,2H-perfluorooctyl)silane through vapor or liquid-phase growth. The functional silane end-groups of the molecules allow assembly onto the SiO_2 such that surfaces not covered by the Au acquire an anti-stiction property. Then, a ~30 µL drop of an ultraviolet light curable epoxy (Norland Optical Adhesive 61) is dispensed onto the substrate, following which, a receiving glass substrate is placed on top of the adhesive layer. Capillary forces cause the epoxy to spread, forming a uniform layer in between the original substrate and the receiving surface. Once cured under UV light, the glass is detached from the SiO_2, peeling off the Au nanoplates and electrical connections as a uniform layer.

RESULTS AND DISCUSSIONS

The self-assembly process of Au nanoplates leads to formation of well-defined nanogaps with nanometer resolution and precision. Figure 3 shows nanogaps of various widths as small as ~10 nm formed through this

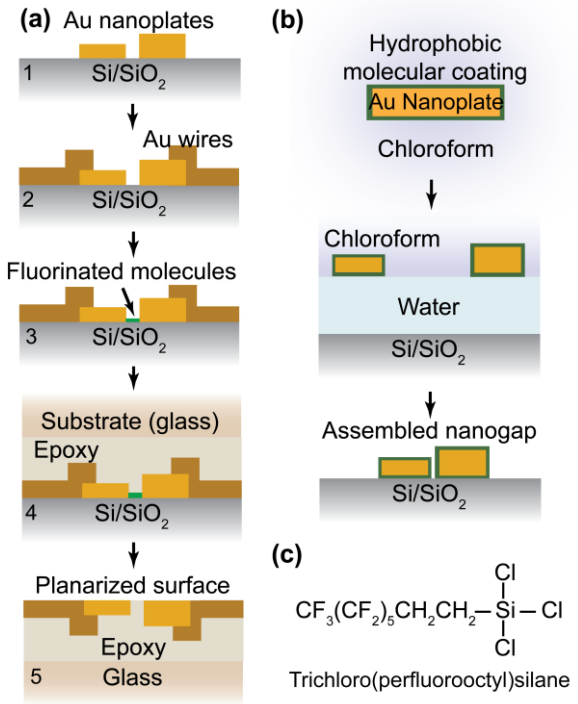

Figure 2: Combined bottom-up self-assembly and top-down lithography formation of electrodes separated by nanogaps and with nanometer uniformity. (a) Nanogaps are formed using self-assembly of Au nanoplates (1) upon which wires and contacts are added using electron-beam lithography and lift-off (2). After anti-stiction treatment of the substrate surface (3) with trichloro(perfluorooctyl)silane, a UV-curable epoxy is used to peel off the nanogap and the interconnects onto a glass substrate to planarize the surface (4). (b) To self-assemble the nanogaps, Au nanoplates are surface functionalized with octadecanethiol to assume hydrophobic surface properties and then are assembled at the water-chloroform interface using hydrophobic-hydrophilic interactions and capillary forces as the solvents evaporate. (c) Chemical structure of trichloro(perfluorooctyl)silane used as anti-stiction coating in the planarization process is illustrated.

bottom-up approach, with notable resolution, edge and surface uniformity not feasible through conventional top-down fabrication techniques. The gap width is influenced by factors including the substrate surface properties, types of immiscible solvents used, molecular coating on the nanoplates, density of Au nanoplates, and temperature used for the assembly process. The smallest nanogap possible is limited by the thickness of the molecular layer coating the nanoplates. However, to reach this limit other experimental conditions, mentioned above, need to be controlled as they influence the assembly process.

Figure 4 illustrates an electrically accessible, ~30 nm gap with <1 nm surface roughness and a planarized surface fabricated using the scheme of Figure 2. In this example, peeling is used to ensure the step height across the nanogap is removed. The peeling also eliminates the edge defects on the lithographically patterned electrical wires and pads, associated with the lift-off process, by exposing the side originally in contact with the SiO_2

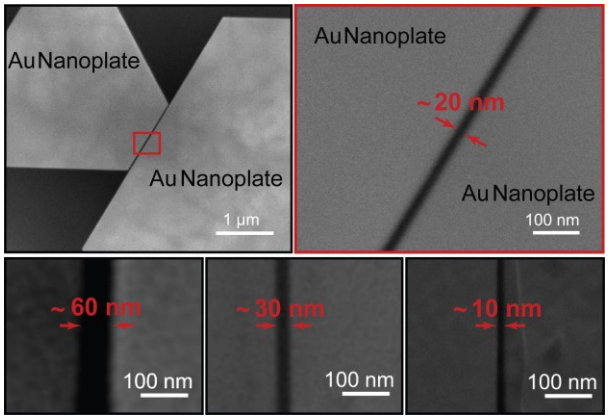

Figure 3: Precisely defined nanogaps with nanometer resolution and surface uniformity formed through the self-assembly of Au nanoplates based on the method shown in Figure 2b.

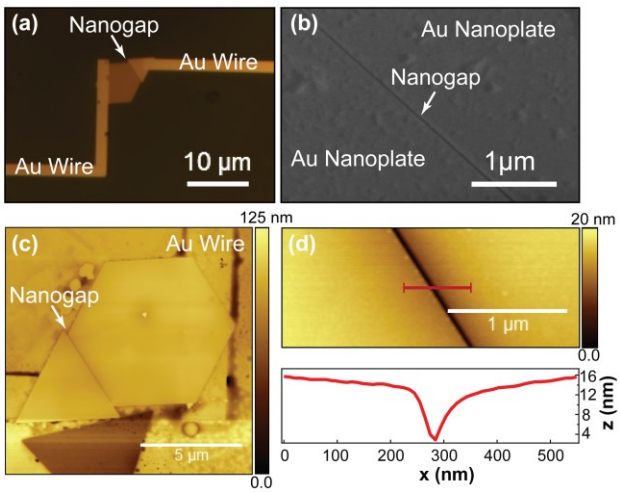

Figure 4: (a) Optical image of a planarized electrically contacted nanogap formed in between Au nanoplates. (b) Scanning-electron micrograph of the corresponding nanogap with a width of ~30 nm. (c) The AFM surface topography of the structure shows uniform surfaces on the Au nanoplates and lithographically patterned Au wires achieved through the peeling technique. (d) A uniform AFM profile is observed across the nanogap.

substrate. The bottom surfaces of the patterned structures assume the surface roughness of the underlying substrate. By revealing this surface after peeling, the electrical connections acquire a roughness much smaller than that associated with the top surface of evaporated Au thin-film. An example of the peeling process improving the lithographically patterned structures is shown in Figure 5, where uniform edges and Au surfaces with <1 nm average roughness are achieved. Such structures can be integrated with the nanogaps formed through self-assembly, or can serve as stand-alone building units of nanoscale devices and systems.

In addition to achieving lateral resolution in defining nanometer-thin gaps between electrodes, controlling vertical heights within nanometers of each other is of interest. This is essential for applications where well-defined non-uniform spatial profiles are necessary. The peeling technique can be extended further to achieve this

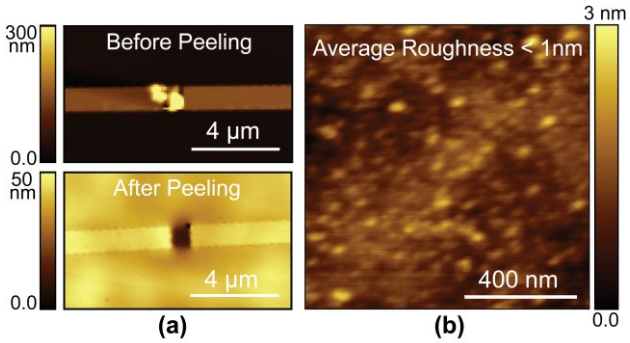

Figure 5: The peeling technique can also be used with the nanoscale patterns formed through lithography and lift-off. It helps eliminate the edge defects imposed by the lift-off process (a) and achieve <1 nm average surface roughness (b) by making accessible for further processing the side of the Au film originally in contact with the flat substrate.

goal. In this next approach, summarized in Figure 6a, a two-dimensional material, such as graphene, due to its well-defined thickness, is patterned to be used as a sacrificial layer, defining the height difference between the neighboring structures. Once the structures are fabricated through use of electron-beam lithography and lift-off, they are peeled off the substrate. The exposed graphene is then etched using oxygen plasma, revealing a recessed profile corresponding to the thickness of the graphene. Figure 6b shows neighboring electrodes fabricated with a 4 nm height difference, illustrating the versatility of the peeling technique to also achieve nanometer vertical resolution. This facilitates the approach to be extended beyond two-terminal structures

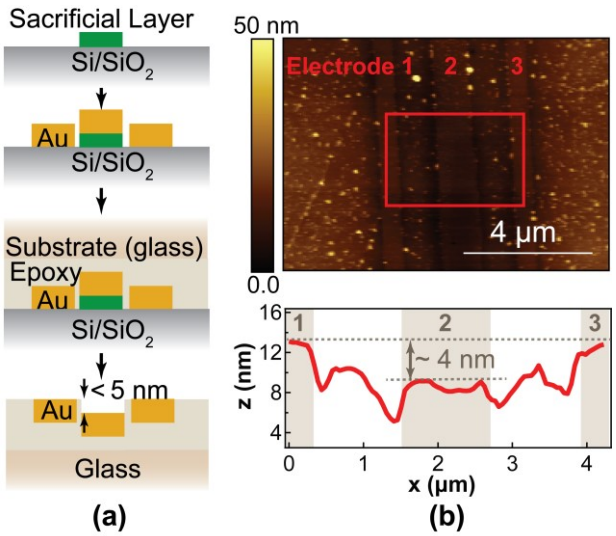

Figure 6: (a) An extension of the peeling technique utilizes atomically well-defined two-dimensional materials patterned through lithography as sacrificial layers to define neighboring vertical dimensions with <5 nm relative height differences. Once peeled off the substrate, the sacrificial layer is etched to produce the desired height variation. An example is shown in (b) where Electrode 2 is recessed by ~4 nm relative to Electrodes 1 and 3 using graphene as the sacrificial material, and evaporated Au as electrodes.

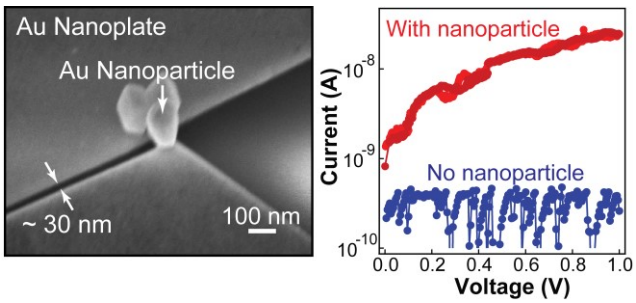

Figure 7: Through dielectrophoretic positioning of Au nanoparticles coated with a molecular layer across the nanogap, vertical molecular tunnel junctions can be formed. The SEM image shows Au nanoparticles coated with cetylpyridinium chloride bridging a ~30 nm gap formed in Au nanoplate electrodes. The current-voltage characteristic compares the current conduction through the laterally self-assembled nanogap (blue curve) with that of the smaller vertical molecular gaps formed upon bridging the lateral gap with Au particles (two I-V traces corresponding to this conformation are shown in red).

to enable multi-terminal designs and more complex applications in integrated systems.

The fabricated electrically-driven nanogaps can be used as building-blocks of nanoscale devices with applications in nanoelectromechanical systems, molecular electronics and active plasmonics [7, 8]. They serve as a platform where further processing is used to achieve tailored functionalities. An example application is shown in Figure 7. Here, Au nanoparticles coated with a layer of cetylpyridinium chloride (CPC) are dielectrophoretically trapped across the gap to form a vertically-defined molecular junction. The current-voltage characteristics of Figure 7 show an increase in conduction through the molecular junction formed based on the nanoparticle, compared to the current conduction through the laterally aligned nanogap prior to nanoparticle trapping. By tailoring the thickness and type of molecular coating employed in functionalizing the nanoparticle or the Au nanoplate surfaces, molecular junctions of varying electronic performance emerge. Subsequently, a range of applications in molecular electronics can be realized.

The proposed fabrication technique provides a suitable platform for manufacturing nanoscale structures with nanometer resolution and surface uniformity. The technique is demonstrated with Au nanoplates and interconnects. However, it can be easily extended to other materials and their combinations. Currently, due to the relatively large size distribution present in the nanoplates, the assembly is often localized and does not span the entire substrate. Further optimization is necessary to enable uniform self-assembly over larger areas with precise control over spatial positioning.

CONCLUSION

The unprecedented precision and resolution of bottom-up assembly is combined with the versatility of top-down lithography to develop a technique for fabricating electrically-driven well-defined nanogaps as small as ~10 nm. A planarization technique is implemented to ensure the surfaces of the resulting electrodes assume the desired uniformity. An extension of this technique further realizes nanometer precision in defining height variations between neighboring structures, enabling electrode architectures of higher complexity. Overall, a platform to enable nanodevices of various functionalities for molecular electronics, plasmonics, and nanoelectromechanical systems is achieved.

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