300 µm DEEP THROUGH SILICON VIA IN LASER-ABLATED CMOS MULTI-PROJECT WAFER FOR COST-EFFECTIVE DEVELOPMENT OF INTEGRATED MEMS

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ABSTRACT

This study has opened a possibility to fabricate through silicon vias (TSV) in a LSI wafer available by commercial multi-project wafer (MPW) service and integrate the LSI and MEMS by wafer bonding. 300 µm deep Cu annular type TSV were fabricated in a TSMC 0.18 µm CMOS LSI MPW cut into 4" diameter. The developed TSV process managed mechanically fragile property of the laser-ablated MPW by low stress TEOS PECVD SiO_2 backfilling, surface planarization, temporally wafer support etc. The LSI and MEMS were integrated by Au-Au thermocompression bonding at 300°C, and the completed device worked via the TSV as designed. "Tohoku TSV CMOS-MEMS platform" presented in this paper gives many chances for cost-effective development of surface-mountable CMOS-integrated MEMS.

INTRODUCTION

Recently, wafer-level MEMS-CMOS integration and packaging technology is a key for the competitiveness of sensors with a very small footprint. It is the case with the latest multi-degree of freedom inertial sensors. This technology is being requested further progress for monolithic combo sensors and other emerging sensors. Actually, this study was motivated by our development of an emerging sensor; a bus-networked CMOS-integrated tactile sensor for human support robots [1]. As shown in Fig. 1 (a), the tactile sensor is directly surface-mounted on a flexible bus line. Therefore, the bonding pads must be located on the backside, because the topside is a sensing side and must be free from bonding wires. In addition, the tactile sensor is physically touched and thus must be mechanically robust. To answer these requirements, the device structure using through silicon vias (TSV) in a CMOS LSI shown in Fig. 1 (b) is preferable.

We have developed our original CMOS LSI for the tactile sensor, which provides functions of 4 differential pairs of capacitance readout, encoding, packet generation, bus communication, configuration etc. [2]. The LSI uses TSMC 0.18 µm mixed signal CMOS process, and is obtained on an 8" multi-project wafer (MPW). For research and development, especially in academia, MPW service is the most practical route to prototype a standard or advanced LSI from a cost point of view.

The MPW contains multiple kinds of LSI from different users. Each user can receive its own LSI on full wafers, where the other LSIs are erased by laser ablation, as shown in Fig. 2. Therefore, we need to fabricate TSV in such a laser-ablated MPW and then integrate it with

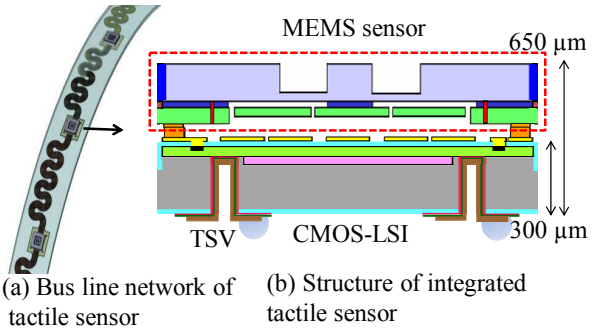


Figure 1: Surface-mounted CMOS-integrated MEMS tactile sensor.

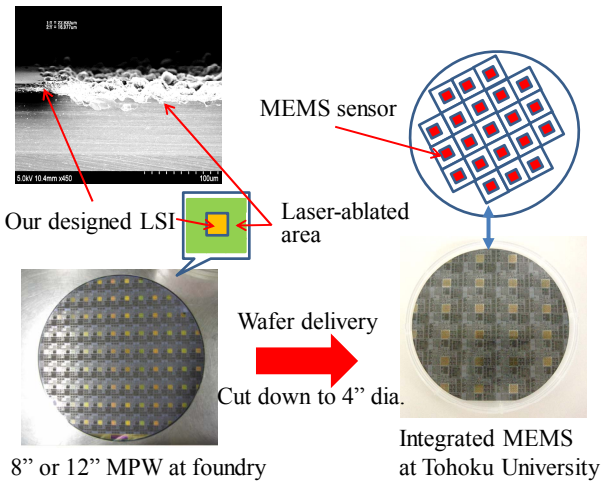


Figure 2: Multi-project wafer (MPW) of LSI with laser-ablated area.

MEMS by wafer bonding. To make matters more difficult, the laser-ablated MPW is very fragile due to surface roughness and damage shown in Fig. 2 (left upper). In this study, we developed a deep TSV process on the laser-ablated MPW for the first time. The developed TSV process will offer industry and academia a lot of chances to develop surface-mountable CMOS-integrated MEMS.

DESIGN

Most of the TSV proposals have targeted three-dimensional integration of memories and processors [3, 4]. In terms of fabrication process, "via last" process, in which TSV are fabricated after the backend of line (BEOL) process of LSI, is major compared with "via first" and "via middle" processes. The "via last" process is only a choice for us, because TSV are fabricated by ourselves in MPW

Table 1: Comparison of via-last TSV.

	Fine	Middle	This work
Depth (μm)	30-50	100-120	**300**
Diameter (μm)	5-10	40-70	110
TSV structure	Cu fill	Cu fill	Cu annular

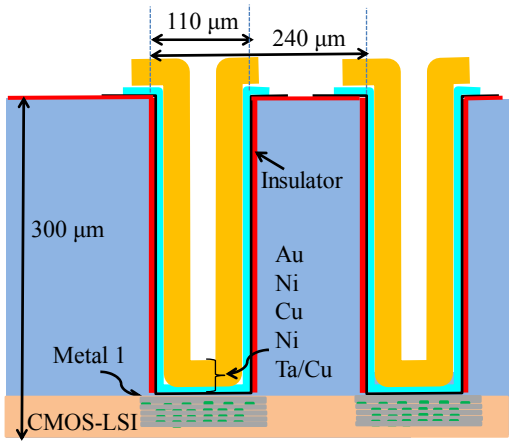


Figure 3: Structure of proposed annular type TSV in LSI.

received from the foundry (TSMC, Taiwan).

As mentioned, our target device is the tactile sensor. To secure mechanical strength up to several kgf/die in normal and shear directions, the thickness of the LSI must be 300 μm or larger. Consequently, the TSV are as deep as the thickness of the LSI. This is another unique requirement in addition to the TSV process on the laser-ablated MPW, because most of existing TSV have considerably different dimensions in depth and diameter [3-6], as summarized in Table 1.

The MPW is finally integrated with a MEMS wafer by Au-Au thermocompression bonding at 300°C [7]. This process as well as soldering process imposes thermal stress because of large difference in the coefficient of thermal expansion between Cu (16.5 ppm/°C) and Si (3.3 ppm/°C). This stress may cause cracks especially in the BEOL of the LSI, because the size of the TSV is large. Therefore, we have selected annular type Cu TSV illustrated in Fig. 3, which is better for stress release than Cu filling type. The minimum pitch of the TSV is 240 μm from the requirement of our tactile sensor. Therefore, the TSV must have almost straight sidewalls rather than tapered ones.

The influences of thermal stress were investigated by a finite element method (FEM) and compared between the Cu filling and annular types. Figure 4 shows simulated stress distributions around TSV of 100 μm diameter and 300 μm depth, assuming a temperature rise of 300°C. The material constants for the simulation are listed in Table 2. The annular type TSV has 1 μm thick insulator SiO_2 and conductor metals (0.5 μm thick Ni and 10 μm Cu) on the sidewall. The Cu filling type TSV has the same SiO_2 and Ni. The maximum Mises stress of 720 MPa was observed in the Cu filling type, while less than 400 MPa in the annular type.

FABLICATION

Planarization of MPW

The MPW made by TSMC 0.18 μm CMOS process is

Table 2: Material constants of FEM model.

	E (GPa)	Poisson's ratio	CTE (ppm/K)
Silicon	130	0.28	3.3
SiO_2	73.1	0.17	0.55
Nickle	201	0.31	13.4
Copper	123	0.35	16.5

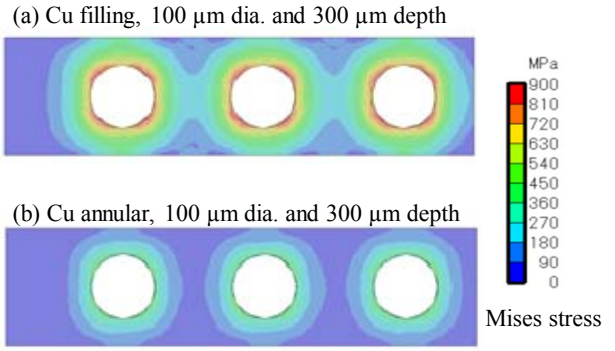


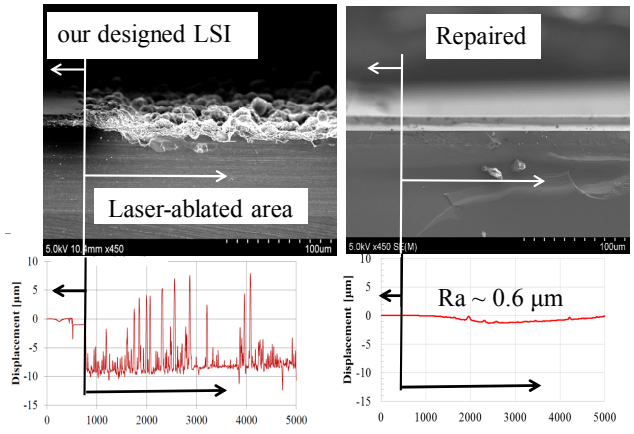
Figure 4: Distribution of Mises stress around (a) Cu filling and (b) annular type TSV calculated by FEM.

received in the form of a full 8" wafer with a thickness of 750 μm. The wafer is cut down to a pair of 4" wafers, which can be processed in Tohoku University. 12" LSI wafers can be processed in the same manner. The peak to valley roughness of the laser-ablated area is approximately 20 μm. Therefore, SiO_2 thicker than 20 μm with extremely low residual film stress is deposited for backfilling it. We developed the condition of TEOS plasma enhanced chemical vaper deposition (PECVD) to meet this requirement. The control of cathode RF power is a key [8], and the optimum condition shows less than 10 MPa compressive stress for 20 μm thick SiO_2 on Si.

Chemical mechanical polishing (CMP) is then applied to finish the LSI surface smooth enough for the following wafer process. Back grinding is done to thin the planarized MPW down to 300 μm in thickness. Figure 5 shows the scanning electron microscope (SEM) images and surface profiles of the laser-ablated area (a) before and (b) after planarization. The roughness of the finished surface is about 0.6 μm Ra, which is acceptable for further processing.

Metallization and bonding bump formation

On the planarized MPW, metal electrodes and bonding bumps are formed as shown in Fig. 6. The outer bonding bump (sealing frame), which is used for integration with MEMS and sealing, is formed by Au electroplating on a sputtered Cr/Ru/Au seed layer using a photoresist mold (Fig. 6 (a)). The surface of the Au bumps is fly-cut using a diamond bit to reduce the variation of height into about 5 μm as well as surface roughness (b). Mechanical stress by fly-cutting forms fragmented crystal grains on the Au surface, which help thermocompression bonding at lower temperature [7]. For rewiring and sensing electrodes, the Cr/Ru/Au seed layer was patterned by wet etching (c). In comparison with dry etching, wet etching is free from plasma damage to LSI and preferable in this process. Figure 7 shows the optical microscope image of the LSI surface after the final step in Fig. 6.



(a) Before planarization (b) After planarization

Figure 5: SEM images and surface profiles of ablated area before and after planarization.

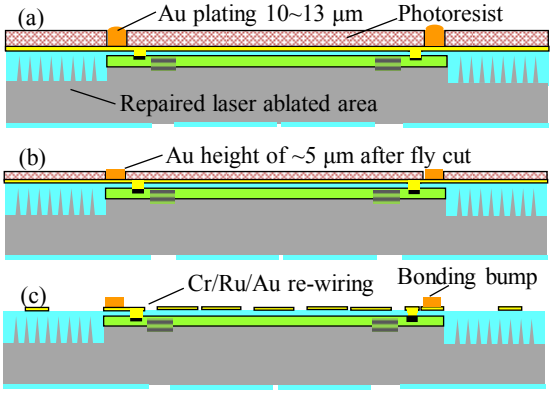


Figure 6: Fabrication process of metal electrodes and bonding bumps.

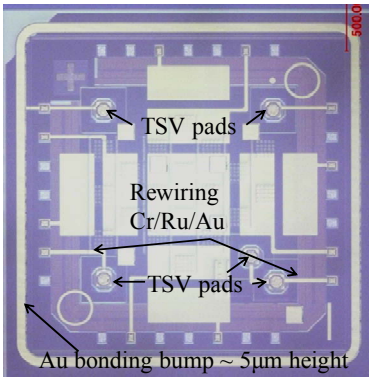


Figure 7: Front side of LSI after process shown in Fig. 6.

Fabrication of deep annular TSV

The fabrication process of the TSV is shown in Fig. 8. After bonding with a support wafer using photoresist to protect the front side, the MPW is etched from the backside by Bosch process using a SiO_2 mask to create via holes (Fig. 8 (d)). The via holes of 110 µm diameter reach the bottom layer of the BEOL, i.e. Metal 1. After removing the support wafer, 2 µm thick SiO_2 is conformally deposited by TEOS PECVD as the insulator of the TSV sidewalls (e). No wafer bending was observed after SiO_2 deposition using the developed low stress PECVD condition. In addition, a dielectric breakdown voltage higher than 8 MV/cm was confirmed using electric test patterns.

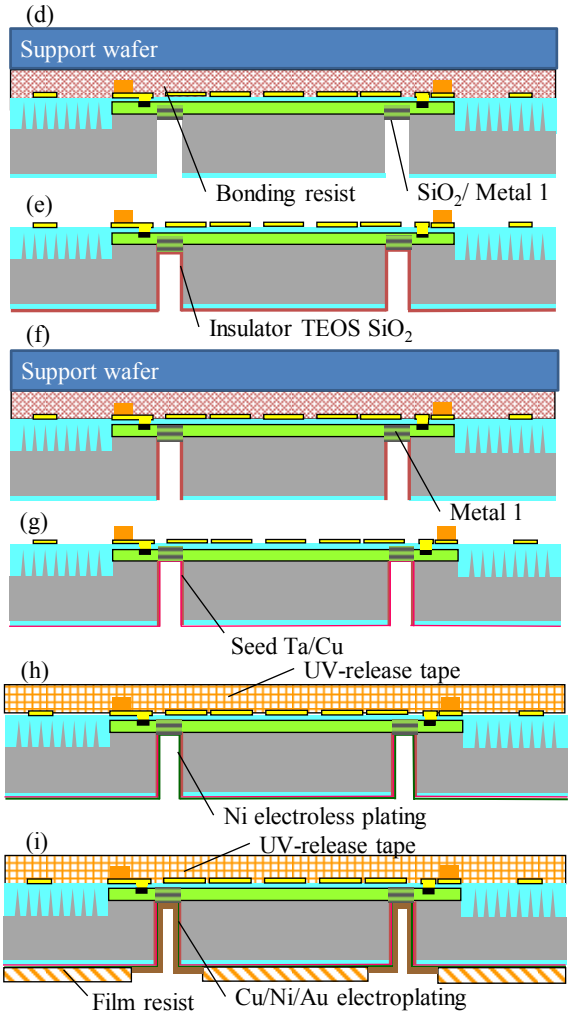


Figure 8: Fabrication process of TSV.

For the electrical connection of the TSV, SiO_2 at the bottom of the via holes is removed by RIE, while SiO_2 on the sidewalls is left unetched (f). Such selectivity is realized by enhanced Ar ion bombardment under the condition that Ar concentration in $C_4F_8 + O_2 + Ar$ etching gas is higher than 80%. 400 nm thick Ta and 1 µm thick Cu are sequentially deposited by RF magnetron sputtering as a barrier layer of Cu diffusion and an adhesion layer, respectively (g).

The LSI front surface is covered with a UV-release tape, and then 0.5 µm thick Ni is deposited by electroless plating using a film resist mask (h). Subsequently, 10 µm thick Cu is deposited by electroplating using Ni as a seed layer (i). When 10 µm thick Cu was grown on the surface, about 1.5 µm thick Cu was observed at the bottom of the via holes. Finally, the UV-release tape and the film resist are peeled off by UV light and alkali solvent, respectively. Figure 9 shows the cross-sectional SEM image of the completed TSV in the TSMC 0.18 µm MPW.

Wafer bonding

The CMOS LSI with the TSV is integrated with MEMS by Au-Au thermocompression bonding, as show in Fig. 10. For this process, the 4" MPW is diced into 16 mm square pieces, which includes 4 dies of our LSI and the other laser-ablated area. The LSI piece has planarized Au

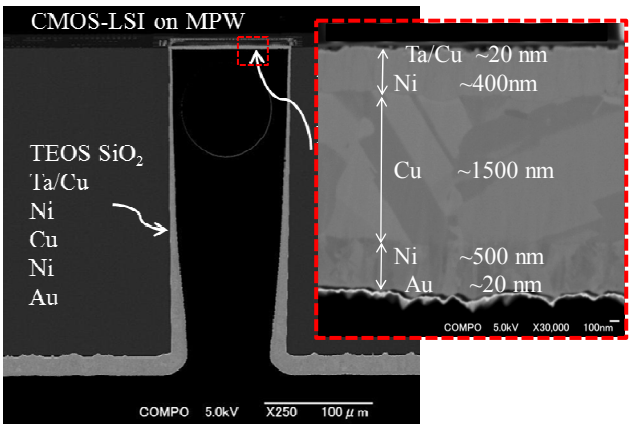


Figure 9: Cross-sectional SEM image of deep annular TSV.

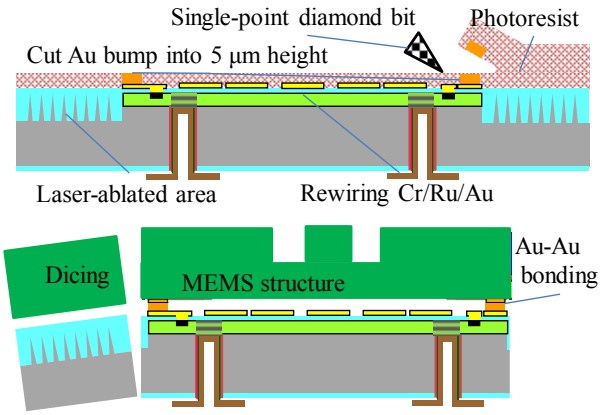


Figure 10: MEMS integration process by thermocompression Au-Au bonding. The Au bumps are planarized by fly cut during the process shown in Fig. 6.

bumps (sealing rings) of 5 μm height, while the MEMS piece has sputtered Cr/Pt/Au patterns as the counterparts of the Au bumps. These pieces are aligned and bonded at 300°C by applying a bonding pressure of 18 MPa. Figure 11 shows 2.5 mm × 2.5 mm dies after blade dicing.

EVALUATION

Electrical test of TSV

For an electrical test, a daisy chain structure where 4 TSVs were connected in series was fabricated by the same process of the TSV. The resistance of the daisy chain, i.e. the TSV and planar Cu interconnection, was measured by Kelvin probe method at 5 mA. For heat run test, the sample was heated at 350°C for 30 min, which was severer than the actual wafer bonding condition. Figure 12 shows measured resistance per via before and after the heat run test. There is no significant difference in the mean and variation of the resistance.

Device evaluation

The integrated device (Fig. 11) was preliminary tested via the TSV. Power, ground and signal lines were connected to the bonding pads at the backside of the die. The pass rate of ESD protection diode circuit test was 100%. Measured oscillation frequency was 948 kHz, which well agreed with the design value. Finally,

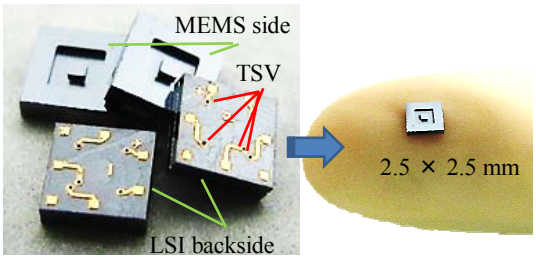


Figure 11: CMOS-MEMS integrated dies with TSV.

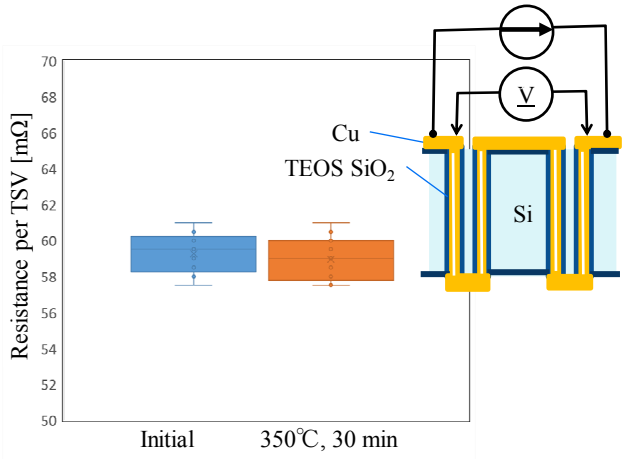


Figure 12: Resistance of TSV measured by Kelvin probe method before and after heating at 350°C for 30 min.

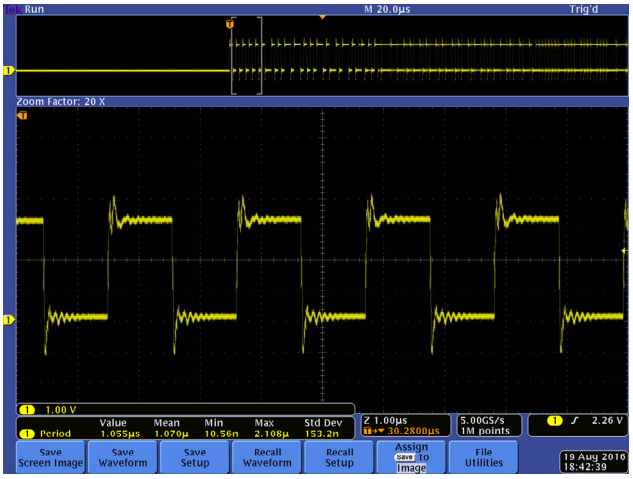


Figure 13: Measured output waveforms from completed die.

the digital output shown in Fig. 13 was decoded by our host software [2], and it was confirmed that the decoded data was interpretable.

CONCLUSION

We fabricated Cu annular type TSV in a laser-ablated 0.18 μm CMOS LSI MPW, and demonstrated wafer-bonding-based CMOS-MEMS integration. The MPW received from TSMC was laser-ablated except for our own dies, which made the wafer mechanically fragile. The laser-induced surface roughness and damage were repaired by low stress TEOS PECVD SiO_2 backfilling and CMP. The TSV are 100 μm in diameter and 300 μm in depth. Such deep TSV were made by low stress conformal

TEOS PECVD, via bottom etching, electroless and electro plating into deep via holes etc. The LSI and MEMS were integrated by Au-Au thermocompression bonding at 300°C. The integrated device was tested in terms of the electrical connectivity of the TSV and the functionality of the LSI, and worked as designed. "Tohoku TSV CMOS-MEMS platform" developed in this study is useful for cost-effective development of surface-mounted integrated MEMS.

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