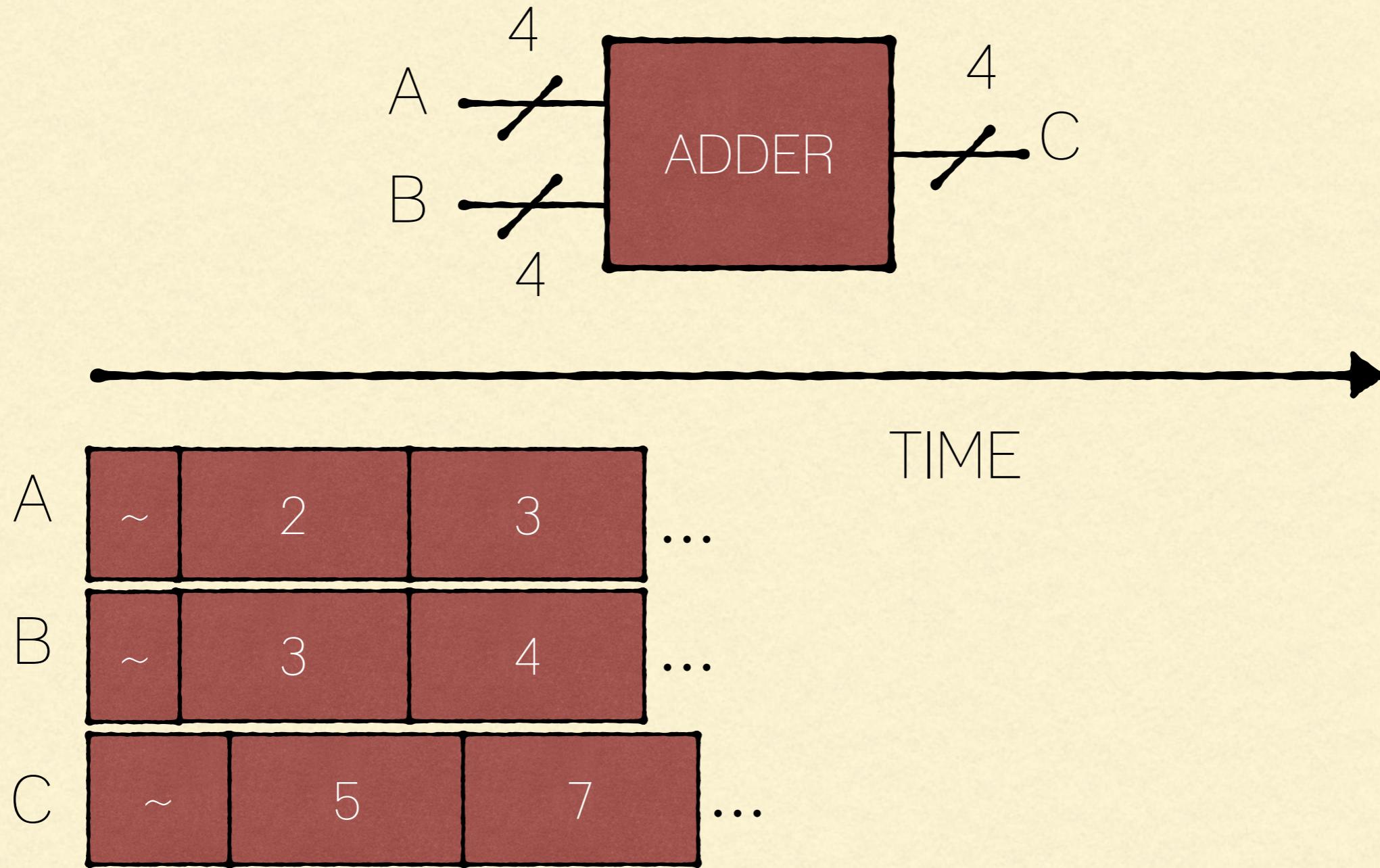
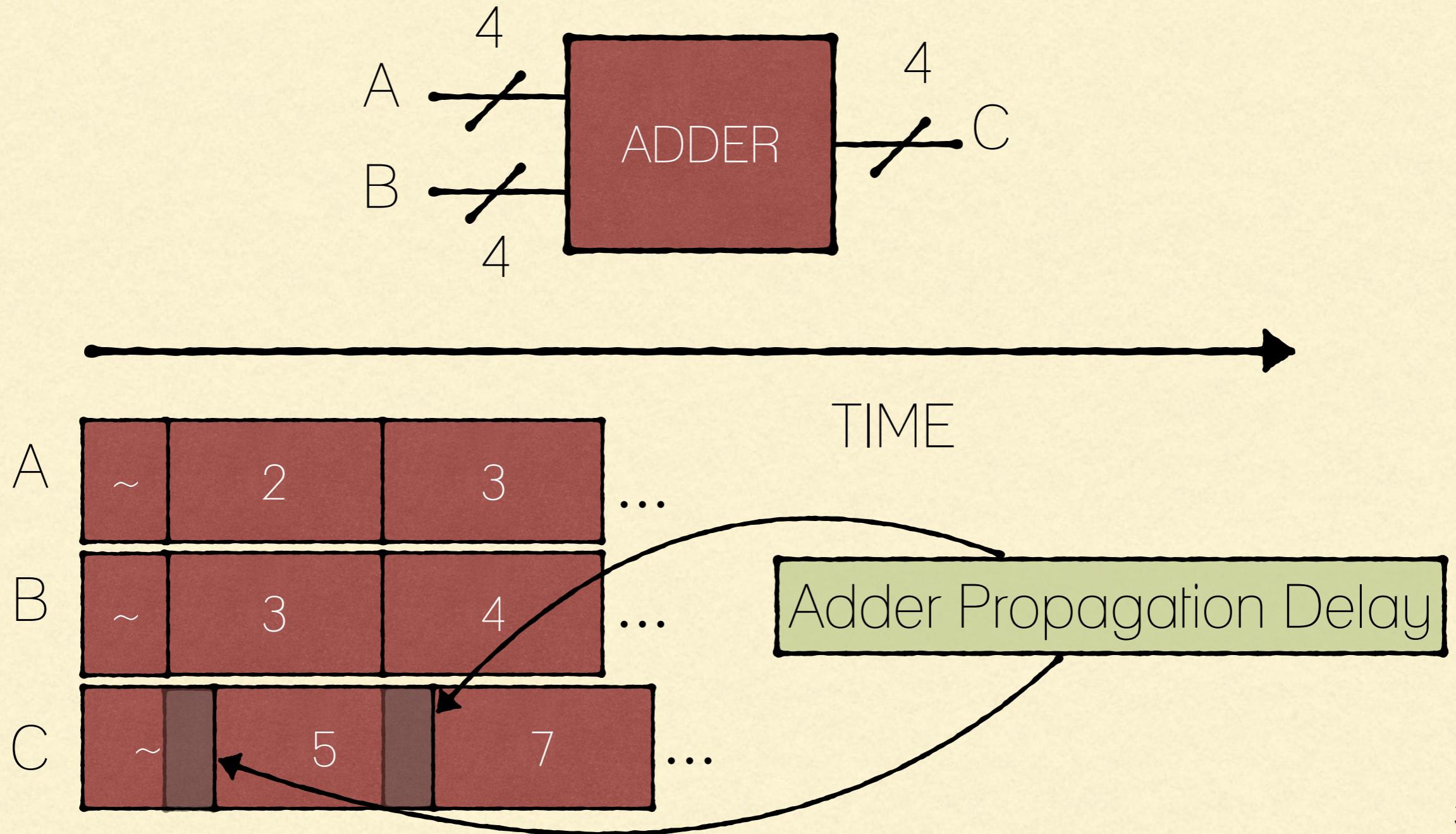

CPU CLOCK & SINGLE-CYCLE DATAPATH PART I

Ayman Hajja, PhD

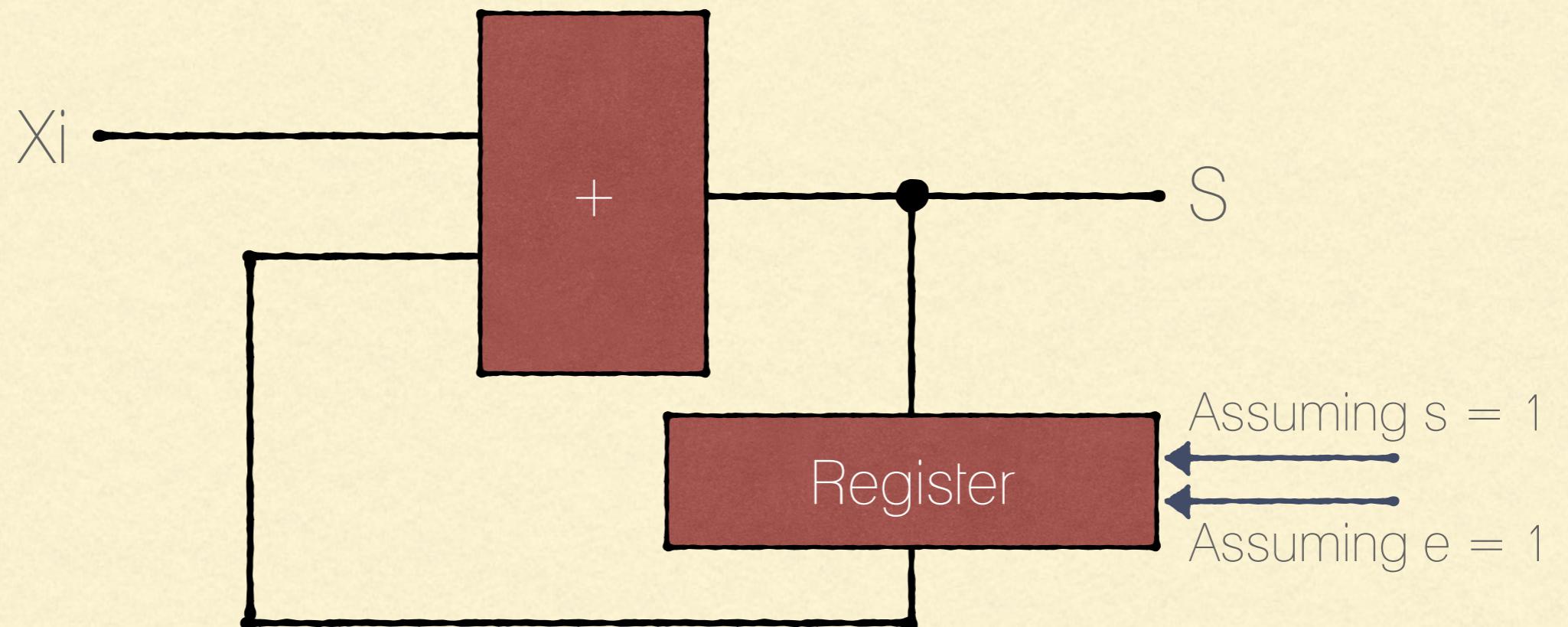
SIGNALS AND WAVEFORMS; CIRCUIT DELAY



SIGNALS AND WAVEFORMS; CIRCUIT DELAY



ACCUMULATOR EXAMPLE



- Register is used to hold and transfer the data to adder
- However, we need to control the next iteration of the loop — too slow/fast?

INTRODUCING EDGE-TRIGGERED D-TYPE FLIP FLOP

- Edge-triggered d-type flip-flop

On the rising edge of the clock, the input d is sampled and transferred to the output. At all other times, the input d is ignored

- Example waveform:

- CLK



- d (input)

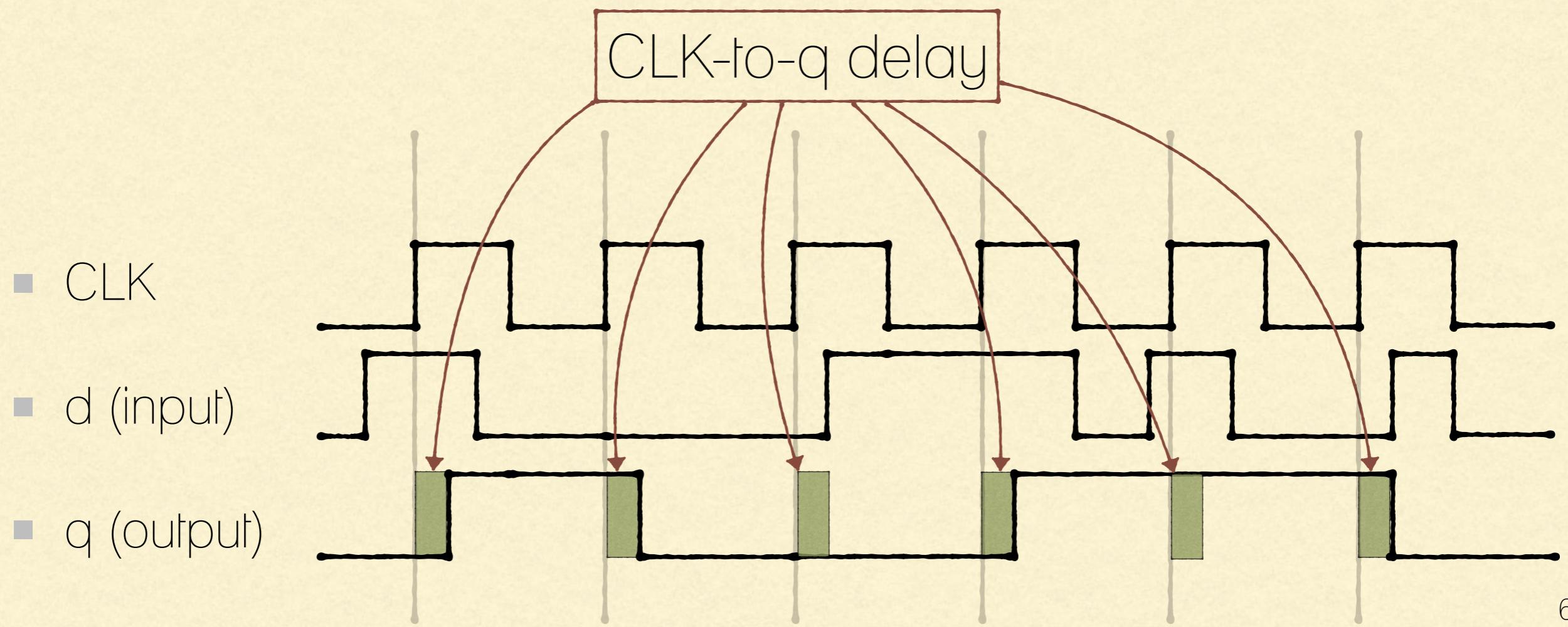


- q (output)

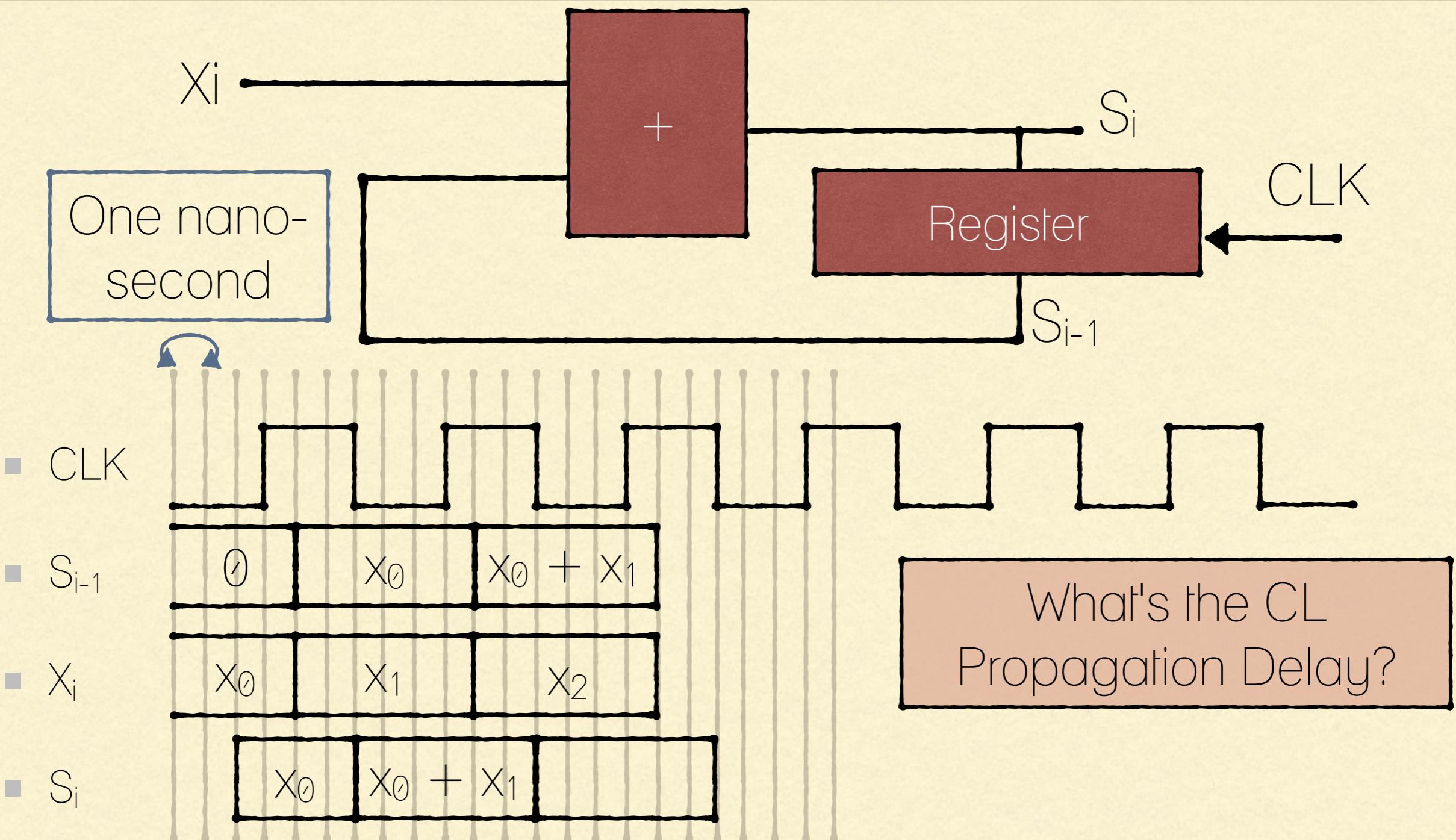


INTRODUCING EDGE-TRIGGERED D-TYPE FLIP FLOP

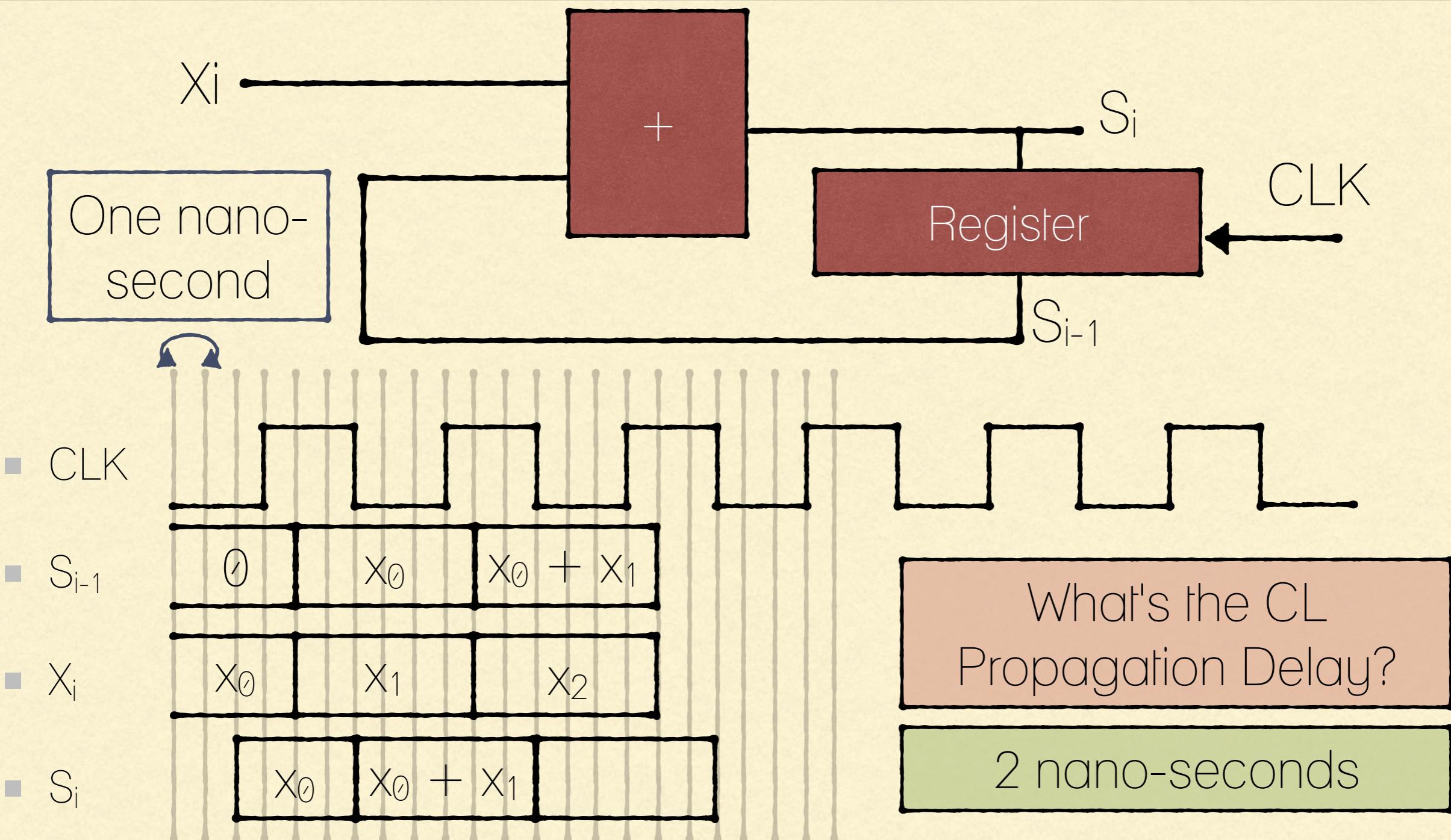
In reality, there's a delay in the flip-flop for the output to be reflected when the input changes



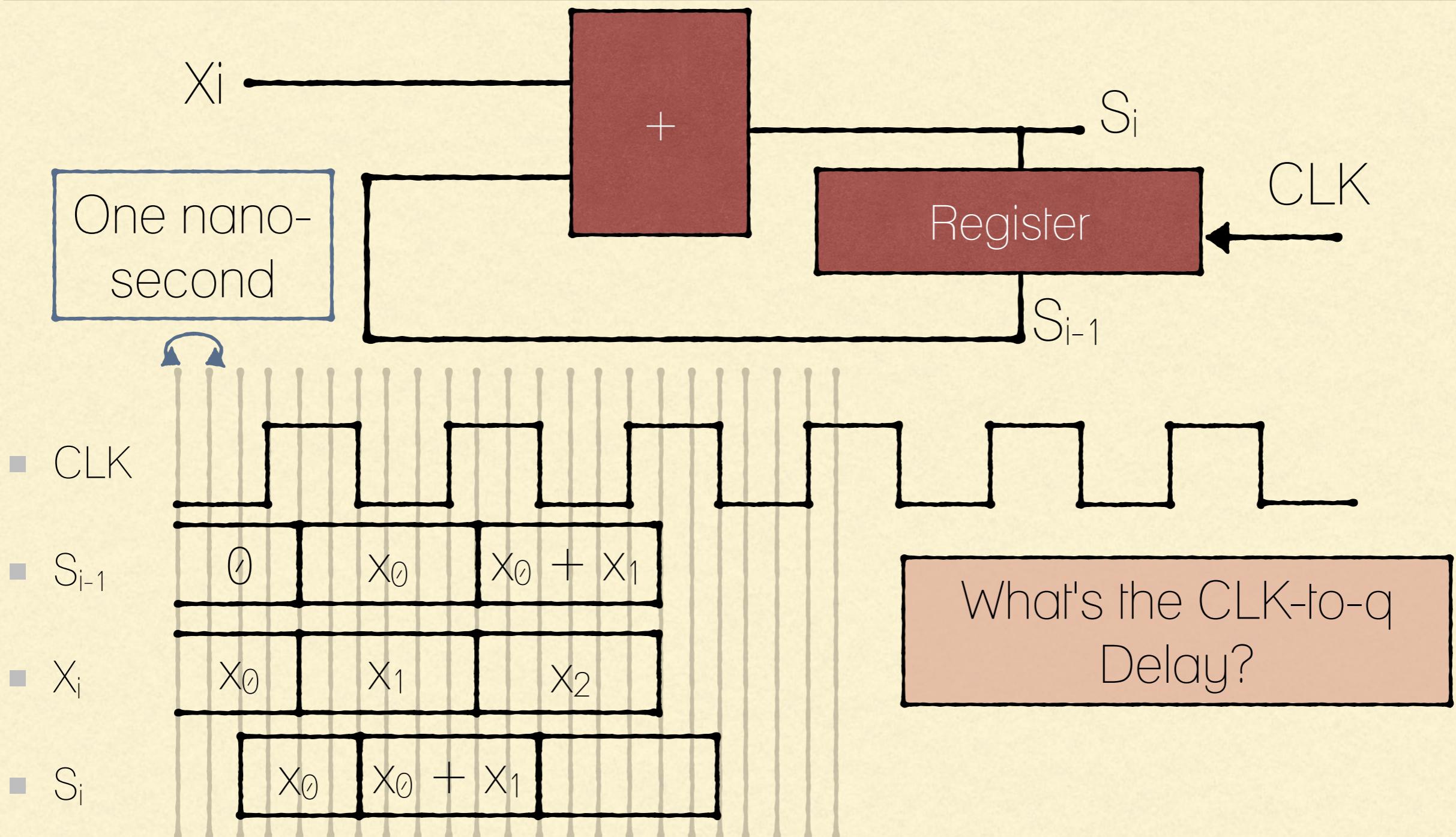
ACCUMULATOR EXAMPLE



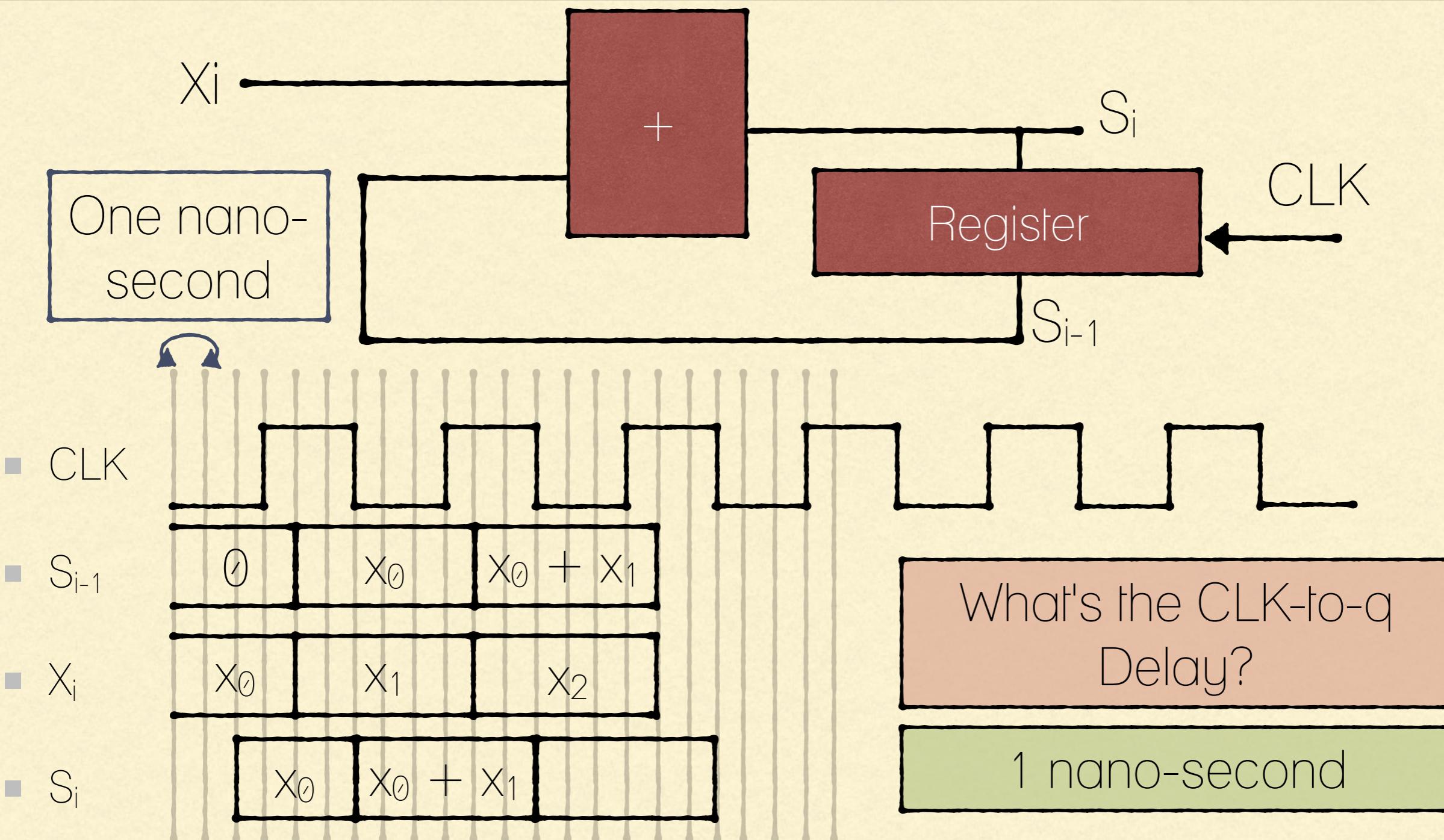
ACCUMULATOR EXAMPLE



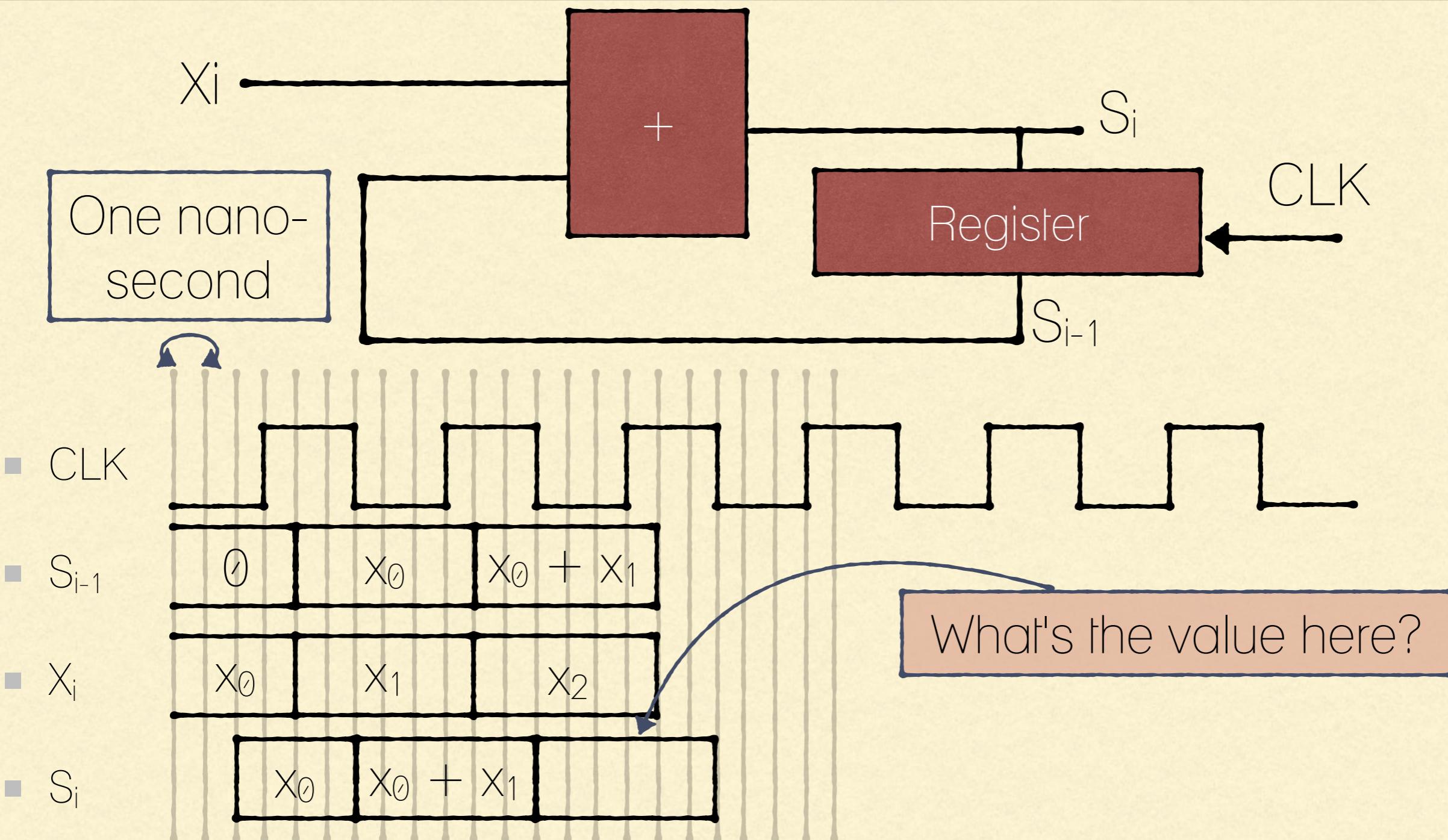
ACCUMULATOR EXAMPLE



ACCUMULATOR EXAMPLE



ACCUMULATOR EXAMPLE



ACCUMULATOR EXAMPLE

