SINGLE-CYCLE DATAPATH PART III

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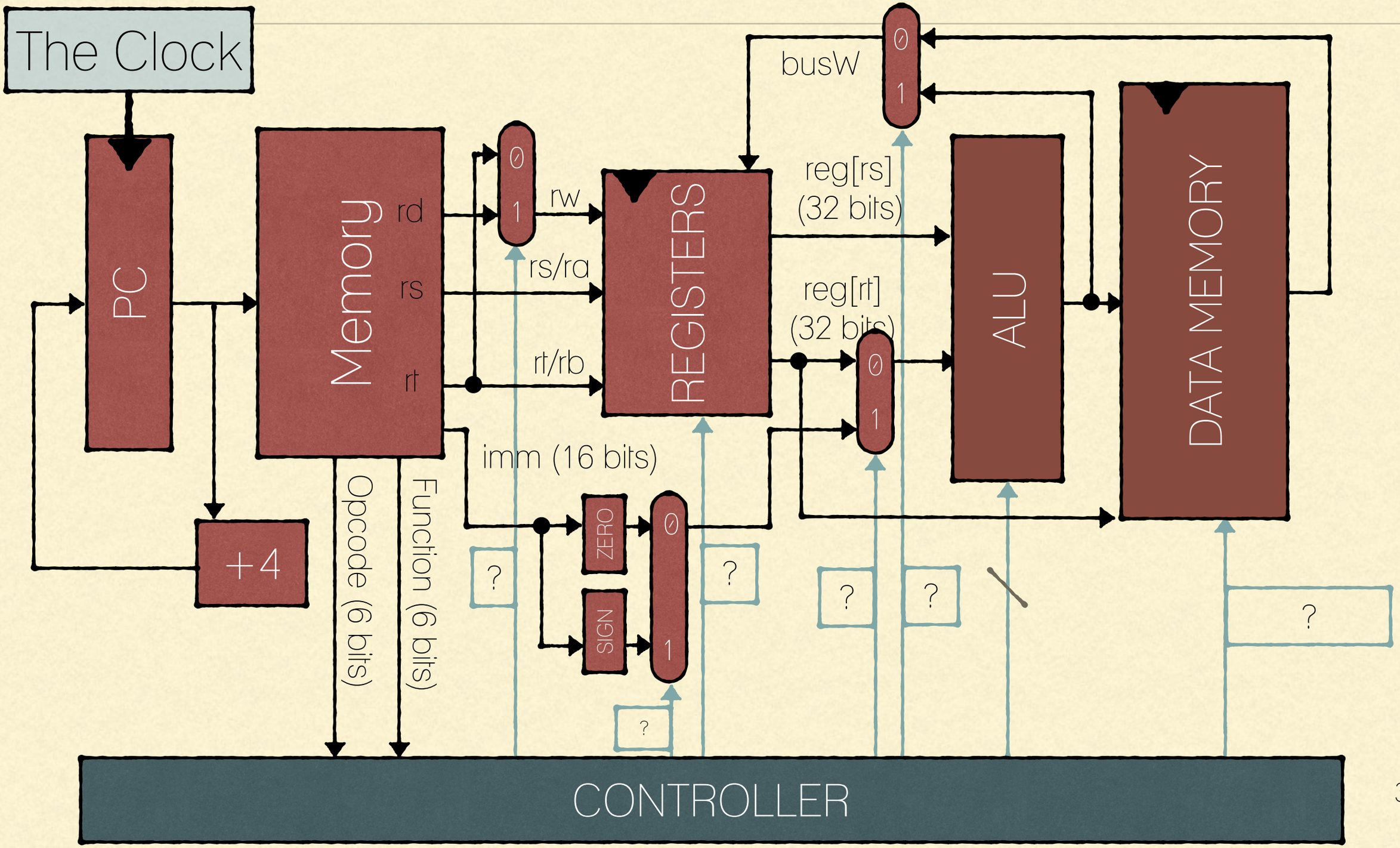
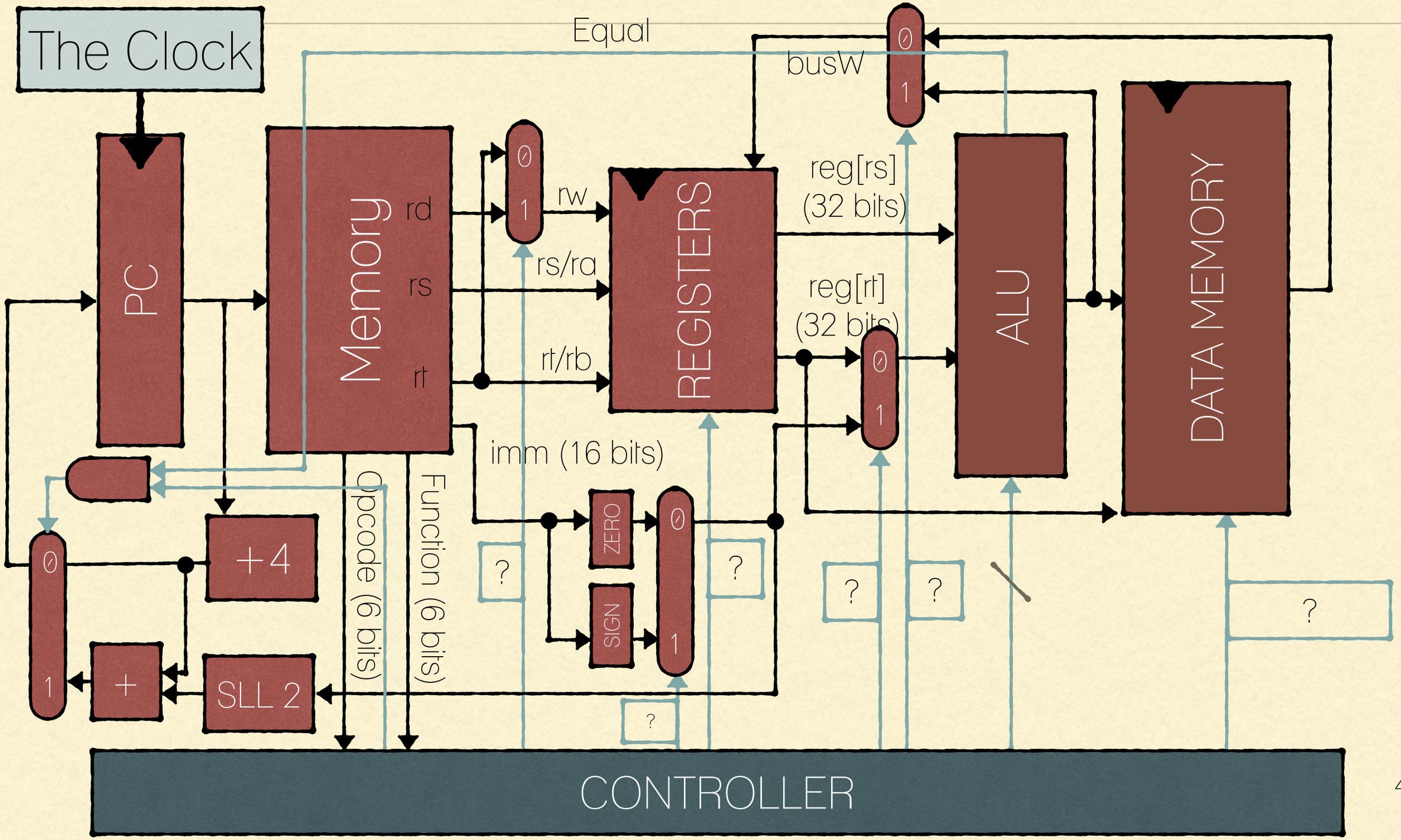
BRANCH OPERATIONS

- if (R[rs] == R[rt])
  - PC ← PC + 4 + {sign_ext(Imm16), 2'b00}
- else:
  - PC ← PC + 4

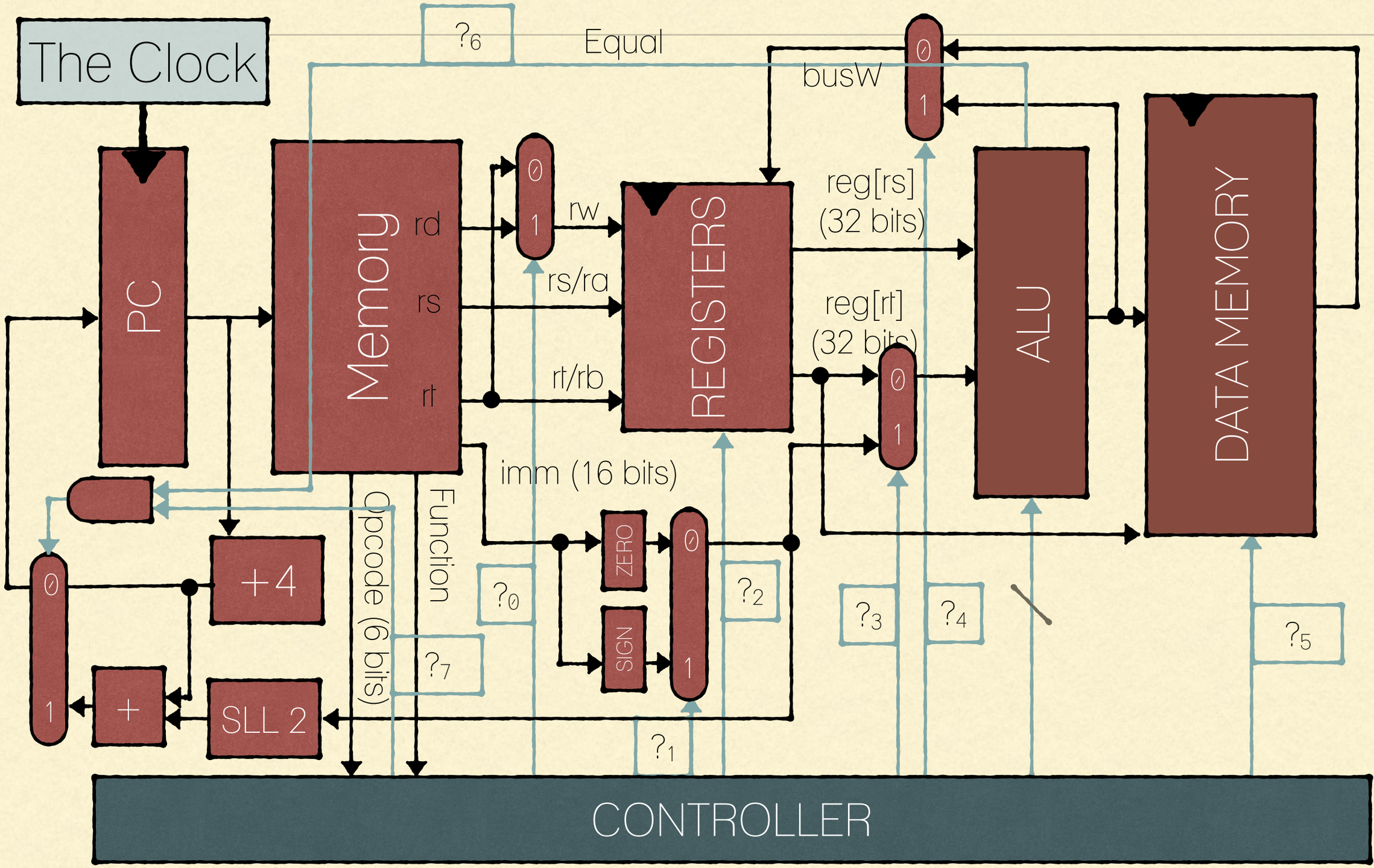
BEFORE ADDING 'BRANCH' HARDWARE



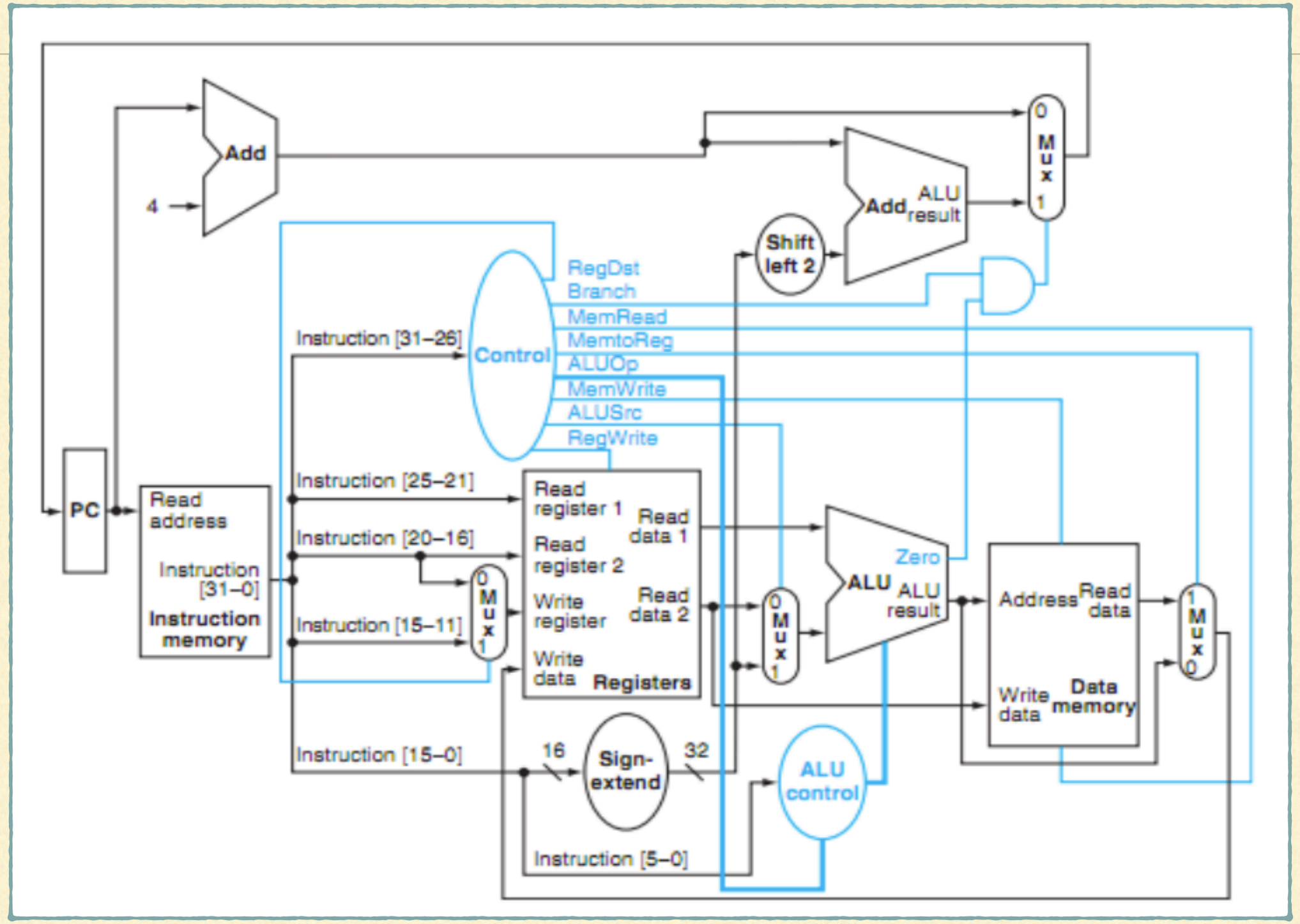
AFTER ADDING 'BRANCH' HARDWARE



AFTER ADDING 'BRANCH' HARDWARE



IN THE BOOK


Add
4
0
M
u
x
1
Add
ALU result
Shift left 2
RegDst
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Instruction [31–26]
Control
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Instruction [5–0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
16
Sign-extend
32
ALU control
Zero
ALU
ALU result
Address
Read data
Write data
Data memory

SINGLE-CYCLE PERFORMANCE

- Assume time for actions are
  - 100ps for register read or write, 200 ps for other events
- Clock period is:

Instr	Instr fetch	Register read	ALU op	Memory access	Register write	Total time
lw	200ps	100 ps	200ps	200ps	100 ps	800ps
sw	200ps	100 ps	200ps	200ps		700ps
R-format	200ps	100 ps	200ps		100 ps	600ps
beq	200ps	100 ps	200ps			500ps

- Clock rate (cycles/second = Hz) = 1/Period (seconds/cycle)