Assuming that the address bus is $\underline{\text{16 bits}}$. Fill the table below

Tag Size	Block Size	Block Offset Size	Number of Blocks/Rows	Number of Comparators	Set Index Size	Cache Size	Cache Architecture
?	8	?	32	?	?	?	Fully Associative
?	?	2	64	?	?	?	Fully Associative
?	?	4	?	?	4	?	Direct Mapped
?	128	?	?	?	?	512 Bytes	Direct Mapped
8	64	?	?	?	?	?	Direct Mapped

Answers

Tag Size	Block Size	Block Offset Size	Number of Blocks/Rows	Number of Comparators	Set Index Size	Cache Size	Cache Architecture
13	8	3	32	32	0	256 Bytes	Fully Associative
14	4	2	64	64	0	256 Bytes	Fully Associative
8	16	4	16	1	4	256 Bytes	Direct Mapped
7	128	7	4	1	2	512 Bytes	Direct Mapped
8	64	6	4	1	2	256 Bytes	Direct Mapped