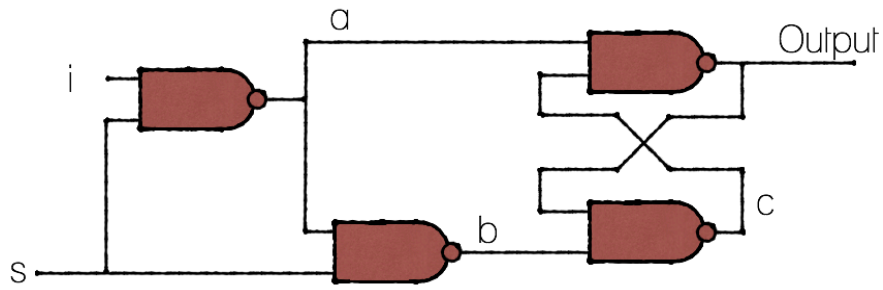
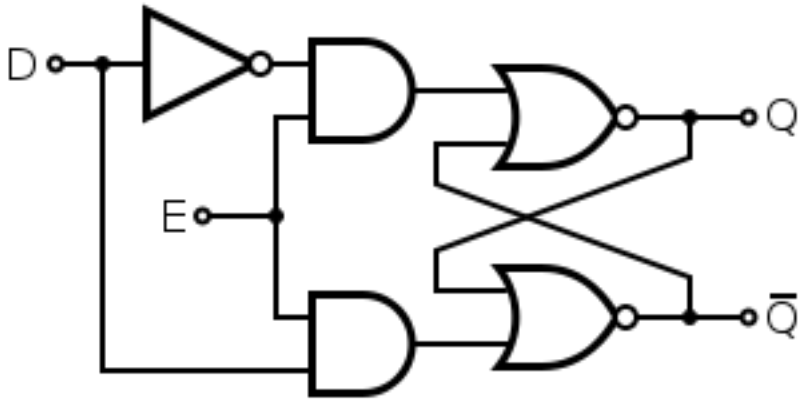
Q1) Fill the table below.



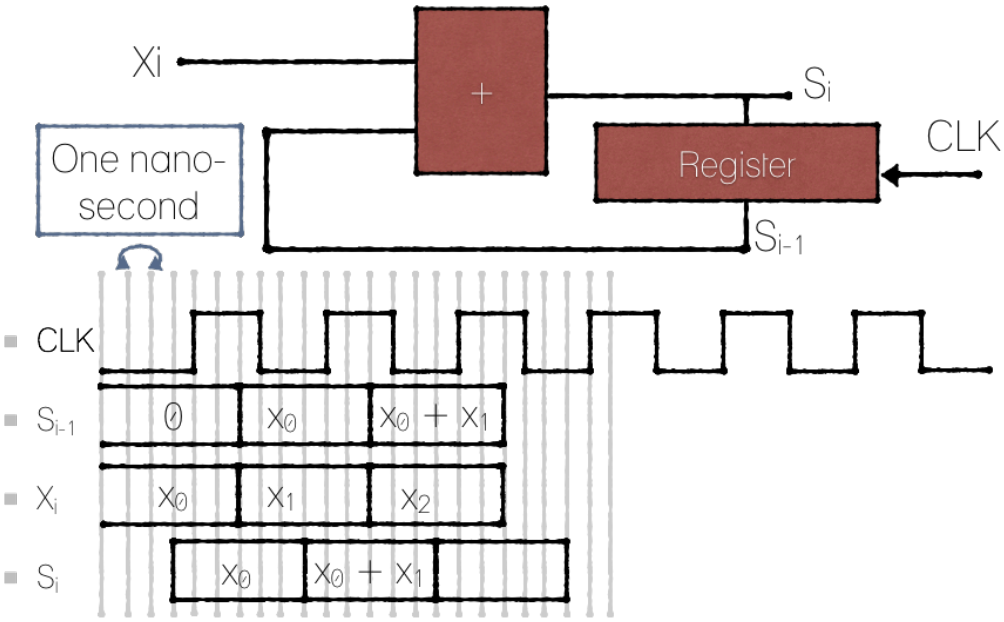
	i	s	Result	Do you need to know previous state to determine output (Yes/No)
First State	0	1	0	No
Second State	0	0	0	Yes
Third State	1	0	0	Yes
Fourth State	1	1	1	No
Fifth State	0	1	0	No

Q2) Fill the table below.



	D	E	Result	Do you need to know previous state to determine output (Yes/No)
First State	1	1	1	No
Second State	1	0	1	Yes
Third State	0	0	1	Yes
Fourth State	0	1	0	No

Q3) What's the combinational logic delay and the CLK-to-Q Delay for the diagram below?



Combinational logic delay: 3 nanoseconds
CLK-to-Q delay: 2 nanoseconds

Q4) Given that we're using an 'Edge-triggered flip-flop', draw the waveform for the output 'q'