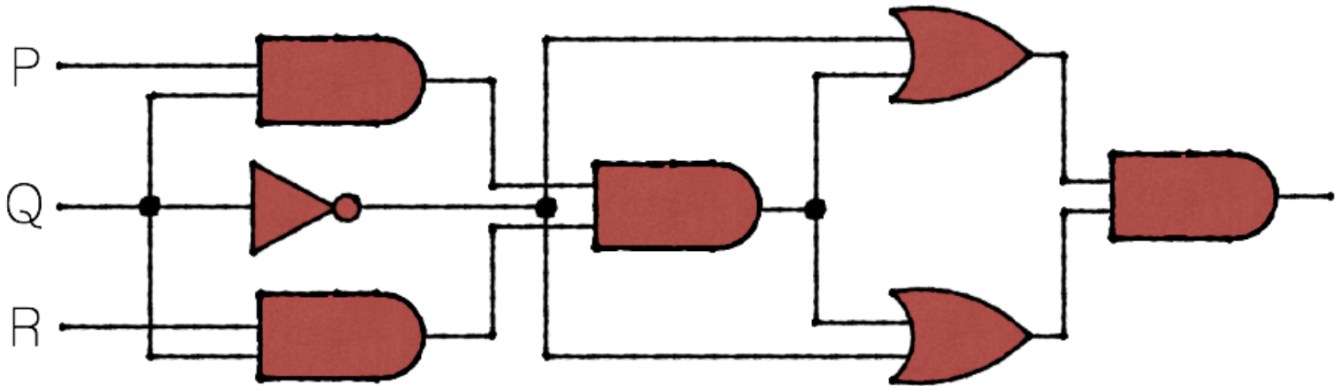


## Assignment 4 (Combinational & Sequential Logic)

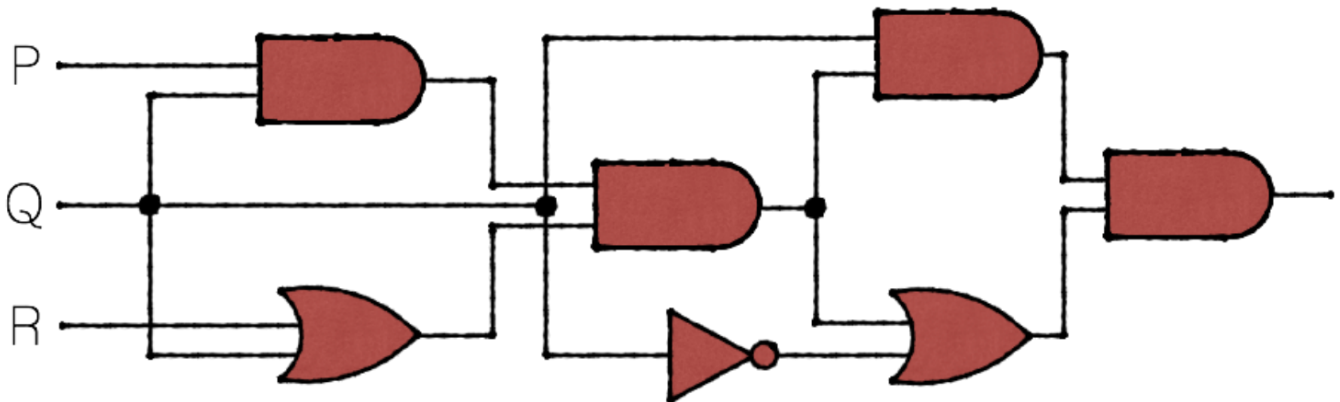
Find the output (boolean expression) for the circuit below (without simplifying):


$$(((P.Q).(Q.R))+\sim Q).(((P.Q).(Q.R))+\sim Q)$$

What is the number of control/select wires for an 8-1 multiplexer?

3

Find the output (boolean expression) for the circuit below (without simplifying):


$$(((P.Q).(Q+R)).Q).(((P.Q).(Q+R))+\sim Q)$$

The variables p, q, and s have the following truth values: p = True, q = True, s = False. What's the truth value for the following boolean expressions:

$$p + \sim q$$

True

The variables p, q, and s have the following truth values: p = True, q = True, s = False. What's the truth value for the following boolean expressions:

$$(p \cdot q) + s$$

True

# Assignment 4 (Combinational & Sequential Logic)

The variables  $p$ ,  $q$ , and  $s$  have the following truth values:  $p = \text{True}$ ,  $q = \text{True}$ ,  $s = \text{False}$ . What's the truth value for the following boolean expressions:

$$p \cdot (q + s)$$

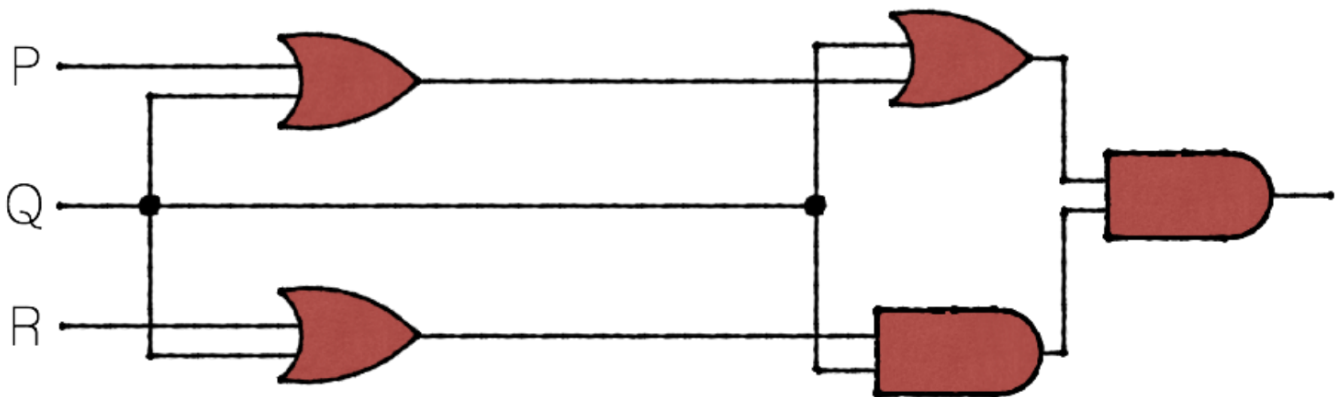
The variables  $p$ ,  $q$ , and  $s$  have the following truth values:  $p = \text{True}$ ,  $q = \text{True}$ ,  $s = \text{False}$ . What's the truth value for the following boolean expressions:

$$p + \sim(q \cdot s)$$

The variables  $p$ ,  $q$ , and  $s$  have the following truth values:  $p = \text{True}$ ,  $q = \text{True}$ ,  $s = \text{False}$ . What's the truth value for the following boolean expressions:

$$\sim(q \cdot p \cdot \sim s)$$

Find the output (boolean expression) for the circuit below (without simplifying):




How many two-input AND gates are required to realize:

$$Y = C \cdot D + E \cdot F + G$$

How many two-input AND gates and two-input OR gates are required to realize:

$$Y = B \cdot D + C \cdot E + A \cdot B$$

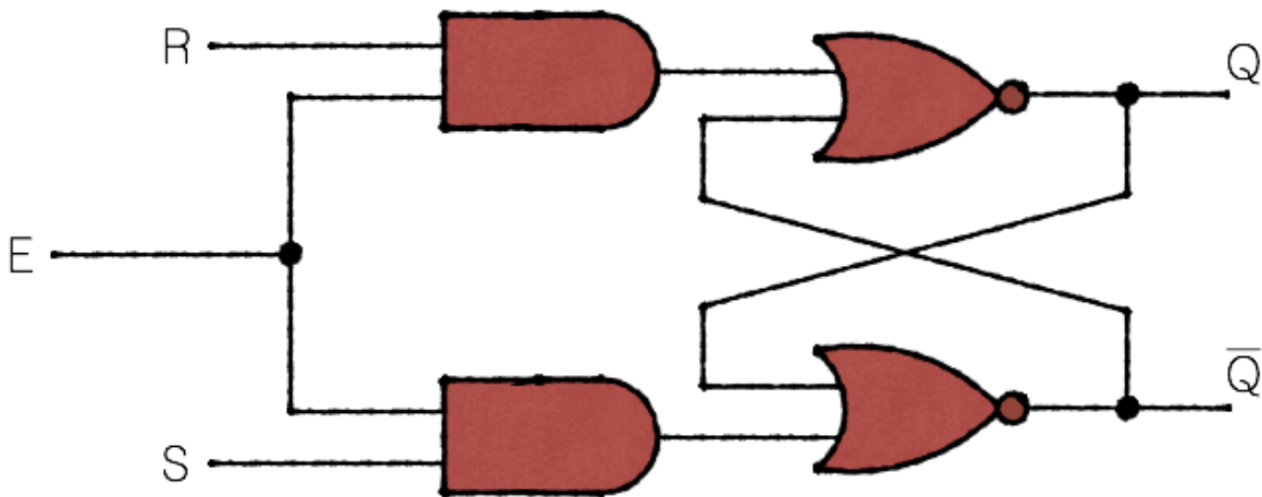
# Assignment 4 (Combinational & Sequential Logic)

Find the boolean expression that describes '?' (without simplifying)

p	q	s	?
0	0	0	0
0	1	1	0
0	1	0	1
0	0	1	1
1	0	0	1
1	1	1	1
1	1	0	0
1	0	1	0

$\sim p.q.\sim s + \sim p.\sim q.s + p.\sim q.\sim s + p.q.s$

The diagram below is called a 'Gated SR Latch' circuit, built from 'NOR's and 'AND's. Provide the Q value for the 1st, 2nd, 3rd, and 4th state.



State	R	E	S	Q
1st State	1	1	0	?
2nd State	0	1	0	?
3rd State	0	1	1	?
4th State	1	1	0	?

1st State = 0, 2nd State = 0, 3rd State = 1, 4th State = 0