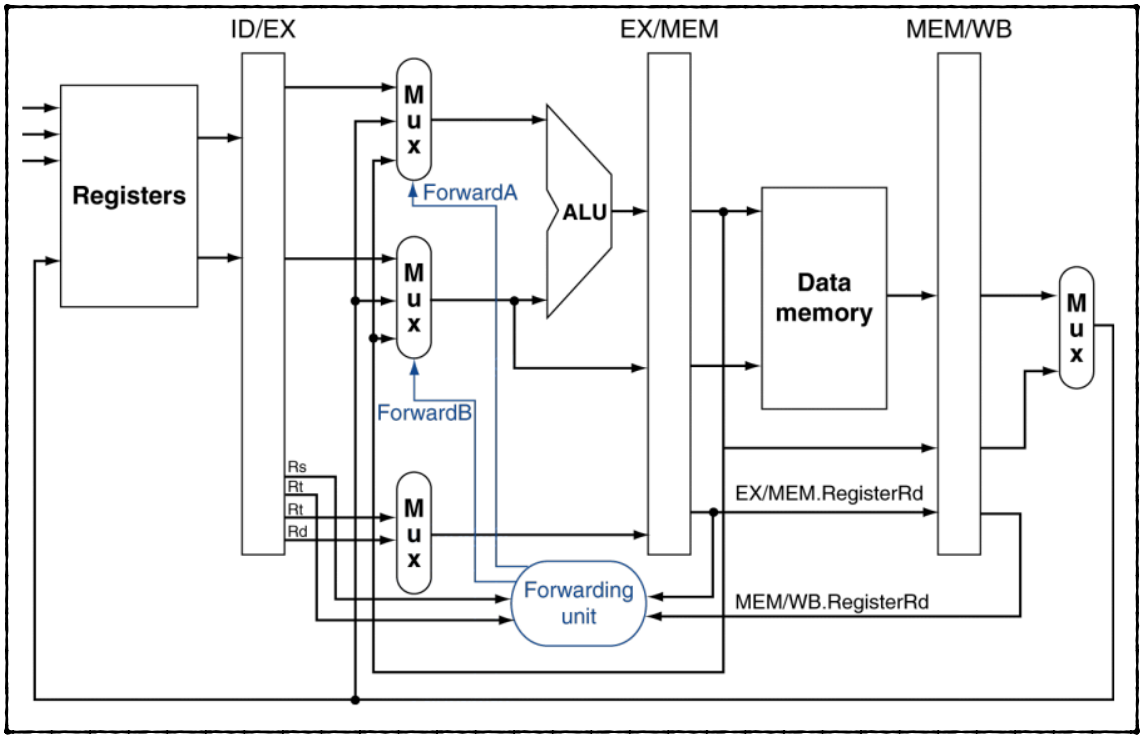

Q1) Fill the table below:

Rs	Rt	EX/MEM.RegisterRd	MEM/WB RegisterRD	ForwardA	ForwardB
00001	00001	10011	00001	01	01
00010	00011	00111	00011	00	01
00001	00010	00011	00001	01	00
00010	00001	00011	00111	00	00
00010	00001	00010	00010	10	00
00010	00001	00010	00011	10	00
00111	00111	00111	00111	10	10
00110	00111	00111	00011	00	10
00110	00111	10001	00111	00	01

Q2) Without using any forwarding, which instruction(s) would have a data dependency problem (list all)

add $t0, $t1, $t2
sub $t4, $t0, $t3 This one
and $t5, $t0, $t6 & this one
or $t7, $t0, $t8
xor $t9, $t6, $t10

Q3) Reorder the following set of instructions to account for the branch delay slot. (insert a no-op only if you must)

add $t0, $t1, $s3
sub $s3, $t2, $t1
beq $t2, $s0, label
add $s0, $s3, $s3

Answer:

add $t0, $t1, $s3
beq $t2, $s0, label
sub $s3, $t2, $t1
add $s0, $s3, $s3

Q4) If we have an 8-stage pipeline, how many CPU cycles would it take to execute 1 instruction

8 cycles

Q5) If we have an 8-stage pipeline, how many CPU cycles would it take to execute 3 instructions

10 cycles