Design Rules Verification Report

Filename : D:\Sources\AnalogIO-CAN-HW\AnalogIO-CAN-

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=15mil) ((OnLayer('GND	0
Clearance Constraint (Gap=8mil)	0
Clearance Constraint (Gap=4mil) (All),(All)	0
Clearance Constraint (Gap=15mil)	0
Clearance Constraint (Gap=8mil)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved:	0
Width Constraint (Min=4mil) (Max=71497.938mil)	0
Power Plane Connect Rule(Relief Connect	0
Power Plane Connect Rule(Direct Connect	0
Minimum Annular Ring (Minimum=3mil) (All)	0
Hole Size Constraint (Min=7.874mil) (Max=248.031mil)	0
Hole To Hole Clearance (Gap=9.842mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mil) (All),(All)	0
Silk To Solder Mask (Clearance=4mil) (IsPad),(All)	0
Silk to Silk (Clearance=0mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (All)	0
Room U_Peripherals (Bounding Region = (2333.047mil,	0
Room U_PowerModule (Bounding Region = (1199.236mil,	0
Room U_CanTransceiver (Bounding Region = (947.063mil,	0
Room ARM4 (Bounding Region = (3490mil, 1530mil,	0
Room U_AnalogueIsolatedReceiver (Bounding Region =	0
Room U_CPU (Bounding Region = (2633.5mil, 1508.5mil,	0
Room ARM1 (Bounding Region = (3490mil, 3570mil,	0
Room ARM2 (Bounding Region = (3490mil, 2890mil,	0
Room ARM3 (Bounding Region = (3490mil, 2210mil,	0
Height Constraint (Min=0mil) (Max=71497.938mil)	0
Total	0