Design Rules Verification Report

Filename : D:\Sources\CANOPEN_CURRENT_MODULE\trunk\HW\Altium_prj\CAN_Curr

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=15mil) (OnLayer('GND Plane')),(All)	0
Clearance Constraint (Gap=15mil) (InNamedPolygon('GND_L04_P047')),(InNet('VCC_5') Or InNet('VCC_3V3') Or	0
Clearance Constraint (Gap=15mil) (InNamedPolygon('GND_L01_P045')),(InNet('VCC_5') Or InNet('VCC_3V3') Or	0
Clearance Constraint (Gap=15mil) (OnLayer('VCC Plane')),(All)	0
Clearance Constraint (Gap=7mil) (InNamedPolygon('GND_L01_P045')Or InNamedPolygon('GND_CAN_L01_P044') Or	0
Clearance Constraint (Gap=4mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=4mil) (Max=71497.938mil) (Preferred=4mil) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Power Plane Connect Rule(Direct Connect)(Expansion=11.811mil) (Conductor Width=4mil) (Air Gap=4mil) (Entries=4)	0
Minimum Annular Ring (Minimum=3mil) (All)	0
Hole Size Constraint (Min=7.874mil) (Max=248.031mil) (All)	0
Hole To Hole Clearance (Gap=9.842mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mil) (All),(All)	0
Silk To Solder Mask (Clearance=4mil) (IsPad),(All)	0
Silk to Silk (Clearance=0mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (All)	0
Room ARM1 (Bounding Region = (4216mil, 4146mil, 6080.405mil, 4975mil) (InComponentClass('ARM1'))	0
Room ARM4 (Bounding Region = (4216mil, 1659mil, 6080.405mil, 2488mil) (InComponentClass('ARM4'))	0
Room ARM2 (Bounding Region = (4216mil, 3317mil, 6080.405mil, 4146mil) (InComponentClass('ARM2'))	0
Room ARM3 (Bounding Region = (4216mil, 2488mil, 6080.405mil, 3317mil) (InComponentClass('ARM3'))	0
Height Constraint (Min=0mil) (Max=71497.938mil) (Prefered=500mil) (All)	0
Total	0