

Simple Capacitor Voltage Balancing for Three-Level NPC Inverter Using Discontinuous PWM Method With Hysteresis Neutral-Point Error Band

Ibrahim Mohd Alsofyani , *Member, IEEE*, and Kyo-Beum Lee , *Senior Member, IEEE*

Abstract—Three-level neutral-point-clamped (3L-NPC) voltage source inverters are widely used in many low- and medium-power applications. However, the 3L-NPC inverter has an inheritance issue of the neutral-point (NP) voltage unbalancing due to the deviation of dc-link capacitor voltages causing distortions for the output waveform quality. Generally, discontinuous pulselwidth modulation (DPWM) is used to diminish the stress on power transistors and prolong their lifespan, however; it is not capable of solving the issue of NP voltage unbalancing. Therefore, this article proposes a simple voltage balancing control based on DPWM with a hysteresis NP voltage band. The balancing control method is only activated once the capacitance voltage error exceeds the hysteresis band by generating a momentary offset on the opposite direction of the DPWM offset. In this way, both top and bottom capacitance voltages will converge within a predefined error band. Various hysteresis error bands are investigated by analyzing the power losses, total harmonic distortions, and common mode voltage. The advantages of this proposed method are its simplicity and ease of control while maintaining the features of DPWM. The effectiveness of the proposed method is validated using simulation and experimental results.

Index Terms—Discontinuous pulselwidth modulation (DPWM), hysteresis neutral-point (NP) error band, NP voltage balancing, three-level NP clamped inverter (3L-NPC).

I. INTRODUCTION

THE three-level neutral-point-clamped (3L-NPC) inverters has advantages of higher efficiency, less total harmonic distortion (THD), and less switching stress across switching devices. Therefore, the 3L-NPC inverters have received an increasing demand for many industrial applications, such as electrical tractions systems, photovoltaic systems, and wind turbines [1]–[5]. Nevertheless, the critical issue with the 3L-NPC inverters is the voltage deviations of the neutral-point (NP)

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Ibrahim Mohd Alsofyani is with the Department of Electrical and Computer Engineering, Ajou University, Suwon 16499, South Korea (e-mail: alsofyani2002@yahoo.com).

Kyo-Beum Lee is with the Department of Electrical and Computer Engineering, Ajou University, Suwon 16499, South Korea (e-mail: kyl@ajou.ac.kr).

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voltage owing to the spilt dc-link voltage. This results in the deterioration of output currents and large stress on switching devices. For this reason, many researchers have attempted to address this problem by modifications on various modulation methods [1].

In recent years, several modulation approaches for the 3L-NPC inverters have been introduced, which can be categorized into continuous pulselwidth modulation (CPWM) methods and discontinuous PWM methods. The CPWM includes two main methods: sinusoidal PWM [6]–[12] and space-vector PWM (SVPWM) [13]–[17]. Although CPWM is capable of improving the system output waveform, there exist capacitance voltage oscillations, which become highly critical at high modulation index (MI) with low power factor (PF) loads [11]. Several methods in the literature were proposed to mitigate the NP voltage oscillations in CPWM. For example, in [16], virtual voltage vectors by adjusting the dwell time were introduced to control the NP current. Nevertheless, this method increases the complexity and cannot guarantee the NP voltage balance. Alternatively, Pou *et al.* [17] proposed a carrier based PWM to simplify [16] and to remove the NP voltage deviation with reduced complexity. Generally, the previous proposed balancing methods for CPWM method have caused higher switching transitions and reduced efficiency.

Compared to CPWM, DPWM is an attractive modulation scheme, which can be applied in power conversion systems to improve the efficiency with no change in the hardware or the topology [18]–[28]. Additionally, the DPWM is capable of minimizing the switching losses of the power transistors at an average of 33.3% and offers better harmonic attributes at high MI when compared to the CPWM strategies [27]. The 60° DPWM method is the most used and extensively studied in the literature. In general, the switch is clamped around the peak of the phase current to minimize the switching losses. In the 60° DPWM method, the switching operation is suspended at the positive or negative dc-bus for 60° of the fundamental period. However, the conventional 60° DPWM suffers from NP voltage fluctuations and large capacitance voltage deviations. The problem of capacitance voltage unbalance can be attributed to the flow of nonzero NP current and the inconsistency in capacitance voltage slopes. Several studies have focused on the NP balancing by modifying the DPWM scheme. In [29], a discontinuous modulation strategy based on varying clamping modes to reduce the NP voltage was proposed. Nevertheless, this method considers only a single PF

angle and requires complex implementation and higher computation burden because it deals with angles and trigonometric functions. Moreover, this method can cause the discontinuous pulselwidth overlapped with the other phases resulting in unsafe operation if the offset voltage is not correctly designed for all operating conditions. The modified DPWM technique studied in [30] minimized the NP voltage oscillations by applying two opposing zero offsets depending on current positions and MI; however, it causes additional switching losses. Another DPWM method was provided in [31], in which the clamping mode changes according the load PF. Yet, this method is effective at lower MI and has poor performance at higher MI. In [32], modified DPWM using special voltage sequence was introduced to reduce the switching loss while balancing the NP voltages. Although good performance was achieved, this method increases the balancing complexity owing to the inclusion of large lookup table for various operating conditions. In [33], DPWM was merged with CPWM to mitigate NP voltage deviation. However, this hybrid modulation requires additional proportional-integral controllers with proper gain design to smoothen the transition between the two modulation schemes. Moreover, additional switching losses will occur owing to the use of CPWM.

This article proposes a simple DPWM strategy using a hysteresis NP voltage error band for the capacitance voltage balancing of 3L-NPC inverter topologies by considering the capacitance voltage slopes. In this article, the NP voltage slopes can be easily controlled by the proposed offset voltage up to zero volt by switching alternatively between positive and negative clamping modes. When the capacitance voltage deviation converges to zero, it can negate most of the 60° clamping interval of DPWM. Nevertheless, it still can provide better efficiency than that of the CPWM method. Unlike the previous modified DPWM methods addressing the balancing issue, the proposed balancing algorithm offers another advantage by adjusting the amount of NP voltage slope using a hysteresis NP voltage error band depending on the application demand to ensure a capacitance voltage balance while maintaining good output waveform quality. Hence, most portion of the 60° clamping period can be maintained whereas the remaining portion will alternatively switch clamping between the positive and negative modes when the capacitance deviation exceeds a predefined hysteresis error band. The proposed control method is advantageous in terms of simplicity, flexibility, ease of control, while it can retain the 60° DPWM characteristics. The proposed NP voltage balancing method is verified by simulation and experimental results.

II. FUNDMENTALS OF 3L-NPC INVERTER

Fig. 1 depicts the 3L-NPC inverter topology. In this topology, the switching-state vectors of a 3L-NPC inverter are shown in Fig. 2. There are 27 combinations of switching states that represent the connection of load terminals to the dc-link terminals. The voltage-switching states are represented by "P," "O," and "N" which indicate a connection to positive dc rail, neutral point, and negative dc rail, respectively. According to the magnitude of the voltage vector, the space voltage vectors can be classified

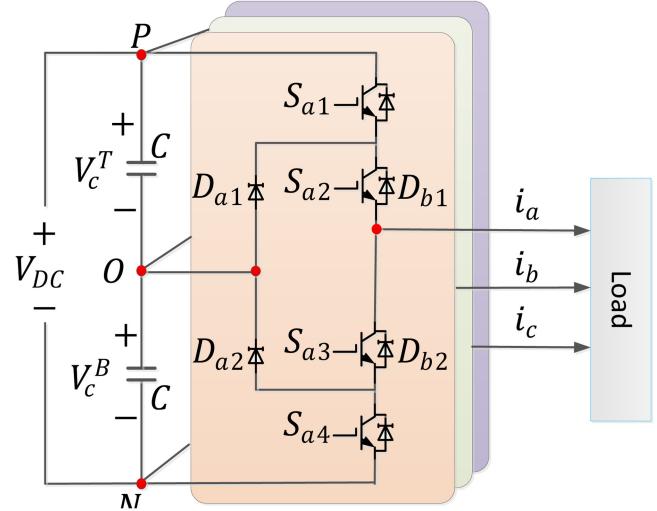


Fig. 1. Circuit diagram of three-level NPC inverter.

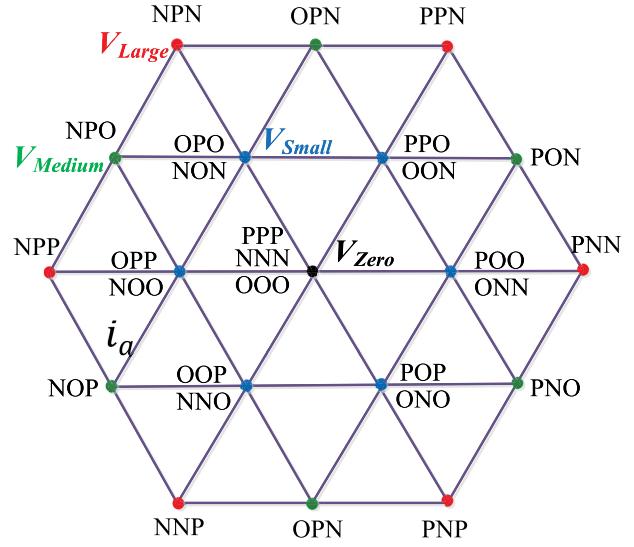


Fig. 2. Switching voltage vectors of a 3L-NPC inverter.

into four categories: large voltage (V_{Large}), medium voltage (V_{Medium}), small voltage (V_{Small}), and zero voltage (V_{Zero}).

The selection of these switching states has various influence on the NP balancing control of the 3L-NPC inverters. The large voltage vector type V_{Large} does not have connection with the NP O. Hence, it has no effect on the NP voltage. However, if the inverter needs a switching state with the medium voltage vector V_{Medium} or small voltage vector V_{Small} , the inverter becomes linked with the NP O, and hence the NP voltage will deviate in accordance of the direction of phase current connected to the NP. Therefore, in the operation of voltage vectors, the NP voltage fluctuates depending on the switching state, while the 3L-inverter is in regular operating mode. On the other hand, when the zero voltage V_{Zero} is applied, the three switches are clamped with O-state, and hence, the NP voltage is not affected.

III. CONVENTIONAL DISCONTINUOUS MODULATION METHOD FOR 3L-NPC INVERTER

Compared to CPWM method, the DPWM strategy has higher capability of diminishing the stress on transistors and minimizing power loss. In addition, the DPWM system efficiency resulting in the increase of the lifespan and the reliability with reduced cost. In the discontinuous modulation, each phase leg of the inverter is clamped to the negative or positive rail voltage for an amount of time. If a large offset voltage is injected, the resultant DPWM signal waveforms can be overlapped with each other, which causes distortions in the phase current. Although there are several different DPWM methods, the conventional 60° DPWM is the most commonly used for the systems with the unity PF. Thus, the three-phase reference voltage signals V_{xs}^* ($x = a, b$, and c) are expressed as

$$\begin{cases} V_{as}^* = V_{mg} \cdot \cos(\omega t) \\ V_{bs}^* = V_{mg} \cdot \cos(\omega t - 2\pi/3) \\ V_{cs}^* = V_{mg} \cdot \cos(\omega t + 2\pi/3) \end{cases} \quad (1)$$

where V_{mg} is the magnitude of the reference voltage, and ω is the angular frequency. Therefore, the conventional 60° DPWM reference voltages (i.e. $V_{a,DPWM}^*$, $V_{b,DPWM}^*$, $V_{c,DPWM}^*$) are obtained by adding a modified zero-sequence component, usually referred to as an offset voltage ($V_{z,DPWM}$) into the phase voltage

$$\begin{cases} V_{a,DPWM}^* = V_{as}^* + V_{z,DPWM} \\ V_{b,DPWM}^* = V_{bs}^* + V_{z,DPWM} \\ V_{c,DPWM}^* = V_{cs}^* + V_{z,DPWM}. \end{cases} \quad (2)$$

The $V_{z,DPWM}$ can be obtained using the maximum (V_{max}) and the minimum (V_{min}) values of the phase voltage references as

$$V_{z,DPWM} = \begin{cases} 0.5 \cdot V_{DC} - V_{max}, & (V_{max} + V_{min} \geq 0) \\ -0.5 \cdot V_{DC} - V_{min}, & (V_{max} + V_{min} < 0) \end{cases} \quad (3)$$

where $V_{max} = \max(V_{as}^*, V_{bs}^*, V_{cs}^*)$ and $V_{min} = \min(V_{as}^*, V_{bs}^*, V_{cs}^*)$.

Figs. 3(a) and (b) shows the phase references with the corresponding zero—sequence components (referred to as an offset) for SVPWM [14] and DPWM methods, respectively. Obviously, the reference voltage using DPWM in Fig. 3(b) is clamped to either positive dc rail or negative dc rail voltage. Within these clamping periods, the corresponding transistors are not used, and the switching power loss is reduced.

Fig. 4 depicts the deviation of dc-link capacitor voltage in the 3L-NPC when the conventional DPWM is applied. It is worth mentioning that when the switch of either phase is locked in *P*-state, the top dc-link capacitor voltage V_c^T is decreased and bottom dc-link capacitor voltage V_c^B is increased. Conversely, if the switch of the same phase is locked in the *N*-state, top and bottom dc-link capacitor voltages are increased and decreased, respectively. These two conditions are illustrated in Fig. 4. To simplify our analysis, several assumptions are made in the illustration.

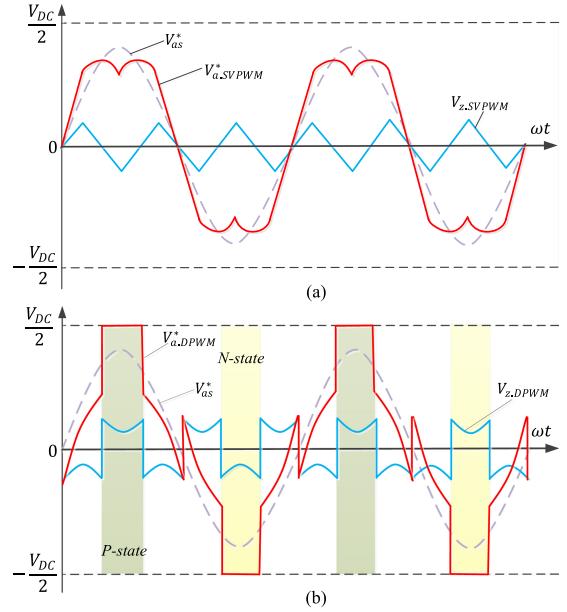


Fig. 3. Reference voltage, offset voltage, and pole reference voltages of the (a) space-vector PWM and (b) 60° discontinuous pulsewidth modulation.

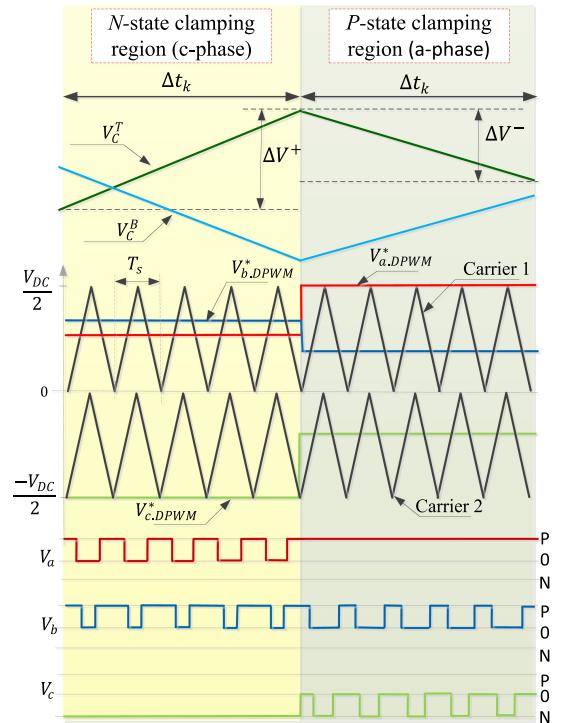


Fig. 4. Behavior of top and bottom capacitance voltages with respect to conventional DPWM.

- 1) The number of carrier cycles are five for each clamping region, which are far less than the actual cycle number.
- 2) The nonclamped voltage references are made instantaneous.
- 3) The top and bottom capacitor voltage slopes are symmetrical.

Hence, if the top capacitance voltage is considered, differential of dc-link capacitor voltage in tiny term can be expressed as

$$\begin{cases} \Delta V^+ = \Delta t_k \cdot I_{NP.N} \cdot \frac{1}{C} \\ \Delta V^- = \Delta t_k \cdot I_{NP.P} \cdot \frac{1}{C} \end{cases} \quad (4)$$

where ΔV^+ and ΔV^- are the positive and negative capacitor voltage slopes, respectively. C is capacitance of dc-link capacitors. I_{NP} is the NP current and the subscripts P and N represent the phase is connected to the positive and negative terminals of the dc-link, respectively. Δt_k is the time duration for the clamping interval. Let the system is sampled at every switching period, with $T_s(k) := T_s(k)$, $k \geq 1$, denoting the k th switching cycle. Then, the clamping interval can be represented as

$$\Delta t_k = \sum_1^k T_s(k). \quad (5)$$

From (4), there are three variables, which can affect the capacitance voltage slopes and contribute to the large deviation of dc-link voltage.

- 1) The nonswitching interval Δt_k , which is dependent on the DPWM type. Thus, the longer the clamping time is, the larger the capacitance voltage slope becomes. Nevertheless, it is 60° in the conventional DPWM used for this article. Notably, both positive and negative clamping states have the same clamping interval Δt_k .
- 2) The size of the dc-link capacitance. Small size of capacitance contributes to larger dc-link voltage slopes, whereas bigger dc-link capacitance causes reduction in the slope of the dc-link voltage.
- 3) The average neutral current unlike 1) and 2) is the most influential variable on the slopes of the top and bottom capacitance voltages. The I_{NP} is proportional to the MI; the higher the MI, the larger the quantity of I_{NP} . As mentioned previously, the I_{NP} is also related to these switching states. The voltage vectors without the O -state do not affect I_{NP} because the current does not flow through inner-side switches, which are connected to the neutral point. Nevertheless, the voltage vectors that contains the O -state affect I_{NP} since the current flows through the inner-side switches.

The calculation of I_{NP} mainly depends on duty ratios for output voltage as given by

$$\begin{cases} D_{\max} = 2 \times V_{DPWM,\max}^*/V_{DC} \\ D_{\text{mid}} = 2 \times V_{DPWM,\text{mid}}^*/V_{DC} \\ D_{\min} = 2 \times V_{DPWM,\min}^*/V_{DC} \end{cases} \quad (6)$$

where D_{\max} , D_{mid} , and D_{\min} are, respectively, the maximum, medium, and minimum values of the output voltages V_x ($x = a, b$, and c). $V_{DPWM,\max}^*$, $V_{DPWM,\text{mid}}^*$, and $V_{DPWM,\min}^*$ are respectively, the maximum, medium, and minimum DPWM reference voltages $V_{x,DPWM}^*$.

Generally, I_{NP} can be calculated as [30]

$$I_{NP} = -(D_{\max} \cdot I_{\max} + D_{\text{mid}} \cdot I_{\text{mid}} + D_{\min} \cdot I_{\min}) \quad (7)$$

where I_{\max} , I_{mid} , and I_{\min} are, respectively, the maximum, medium, and minimum values of output current. In the case of P -state clamping, D_{\max} is responsible for causing the corresponding output voltage to be connected with positive terminal of dc-link for Δt_k . Additionally, D_{\max} has the greatest effect on the I_{NP} than the other signals. By considering D_{\max} and neglecting D_{mid} and D_{\min} , the $I_{NP,P}$ can be calculated as

$$I_{NP,P} = -D_{\max,P} \cdot I_{\max,P}. \quad (8)$$

Similarly, for N -state clamping, D_{\min} causes the corresponding output voltage to be connected with negative rail of dc-link for the complete clamping interval. By considering the D_{\min} and neglecting D_{\max} and D_{mid} , the $I_{NP,N}$ can be expressed as

$$I_{NP,N} = -D_{\min,N} \cdot I_{\min,N}. \quad (9)$$

By substituting $I_{NP,P}$ and $I_{NP,N}$ into (4), the differential capacitor voltages can be expressed as

$$\begin{cases} \Delta V^+ = -\Delta t_k \cdot D_{\max,N} \cdot I_{\max,N} \cdot \frac{1}{C} \\ \Delta V^- = -\Delta t_k \cdot D_{\min,P} \cdot I_{\min,P} \cdot \frac{1}{C} . \end{cases} \quad (10)$$

In order to obtain a balanced capacitance voltage, the differential voltage slopes must be equal as given by

$$\Delta V^+ = \Delta V^- . \quad (11)$$

According to the previous discussion, the condition (11) cannot be guaranteed in the conventional DPWM as the 60° clamping interval Δt_k for both $D_{\max,N}$ and $D_{\min,P}$ is fixed. Additionally, the NP current will vary in every clamping region causing NP voltage fluctuations.

IV. PROPOSED DPWM WITH HYSTERESIS CAPACITOR VOLTAGE CONTROL FOR 3L-NPC INVERTER

Although there have been several studies reported on DPWM addressing the NP capacitance balancing, the goal of this article is to obtain a simple and adjustable balancing strategy without negating the characteristics of the conventional DPWM method.

In the proposed balancing strategy, the condition (11) is fulfilled by introducing a simple offset voltage triggered by a hysteresis capacitance-voltage band for controlling the slopes of the differential capacitance voltage. To attain minimum switching losses of the inverter, it is desirable to maintain proper clamping interval while balancing the capacitance voltage. Fig. 5 shows the proposed DPWM method using the hysteresis capacitance voltage error band (ΔHB_{cv}) for the 3L-NPC inverter. The concept of the proposed method is to control the NP voltage deviation by adjusting the differential of dc-link capacitor-voltage through the absolute of capacitor voltage difference CV_{err} as described by

$$|CV_{\text{err}}| = |V_c^T - V_c^B|. \quad (12)$$

In order to eliminate the deviation of the NP voltage, the offset voltage must be injected to the reference voltage when the slope of capacitance voltage exceeds the proposed hysteresis capacitance-voltage band ΔHB_{cv} . The NP voltage control

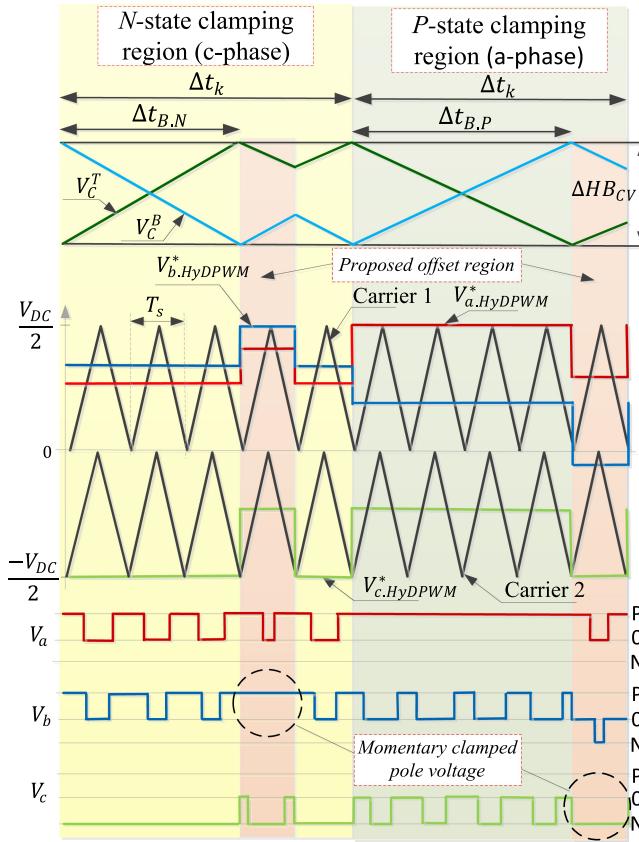


Fig. 5. Behavior of top and bottom capacitance voltages with respect to the proposed DPWM under hysteresis capacitance voltage error band.

method can curtail the capacitance voltage slopes by utilizing an opposite voltage offset ($V_{z2.DPWM}$) depending on the magnitude of top and bottom capacitor voltages as given by

$$V_{z2.DPWM} = \begin{cases} 0.5 \cdot V_{DC} - V_{DPWM,max}^*, & (V_c^T \geq V_c^B) \\ -(0.5 \cdot V_{DC} + V_{DPWM,min}^*), & (V_c^T < V_c^B). \end{cases} \quad (13)$$

This is to ensure that the resultant voltage references do not go beyond the maxima and minima of the dc-link capacitance voltage. $V_{z2.DPWM}$ has an opposite influence from $V_{z1.DPWM}$ on the slope direction of the NP voltage. Once $V_{z2.DPWM}$ is injected on the conventional DPWM voltage reference, the clamping modes will switch alternatively for almost every sampling interval T_s instead of Δt_k . This means one phase will be clamped whereas the other two phases are switching within very short period.

Nevertheless, application of the voltage offset $V_{z2.DPWM}$ throughout the system operation will diminish the 60°clamping period and affect other features of the DPWM method. For this reason, it is desirable to set a proper ΔHB_{cv} to stabilize the NP voltage and simultaneously maintain the good features of DPWM method.

Hence, a new offset voltage $V_{z3.DPWM}$ should be calculated considering the designed ΔHB_{cv} , which yields

$$V_{z3.DPWM} = \begin{cases} 0, & (|CV_{err}| < \Delta HB_{cv}) \\ V_{z2.DPWM}, & (|CV_{err}| \geq \Delta HB_{cv}). \end{cases} \quad (14)$$

After inclusion of new voltage offset $V_{z3.DPWM}$, the new reference signals $V_{x.HysDPWM}^*$ ($x = a, b, c$) can be defined as

$$\begin{cases} V_{a.HysDPWM}^* = V_{a.DPWM}^* + V_{z3.DPWM} \\ V_{b.HysDPWM}^* = V_{b.DPWM}^* + V_{z3.DPWM} \\ V_{c.HysDPWM}^* = V_{c.DPWM}^* + V_{z3.DPWM}. \end{cases} \quad (15)$$

According to (15), the new reference DPWM voltages $V_{x.HysDPWM}^*$ will operate like the conventional reference voltages $V_{x.DPWM}^*$ as long as the $|CV_{err}|$ is below the predefined ΔHB_{cv} for a time duration $\Delta t_{B,x}$ ($x = N, P$). Thus, the clamping interval Δt_k must be reduced by $\Delta t_{B,x}$ ($x = N, P$) according to the clamping region as illustrated in Fig. 5. Since the capacitance voltage slopes are different, the time intervals $\Delta t_{B,N}$ and $\Delta t_{B,P}$ are not similar, and hence, the $D_{max,P}$ and $D_{max,N}$ will vary according to the new clamping intervals. When the capacitance voltage error $|CV_{err}|$ exceeds the predefined hysteresis capacitance voltage band, $V_{z2.DPWM}$ will be activated and injected on the $V_{x.DPWM}^*$, in which the clamping of P -state and N -state will switch back and forth for the remaining Δt_k as depicted in Fig. 5. By considering the upper capacitance voltage during N -state clamping, the ΔHB_{cv} can be calculated as

$$\Delta HB_{cv} = \Delta t_{B,N} \cdot I_{NP.N} \cdot \frac{1}{C}. \quad (16)$$

Similarly, in the P -state clamping, the ΔHB_{cv} can be expressed as

$$\Delta HB_{cv} = \Delta t_{B,P} \cdot I_{NP.P} \cdot \frac{1}{C}. \quad (17)$$

As previously mentioned, the setting of hysteresis capacitance-voltage band ΔHB_{cv} is essential for ensuring a proper NP voltage control while maintaining a suitable nonswitching interval, so it should be adjusted to have optimal operation for 3L-inverter system. Because if the ΔHB_{cv} is set too small, this will result in a very high switching between the clamping of P -state and N -state causing the 60°clamping period of DPWM strategy totally diminished. On the other hand, if the ΔHB_{cv} is designed to be too large, the capacitance voltage deviation will still exist. Therefore, in this article, the selection of ΔHB_{cv} is empirically determined to compromise between a regulated capacitance voltage and a desirable DPWM performance.

V. SIMULATION RESULTS

Simulations using a PSIM software tool have been conducted to confirm the validity of the proposed method. The dc-link voltage V_{dc} is 250 V which is distributed evenly between top capacitance voltage V_c^T and bottom capacitance voltage V_c^B .

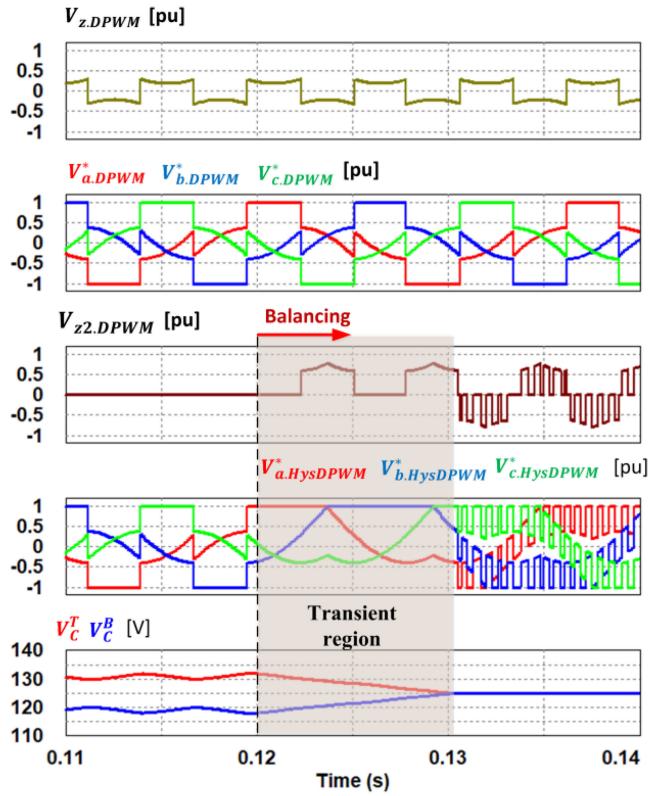


Fig. 6. Simulation waveforms of transient state performance from conventional DPWM to proposed DPWM without applying the hysteresis capacitance band.

The dc-link capacitance is $2200 \mu\text{F}$ and the switching frequency is 10 kHz .

Fig. 6 shows the simulation results of capacitor voltage balancing from the conventional DPWM to proposed DPWM with $\Delta HB_{cv} = 0 \text{ V}$ which means that there is no a hysteresis capacitance band. The proposed offset $V_{z2,DPWM}$ and modified reference DPWM voltages are also plotted at the same figure. To see the impact on the proposed reference DPWM, the behavior of conventional offset and conventional reference DPWM is also added for the comparison purpose as seen in Fig. 6. The balancing of capacitance voltages begins at 0.12 s . Before balancing starts, it can be observed that P -state clamping reduces V_c^T slope and increases V_c^B slope. On the other hand, that N -state clamping increases V_c^T slope and reduces V_c^B slope. Nevertheless, in both 60° clamping regions of the conventional DPWM, the capacitance voltages are not balanced. When the balancing begins, the proposed offset $V_{z2,DPWM}$ is activated. It can be obvious from the proposed reference voltages that the P -state clamping for two phases was maintained throughout the transient operation causing the top capacitor voltage continues to decrease and the bottom capacitor voltage to increase till the balancing range is reached. Notably, the $V_{z2,DPWM}$ depends on magnitudes of top and bottom capacitance voltage in addition to the maximum and minimum values of V_x^* ($x = a, b$, and c) according to (13). It can be observed that the proposed offset only alternates between zero and positive values during the transient state

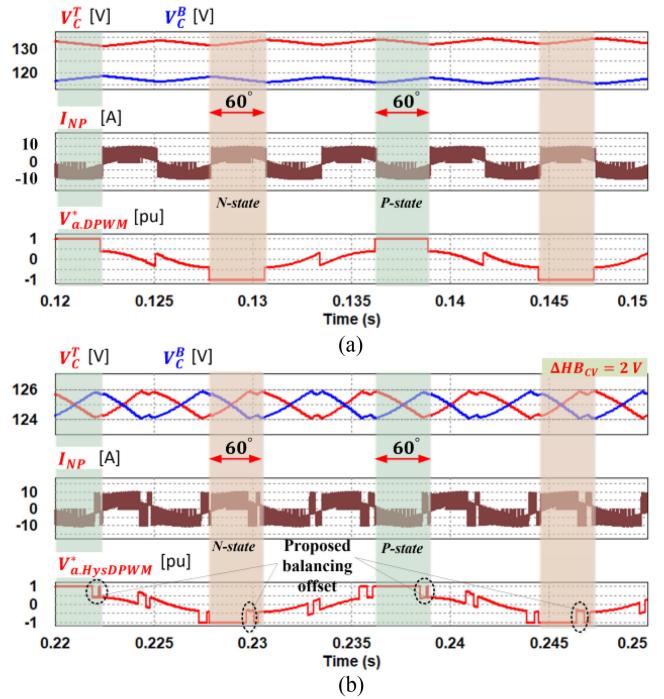


Fig. 7. Simulation waveforms of steady state performance for (a) conventional DPWM and (b) proposed DPWM ($\Delta HB_{cv} = 2 \text{ V}$).

operation because the top capacitance voltage is greater than bottom capacitance voltage. Nevertheless, the proposed offset starts to have positive and negative cycles throughout the steady state operation where there is an oscillation between the positive and negative capacitance voltages. Obviously, the new reference voltages start operation according to offset voltage $V_{z2,DPWM}$ resulting in the balance of capacitance. This is consistent with the analysis in Section IV.

Fig. 7(a) shows the simulation results of the steady state performance for the capacitance voltage deviation, NP current I_{NP} , and $V_{a,DPWM}^*$, when applying the conventional DPWM method. Although there is a large capacitance voltage deviation, it is obvious that the NP current I_{NP} changes according to the clamping region slope as shown in Fig. 7(a). By applying the proposed DPWM strategy with setting $\Delta HB_{cv} = 2 \text{ V}$, the proposed DPWM reference voltage $V_{a,HysDPWM}^*$ can control the V_c^T and V_c^B slopes within the defined hysteresis voltage band as shown in Fig. 7(b). It can be observed that once the capacitance voltage exceeds the defined band, the proposed $V_{a,HysDPWM}^*$ imposes momentarily an offset within each 60° clamping region on the opposite direction to change the direction of the NP current I_{NP} , and hence, force both V_c^T and V_c^B slopes to be converged within the defined band.

Figs. 8 and 9 illustrated the performance of proposed NP voltage balancing control under various hysteresis capacitance voltage bands ΔHB_{cv} when it is applied at 0.12 s . In Fig. 8, the load is $L = 6 \text{ mH}$, $R = 10 \Omega$ when MI is 0.8 with a PF of 0.98. In Fig. 9, the MI is 0.25 and the load is changed to $L = 6 \text{ mH}$, $R = 1 \Omega$, and hence, the PF is 0.404. It is clearly

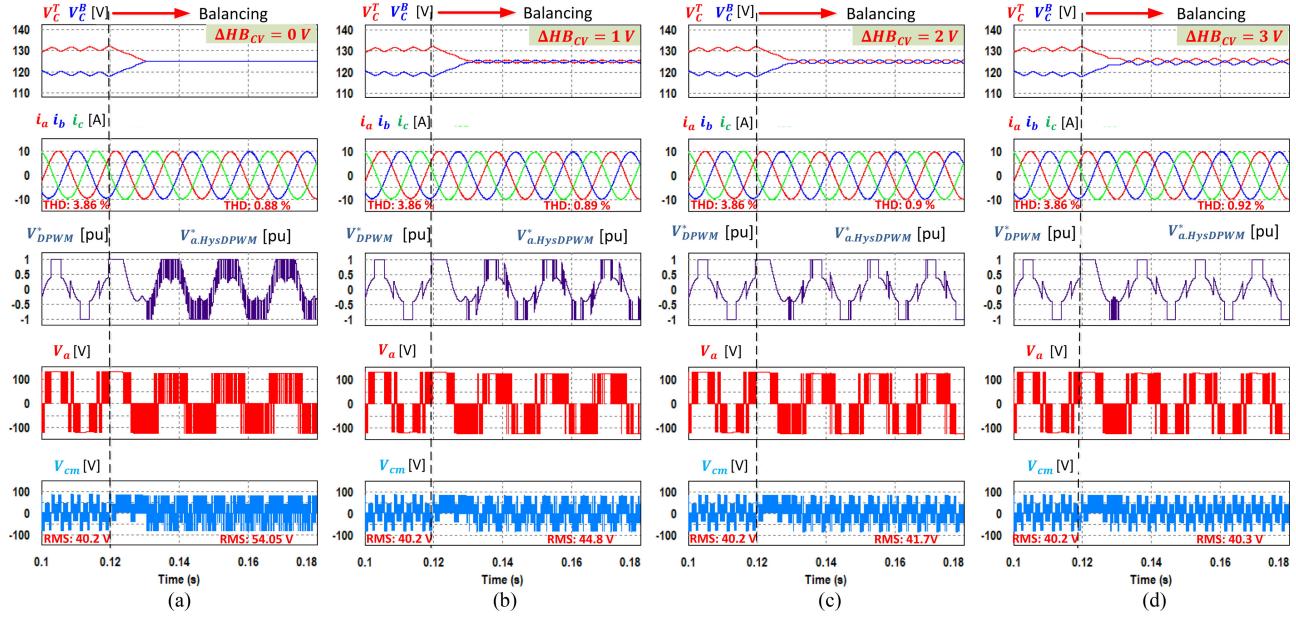


Fig. 8. Simulation results of the NP voltage balance control of the proposed DPWM method when MI is 0.8 at (a) $\Delta HB_{cv} = 0 \text{ V}$, (b) $\Delta HB_{cv} = 1 \text{ V}$, (c) $\Delta HB_{cv} = 2 \text{ V}$ and (d) $\Delta HB_{cv} = 3 \text{ V}$.

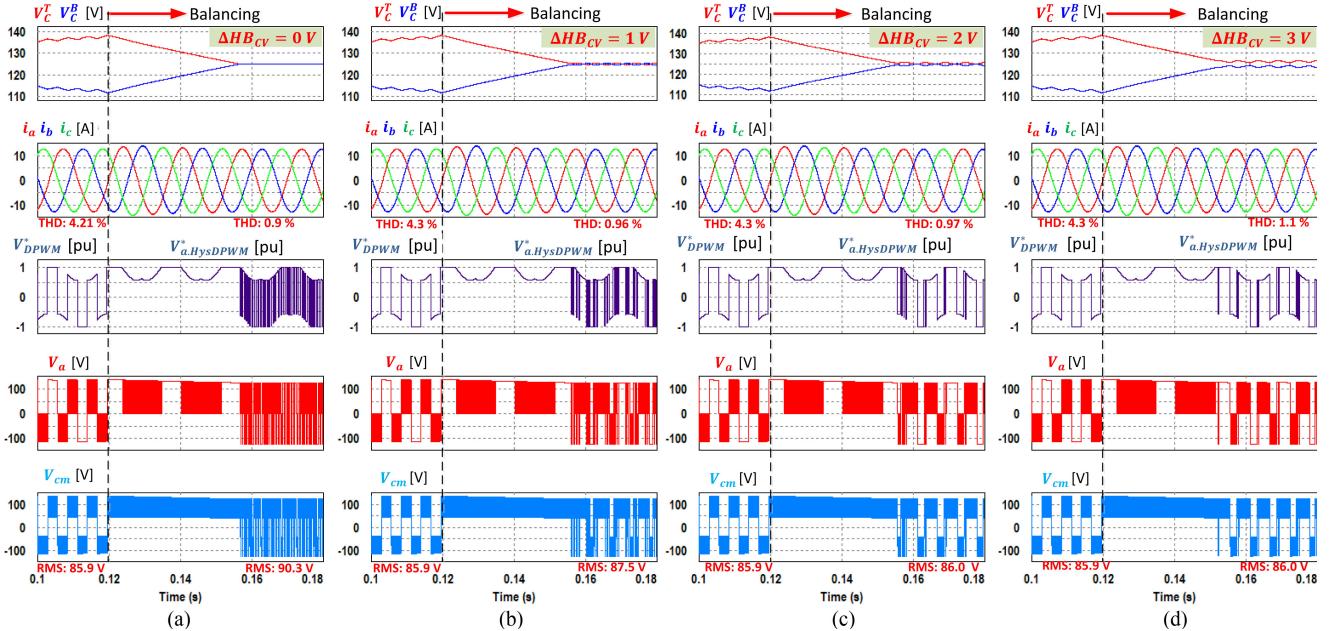


Fig. 9. Simulation results of the NP voltage balance control of the proposed DPWM method when MI is 0.25 at (a) $\Delta HB_{cv} = 0 \text{ V}$, (b) $\Delta HB_{cv} = 1 \text{ V}$, (c) $\Delta HB_{cv} = 2 \text{ V}$ and (d) $\Delta HB_{cv} = 3 \text{ V}$.

TABLE I

PARAMETERS OF SWITCH AND DIODE AT 125 °C

	Parameter	Value
Switch	E_{on}	3.6 mJ
	E_{off}	2.9 mJ
	V_{CE}	2.4 V
Diode	E_{rr}	2.0 mJ
	V_d	2.3 V

shown that, the conventional DPWM method suffers from large voltage deviation before the NP voltage control before 0.12 s under both RL loads, though it contains the nonswitching regions as indicated by the a-phase pole voltage (V_a). Notably, the NP deviation at low MI is higher owing to the small voltage vectors with O -state.

Nevertheless, after the proposed NP control algorithm is applied using the four hysteresis capacitance voltage bands (i.e. 0, 1, 2, and 3 V), both top and bottom capacitance voltages have been converged within the voltage band as indicated by

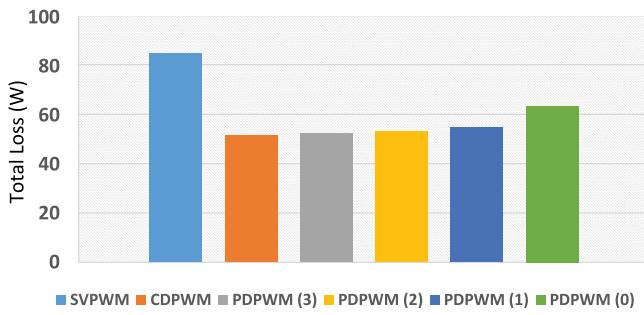


Fig. 10. Total loss comparison between the SVPWM, the conventional DPWM, and the proposed DPWM (under $\Delta HB_{cv} = 0, 1, 2$, and 3 V) with PF = 0.98 at junction temperature 125°C .

ΔHB_{cv} . According to each ΔHB_{cv} , the output of currents, a-phase reference voltage, a-phase pole voltage V_a , and common mode voltage (V_{cm}) will have different performances as shown and in Figs. 8 and 9, respectively. It is evident that the clamping region in a-phase reference voltage is consistent with the a-phase reference voltage for both MI cases, especially when $\Delta HB_{cv} \geq 1$. It can be observed from proposed DPWM under $\Delta HB_{cv} = 0$ shown in Figs. 8(a) and 9(a) that both capacitance voltages have almost zero voltage deviation and the current quality significantly improves by comparing the THD to that of the conventional DPWM. Nevertheless, the characteristics of DPWM, especially the 60° clamping region are totally lost as indicated by the a-phase pole voltage V_a . Consequently, this will increase the stress on transistors and lead to higher power loss as will be proven in the coming discussion. It is worth mentioning that in the case of zero-voltage band, the clamping only occurs for almost every sampling interval T_s , as previously discussed. Additionally, the rms value of common mode voltage V_{cm} for the proposed DPWM under $\Delta HB_{cv} = 0$ is increased for both MI values when compared to conventional DPWM method. Obviously, increasing the hysteresis capacitance voltage band ΔHB_{cv} to 1, 2, and 3 V can reduce the switching in the clamping regions in both MI as depicted by Figs. 8 and 9, while maintaining comparable current waveforms with that under $\Delta HB_{cv} = 0$. Moreover, the common mode voltage for the proposed DPWM with larger ΔHB_{cv} is not affected, especially when $\Delta HB_{cv} \geq 2$ V under both RL loads.

To show the efficiency effect of the proposed method under various hysteresis voltage bands, the total power losses (conduction loss and switching loss) are analyzed by PSIM simulation tool, and IGBT modeling is performed using LUH50G1204's features of LS industrial systems as given in Table I. The junction temperature is 125°C which has maximum limit of IGBT. The proposed DPWM (PDPWM) method under four hysteresis bands (i.e. 0, 1, 2, and 3 V) will be compared to the conventional DPWM (CDPWM) and SVPWM as shown in Fig. 10. For easy identification, PDPWM (0), PDPWM (1), PDPWM (2), and PDPWM (3) indicate the PDPWM under $\Delta HB_{cv} = 0, 1, 2$, and 3 V, respectively. It can be observed that power loss in PDPWM (0) is still smaller than that of the SVPWM because PDPWM (0) still contains non-switching phase for very short time intervals through the system operation. Nevertheless, the

remaining proposed DPWM methods under $\Delta HB_{cv} \geq 1$ V have almost comparable reduced total loss to that of conventional DPWM as the clamping intervals are larger than that under PDPWM (0). In addition, Fig. 11 shows the power losses caused by the CDPWM and the PDPWM according to hysteresis bands at different values of MI and PF. The PF is calculated as the phase difference between the current and the voltage caused by the variation of inductance while maintaining the resistance value ($10\ \Omega$). At higher PF, the switching losses are the highest for the PDPWM (0) at different MI. However, at very low PF, the total losses variation of the PDPWM at all hysteresis bands decreases compared to higher PF. Hence, they have almost the same switching losses at very low PF. Moreover, it can be seen that PDPWM (2), PDPWM (3) and CDPWM exhibit comparable switching losses under all operating condition.

Fig. 12 shows the common mode voltage comparison V_{cm} between the CDPWM and the PDPWM (under $\Delta HB_{cv} = 0, 1, 2$, and 3 V) at different operating conditions. It can be found that the rms value of V_{cm} increases with the reduction of the MI. Obviously, the PDPWM (0) causes the largest V_{cm} especially at MI = 6 and MI = 8. Additionally, the other proposed DPWM methods under $\Delta HB_{cv} \geq 1$ V for most operating conditions have approximately identical common mode voltage to that of conventional DPWM. As observed earlier in Fig. 9, the common mode voltage for all methods becomes slightly comparable at lower MI.

The NP voltage variation for the proposed DPWM (under $\Delta HB_{cv} = 0, 1, 2$, and 3 V) is also evaluated for various MIs and PFs as shown in Fig. 13. In this test, the averaged NP voltage oscillation V_{NP} was calculated with respect to half dc-link voltage as in [34]

$$\Delta V_{NP} (\%) = \left(\frac{|0.5 \cdot V_{DC} - V_c^T|}{0.5 \cdot V_{DC}} \right) \times 100. \quad (18)$$

As is evident, the proposed method PDPWM (0) reduces the NP voltage oscillation significantly (below 0.5%) compared to those with higher hysteresis capacitance voltage bands as shown in Fig. 13(a). It can be observed, with MI = 1, the performance of the PDPWM (0) slightly increases for lower PFs. However, as previously seen, PDPWM (0) causes the highest switching losses and highest common mode voltage. Obviously, the proposed DPWM under larger hysteresis bands can cause higher NP voltage oscillations, especially at lower PF. However, the NP oscillation for propped DPWM with hysteresis bands can be controlled within acceptable tolerance range (below 1.5%).

VI. EXPERIMENTAL RESULTS

The effectiveness of the proposed DPWM method is verified in experiment using a three-level NPC inverter as shown in Fig. 14. The inverter is controlled by using a TMS320F28335 digital-signal processor. The experimental parameters and operating conditions are the same as those in the simulation.

Figs. 15 and 16 show the NP balancing control using the proposed DPWM method at MI = 0.8 (PF = 0.98) and 0.25 (PF = 0.404), respectively. Obviously, the unbalance of the upper and lower dc capacitor voltages exists owing to the conventional

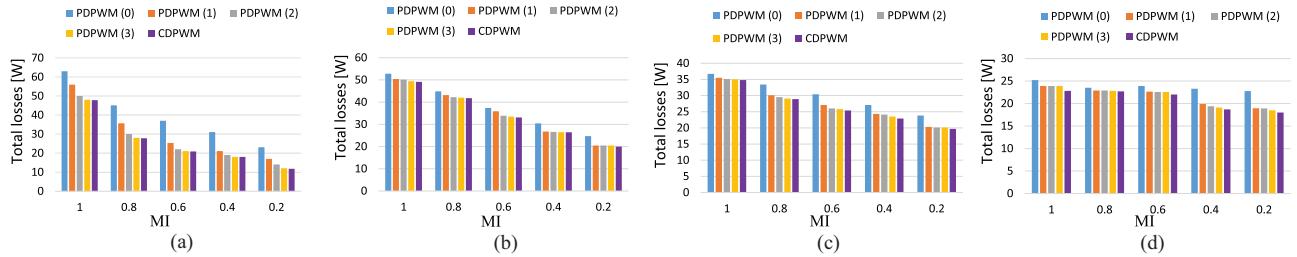


Fig. 11. Total power loss comparison between the conventional DPWM and proposed DPWM (under $\Delta HB_{cv} = 0, 1, 2$, and 3 V) for various MIs at (a) PF = 1, (b) PF = 0.75, (c) PF = 0.5, (d) PF = 0.25.

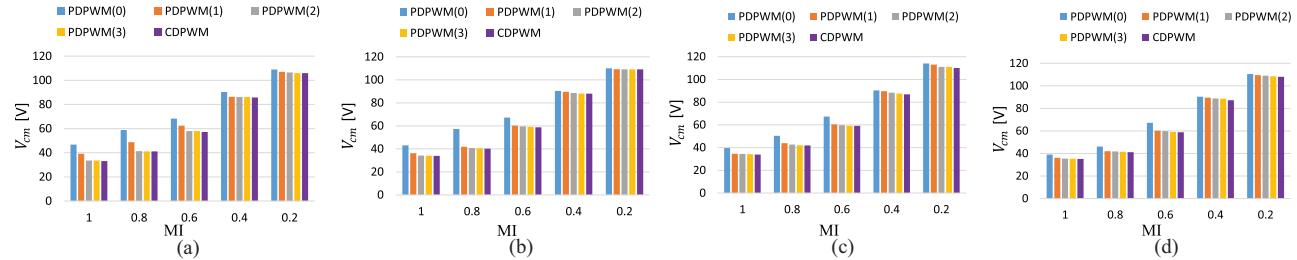


Fig. 12. Common mode voltage variation of the conventional DPWM and proposed DPWM (under $\Delta HB_{cv} = 0, 1, 2$, and 3 V) for various MIs at (a) PF = 1, (b) PF = 0.75, (c) PF = 0.5, (d) PF = 0.25.

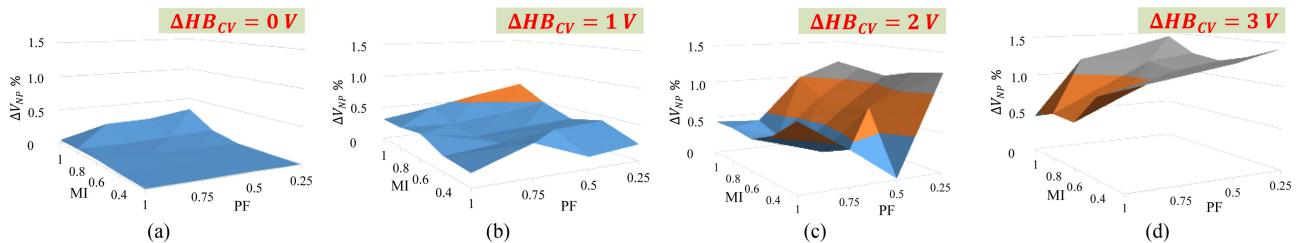


Fig. 13. NP voltage variation at different operating conditions for the proposed DPWM method at (a) $\Delta HB_{cv} = 0$ V, (b) $\Delta HB_{cv} = 1$ V, (c) $\Delta HB_{cv} = 2$ V and (d) $\Delta HB_{cv} = 3$ V.



Fig. 14. Experimental setup.

DPWM method. As mentioned previously, the amount of capacitance voltage deviation is higher at low MI because of the small voltage vectors containing O -states. Consequently, this results in high distortions of the current harmonic components of in both

MI levels. Moreover, the line-to-line voltage V_{ab} is distorted especially at low MI because of the dc voltage deviation during the conventional DPWM method.

However, after the proposed DPWM strategy with the four bands ($\Delta HB_{cv} = 0, 1, 2$, and 3 V) is applied, the reference voltage $V_{a,DPWM}^*$ of conventional DPWM method is modified to the reference voltage $V_{a,HysDPWM}^*$ of proposed DPWM method. It is clearly shown that the voltages of dc capacitors become balanced and the capacitance voltage error $|CV_{err}|$ greatly reduces, resulting in decreasing the THD level according to the hysteresis band defined by ΔHB_{cv} and improving the line-to-line voltage. For example, in the case of $\Delta HB_{cv} = 0$ V, the current THD changed from 5.35% to 1.02% for MI 0.8 and from 6.76% to 1.41% for 0.25 MI as shown in Figs. 15(a) and 16(a), respectively. It can be observed when increasing the hysteresis voltage bands ΔHB_{cv} to 1, 2, and 3 V for both MIs, the clamping region of proposed reference voltage $V_{a,HysDPWM}^*$ gradually becomes identical to the conventional reference voltage $V_{a,DPWM}^*$ with small distortions as shown in Figs. 15 (b)–(d) and 16 (b)–(d). Although, the capacitance

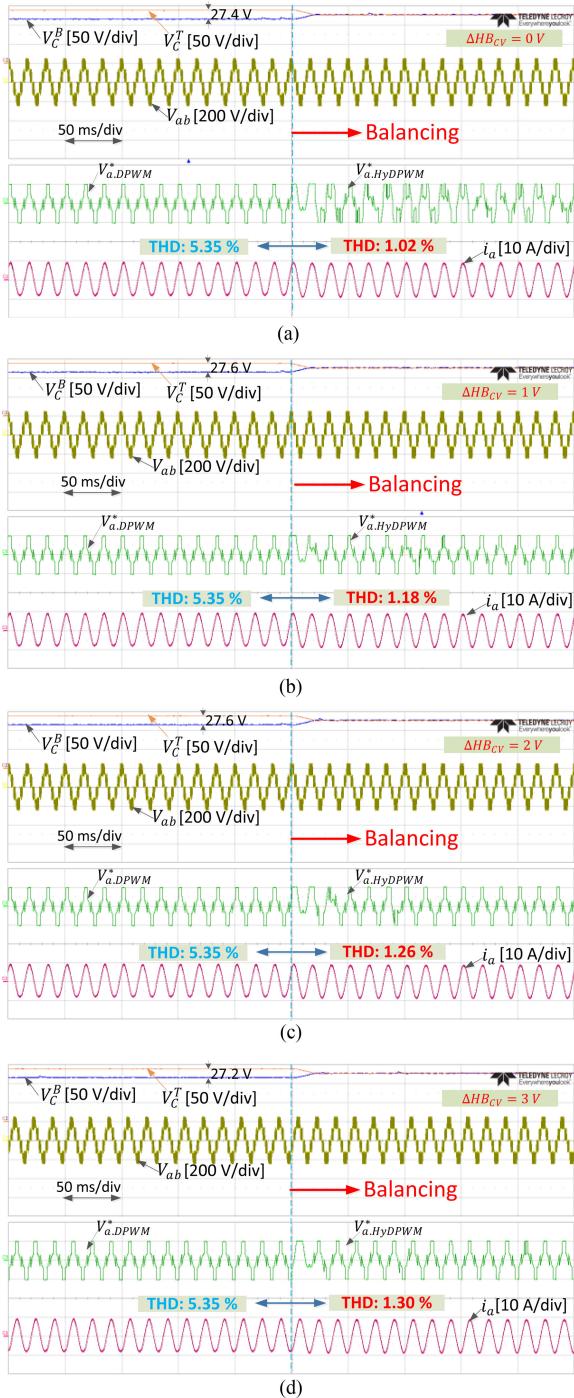


Fig. 15. Experimental results of capacitance voltage balancing for the proposed DPWM (under $\Delta HB_{cv} = 0, 1, 2$, and 3 V) when MI is 0.8.

voltage deviation increases for $\Delta HB_{cv} > 0$, the THD levels are still comparable to that of $\Delta HB_{cv} = 0$ for both MI cases.

Figs. 17 and 18 show the steady-state performances of the capacitor voltages, a-phase voltage V_a and current i_a , and line to line voltage V_{ab} for the proposed scheme under the four capacitance voltage error bands ($\Delta HB_{cv} = 0, 1, 2$, and 3 V) for both MI conditions. It can be seen that in both MI cases the

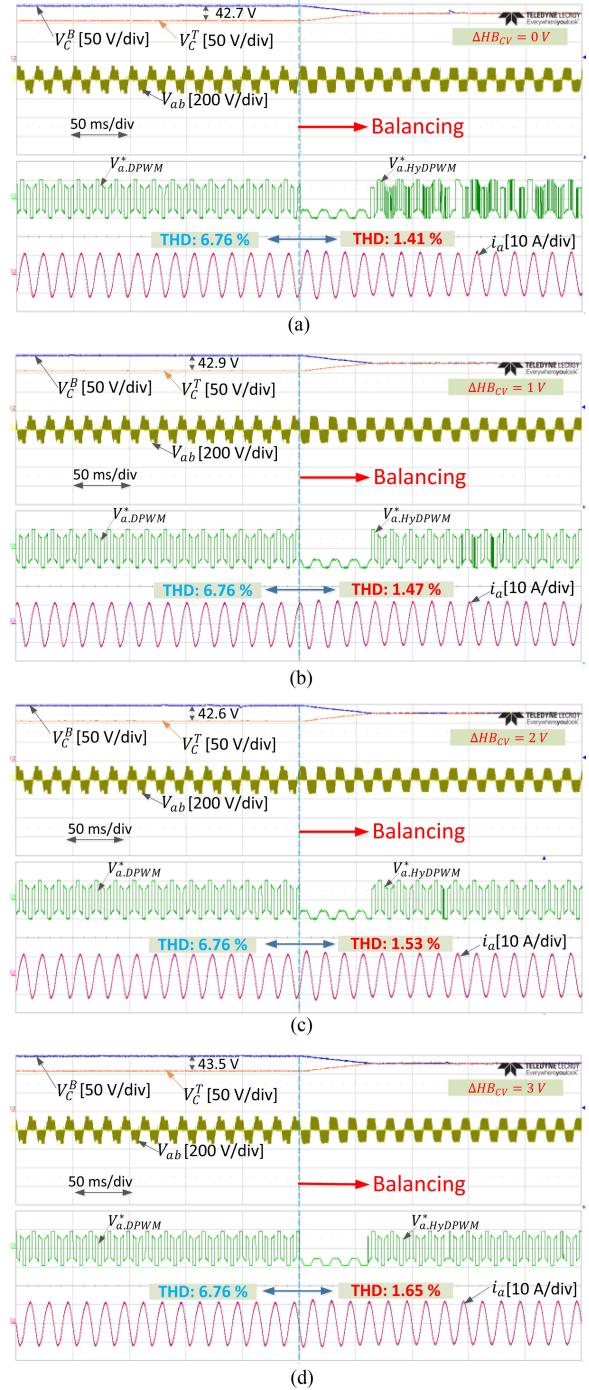


Fig. 16. Experimental results of capacitance voltage balancing for the proposed DPWM (under $\Delta HB_{cv} = 0, 1, 2$, and 3 V) when MI is 0.25.

NP capacitance voltage are well regulated under all capacitance voltage error bands. Nevertheless, the clamping region of the pole voltage V_a depends considerably on setting ΔHB_{cv} of the proposed DPWM. It can be observed from the proposed DPWM under $\Delta HB_{cv} = 0$ shown in Figs. 17(a) and 18(a) that the clamping regions of pole voltage V_a is not consistent and has the highest switching compared to those with $\Delta HB_{cv} > 0$. This confirms the previous analysis that the switching losses increase at $\Delta HB_{cv} = 0 \text{ V}$. Although the pole voltages when

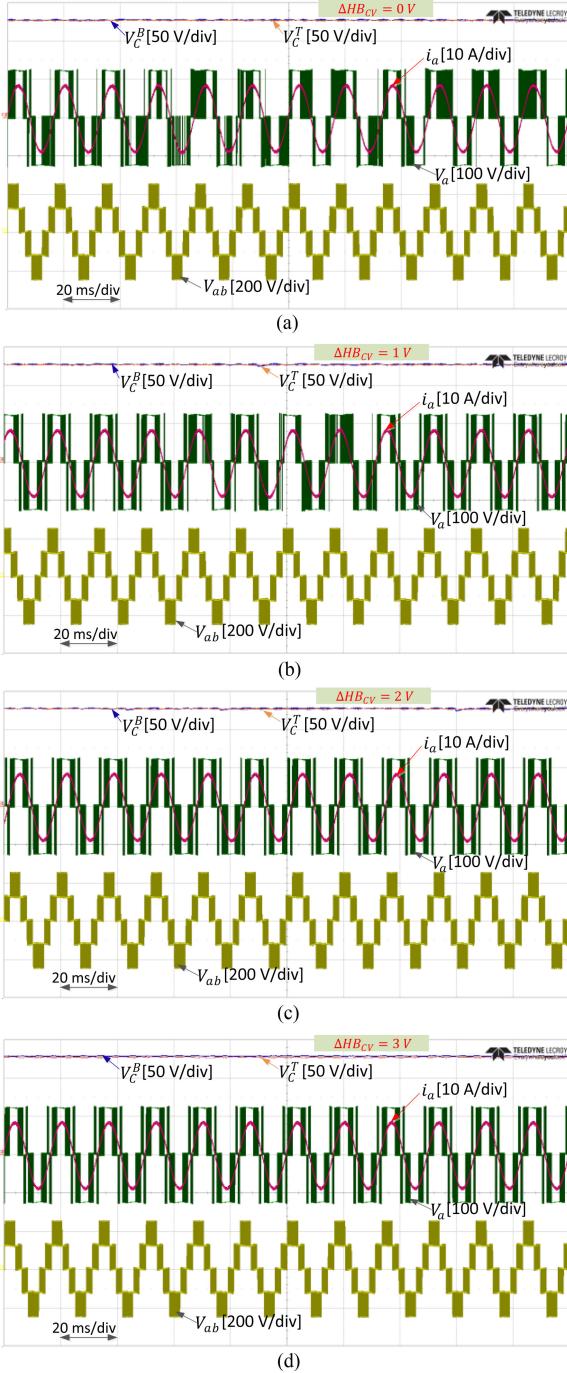


Fig. 17. Experimental results at steady state of balanced capacitance voltage using proposed DPWM (under $\Delta HB_{cv} = 0, 1, 2$, and 3 V) when MI is 0.8.

$\Delta HB_{cv} = 2$ and 3 V in both MI cases have slightly higher capacitance voltage deviation, they offer consistent and stable clamping region while maintaining good current quality as depicted in Fig. 17 (c) and (d) and Fig. 18 (c) and (d).

Fig. 19 illustrates the current THD comparison for the proposed DPWM method under four ΔHB_{cv} values: 0, 1, 2, and 3 V for various MI values when $PF \approx 1$. It is obvious that the THD level is the smallest when $\Delta HB_{cv} = 0\text{ V}$, at MI = 0.1.

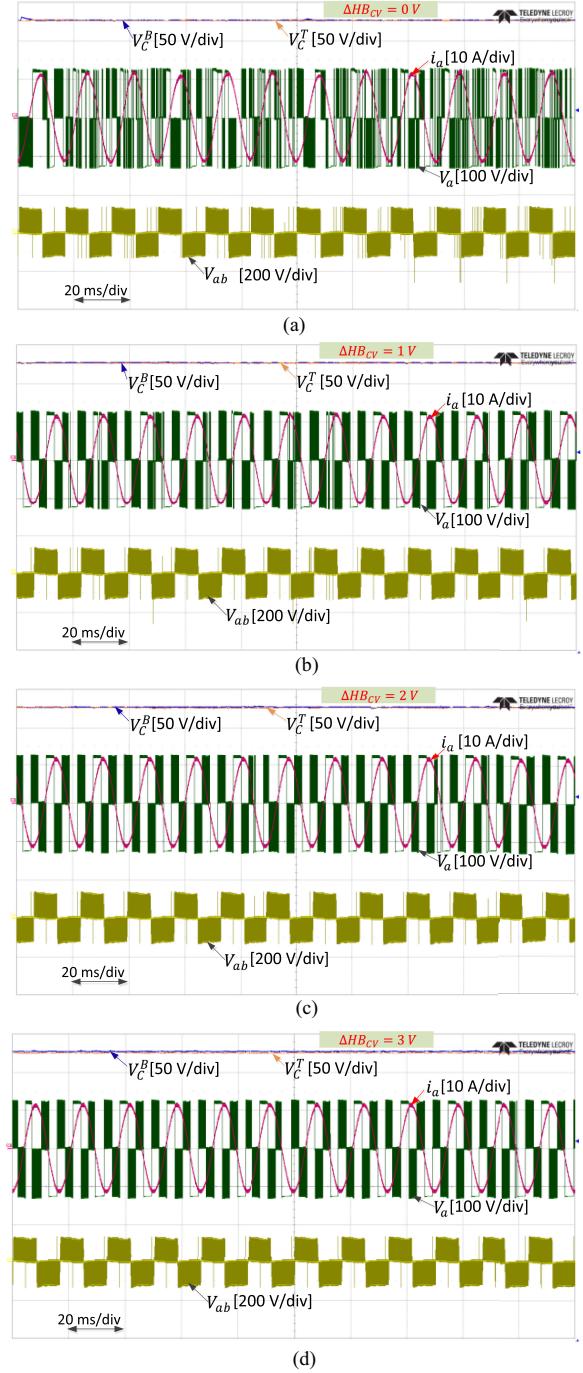


Fig. 18. Experimental results at steady state of balanced capacitance voltage using proposed DPWM (under $\Delta HB_{cv} = 0, 1, 2$, and 3 V) when MI is 0.25.

Nevertheless, at higher MI than 0.1, the current THD decreases with almost comparable levels for all ΔHB_{cv} values.

The experimental results of common mode voltage V_{cm} for high and low MI conditions are shown in Figs. 20 and 21, respectively. The common mode voltage V_{cm} under the proposed DPWM of $\Delta HB_{cv} = 0$ is highly affected with the largest rms value in the high MI case as shown in Fig. 20(a). It can be noticed that the common mode voltages when $\Delta HB_{cv} = 2$ and 3 V in high MI condition have almost 25% reduction compared to

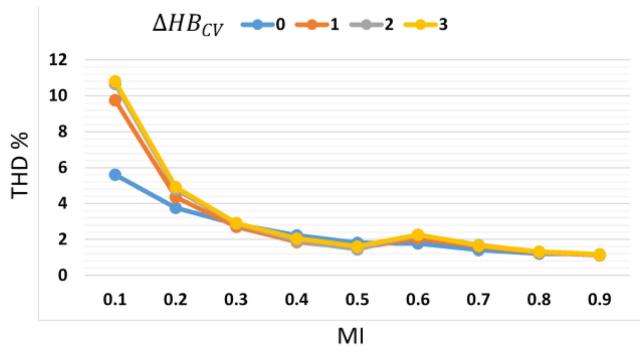


Fig. 19. Current THD comparisons between the proposed DPWM (under $\Delta HB_{cv} = 0, 1, 2$, and 3 V) at different MI with $\text{PF} \approx 1$.

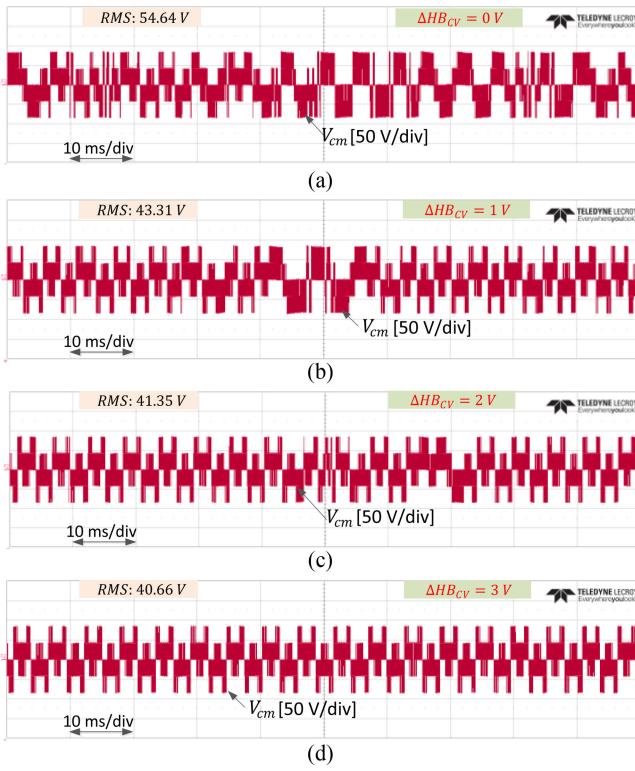


Fig. 20. Common mode voltage of proposed DPWM (under $\Delta HB_{cv} = 0, 1, 2$, and 3 V) when MI is 0.8.

that under $\Delta HB_{cv} = 0\text{ V}$ as depicted in Figs. 20(c) and (d). Nevertheless, the V_{cm} results at the low MI are approximately comparable under all capacitance voltage error bands as shown in Fig. 21.

Finally, Fig. 22 shows the measured efficiency comparison between the CPWM, the CDPWM, and the proposed method under various hysteresis voltage bands using Yokogawa WT3000 power analyzer. It is clearly observed that the CDPWM illustrates the highest efficiency, whereas CPWM has the lowest efficiency for all the MI values. It can be seen from the graph, all the proposed DPWM methods including PDPWM (0) have higher efficiency than the CPWM. Additionally, the efficiency of the proposed DPWM with $\Delta HB_{cv} = 3\text{ V}$ become comparable to that of the CDPWM.

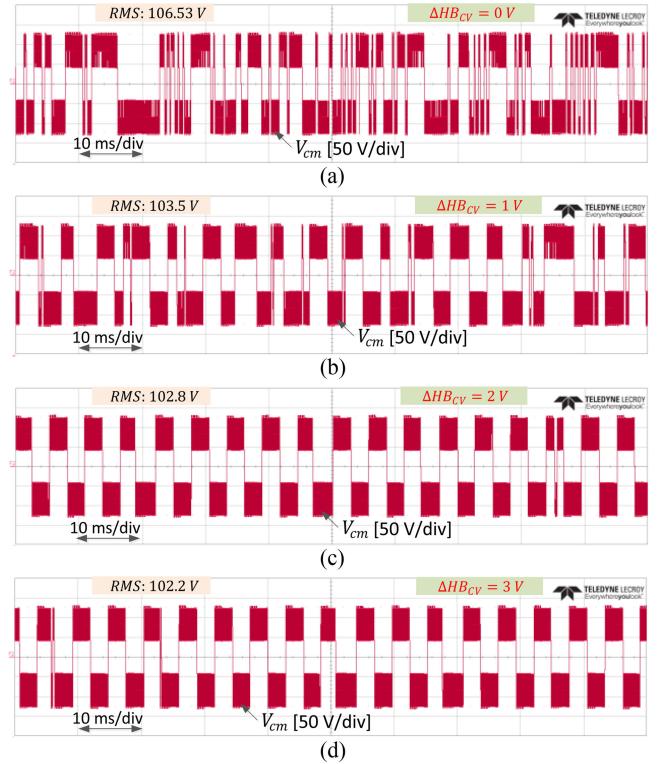


Fig. 21. Common mode voltage of proposed DPWM (under $\Delta HB_{cv} = 0, 1, 2$, and 3 V) when MI is 0.25.

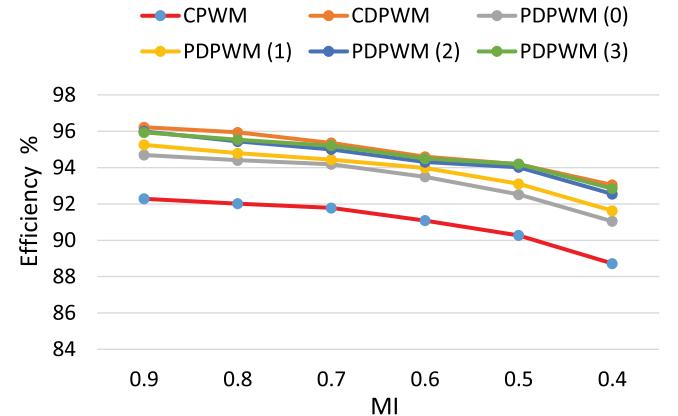


Fig. 22. Efficiency comparison between the CPWM, the CDPWM, and the PDPWM (under $\Delta HB_{cv} = 0, 1, 2$, and 3 V) at different MI with $\text{PF} \approx 1$.

VII. CONCLUSION

This article proposed a simple DPWM strategy using a hysteresis capacitance voltage band for the NP voltage balancing of 3L-NPC inverter topology. Based on the paper analysis, the change in capacitance voltage slope differs in each clamping mode resulting in the deviation of the capacitance voltages. The offset voltage of the proposed DPWM is triggered by a hysteresis band. Thus, the capacitance voltage slopes can be converged according to the amount of the hysteresis voltage band by adjusting the time intervals of each clamping mode in the proposed DPWM.

The proposed balancing method was investigated under various capacitance voltage error bands for power loss, current distortion, common mode voltage, and pole voltage shape at different operating modulation indices and PFs. It has been shown that the proposed DPWM can achieve zero capacitance voltage balance. This causes higher number of switching transitions and increase the common mode voltage compared to the conventional DPWM. Nevertheless, it has higher efficiency than the CPWM methods. The performance of the proposed DPWM for higher hysteresis voltage bands can mitigate the unbalance in dc-link capacitor voltages while maintaining comparable features to those of the conventional DPWM. The effectiveness of the proposed technique was proven through the simulation and experimental results.

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Ibrahim Mohd Alsofyani (Member, IEEE) received the M.Eng. degree in electrical mechatronics and automatic control and the Ph.D. degree in electrical engineering from the Universiti Teknologi Malaysia, Johor Bahru, Malaysia, in 2011 and 2014, respectively. From 2014 to 2016, he was a Research Associate and then Postdoctoral Fellow with the UTMPROTTON Future Drive Laboratory, Universiti Teknologi Malaysia. From 2016 to 2017, he was a Lecturer with the Faculty of Engineering, Lincoln University College, Selangor, Malaysia. In 2017, he was a Research Professor with the School of Electrical and Computer Engineering, Ajou University, Suwon, South Korea, where he became an Assistant Professor in 2018. His current research interests include electric machine drives, renewable power generations, and power electronic converters.

Dr. Alsofyani was a recipient of the Brain Korea 21 Fellowship in 2017 and Ajou University Research Excellence Award in 2019.



Kyo-Beum Lee (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical and electronic engineering from the Ajou University, Suwon, South Korea, in 1997 and 1999, respectively, and the Ph.D. degree in electrical engineering from the Korea University, Seoul, South Korea, in 2003.

From 2003 to 2006, he was with the Institute of Energy Technology, Aalborg University, Aalborg, Denmark. From 2006 to 2007, he was with the Division of Electronics and Information Engineering, Chonbuk National University, Jeonju, South Korea.

In 2007, he was with the Department of Electrical and Computer Engineering, Ajou University, Suwon, South Korea. His research interests include electric machine drives, renewable power generations, and electric vehicle applications.

Dr. Lee is an Associated Editor for the *IEEE TRANSACTIONS ON POWER ELECTRONICS*, the *IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS*, and the *Journal of Power Electronics*.