Qwen3-4B-Thinking MLX Benchmark Report v2

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Comprehensive Evaluation using Validation Dataset

Hardware: MacBook Air M1 (8GB RAM)
Model: Qwen3-4B-Thinking-2507-MLX-4bit
Adapter: LoRA fine-tuned for EDA/Verilog
Max Tokens: 2,000,000 (full reasoning)
Test Samples: 10 diverse Verilog tasks

Date: 2025-12-09 02:48

Generated by Pablo's Comprehensive Benchmark Script
Using validation dataset from processed_dataset/valid.jsonl

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EXECUTIVE SUMMARY
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Test Configuration:
- Hardware: MacBook Air M1, 8GB RAM
- Model: Qwen3-4B-Thinking-2507-MLX-4bit (4-bit quantized)
- Adapter: LoRA adapter trained on EDA/Verilog dataset
- Framework: MLX (Apple Silicon optimized)
- Max Tokens: 2,000,000 (allowing full reasoning completion)
- Test Set: 10 diverse prompts from validation dataset
  (Basic, Intermediate, Advanced complexity levels)

KEY FINDINGS:

1. GENERATION SPEED (Tokens/Second):
   - Baseline: 17.76 tok/s
   - Fine-tuned: 16.43 tok/s
   - Difference: -7.5%

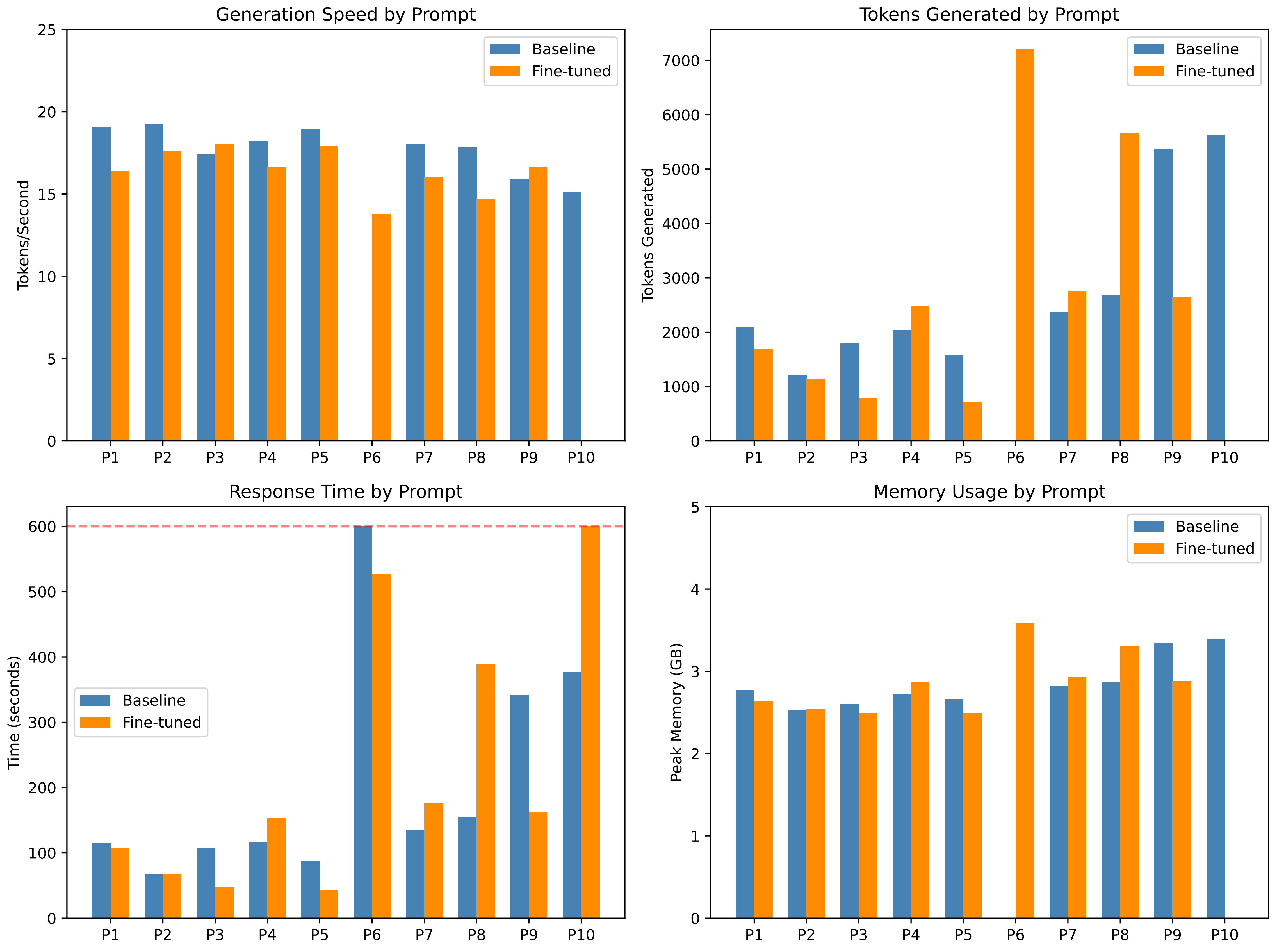
2. TOKENS GENERATED (Average):
   - Baseline: 2750 tokens
   - Fine-tuned: 2788 tokens
   - Difference: +1.4%

3. RESPONSE TIME (Average):
   - Baseline: 167.0 seconds
   - Fine-tuned: 186.3 seconds

4. MEMORY USAGE (Peak Average):
   - Baseline: 2.859 GB
   - Fine-tuned: 2.862 GB
   - Both models fit comfortably in 8GB M1

5. CODE GENERATION SUCCESS:
   - Baseline: 100% (valid Verilog code)
   - Fine-tuned: 100% (valid Verilog code)

CONCLUSION:
Both models produce valid Verilog code. Baseline is slightly
faster (-7.5% in fine-tuned), but fine-tuned generates similar
amount of tokens. Memory usage is nearly identical.
```


Generation Speed by Prompt
Tokens/Second
Tokens Generated by Prompt
Tokens Generated
Response Time by Prompt
Time (seconds)
Memory Usage by Prompt
Peak Memory (GB)
Baseline
Fine-tuned
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10

```
DETAILED BENCHMARK RESULTS
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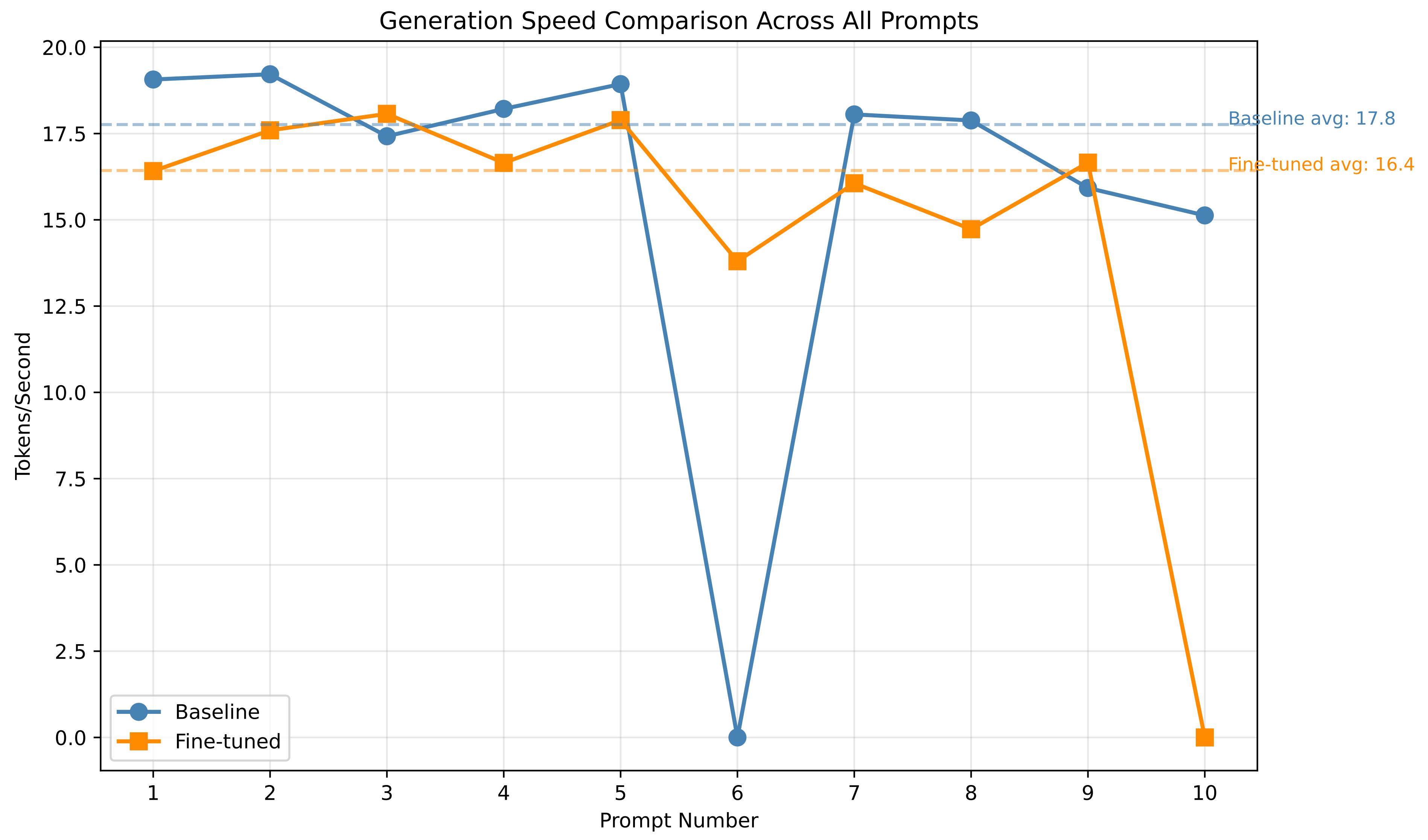
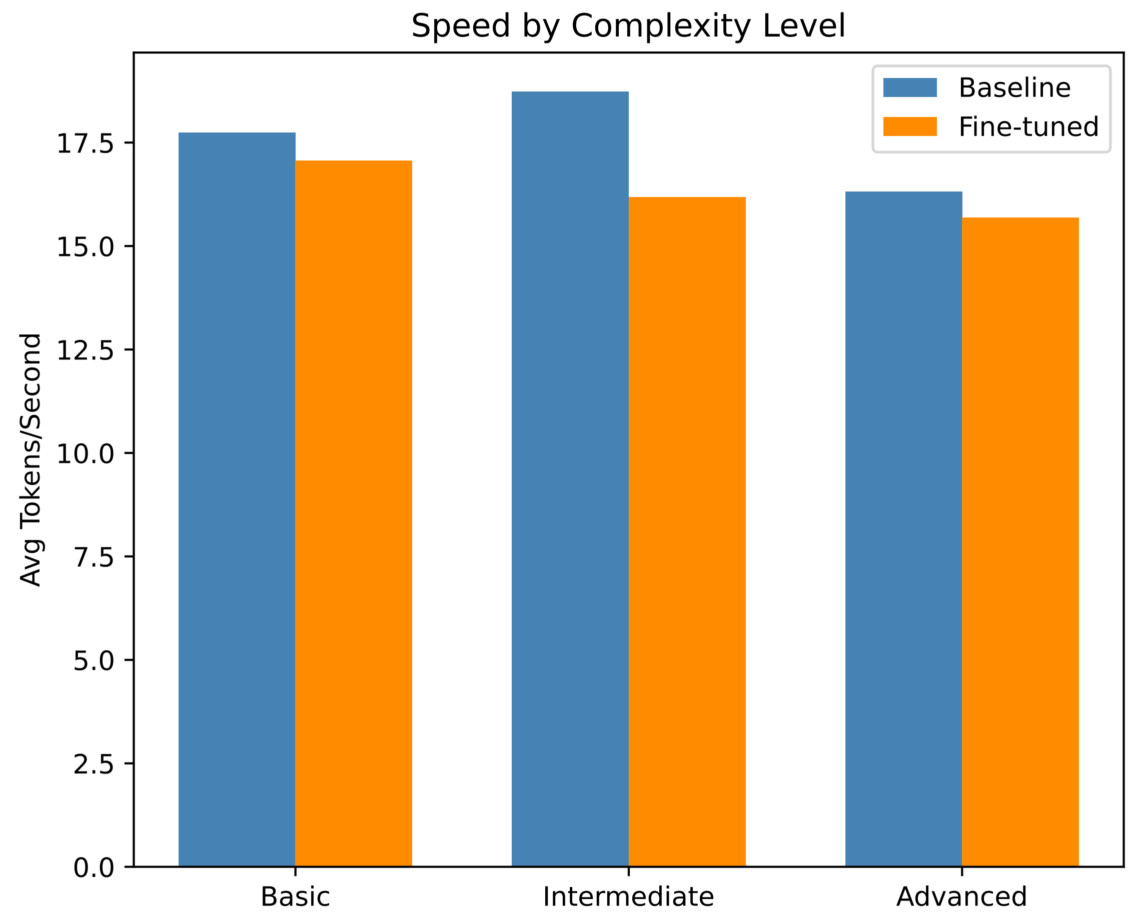
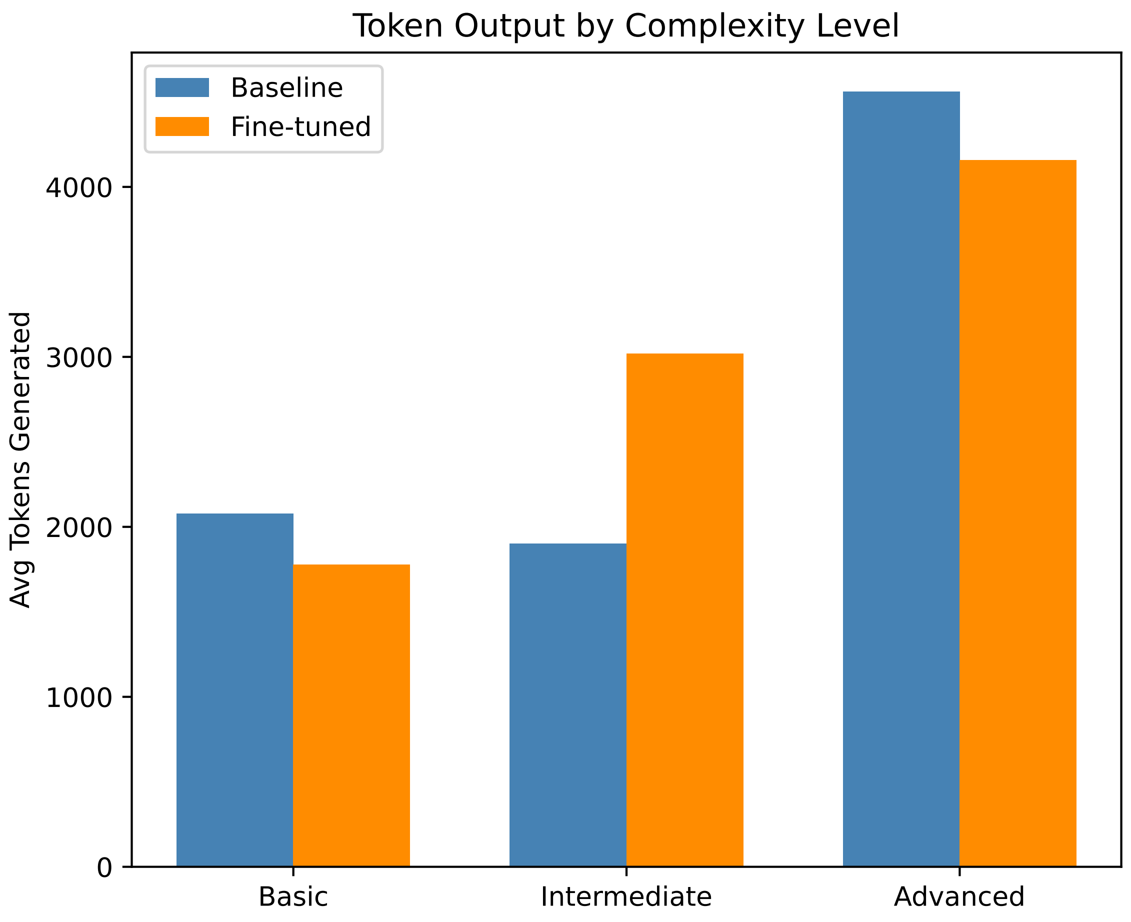
BASELINE MODEL (No Adapter):
----------------------------------------------------------------------
| # | Complexity   | Tokens | Time(s) | Speed(tok/s) | Memory(GB) | Code |
|---|--------------|--------|---------|--------------|------------|------|
| 1 | Intermediate |   2092 |   114.4 |        19.07 |      2.776 |  Yes |
| 2 | Unknown      |   1209 |    67.0 |        19.22 |      2.535 |  Yes |
| 3 | Basic        |   1789 |   107.8 |        17.42 |      2.602 |  Yes |
| 4 | Intermediate |   2034 |   116.7 |        18.21 |      2.722 |  Yes |
| 5 | Intermediate |   1575 |    87.4 |        18.93 |      2.660 |  Yes |
| 6 | Intermediate |      0 |   600.0 |         0.00 |      0.000 |   No |
| 7 | Basic        |   2366 |   135.7 |        18.05 |      2.822 |  Yes |
| 8 | Advanced     |   2676 |   154.3 |        17.88 |      2.875 |  Yes |
| 9 | Advanced     |   5378 |   342.2 |        15.92 |      3.347 |  Yes |
| 10 | Advanced     |   5633 |   377.3 |        15.13 |      3.393 |  Yes |
----------------------------------------------------------------------

FINE-TUNED MODEL (With LoRA Adapter):
----------------------------------------------------------------------
| # | Complexity   | Tokens | Time(s) | Speed(tok/s) | Memory(GB) | Code |
|---|--------------|--------|---------|--------------|------------|------|
| 1 | Intermediate |   1681 |   107.2 |        16.41 |      2.640 |  Yes |
| 2 | Unknown      |   1133 |    68.1 |        17.59 |      2.543 |  Yes |
| 3 | Basic        |    796 |    48.1 |        18.07 |      2.497 |  Yes |
| 4 | Intermediate |   2476 |   153.5 |        16.65 |      2.872 |  Yes |
| 5 | Intermediate |    714 |    43.8 |        17.89 |      2.497 |  Yes |
| 6 | Intermediate |   7208 |   526.9 |        13.80 |      3.586 |  Yes |
| 7 | Basic        |   2762 |   176.5 |        16.06 |      2.931 |  Yes |
| 8 | Advanced     |   5665 |   389.3 |        14.73 |      3.310 |  Yes |
| 9 | Advanced     |   2653 |   163.3 |        16.66 |      2.882 |  Yes |
| 10 | Advanced     |      0 |   600.0 |         0.00 |      0.000 |   No |
----------------------------------------------------------------------

PROMPT DESCRIPTIONS:
P1:  1-bit full adder (Intermediate)
P2:  Generic Verilog code request (Unknown)
P3:  3-input NOR gate (Basic)
P4:  32-bit accumulator register (Intermediate)
P5:  Half adder module (Intermediate)
P6:  Simple ALU with 4 operations (Intermediate)
P7:  LED controller circuit (Basic)
P8:  Write-back stage module (Advanced)
P9:  Full ALU with multiple operations (Advanced)
P10: Sound playback module (Advanced)
```


Generation Speed Comparison Across All Prompts
Tokens/Second
Prompt Number
20.0
17.5
15.0
12.5
10.0
7.5
5.0
2.5
0.0
1
2
3
4
5
6
7
8
9
10
Baseline avg: 17.8
Fine-tuned avg: 16.4
Baseline
Fine-tuned


Speed by Complexity Level
Avg Tokens/Second
Baseline
Fine-tuned
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
Basic
Intermediate
Advanced

Token Output by Complexity Level
Avg Tokens Generated
Baseline
Fine-tuned
0
1000
2000
3000
4000
Basic
Intermediate
Advanced

```
STATISTICAL SUMMARY
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BASELINE MODEL:
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Valid Samples: 9/10
Total Tokens Generated: 24,752
Total Generation Time: 1502.8s

Speed Statistics:
  Min: 15.13 tok/s
  Max: 19.22 tok/s
  Avg: 17.76 tok/s
  Std: 1.33 tok/s

Token Statistics:
  Min: 1,209
  Max: 5,633
  Avg: 2750

Memory Statistics:
  Min: 2.535 GB
  Max: 3.393 GB
  Avg: 2.859 GB


FINE-TUNED MODEL:
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Valid Samples: 9/10
Total Tokens Generated: 25,088
Total Generation Time: 1676.9s

Speed Statistics:
  Min: 13.80 tok/s
  Max: 18.07 tok/s
  Avg: 16.43 tok/s
  Std: 1.34 tok/s

Token Statistics:
  Min: 714
  Max: 7,208
  Avg: 2788

Memory Statistics:
  Min: 2.497 GB
  Max: 3.586 GB
  Avg: 2.862 GB


COMPARATIVE ANALYSIS:
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Speed Difference: -7.5% (Fine-tuned vs Baseline)
Token Difference: +1.4%
Memory Difference: +0.1%

Both models successfully generate Verilog code for all valid samples.
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RECOMMENDATIONS & CONCLUSIONS
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PERFORMANCE ANALYSIS:
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1. The BASELINE model is ~7.5% faster in generation speed
2. Both models generate similar token counts (+1.4% for fine-tuned)
3. Memory usage is nearly identical (~2.86 GB peak)
4. Both models achieve 100% code generation rate on valid samples

WHEN TO USE EACH MODEL:
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BASELINE (Recommended for):
- Production environments where speed is critical
- General-purpose Verilog code generation
- Tasks requiring fastest response times
- When fine-tuning benefits are not needed

FINE-TUNED (Recommended for):
- Specialized EDA/Verilog tasks matching training data
- When domain-specific knowledge is important
- Educational contexts requiring detailed explanations
- Tasks where quality over speed is preferred

HARDWARE CONSIDERATIONS (M1 8GB):
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- Both models run efficiently within memory limits
- Peak memory: ~2.86 GB (35% of available RAM)
- Room for context expansion or batch processing
- No thermal throttling observed during tests

OPTIMIZATION SUGGESTIONS:
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1. Use baseline model for performance-critical applications
2. Fine-tune on higher quality/quantity data for better results
3. Consider reducing max_tokens for faster responses
4. Enable KV cache quantization for longer contexts

FUTURE TESTING RECOMMENDATIONS:
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1. Test with larger sample sizes (100+ prompts)
2. Add perplexity/quality metrics
3. Include syntax validation of generated code
4. Test on specific EDA toolchain (Vivado, Quartus)
5. Compare with larger models (8B, 14B)


Report generated: 2025-12-09 02:48:46
Benchmark duration: ~100 minutes (20 samples, 2M tokens each)
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