Task 3

Design of sequential digital systems: Flip-flops and counters

INTRODUCTION:

The main goals of this task are:

- To improve the skills required to design the schematics of a digital circuit and simulate them using Xilinx ISE.
- To improve the skills required to implement sequential digital circuits using flip-flops and counters.

This task proposes the students a set of exercises related to the design of sequential digital systems. During the first week of this task, students will have to design and simulate the proposed exercises using Xilinx ISE. During the second week, students will have to implement one of the exercises done during the first week.

Important notice: Some of these exercises require preparations made prior to the beginning of the session. Please, read all the task to ensure you are correctly prepared for every session.

PART 1: DESIGN AND SIMULATION (FIRST WEEK)

During the first session of this task, three exercises are proposed to the students with their own simulation. The goal of these exercises is to understand three various kinds of application for sequential circuits using synchronized flip-flops: a circuit used to delay a digital signal, an n-state counter and a frequency divider.

Exercise 1: Delay circuit (35%)

Design a 4-bit output sequential circuit which output Q0Q1Q2Q3 displays the following sequence of values:

0000 → 1000 → 1100 → 1110 → 1111 → 0000 →1000 → …

The solution to this exercise uses four D-type flip-flops (fdc component in Xilinx ISE). Name these flip-flops as D0, D1, D2 and D3. All of them will have to be connected to the same clock signal (input CLK) and to the same asynchronous reset (input CLR).

To verify the correctness of the design using simulation, a testbench is provided as "p3ej1_tb.vhd" To ensure that the testbench correctly works, the following conditions must be fulfilled:

- File name for schematic: p3ej1.sch
- Input signal names: CLK, CLR
- Output signal names: Q0, Q1, Q2, Q3

During the simulation, analyze the behavior of the circuit's outputs after resetting the circuit. Justify the purpose of this kind of design (delaying a digital signal).

Exercise 2: N-state counter (35%)

The Xilinx ISE's cb4cled component is a counter available in the provided libraries. It is a bidirectional 4-bit counter (16 different values) with a load input (signal L), clock enable (signa CE), counting direction (signal UP) which defines the circuit to count upwards or backwards, and an asynchronous reset. For a more detailed description of this component read the provided information (right click Object properties Symbol info).

Students must create a cyclic counting circuit from N to 15. The value of N will be the youngest member of the group's most significant digit of her/is DNI (not zero). To achieve this result, students must add the required external logic to the counter using basic logic gates. The solution must be a synchronous circuit except for the asynchronous reset. One cycle after the initial reset ("0000"), the counter's value must be N and then continue the cyclic sequence N to 15.

To verify the correctness of the design using simulation a testbench is provided as "p3ej2_tb.vhd" To ensure that the testbench correctly works, the following conditions must be fulfilled:

- File name for schematic: p3ej2.sch
- Input signal names: CLK, INIT
- Output signal names: Q0, Q1, Q2, Q3

Exercise 3: Using a counter as a frequency divider (30%)

The Xilinx ISE's cd4cle component is a counter available in the provided libraries. It is a BCD counter (0 to 9). For a more detailed description of this component read the provided information (right click Object properties Symbol info).

Students must use two of these components connected in cascade with the required logic to achieve a circuit which SIG_DIV output will show a high pulse every 15 CLK cycles. I.e. SIG_DIV will have the frequency of CLK divided by 15.

To verify the correctness of the design using simulation a testbench is provided as "p3ej3_tb.vhd" To ensure that the testbench correctly works, the following conditions must be fulfilled:

- File name for schematic: p3ej3.sch
- Input signal names: CLK, INIT
- Output signal names: SIG_DIVLogic circuit (20%)

PART 2: IMPLEMENTATION (SECOND WEEK)

Important notice: This exercise requires mandatory preparation prior to the beginning of the session.

Implement the designs corresponding to exercises 1 (50%) and 2 (50%) using the minimum number of integrated circuits. To achieve this goal, follow these steps:

- Verify the correctness of the schematic created during the design stage. Optimize the number of components required to complete the implementation. Consider the differences between the Xilinx ISE's components and the provided flip-flops and counters (74HC175 and 74HC163). Examine their data sheets to identify these differences and any other requirement. Use the minimum number of components to simplify the circuit assembly.
- In case of any modification to the schematic, generate a new file and simulate it using the provided testbench in Xilinx ISE to ensure that the new design is correct.
- Using the optimized schematic design, create the assembly diagram using the back annotate technique presented during tutorial. This assembly diagram must be presented to the teacher at the beginning of the session to receive a mark. A correct assembly diagram should be clear, complete and avoid any ambiguity. It should allow anyone to fulfill the circuit assembly without asking the teacher or reading any other document.

The assembly will only achieve the maximum grade if the circuit's functionality has been completely achieved and the minimum number of components has been used. Otherwise, a correct implementation using more components or an erratic implementation (with a few errors) will be applied a 0.8 correction factor to its grade.

EVALUATION

The grade of Task 3 is obtained using the following formula:

$$Grade_{T3} = 0.3 \cdot Design + 0.35 \cdot Implementation + 0.35 \cdot Exam$$

- **Design:** the evaluation of the design requires the submission to Moodle of a single compressed file containing the following elements:
  - **Every schematic file generated:** These files have the "sch" extension.
  - **PDF documentation:** This PDF must contain the screen shots of the simulations for every exercise obtained using the simulation tool. This submission is required to obtain a grade in this part of the task.

  Important notice: To ensure that the submission corresponds to the design made during the session, it must be completed within the first 15 minutes after the end of the session. Every submission made after these 15 minutes will be graded with a 0.
  The evaluation of the design will consider the following elements:
  - The correctness of logic function simplification
  - The clarity of the schematic design
  - The completeness of the simulation (every input combination should be tested)
- **Implementation:** the evaluation of the implementation will be performed during the second session of the task. The evaluation of the second part of the task will consider the following elements:
  - **Assembly diagram:** Every team must show their assembly diagram at the beginning of the session. Those teams that do not present this diagram will be graded with 0 points in this part. At the end of the session, students must hand the diagram to the teacher.
  - **Assembly evaluation.** This evaluation will verify the correctness of the assembly. When a group of students finishes an assembly, they must ask the teacher to evaluate it. Every input combination will be evaluated. The evaluation has to be finished during the assembly session.
- **Exam:** During the first 15 minutes of the session that follows this task, an exam related to the designs of this task will take place. The purpose of this exam is to verify that the students have acquired the required knowledge about the concepts and designs presented during the task.