Task 2

Design and Implementation of Digital Combinational Systems using Multiplexers and Decoders

INTRODUCTION:

The main goals of this task are:

- To keep on using Xilinx ISE for the design of schematics and the simulation of digital circuits.
- To use complex combinational elements such as multiplexers and decoders.

This task proposes the students a set of exercises related to the design of logical functions using multiplexers and decoders. During the first week of this task, students will have to design and simulate the proposed exercises using Xilinx ISE. During the second week, students will have to implement one of the exercises done during the first week.

Important notice: Some of these exercises require preparations made prior to the beginning of the session. Please, read all the task to ensure you are correctly prepared for every session.

PART 1: DESIGN AND SIMULATION (FIRST WEEK)

Exercise 1: DNI digit detection using multiplexers (50%)

Repeat exercise 1 from task 1 using a multiplexer to solve it. Design a logic circuit that detects when its input corresponds to the last four different digits of the youngest member's DNI. The circuit must also detect the values 12 and 14 if the letter is within the range [A-L] or the values 13 and 15 if the letter is within the range [M-Z].

For example, if using the following ID number 12457507V, the logic circuit will set its output to '1' when one of the following values is set into its input: 7, 0, 5, 4, 13 and 15. This set of values define the following truth table:

Value	A	B	C	D	**Z**
0	0	0	0	0	**1**
1	0	0	0	1	**0**
2	0	0	1	0	**0**
3	0	0	1	1	**0**
4	0	1	0	0	**1**
5	0	1	0	1	**1**
6	0	1	1	0	**0**
7	0	1	1	1	**1**
8	1	0	0	0	**0**
9	1	0	0	1	**0**
10	1	0	1	0	**0**
11	1	0	1	1	**0**
12	1	1	0	0	**0**
13	1	1	0	1	**1**

14	1	1	1	0	**0**
15	1	1	1	1	**1**

Each group must fill its own truth table to obtain the function Z:

a) Design and simulate the combinational circuit in Xilinx ISE using the following components:
   - 1 x 4-1 multiplexer (m4-1 component in Xilinx)
   - any number of logic gates.

   Simulate the previous circuit to verify its correctness.
b) Create a second design of the function Z using only:
   - 2 x 4-1 multiplexers (m4-1 component in Xilinx)
   - 1 x 2-input OR gate
   - Any number of NOT gates

   Simulate this second circuit to verify its correctness.

To verify the correctness of each design using simulation, a set of testbenches is provided. This set consists of the following files: “p2ej1a_tb.vhd” and “p2ej1b_tb.vhd”. To ensure that the testbench correctly works, the following conditions must be fulfilled:

- File name for schematic a): p2ej1a.sch
- File name for schematic b): p2ej1b.sch
- Input signal names: A, B, C, D
- Output signal name: Z

Exercise 2: DNI digit detection using decoders (50%)

Repeat exercise the previous exercise using the following components:

- 2 x 3-to-8 (D3_8E) decoders
- Any number of logic gates

To verify the correctness of each design using simulation a set of testbench is provided. This set consists of the following files: “p2ej2_tb.vhd”. To ensure that the testbench correctly works, the following conditions must be fulfilled:

- File name for schematic: p2ej2.sch
- Input signal names: A, B, C, D
- Output signal name: Z

PART 2: IMPLEMENTATION (SECOND WEEK)

Important notice: This exercise requires mandatory preparation prior to the beginning of the session.

Implement the design corresponding to either exercise 1 a) or exercise 1 b). To decide on which exercise you will implement follow these steps:

1. Create the assembly diagrams of both exercises. For both assembly diagrams consider the next steps:
   a) Using the schematic created during the first week, create a new design which only uses the following components:
      - 1x74HC04 (6 NOT)
      - 1x74HC08 (4 AND2)
      - 2x74HC21 (2 AND4)
      - 1x74HC32 (4 OR2)
      - 1x74HC253 (2 MUX 4-1)
   b) Simulate the new schematic to ensure that the new design fulfills the original functionality.
   c) Using the optimized schematic design, create the assembly diagram using the back annotate technique presented during the tutorial.
2. Analyze and compare both assembly diagrams and select the one that will be easier to implement, i.e. the one with lower number of integrated circuits.

Note: A difference between the Xilinx component M4-1 and the multiplexer 74HC253 is that the later includes an output enable (OE) for each of its multiplexers. When a multiplexer's output is disabled, the corresponding output pin becomes a third state (Z → high impedance). Thus, allowing the creation of a **wired-or** by connecting both outputs and **ensuring that there is always a disabled output**.

This assembly diagram must be presented to the teacher at the beginning of the session to receive a mark. During the session, the students' only task will be the implementation of the digital circuit and not the generation of the assembly diagram.

A correct assembly diagram should be clear, complete and avoid any ambiguity. It should allow anyone to fulfill the circuit assembly without asking the teacher or reading any other document.

EVALUATION

The grade of Task 2 is obtained using the following formula:

$$Grade_{T2} = 0.3 \cdot Design + 0.35 \cdot Implementation + 0.35 \cdot Exam$$

- **Design:** the evaluation of the design requires the submission to Moodle of a single compressed file containing the following elements:
  - **Every schematic file generated:** These files have the "sch" extension.
  - **PDF documentation:** This PDF must contain the screen shots of the simulations for every exercise obtained using the simulation tool. This submission is required to obtain a grade in this part of the task.

  Important notice: To ensure that the submission corresponds to the design made during the session, it must be completed within the first 15 minutes after the end of the session. Every submission made after these 15 minutes will be graded with a 0.
  The evaluation of the design will consider the following elements:
  - The correctness of logic function simplification
  - The clarity of the schematic design
  - The completeness of the simulation (every input combination should be tested)
- **Implementation:** the evaluation of the implementation will be performed during the second session of the task. The evaluation of the second part of the task will consider the following elements:
  - **Assembly diagram:** Every team must show their assembly diagram at the beginning of the session. Those teams that do not present this diagram will be graded with 0 points in this part. At the end of the session, students must hand the diagram to the teacher.
  - **Assembly evaluation.** This evaluation will verify the correctness of the assembly. When a group of students finishes an assembly, they must ask the teacher to evaluate it. Every input combination will be evaluated. The evaluation has to be finished during the assembly session.
- **Exam:** During the first 15 minutes of the session that follows this task, an exam related to the designs of this task will take place. The purpose of this exam is to verify that the students have acquired the required knowledge about the concepts and designs presented during the task.