Task 1

Design and Implementation of Logic Functions

INTRODUCTION:

The main goals of this task are:

- To improve the skills required to design the schematics of a digital circuit and simulate them using Xilinx ISE. To apply the knowledge acquired in task 0a (Xilinx ISE tutorial).
- To improve the skills required to implement digital circuits using the required integrated circuits. To apply the knowledge acquired in task 0b (assembly tutorial)

This task proposes the students a set of exercises related to the design of logical functions using basic logic gates. During the first week of this task, students will have to design and simulate the proposed exercises using Xilinx ISE. During the second week, students will have to implement one of the exercises done during the first week.

Important notice: Some of these exercises require preparations made prior to the beginning of the session. Please, read all the task to ensure you are correctly prepared for every session.

PART 1: DESIGN AND SIMULATION (FIRST WEEK)

Exercise 1: Truth table (50%)

Design a logic circuit that detects when its input corresponds to any of the last four different digits of the youngest member's ID number. The circuit must also detect the values 12 and 14 if the letter is within the range [A-L] or the values 13 and 15 if the letter is within the range [M-Z].

For example, if using the following ID number 12457507V, the logic circuit will set its output to '1' when one of the following values is set into its input: 7, 0, 5, 4, 13 and 15. This set of values define the following truth table:

Value	A	B	C	D	**Z**
0	0	0	0	0	**1**
1	0	0	0	1	**0**
2	0	0	1	0	**0**
3	0	0	1	1	**0**
4	0	1	0	0	**1**
5	0	1	0	1	**1**
6	0	1	1	0	**0**
7	0	1	1	1	**1**
8	1	0	0	0	**0**
9	1	0	0	1	**0**
10	1	0	1	0	**0**
11	1	0	1	1	**0**
12	1	1	0	0	**0**
13	1	1	0	1	**1**
14	1	1	1	0	**0**
15	1	1	1	1	**1**

Each group must fill its own truth table to obtain the function Z:

a) Simplify the function Z using Karnaugh maps. Design the logic circuit corresponding to the simplified function using Xilinx ISE. Simulate the previous circuit to verify its correctness.
b) Create a second design of the function Z using only NAND gates. Simulate this second circuit to verify its correctness.

To verify the correctness of each design using simulation, a set of testbenches is provided. This set consists of the following files: “p1ej1a_tb.vhd” and “p1ej1b_tb.vhd”. To ensure that the testbench correctly works, the following conditions must be fulfilled:

- File name for schematic a): p1ej1a.sch
- File name for schematic b): p1ej1b.sch
- Input signal names: A, B, C, D
- Output signal name: Z

Exercise 2: Maxterms and Minterms (30%)

Considering the following four-variable logic function:

$$\boldsymbol{Z = \overline{A + B} + B\,\overline{C}\,D + A\,\overline{B}\,\overline{C}\,\overline{D}}$$

Consider variable “A” as the most significant input and variable “D” as the least significant input (A B C D), provide a solution for the following items:

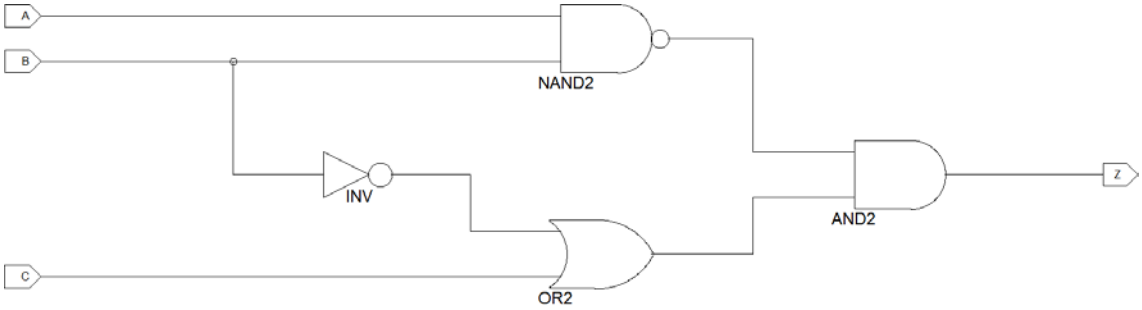
a) Present the truth table for function Z.
b) Using Karnaugh maps, represent function Z as the minimum sum of products.
c) Using Karnaugh maps, represent function Z as the minimum product of sums.
d) Design, using Xilinx ISE, the solutions to b) and c) and verify the correctness of these designs showing their equivalence using simulation.

To verify the correctness of each design using simulation a set of testbench is provided. This set consists of the following files: “p1ej2a_tb.vhd” and “p1ej2b_tb.vhd”. To ensure that the testbench correctly works, the following conditions must be fulfilled:

- File name for schematic a): p1ej2a.sch
- File name for schematic b): p1ej2b.sch
- Input signal names: A, B, C, D
- Output signal name: Z

Exercise 3: Logic circuit (20%)

Consider the following combinational logic circuit:



a) Present the logic function that represents output Z as the combination of the inputs A, B and C. Design the circuit using Xilinx ISE and verify that the function has been correctly defined by means of simulation.
b) Design using Xilinx ISE a simplified combinational circuit, equivalent to the former, using only NOR and NOT gates. Verify its correctness by means of simulation.

To verify the correctness of each design using simulation a set of testbench is provided. This set consists of the following files: “p1ej3a_tb.vhd” and “p1ej3b_tb.vhd”. To ensure that the testbench correctly works, the following conditions must be fulfilled:

- File name for schematic a): p1ej3a.sch
- File name for schematic b): p1ej3b.sch
- Input signal names: A, B, C
- Output signal name: Z

PART 2: IMPLEMENTATION (SECOND WEEK)

Important notice: This exercise requires mandatory preparation prior to the beginning of the session.

- Implement the design corresponding to exercise 2 using the minimum number of integrated circuits. To achieve this goal, follow these steps:
- Verify the correctness of the schematic created during the design stage. Optimize the number of components required to complete the implementation.
- In case of any modification to the schematic, generate a new file and simulate it using the provided testbench in Xilinx ISE to ensure that the new design is correct. Ensure that the resulting schematic design only uses the following logic gates:
    - 74HC04 integrated circuit: 6 NOT gates
    - 74HC08 integrated circuit: 4 2-input AND gates
    - 74HC21 integrated circuit: 2 4-input AND gates
    - 74HC32 integrated circuit: 4 2-input OR gates
- Using the optimized schematic design, create the assembly diagram using the back annotate technique presented during tutorial. This assembly diagram must be submitted to Moodle the day before the session to gain access to the laboratory. During the session, the students' only task will be the implementation of the digital circuit and not the generation of the assembly diagram.

A correct assembly diagram should be clear, complete and avoid any ambiguity. It should allow anyone to fulfill the circuit assembly without asking the teacher or reading any other document.

EVALUATION

The grade of Task 1 is obtained using the following formula:

$$Grade \quad \text{Task } 1 = 0.3 \cdot Design + \ 0.35 \cdot Implementation + 0.35 \cdot Exam$$

- **Design:** the evaluation of the design will be completed during the first session of the task. When a group of students finishes an exercise, they must ask the teacher to evaluate it.
  To fulfill the evaluation, every group must submit the results of every exercise to Moodle. This upload will be a simple PDF report including the screen shots of both the schematics and the simulations for every exercise obtained using Xilinx ISE. This submission is required to obtain a grade in this part of the task.
  Important notice: To ensure that the submission corresponds to the design made during the session, it must be completed within the first 15 minutes after the end of the session. Every submission made after this 15 minutes will be graded with a 0.
  The evaluation of the design will consider the following elements:
  - The correctness of logic function simplification
  - The clarity of the schematic design
  - The completeness of the simulation (every input combination should be tested)
- **Implementation:** the evaluation of the implementation will be performed during the second session of the task. When a group of students finishes an assembly, they must ask the teacher to evaluate it.
  Important notice: No assembly will be graded if the corresponding assembly diagram is not presented to the teacher and submitted to Moodle.
  The evaluation of the assembly will consider the following elements:
  - The correctness and completeness of the implementation. Every input combination will be evaluated.
- **Exam:** During the first 15 minutes of the session that follows this task, an exam related to the designs of this task will take place. The purpose of this exam is to verify that the students have acquired the required knowledge about the concepts and designs presented during the task.