Home Grown Caching interface

- **Introduce MemoryManager class.**
  - **Access is made through View objects with RW intent & location, open/close semantic.**
  - **Automatic for data parallel expression template engine**

- **A=B*C+Cshift(D,1,Xdir);**

This is a data parallel interface across all nodes, array elements dpcpp is not data parallel in same F90 sense.

- **Under the hood, communication is performed**
  - **Data is possibly moved to/from device**
  - **Works on KNL, HIP, CUDA and SYCL. Buffer works only on SYCL.**

- **MemoryManager tracks entire buffers in a *software cache* with O(1) overhead**
  - **O(1) Hash table maps Host pointers to cache table entries**
    - **Consistent, CpuDirty, AccDirty states**
    - **(I prev. designed the IBM BlueGene/Q multicore L1p prefetching cache… :))**
  - **Linked list LRU queue prioritises evictable arrays**
    - **O(1) push, pop and erase via indirection from Hash table**
  - **EvictNext or EvictLast prio for user avoidance of cache thrashing. Full control of algorithm**