1. Description

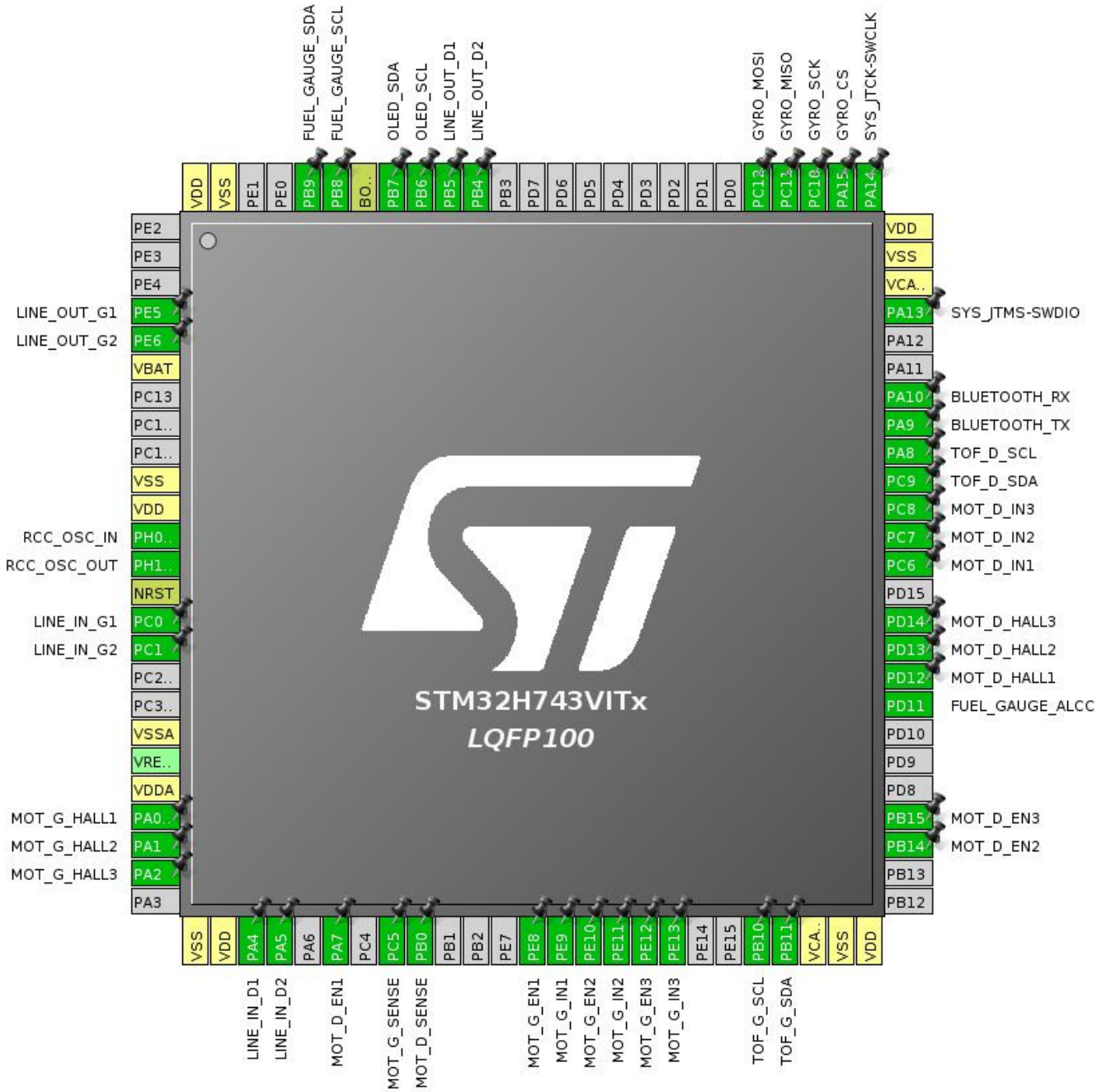
1.1. Project

Project Name	NARA
Board Name	No information
Generated with:	STM32CubeMX 4.25.0
Date	04/02/2018

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H7x3
MCU name	STM32H743VITx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration

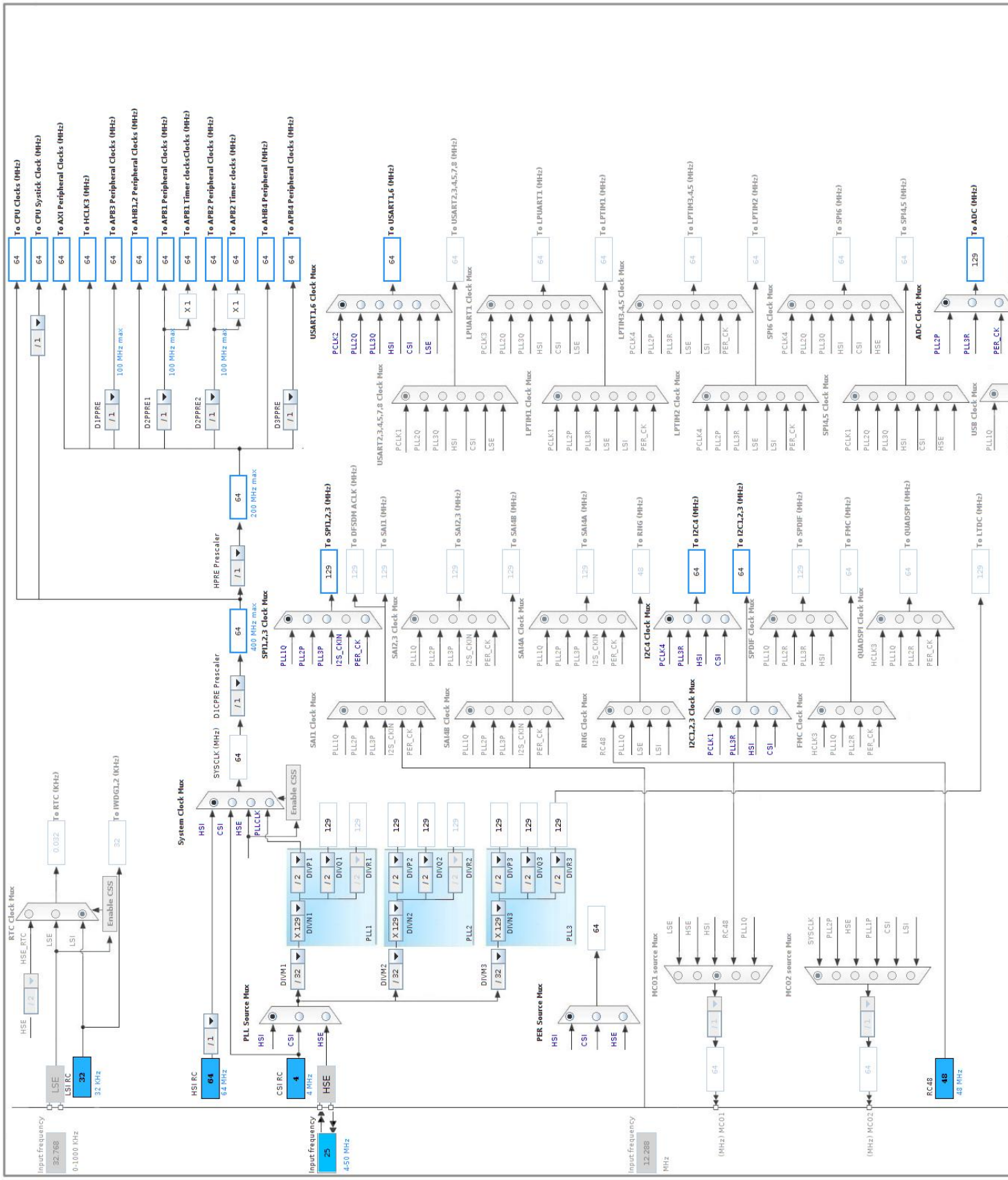


3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
4	PE5	I/O	TIM15_CH1	LINE_OUT_G1
5	PE6	I/O	TIM15_CH2	LINE_OUT_G2
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	ADC1_INP10	LINE_IN_G1
16	PC1	I/O	ADC1_INP11	LINE_IN_G2
19	VSSA	Power		
21	VDDA	Power		
22	PA0-WKUP	I/O	TIM2_CH1	MOT_G_HALL1
23	PA1	I/O	TIM2_CH2	MOT_G_HALL2
24	PA2	I/O	TIM2_CH3	MOT_G_HALL3
26	VSS	Power		
27	VDD	Power		
28	PA4	I/O	ADC1_INP18	LINE_IN_D1
29	PA5	I/O	ADC1_INP19	LINE_IN_D2
31	PA7	I/O	TIM8_CH1N	MOT_D_EN1
33	PC5	I/O	ADC1_INP8	MOT_G_SENSE
34	PB0	I/O	ADC1_INP9	MOT_D_SENSE
38	PE8	I/O	TIM1_CH1N	MOT_G_EN1
39	PE9	I/O	TIM1_CH1	MOT_G_IN1
40	PE10	I/O	TIM1_CH2N	MOT_G_EN2
41	PE11	I/O	TIM1_CH2	MOT_G_IN2
42	PE12	I/O	TIM1_CH3N	MOT_G_EN3
43	PE13	I/O	TIM1_CH3	MOT_G_IN3
46	PB10	I/O	I2C2_SCL	TOF_G_SCL
47	PB11	I/O	I2C2_SDA	TOF_G_SDA
48	VCAP1	Power		
49	VSS	Power		
50	VDD	Power		
53	PB14	I/O	TIM8_CH2N	MOT_D_EN2
54	PB15	I/O	TIM8_CH3N	MOT_D_EN3
58	PD11	I/O	I2C4_SMBA	FUEL_GAUGE_ALCC

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
59	PD12	I/O	TIM4_CH1	MOT_D_HALL1
60	PD13	I/O	TIM4_CH2	MOT_D_HALL2
61	PD14	I/O	TIM4_CH3	MOT_D_HALL3
63	PC6	I/O	TIM8_CH1	MOT_D_IN1
64	PC7	I/O	TIM8_CH2	MOT_D_IN2
65	PC8	I/O	TIM8_CH3	MOT_D_IN3
66	PC9	I/O	I2C3_SDA	TOF_D_SDA
67	PA8	I/O	I2C3_SCL	TOF_D_SCL
68	PA9	I/O	USART1_TX	BLUETOOTH_TX
69	PA10	I/O	USART1_RX	BLUETOOTH_RX
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
77	PA15	I/O	SPI3_NSS	GYRO_CS
78	PC10	I/O	SPI3_SCK	GYRO_SCK
79	PC11	I/O	SPI3_MISO	GYRO_MISO
80	PC12	I/O	SPI3_MOSI	GYRO_MOSI
90	PB4	I/O	TIM3_CH1	LINE_OUT_D2
91	PB5	I/O	TIM3_CH2	LINE_OUT_D1
92	PB6	I/O	I2C1_SCL	OLED_SCL
93	PB7	I/O	I2C1_SDA	OLED_SDA
94	BOOT0	Boot		
95	PB8	I/O	I2C4_SCL	FUEL_GAUGE_SCL
96	PB9	I/O	I2C4_SDA	FUEL_GAUGE_SDA
99	VSS	Power		
100	VDD	Power		

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN8

mode: IN9

IN10: IN10 Single-ended

mode: IN11

IN18: Single-ended

mode: IN19

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

<html><img src='jar:file:/home/zhonx/.opt/STM32CubeMX/plugins/ipmanager.jar!/com/st/microxplorer/plugins/ipmanager/util/error10x10.png'   ADC_Settings</html>:

Clock Prescaler	Asynchronous clock mode divided by 4
Resolution	ADC 16-bit resolution
Scan Conversion Mode	**Disabled ***
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Boost Mode	Enabled
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	**4 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 8
Sampling Time	1.5 Cycles

Offset Number	No offset
Rank	**2 ***
Channel	**Channel 9 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Rank	**3 ***
Channel	**Channel 10 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Rank	**4 ***
Channel	**Channel 11 ***
Sampling Time	1.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. I2C1

I2C: I2C

5.2.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled

Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.3. I2C2

I2C: I2C

5.3.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.4. I2C3

I2C: I2C

5.4.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.5. I2C4

I2C: SMBus-Alert-mode

5.5.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

SMBus Features:

Packet Error Check Mode	PEC Disabled
Peripheral Mode	Peripheral Mode Smbus Slave

SMBus Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	1

Timeout configuration:

Extended Clock Timeout	Disabled
Idle Clock Timeout Detection	Disabled
Timeout Time (ns)	25000000
Timeout	0x0000830D

5.6. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.6.1. Parameter Settings:

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	16

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	0 WS (1 CPU cycle)

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

PLL range Parameters:

PLL1 clock Input range	Between 2 and 4 MHz
PLL2 input frequency range	Between 2 and 4 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range
PLL Fractional Part	0
PLL2 Fractional Part	0

5.7. SPI3

Mode: Full-Duplex Master
Hardware NSS Signal: Hardware NSS Output Signal

5.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**64.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	00 Cycle
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

5.8. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.9. TIM1

Slave Mode: Trigger Mode

Trigger Source: ITR1

Channel1: Output Compare CH1 CH1N

Channel2: Output Compare CH2 CH2N

Channel3: Output Compare CH3 CH3N

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable
Slave Mode Controller	Trigger Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	0

Clear Input:

Clear Input Source	Disable

Output Compare Channel 1 and 1N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

Output Compare Channel 2 and 2N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

Output Compare Channel 3 and 3N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

5.10. TIM2

Clock Source : Internal Clock

Combined Channels: XOR ON / Hall Sensor Mode

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection TRGO	Output Compare (OC2REF)

Hall Sensor:

Prescaler Division Ratio	No division
Polarity	Rising Edge
Input Filter	0
Commutation Delay	0

5.11. TIM3

Channel1: Output Compare CH1

Channel2: Output Compare CH2

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0

Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

Output Compare Channel 1:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High

Output Compare Channel 2:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High

5.12. TIM4

Clock Source : Internal Clock

Combined Channels: XOR ON / Hall Sensor Mode

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection TRGO	Output Compare (OC2REF)

Hall Sensor:

Prescaler Division Ratio	No division
Polarity	Rising Edge
Input Filter	0
Commutation Delay	0

5.13. TIM8

Slave Mode: Trigger Mode

Trigger Source: ITR2

Channel1: Output Compare CH1 CH1N

Channel2: Output Compare CH2 CH2N

Channel3: Output Compare CH3 CH3N

5.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable
Slave Mode Controller	Trigger Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	0

Clear Input:

Clear Input Source	Disable

Output Compare Channel 1 and 1N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

Output Compare Channel 2 and 2N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

Output Compare Channel 3 and 3N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

5.14. TIM15

Channel1: Output Compare CH1

Channel2: Output Compare CH2

5.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0

Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Output Compare Channel 1:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 2:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

5.15. USART1

Mode: Asynchronous

5.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	7 Bits (including Parity)

Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Prescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_INP10	Analog mode	No pull-up and no pull-down	n/a	LINE_IN_G1
	PC1	ADC1_INP11	Analog mode	No pull-up and no pull-down	n/a	LINE_IN_G2
	PA4	ADC1_INP18	Analog mode	No pull-up and no pull-down	n/a	LINE_IN_D1
	PA5	ADC1_INP19	Analog mode	No pull-up and no pull-down	n/a	LINE_IN_D2
	PC5	ADC1_INP8	Analog mode	No pull-up and no pull-down	n/a	MOT_G_SENSE
	PB0	ADC1_INP9	Analog mode	No pull-up and no pull-down	n/a	MOT_D_SENSE
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	OLED_SCL
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	OLED_SDA
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	TOF_G_SCL
	PB11	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	TOF_G_SDA
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	TOF_D_SDA
	PA8	I2C3_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	TOF_D_SCL
I2C4	PD11	I2C4_SMBA	Alternate Function Open Drain	No pull-up and no pull-down	Low	FUEL_GAUGE_ALCC
	PB8	I2C4_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	FUEL_GAUGE_SCL
	PB9	I2C4_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	FUEL_GAUGE_SDA
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI3	PA15	SPI3_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	GYRO_CS
	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	GYRO_SCK
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	GYRO_MISO
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	GYRO_MOSI
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PE8	TIM1_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_G_EN1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_G_IN1
	PE10	TIM1_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_G_EN2
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_G_IN2
	PE12	TIM1_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_G_EN3
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_G_IN3
TIM2	PA0-WKUP	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_G_HALL1
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_G_HALL2
	PA2	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_G_HALL3
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	LINE_OUT_D2
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	LINE_OUT_D1
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_D_HALL1
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_D_HALL2
	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_D_HALL3
TIM8	PA7	TIM8_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_D_EN1
	PB14	TIM8_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_D_EN2
	PB15	TIM8_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_D_EN3
	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_D_IN1
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_D_IN2
	PC8	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOT_D_IN3
TIM15	PE5	TIM15_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	LINE_OUT_G1
	PE6	TIM15_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	LINE_OUT_G2
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	BLUETOOTH_TX
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	BLUETOOTH_RX

6.2. DMA configuration

nothing configured in DMA service

6.3. BDMA configuration

nothing configured in DMA service

6.4. MDMA configuration

nothing configured in DMA service

6.5. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
USART1 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
SPI3 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
I2C4 event interrupt	unused		
I2C4 error interrupt	unused		
TIM15 global interrupt	unused		
HSEM1 global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32H7
Line	STM32H7x3
MCU	STM32H743VITx
Datasheet	030538_Rev1

7.2. Parameter Selection

Temperature	25
Vdd	3.0

8. Software Pack Report