SDRAM Controller to interface MT48LC16M4A2 with 80386DX

EE 5313

Microprocessor Systems

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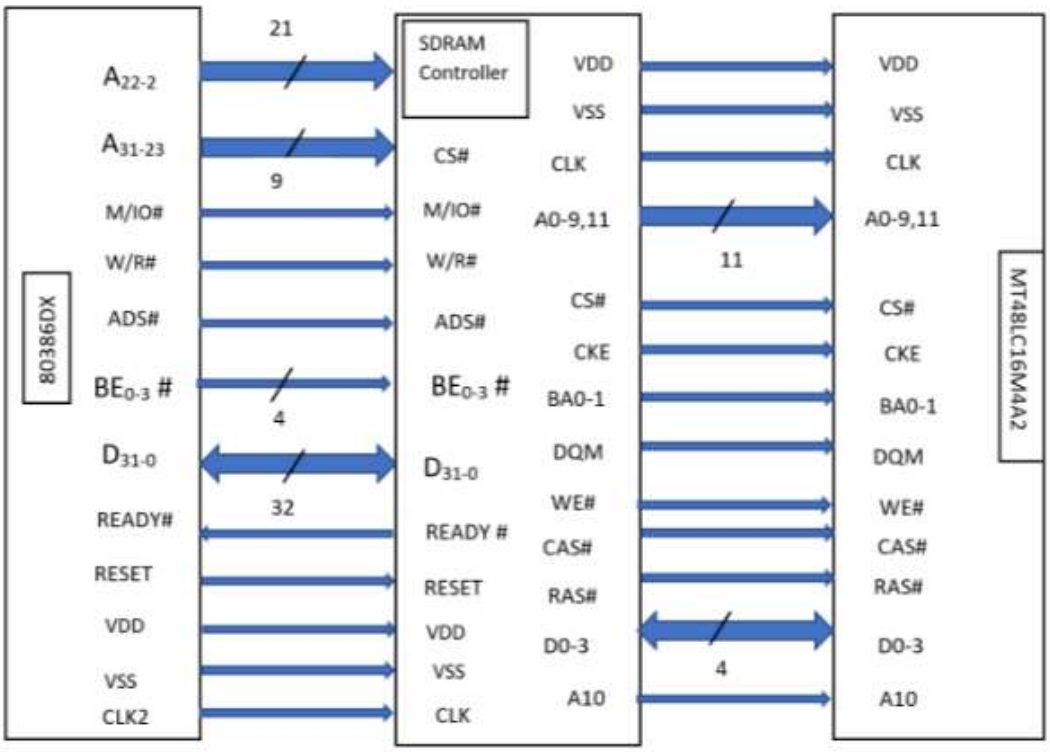
1002059004 LIN, HAO-TING

1002011190 Padmanathan Kannan

Interfacing between SDRAM and 80386DX:

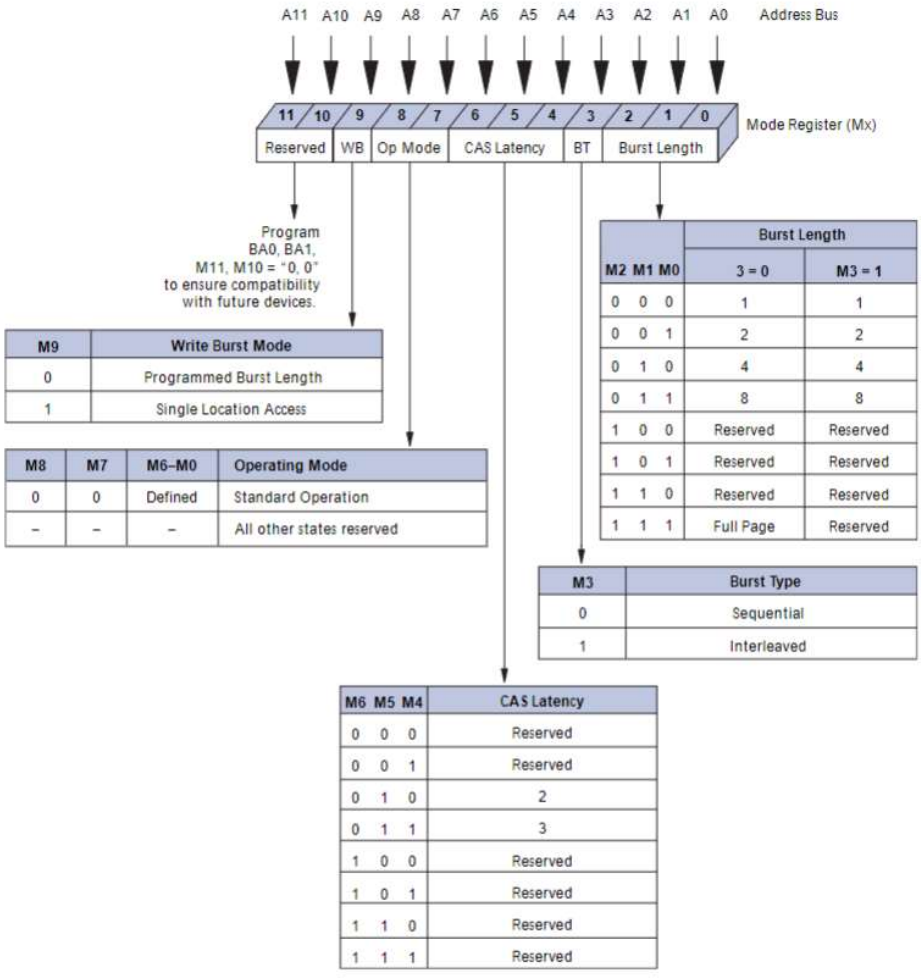


ADS#, W/R#, and M/IO# signals decide the command of READ and WRITE.
CS#, RAS#, CAS#, WE# will determine the operation and command of SDRAM.
A10 signal determines the number of the banks to be Precharged.
DQM signal determines which data bus to transfer data.

Characteristics:

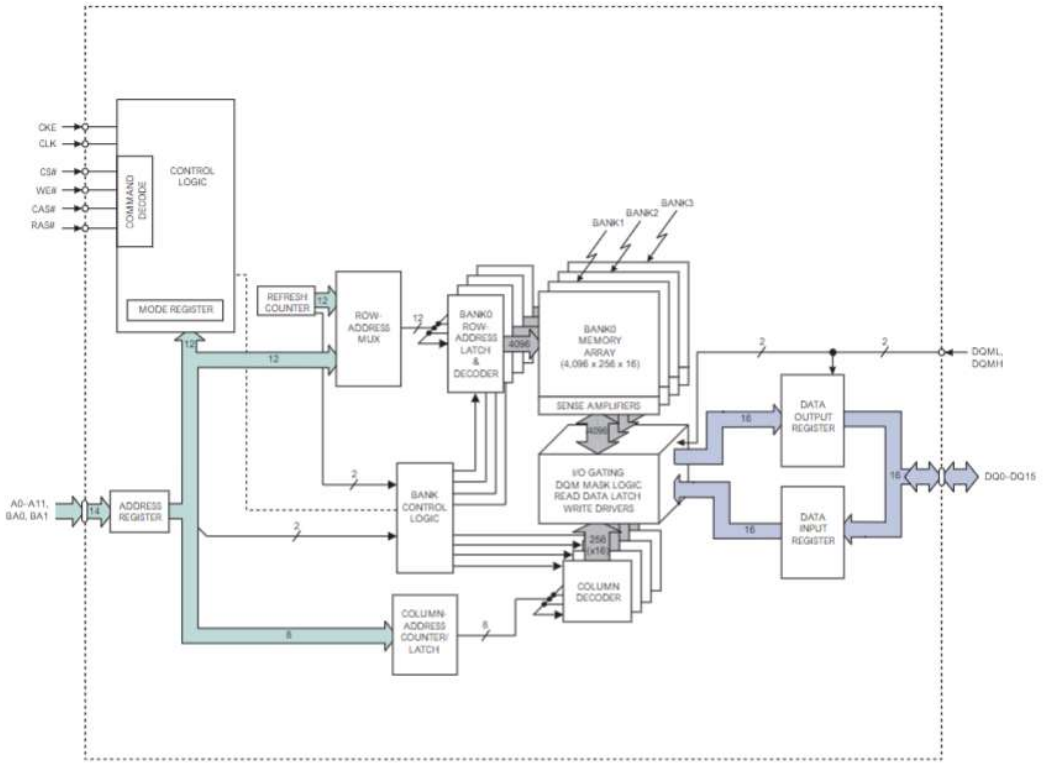
- MT48LC16M4A2 : 4 MEG x 4 x 4 banks
- Speed Grade: -7E
- Frequency = 133MHz
- Cycle Time is 7.5ns
- CL = 2, Burst Length = 8, Refresh Time = 64ms

Load Mode Register:

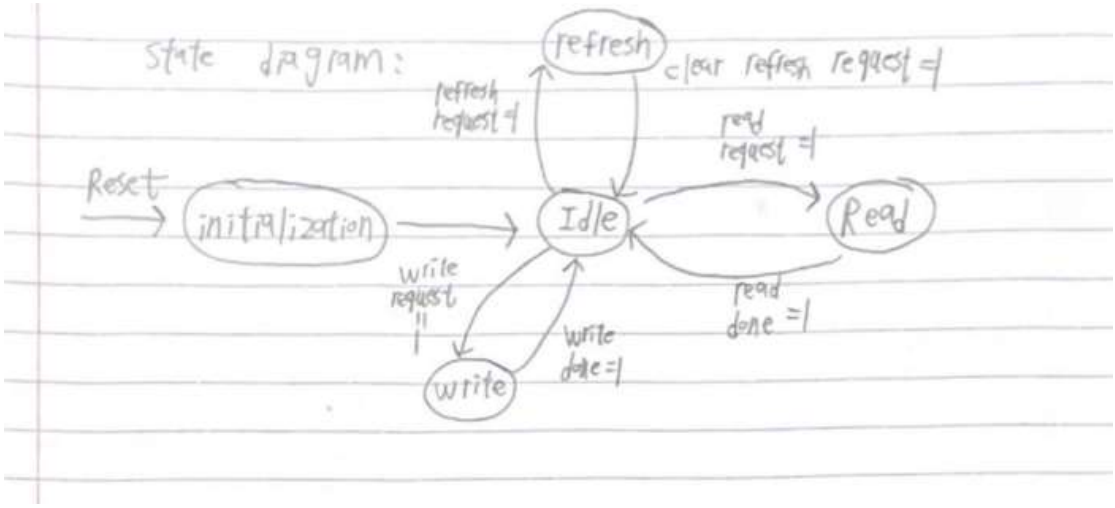


The load mode register decides Burst Length, Burst Type, and CAS Latency. Besides, it decides the operation mode. The bits and how they are decided are shown in the figure. The signals are A0-A11 that are loaded in Load Mode Register.

SDRAM Architecture:

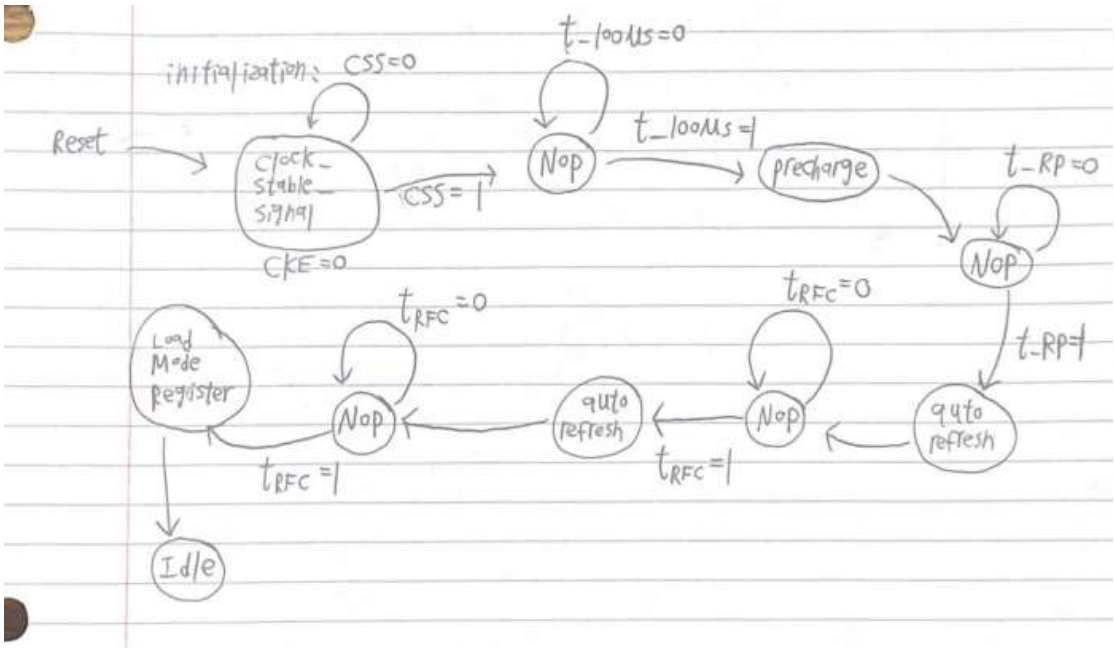


TOP state diagram:



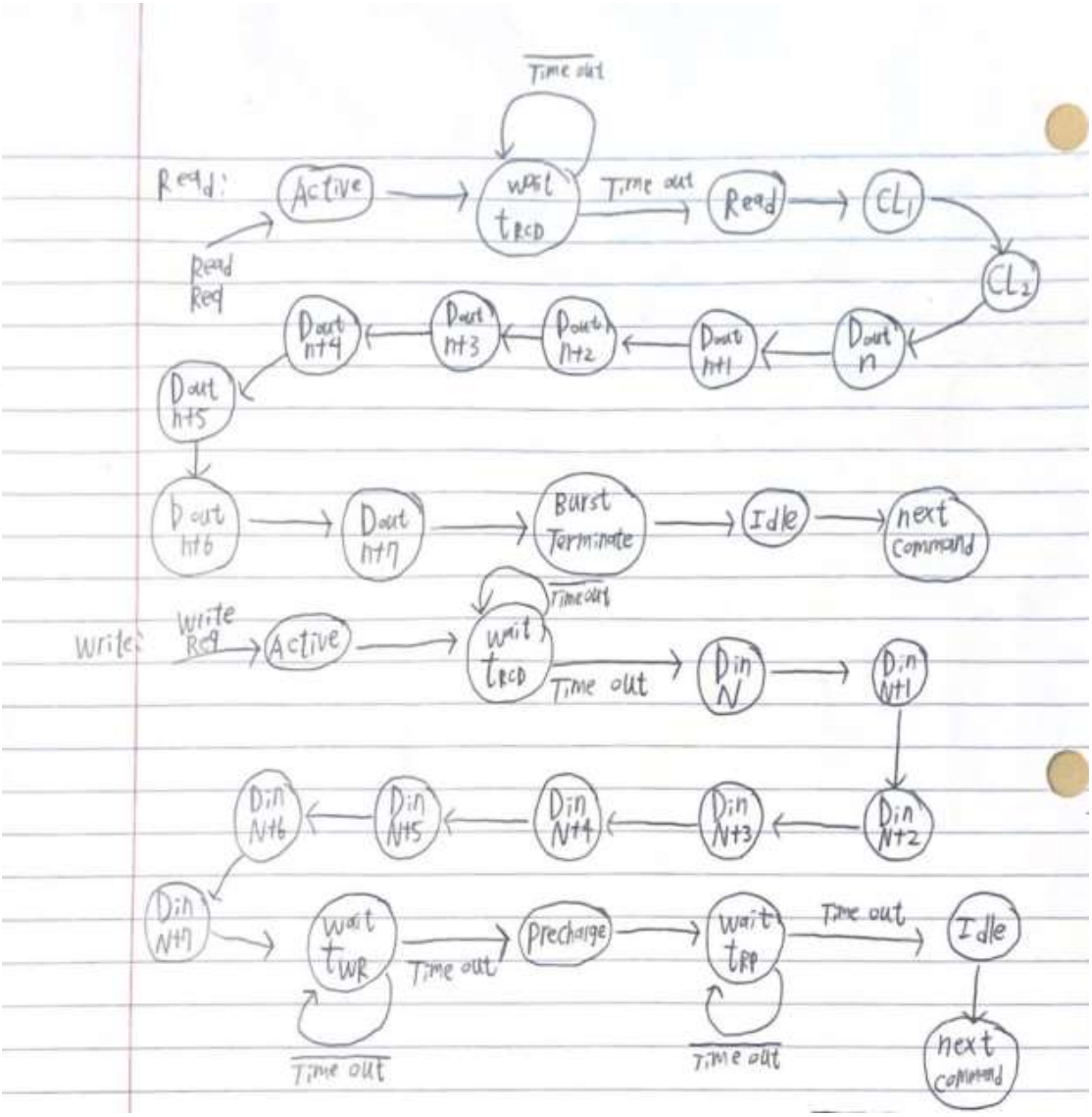
The figure above is for top state diagram. After initialization, the SDRAM will enter the IDLE state. During the IDLE state, the SDRAM can operate refresh, read, or write.

Initialization state diagram:

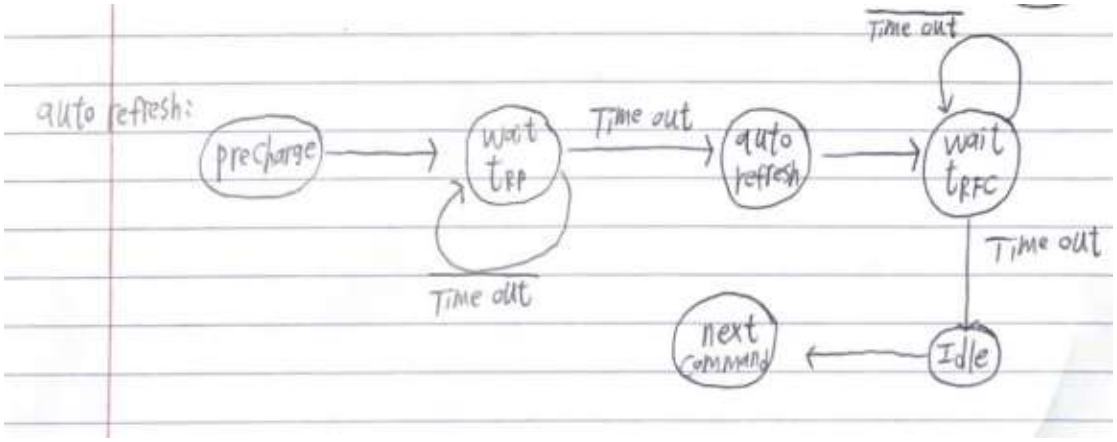


The figure above is SDRAM initialization state diagram. SDRAM must do this process before operating any command. Besides, it needs 100-micron seconds before issuing any command.

Read and Write state diagram:



Auto Refresh diagram:



TRANSITION TABLES:

TOP:

Current State	Next State	Condition
X	Initialization	Reset=1
Initialization	Idle	X
Idle	Read	Read_REQ=1
Read	Idle	Read_DONE=1
Idle	Write	Write_REQ=1
Write	Idle	Write_DONE=1
Idle	Refresh	Refresh_REQ=1
Refresh	Idle	Clear_Refresh_REQ=1

Initialization:

Current State	Next State	Condition
X	Clock_Stable_Signal	Reset=1
Clock_Stable_Signal	NOP	PLL=0
Clock_Stable_Signal	Clock_Stable_Signal	PLL=1
NOP	Precharge	t_100µs=0
NOP	NOP	t_100µs=1
Precharge	Wait_tRP	X
Wait_tRP	Wait_tRP	!Timeout
Wait_tRP	Auto_Refresh	Timeout
Auto_Refresh	Wait_tRFC	X
Wait_tRFC	Wait_tRFC	!Timeout
Wait_tRFC	Auto_Refresh	Timeout
Auto_Refresh	Wait_tRFC	X
Wait_tRFC	Wait_tRFC	!Timeout
Wait_tRFC	Load_Mode_Register	Timeout
Load_Mode_Register	Idle	X

Read:

Current State	Next State	Condition
X	Active	Read_REQ=1
Active	Wait_tRCD	X
Wait_tRCD	Wait_tRCD	!Timeout
Wait_tRCD	Read	Timeout
Read	CL1	X
CL1	CL2	X
CL2	Dout n	X
Dout n	Dout n+1	X
Dout n+1	Dout n+2	X
Dout n+2	Dout n+3	X
Dout n+3	Dout n+4	X
Dout n+4	Dout n+5	X
Dout n+5	Dout n+6	X
Dout n+6	Dout n+7	X
Dout n+7	Burst Terminate	X
Burst Terminate	Idle	X
Idle	Next Command	X

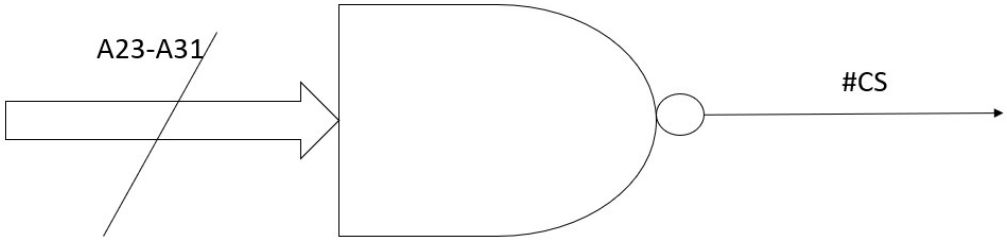
Write:

Current State	Next State	Condition
X	Active	Write_REQ
Active	Wait_tRCD	X
Wait_tRCD	Wait_tRCD	!Timeout
Wait_tRCD	Din N	Timeout
Din N	Din N+1	X
Din N+1	Din N+2	X
Din N+2	Din N+3	X
Din N+3	Din N+4	X
Din N+4	Din N+5	X
Din N+5	Din N+6	X
Din N+6	Din N+7	X
Din N+7	Wait_tWR	X
Wait_tWR	Wait_tWR	!Timeout
Wait_tWR	Precharge	Timeout
Precharge	Wait_tRP	X
Wait_tRP	Wait_tRP	!Timeout
Wait_tRP	Idle	Timeout
Idle	Next Command	X

Auto Refresh:

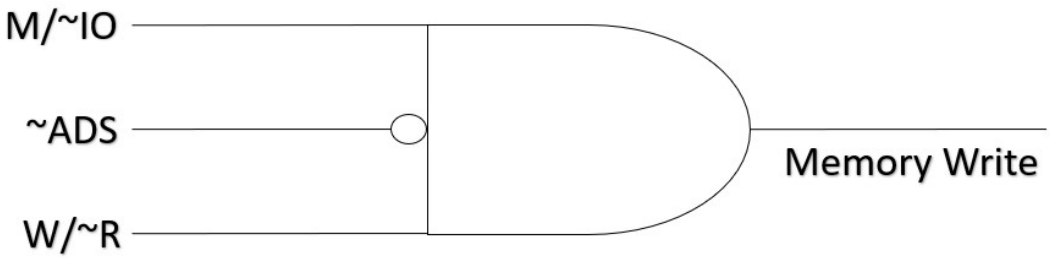
Current State	Next State	Condition
Precharge	Wait_tRP	X
Wait_tRP	Wait_tRP	!Timeout
Wait_tRP	Auto Refresh	Timeout
Auto Refresh	Wait_tRFC	X
Wait_tRFC	Wait_tRFC	!Timeout
Wait_tRFC	Idle	Timeout
Idle	Next Command	X

Decoder:

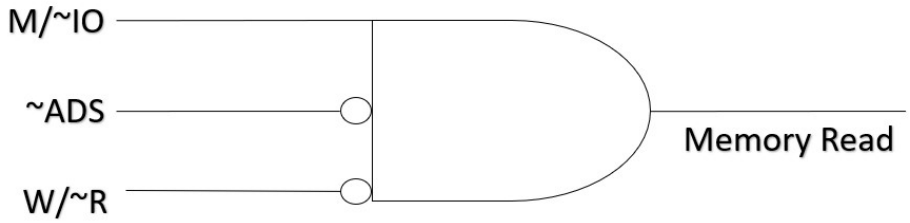


We have A0-A31 for address. In our design, we will have 8 bits for column address, 12 bits for row address, 2 bits for BA0 and BA1, 2 bits for 80386DX bank select. The rest bits, A23-A31, 2ill be decoded as #CS(chip select) signal.

Memory Write Signal:



Memory Read Signal:



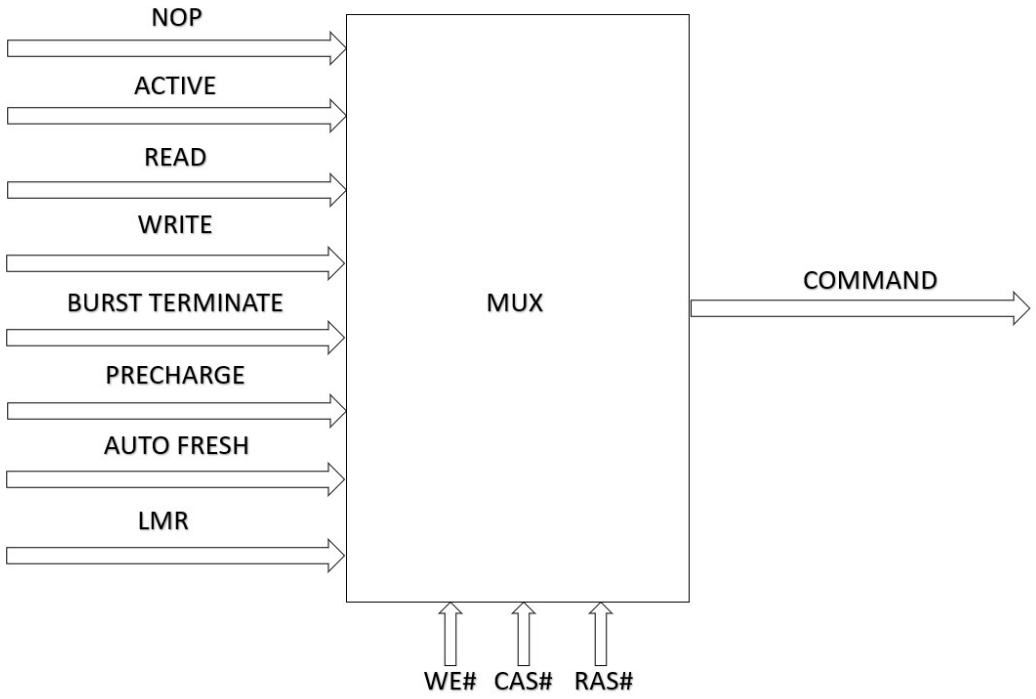
The signals of M/IO, ADS, and W/R are active low, and all of them are generated from CPU. These three signals decide SDRAM operation read or write.

M/IO	W/R	Result
1	1	Memory Read
1	0	Memory Write

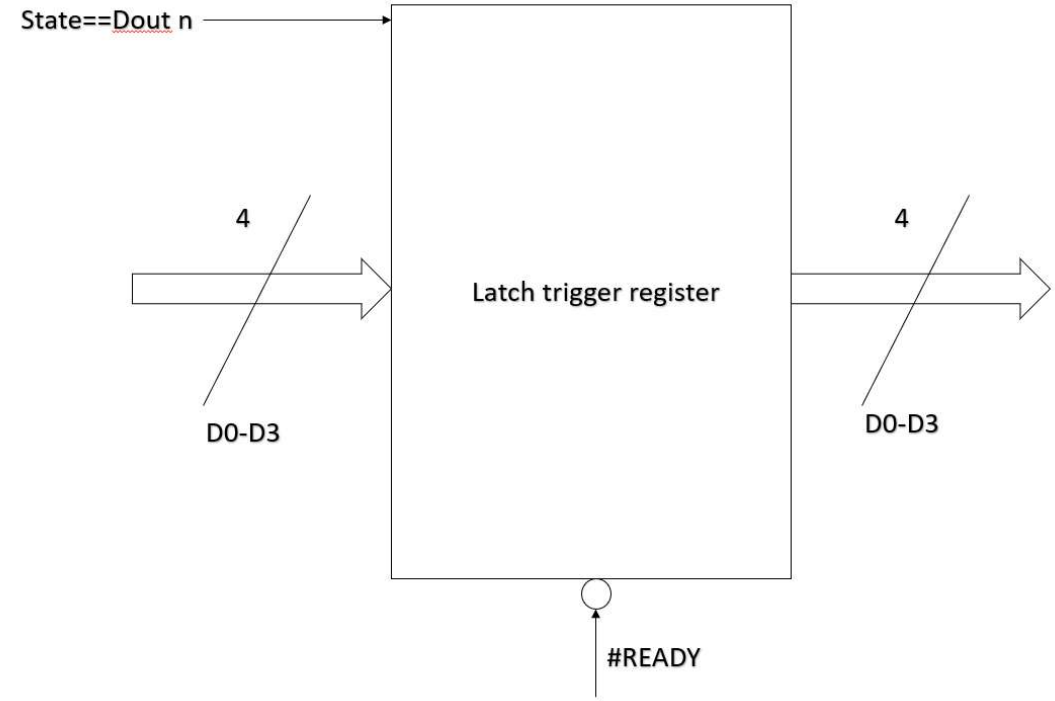
Command Signal table:

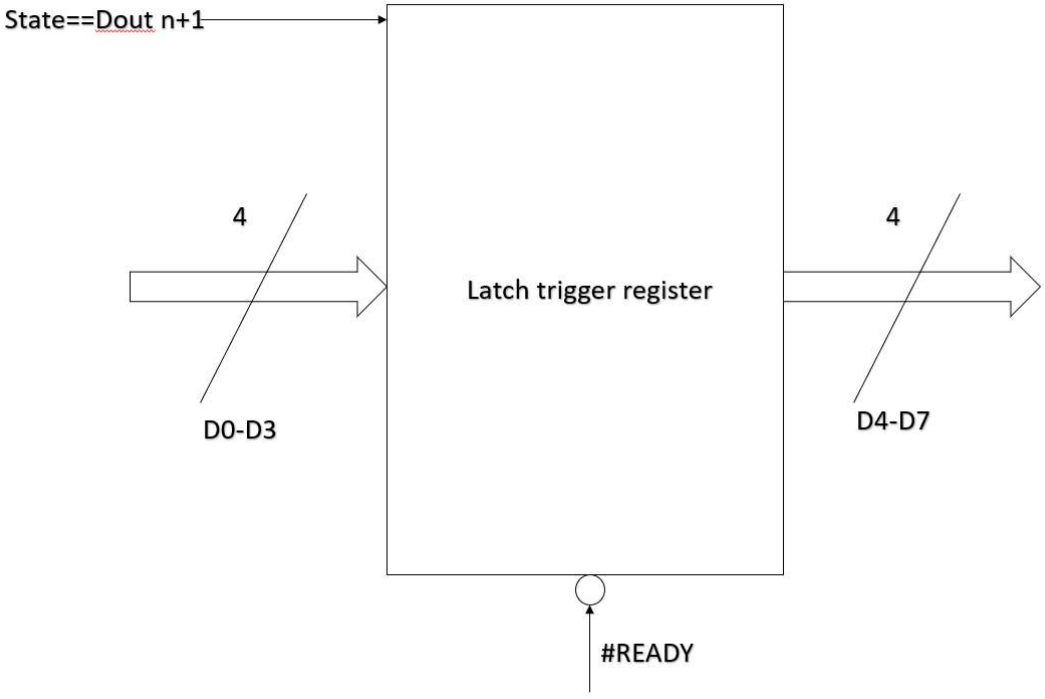
Name (Function)	CS#	RAS#	CAS#	WE#
COMMAND INHIBIT (NOP)	H	X	X	X
NO OPERATION (NOP)	L	H	H	H
ACTIVE (Select bank and activate row)	L	L	H	H
READ (Select bank and column, and start READ burst)	L	H	L	H
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L
BURST TERMINATE	L	H	H	L
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L
AUTO REFRESH or SOFT REFRESH (Enter self refresh mode)	L	L	L	H
LOAD MODE REGISTER	L	L	L	L

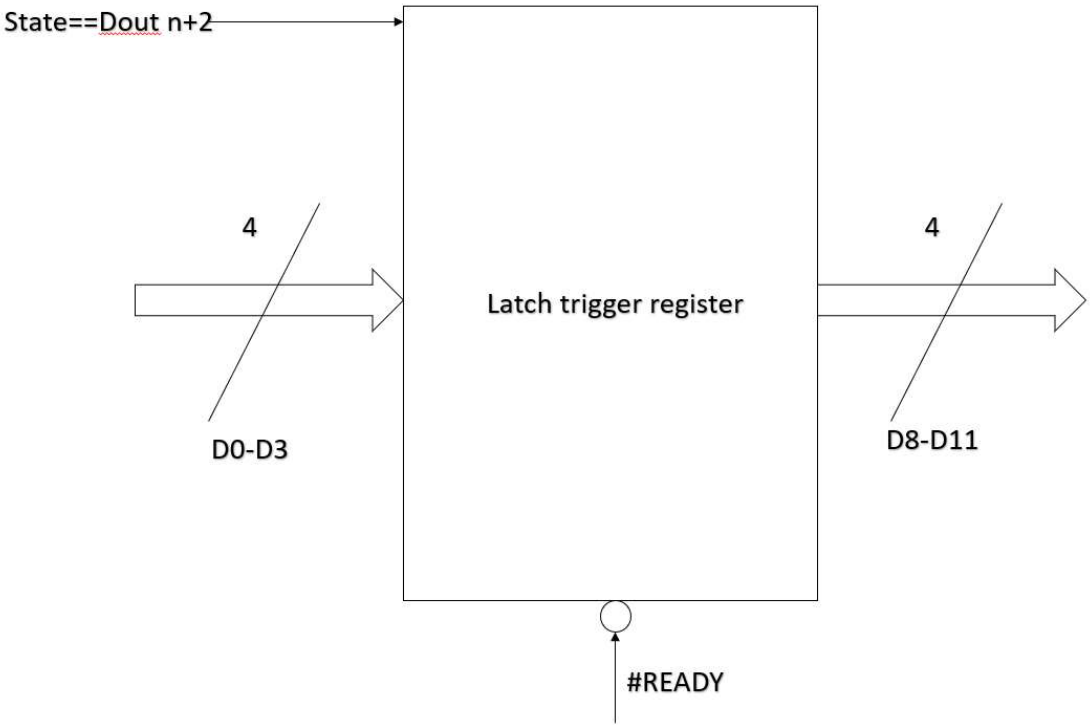
Command signal design:

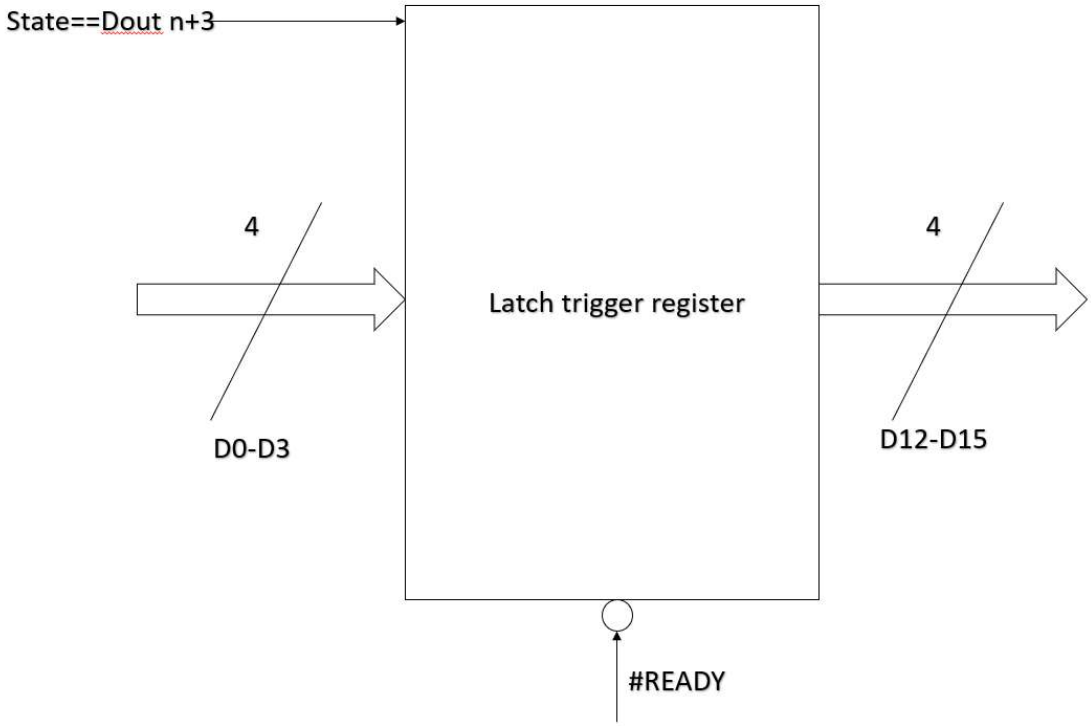


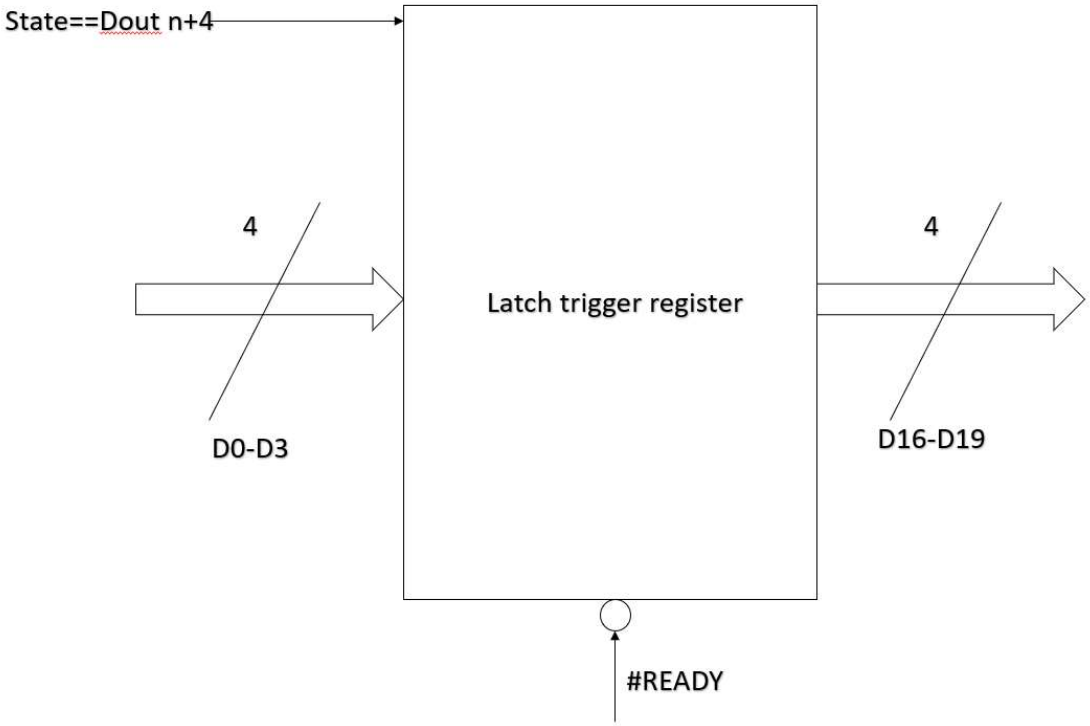
During the different state, the register will output the D0 to D3 depending on the state.

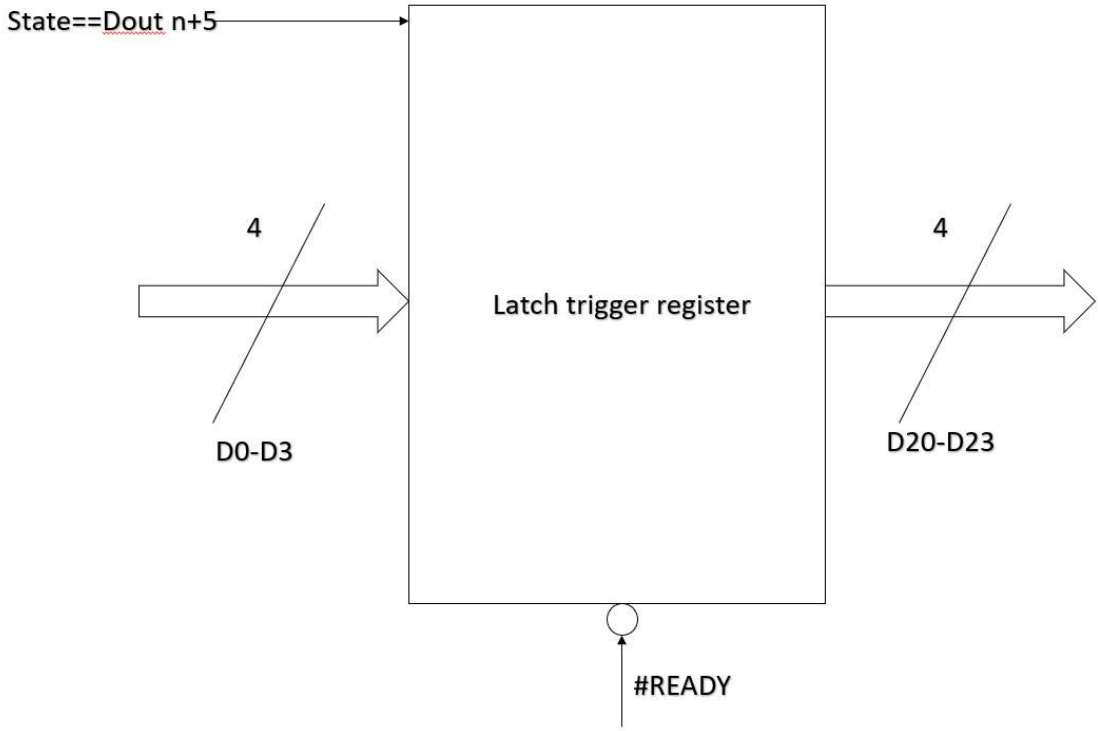


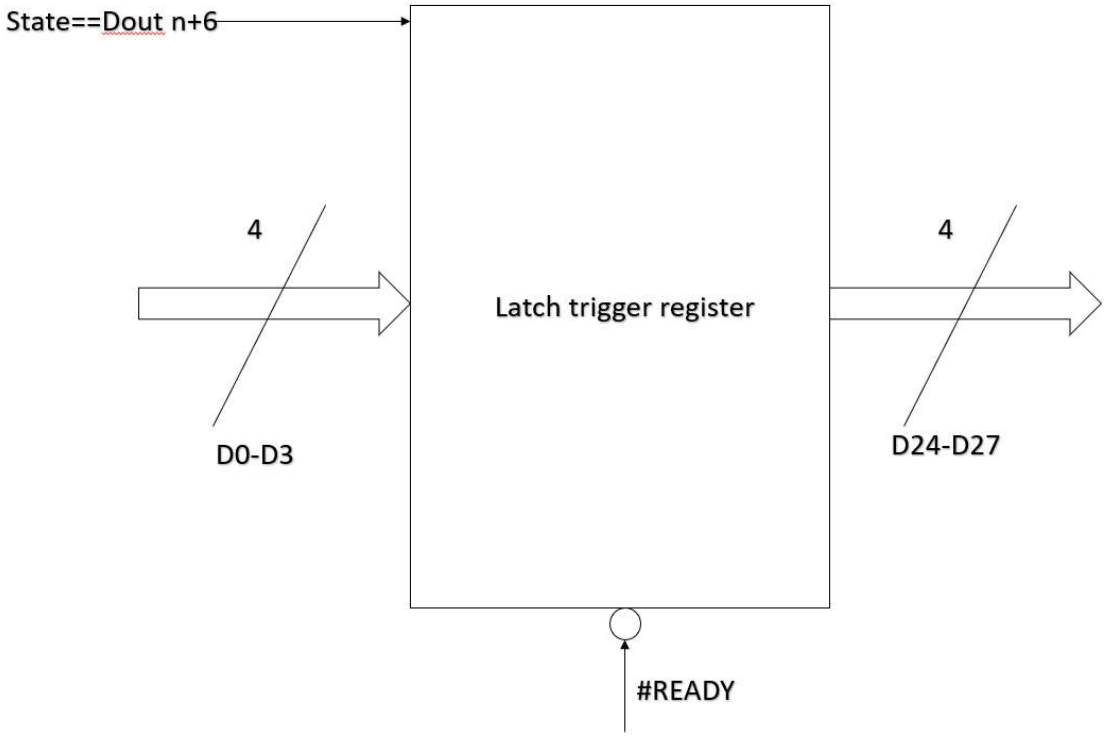


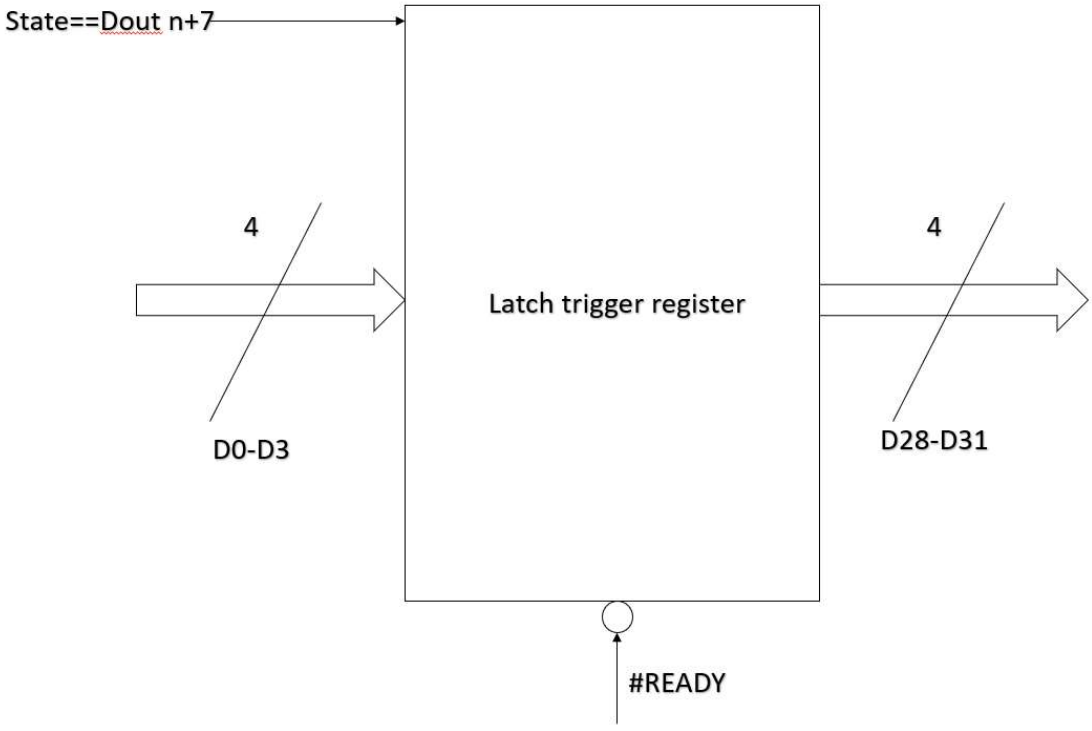

State==Dout n+2
4
Latch trigger register
4
D0-D3
D8-D11
#READY


State==Dout n+3
4
Latch trigger register
4
D0-D3
D12-D15
#READY

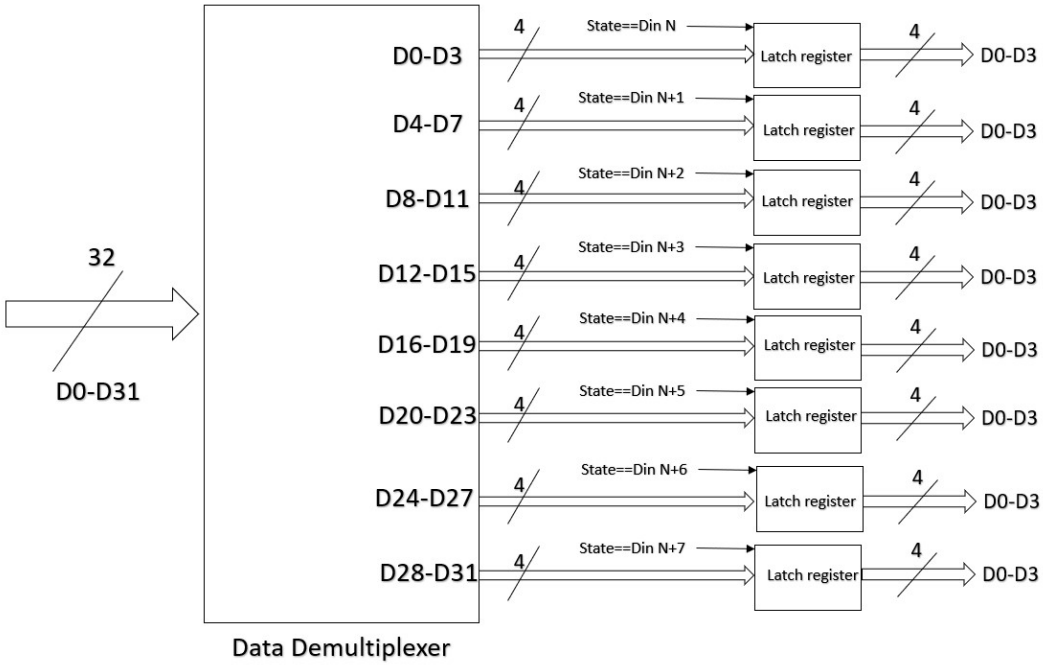

State==Dout n+4
4
Latch trigger register
4
D0-D3
D16-D19
#READY

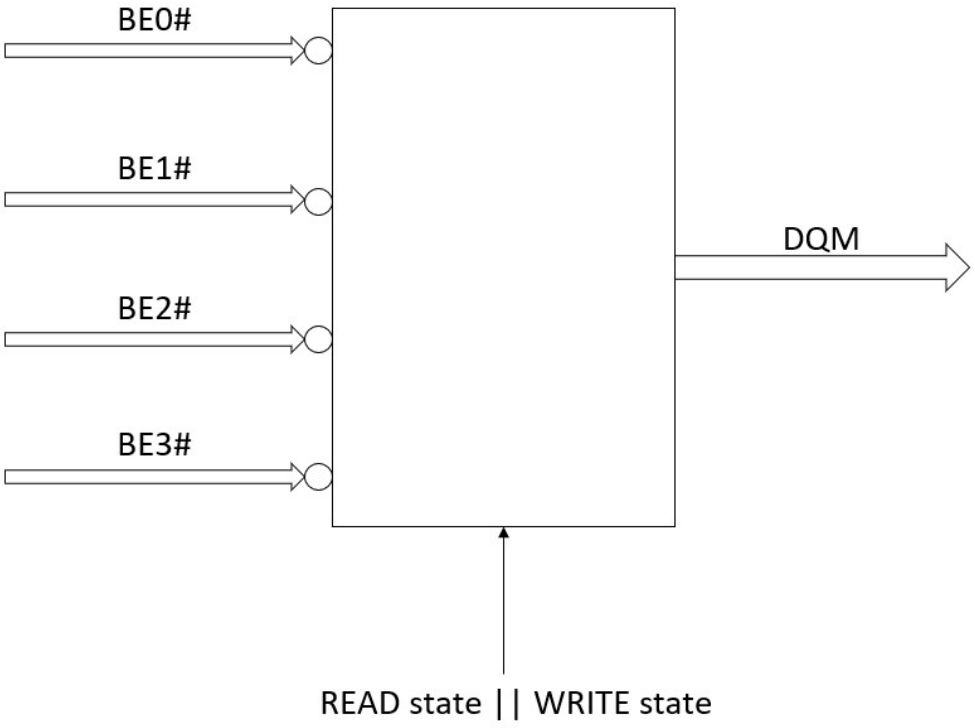

State==Dout n+5
4
Latch trigger register
4
D0-D3
D20-D23
#READY


State==Dout n+6
4
Latch trigger register
4
D0-D3
D24-D27
#READY


State==Dout n+7
4
Latch trigger register
4
D0-D3
D28-D31
#READY

During the writing process, we design a data demultiplexer, Which is to demultiplex D0-D31 to different D0-D3.

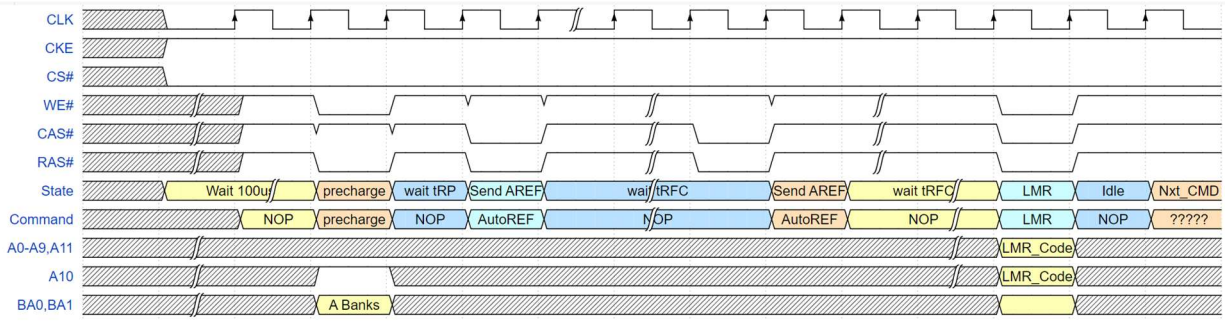




BE0-BE3 are signals that come from 80386X. They are D0-D7, D8-D15, D16-D23, D24-D31 respectively.

Timing Diagrams:

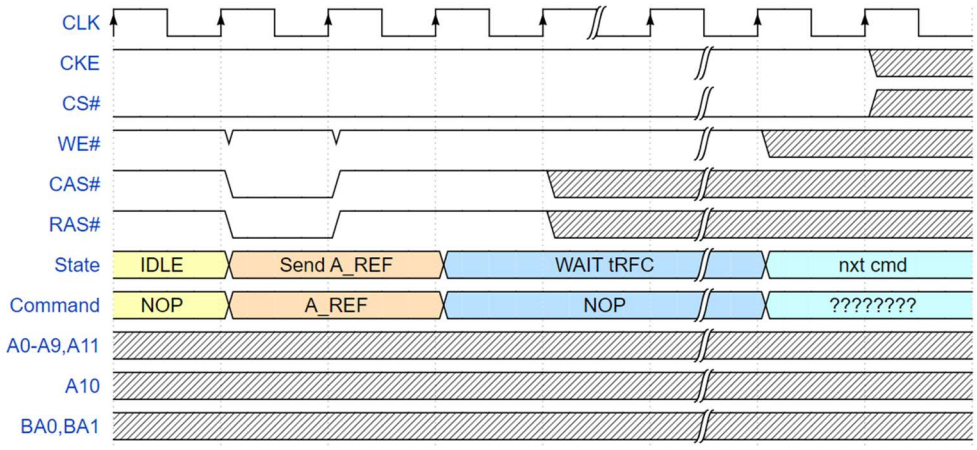
Initialization:



Clock Cycles and Timings:

- Note: For -7E speed grade, the cycle time is 7.5ns.
- Before issuing any command, we have to wait for **100us**. Also, 100us / 7.5ns is 13330 clock cycles. Thus, is it takes *13330 clock cycles*.
- For PRECHARGE (tRP), it takes **15ns** which is *2 clock cycles*.
- For AUTOREFRESH (tRFC), it takes **66ns**. So, it takes *9 clock cycles*. Since we issue it twice, it takes *18 clock cycles* on the whole.
- For LMR: LOAD_MODE_REGISTER (tMRD), the time is **15ns**. Thus, it takes *2 clock cycles*.

Auto Refresh:



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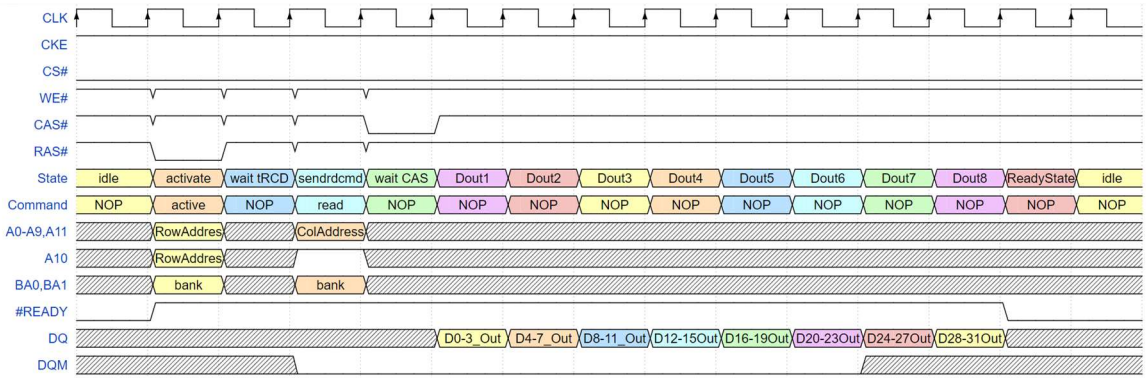
SDRAM Read:



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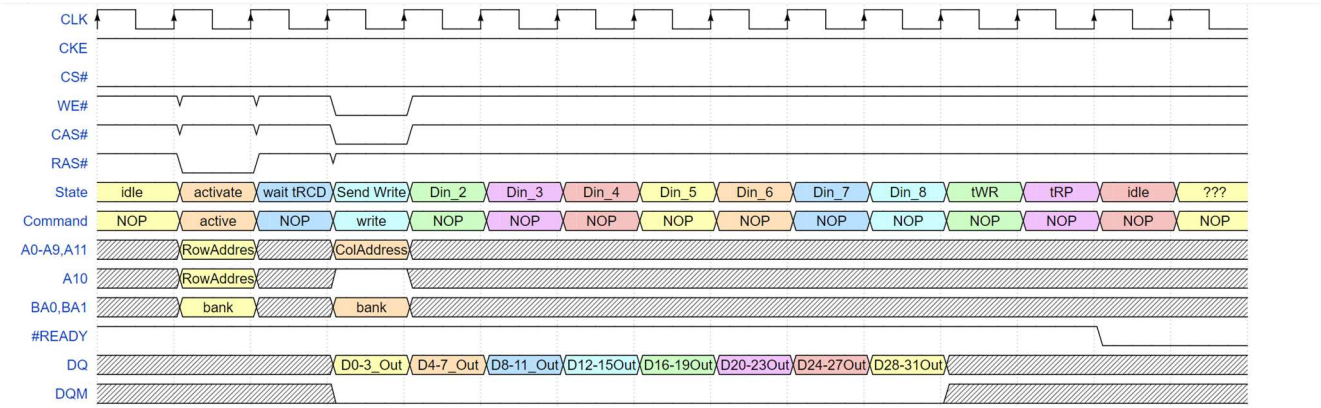
- For AUTOREFRESH (tRFC), it takes **66ns**. So, it takes *9 clock cycles*. Since we issue it twice, it takes *18 clock cycles* on the whole.
- For CAS LATENCY (Wait_CL), it takes **15ns** which is *2 clock cycles*.
- For Active to Read/Write delay (tRCD), the time is **15ns**. Thus, it takes *2 clock cycles*.

SDRAM Write:



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- Note: For -7E speed grade, the cycle time is 7.5ns.
- For PRECHARGE (tRP), it takes **15ns** which is *2 clock cycles*.
- For AUTOREFRESH (tRFC), it takes **66ns**. So, it takes *9 clock cycles*. Since we issue it twice, it takes *18 clock cycles* on the whole.
- For Active to Read/Write delay (tRCD), the time is **15ns**. Thus, it takes *2 clock cycles*.
- For Write Recovery Time (tWR), the time taken is **15ns**. Thus, it takes *2 clock cycles*.