	ITER, SIKSHA 'O' ANUSANDHAN **Deemed to be University**		**LESSON PLAN**
Programme	**B.Tech.**	Academic Year	**2023-24**
Department	**CSE/CSIT/CYSC/AIML/DASC/CIOT**	Semester	**3rd**
Instructor	**Dr. ARYA TRIPATHY**	Grading Pattern	**1**
Subject Code	**EET 1211**		
Subject Name	**Digital Logic Design**		

Text Books(s):

(1) Fundametals of Logic Design by Roth, Kinney and Raghunandan, Cengage.

Course Format: 3 Classes/week, 1 hr/Class; 1 Lab/Week,2 hr/Lab

Course Outcomes	Students will be able to	
	CO1	Able to State and explain different number systems, binary codes.
	CO2	Able to apply the principles of Boolean algebra, Karnaugh map and Quine-McCluskey Method to simplify logic expressions and implement it using gates.
	CO3	Able to Analyse and design various combinational circuits.
	CO4	Able to Analyse and design Memory and Programmable Logic Devices.
	CO5	Able to Analyse and understand latches, flip-flops, registers and counter operations.
	CO6	Able to implement various digital circuits using HDL and Standard ICs..

Lecture/ Lab)	**Lessons/Topics to be covered**	**Book reference (sections)**	**Mapping with COs**
Week #1:			
Lecture#1	Digital Systems and Switching Circuits.	1.1 (pg. 2-4)	**CO1**
Lecture#2	Number Systems and Conversion.	1.2 (pg.4-8)	**CO1**
Lecture#3	Binary Arithmetic and Representation of Negative Numbers	1.3-1.4 (pg.8-17)	**CO1**
Lab#1	Introduction to Different ICs.		**CO6**
Week #2:			

Lecture#4	Binary Codes.	1.5 (pg. 17-19)	**CO1**
Lecture#5	Introduction to Boolean Algebra.	2.1-2.3 (pg.26-30)	**CO2**
Lecture#6	Basic theorems	2.4-2.5 (pg.30-35)	**CO2**
Lab#2	Examine the operation of logic gates.		**CO6**
Week #3:			
Lecture#7	Simplification Theorems and Multiplying Out and Factoring	2.6-2.7 (pg.35-40)	**CO2**
Lecture#8	Complimenting Boolen Expression, Multiplying Out and Factoring Expressions	2.8,3.1 (pg.41-51)	**CO2**
Lecture#9	Exclusive-OR and Equivalence Operations. The Consensus Theorem	3.2-3.3 (pg. 51-54	**CO2**
Lab#3	Examine and analyze the gate level minimization for boolean function.		**CO6**
Week #4:			
Lecture#10	Algebraic Simplification of Switching Expressions and Proving Validity of an Equation.	3.4-3.5 (pg.55-64)	**CO2**
Lecture#11	Conversion of English Sentences to Bollean Equations, Canonical Form and Generation of switching Equation from truth table	4.1-4.3 (pg.70-77)	**CO2**
Lecture#12	General Minterm and Maxterm Expansions.Incompletely Specified Functions.	4.4-4.5 (pg.77-81)	**CO2**
Lab#4	Design of multilevel NAND gate circuits.		**CO6**
Week #5:			
Lecture#13	Examples of Truth Table Construction	4.6 (pg.81-84)	**CO2**
Lecture#14	Two and Three-Variable Karnaugh Maps	5.2 (pg.96-100)	**CO2**
Lecture#15	Four-Variable Karnaugh Maps.	5.3 (pg.100-103)	**CO2**
Lab#5	Design of multilevel NOR gate circuits.		**CO6**
Week #6:			

Lecture#16	Determination of Minimum Expressions Using Essential Prime Implicants	5.4 (pg.103-108)	**CO2**
Lecture#17	Design of Binary Adder and Subtractor	9.9 (pg.233-240)	**CO2**
Lecture#18	Binary Comparator.	9.10 (pg.240-246)	**CO2**
Lab#6	Construct and test various binary adder and subtractor circuits.		**CO6**
Week #7:			
Lecture#19	Five-Variable Karnaugh Maps.	5.5 (pg.108-111)	**CO2**
Lecture#20	Determination of Prime Implicants and the Prime Implicant Chart.	6.1-6.2 (pg.128-134)	**CO2**
Lecture#21	Petrick's Method, Simplification of Incompletely Specified Functions and Simplification Using Map-Entered Variables .	6.3-6.5 (pg.134-142)	**CO2**
Lab#7	Introduction to VHDL		**CO6**
Week #8:			
Lecture#22	Multi-Level Gate Circuits, NAND and NOR Gates.Design of Two-Level NAND- and NOR-Gate Circuits	7.1-7.3 (pg.148-157)	**CO2**
Lecture#23	Design of Multilvel-Level NAND and NOR-Gate Circuits.Circuit Conversion Using Alternative Gate Symbols	7.4-7.5 (pg.157-162)	**CO2**
Lecture#24	Review of Combinational Circuit Design. Design of Circuits with Limited Gate Fan-In.	8.1-8.2 (pg.176-179)	**CO3**
Lab#8	Design, construct and test the combinational circuit to solve a given problem.		**CO6**
Week #9:			

Lecture#25	Gate Delays and Timing Diagrams.Hazards in Combinational Logic. Simulation and Testing of Logic Circuits.	8.3-8.5 (pg.179-190)	**CO3**
Lecture#26	Multiplexers.	9.1-9.2 (pg.202-211)	**CO3**
Lecture#27	Three-State Buffers.Decoders and Encoders.	9.3-9.4 (pg.212-217)	**CO3**
Lab#9	Design of Encoder, Decoder and Multiplexer circuits.		**CO6**
Week #10:			
Lecture#28	Read-Only Memories.	9.5 (pg.217-222)	**CO4**
Lecture#29	Programmable Logic Devices.	9.6 (pg.222-227)	**CO4**
Lecture#30	Complex Programmable Logic Devices.Field-Programmable Gate Arrays.	9.7-9.8 (pg.227-233)	**CO4**
Lab#10	Design of Programmable Logic Devices.		**CO6**
Week #11:			
Lecture#31	VHDL Description of Combinational Circuits. VHDL Models for Multiplexers. VHDL Modules.	10.1-10.3 (pg.258-270)	**CO6**
Lecture#32	Signals and Constants. Arrays.VHDL Operators.	10.4-10.6 (pg.270-276)	**CO6**
Lecture#33	Packages and Libraries. IEEE Standard Logic.	10.7-10.8 (pg.276-281)	**CO4**
Lab#11	Digital System Design .		**CO6**
Week #12:			

Lecture#34	Set-Reset Latch. Gated Latches.	11.1-11.3 (pg.294-304)	**CO5**
Lecture#35	D, S-R and J-K Flip-Flop.	11.4-11.6 (pg.304-310)	**CO5**
Lecture#36	T Flip-Flop.Flip-Flops with Additional Inputs. Asynchronous Sequential Circuits	11.7-11.9 (pg.310-317)	**CO5**
Lab#12	Construct, test and investigate the operation of various flip-flop circuits.		**CO6**
Week #13:			
Lecture#37	Registers and Register Transfers, Shift Registers, Binary Ripple Counter.	12.1-12.3 (pg.332-343)	**CO5**
Lecture#38	Design of Synchronous Binary Counters. Counters for Other Sequence	12.4-12.5 (pg.343-355)	**CO5**
Lecture#39	Synchronous Counter Design Using S-R and J-K Flip-Flops. Derivation of Flip-Flop Input Equations.	12.6-12.7 (pg.355-362)	**CO5**
Lab#13	Construct, test and investigate the operation of shift register and counter circuits.		**CO6**