8 - BIT ALU

Satyajeet Padhy
Department of Electronics Engineering,
National Institute of Technology, Rourkela
padhysatyajeet@gmail.com

Abstract - This project implements an 8-bit Arithmetic Logic Unit (ALU) designed and verified at the MOSFET (transistor) level in esim. The ALU performs eight operations selected by a 3-bit control word (S2 S1 S0): OR, XNOR, XOR, AND, INC, ADD, DEC, and SUB (see table below). All basic logic gates (NOT, OR, XOR, XNOR, AND) and 2:1 multiplexers were realized as discrete MOSFET circuits using 180 nm technology with Vdd = 5 V; those gates were used as building blocks to create half-adders / half-subtractors and the multi-bit datapath. Multi-bit operations are implemented by replicating the bit-slice circuitry across 8 bits and by appropriate carry handling for arithmetic results. The design includes a dedicated carry flag (MSB) logic so that operations that produce results wider than 1 bit present their MSB as a carry flag; for purely bitwise logical ops the carry flag is forced to 0. Functional verification (opcode sweeps and representative vectors) was performed in esim; schematics and waveforms are included in the report. (Report formatting follows the provided example.)

Index Terms – CMOS.

I. Circuit Details

The 8-bit ALU was designed at the MOSFET level in esim using 180 nm CMOS technology with a supply voltage of 5 V. All basic logic gates such as NOT, OR, AND, XOR, and XNOR were first implemented using MOSFET transistors and then combined to form half adders (using XOR and AND) and half subtractors (using XOR, AND, and NOT). These were used to build the arithmetic operations of the ALU. The ALU performs eight operations—OR, XNOR, XOR, AND, increment, addition, decrement, and subtraction—selected by the control inputs Sel2 Sel1 Sel0. For increment and decrement, one input was tied to Vdd = 5 V. The selection between the eight operations was achieved using an 8:1 multiplexer constructed from seven 2:1 MUXes, each implemented at the MOSFET level. The carry flag was generated from the MSB of the arithmetic operations using a combination of 4:1 and 2:1 MUXes, while for logical operations the carry was forced to zero. This modular and transistor-level implementation ensures accurate realization of logic and arithmetic functions in CMOS technology.

TABLE I. TRUTH TABLE OF ALU

S_2	S_1	S_0	OPERATION
0	0	0	OR
0	0	1	XNOR
0	1	0	XOR
0	1	1	AND
1	0	0	INCREMENT
1	0	1	ADDITION
1	1	0	DECREMENT
1	1	1	SUBTRACTION

Table 1: Truth table of ALU

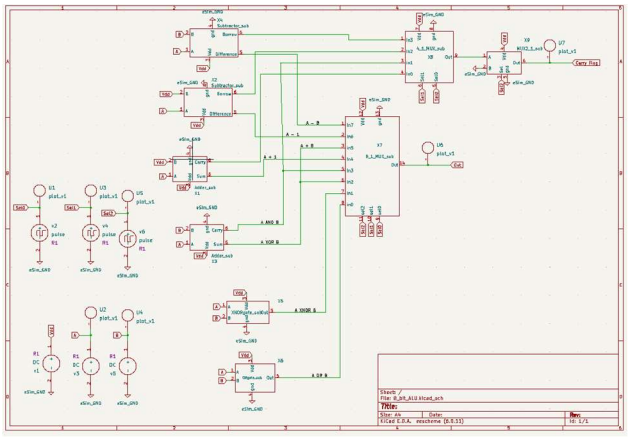
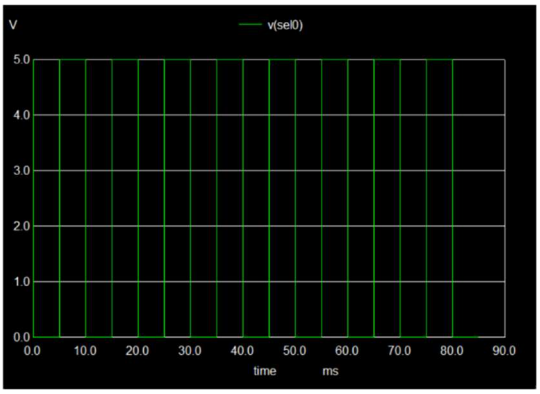
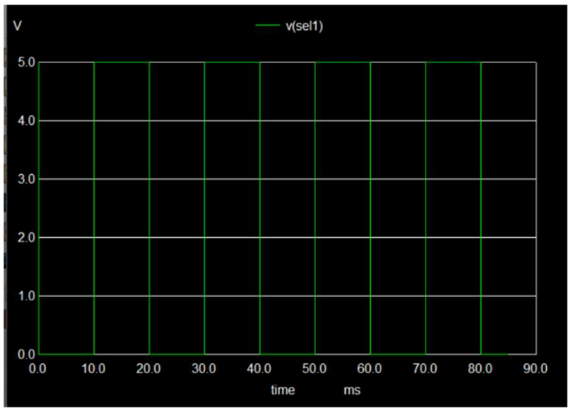
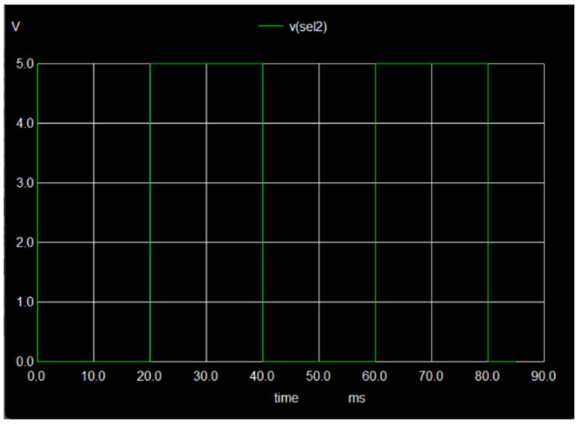
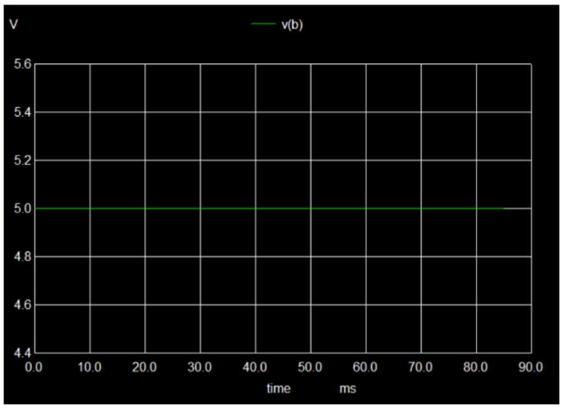


Figure 1: Implemented circuit diagram.









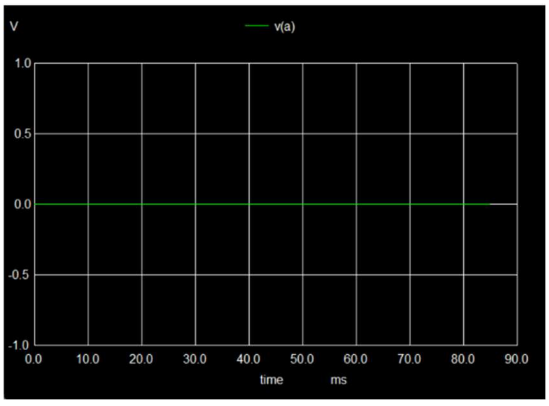
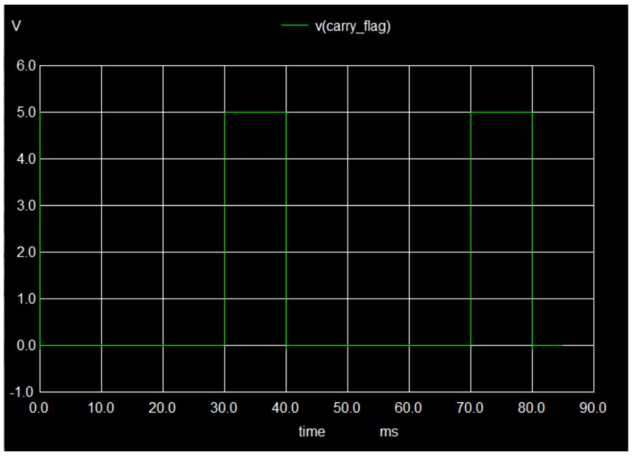


Figure 2: Implemented waveform
Select lines(sel0,sel1,sel2) and Inputs(A,B)



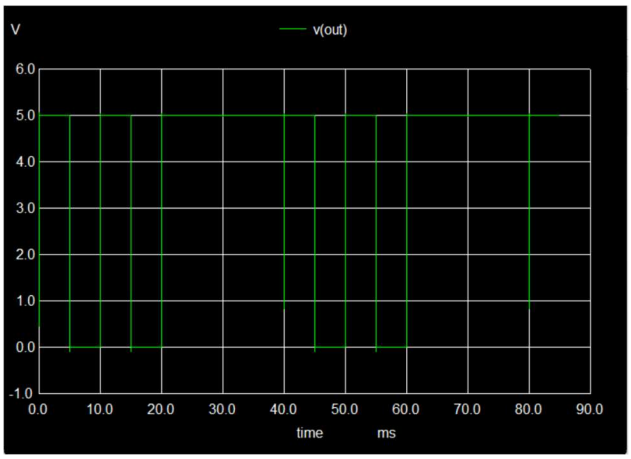


Figure 3: Implemented waveform(Output)

II. References

[1] Manit Kantawala, “Design and implementation of 8 bit and 16 bit ALU using Verilog language” in nternational Journal of Engineering Applied Sciences and Technology, 2018 Vol. 3, Issue 2, ISSN No. 2455-2143, Pages 30-34 Published Online June 2018 in IJEAST (http://www.ijeast.com)

[2] C.Arunabala, Ch. Jyothirmayi, D N S V Sreeja.T, Suma Burra, Hrithika Reddy Udumula, I.R.Anusha Devi, “Design of a 4 bit Arithmetic and Logical unit with Low Power and High Speed” in International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075 (Online), Volume-10 Issue-5, March 2021

Github Link to Repository :
https://github.com/padhysatyajeet/8-Bit-ALU