Performance Evaluation of 6T, 7T & 8T SRAM at 90 nm Technology

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***Abstract*— This article addresses the growing intricacy and power dissipation in high-speed systems with smaller technology by designing, simulating, and analyzing 6T, 7T, and 8T SRAM cells. Schematic drawing, layout modification, DRC, LVS are all done with the Cadence Virtuoso tool. Using gdpk90 technology, important dimensions including average power, propagation delay, power delay product, and cell size are assessed for SRAM cells. The simulations were run at 27°C consistently.**

Keywords*— SRAM, DRC, LVS, Propagation Delay, layout design, Average power.*

I. INTRODUCTION

Designing effective, low-power electronics is a difficult task because of the growing market for gadgets such as wireless devices, multimedia goods, and smartphones. For high-speed, high-density applications like cache memory, mobile devices, and cameras, SRAM is necessary since it has the benefit of storing data without refreshing when powered. Technology can be scaled down to use less dynamic power, space, and time. Leakage current and power dissipation can be reduced by employing strategies such as transistor stacking, supply voltage reduction, and high-threshold transistor use. Studies comparing 6T, 7T, and 8T SRAM cells show increases in power efficiency; improved designs dramatically boost performance and energy economy while cutting access time.

II. 6T SRAM

A. Operation of 6T SRAM

Two cross-coupled inverters and two access transistors are the components of a typical 6T SRAM memory cell. These components are utilized to read and write data stored at two internal nodes, P and Q. The bit line (BL) and bit line bar (BLB) are pre-charged to VDD during a read operation. Next, the access transistors NM3 and NM4 are turned "ON" via the word line (WL), which connects the internal nodes P and Q to the bit lines. When writing, the WL is also pushed high, enabling the writing of a '0' or a '1' to the memory cell, contingent on the starting states of nodes P and Q. The bit lines (BL and BLB) are left floating when the cell is in hold mode, and the WL stays OFF.

Sometimes, a rise in voltage at one of the internal nodes (P or Q) might cause failures in the read operation. This can then cause the other inverter to invert erroneously, resulting in a drop in voltage at the corresponding node (Q or P), which can eventually cause data loss. The schematic view of the 6t sram is given below:

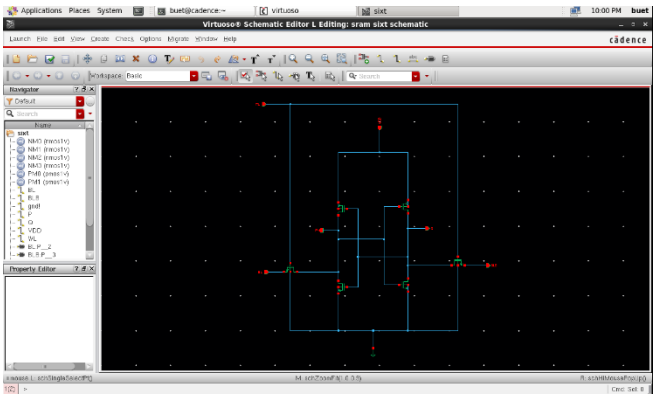

Fig 1: Schematic view of 6T SRAM

B. Transient Analysis of 6T SRAM

During the transient analysis of the 6T SRAM we considered the world line, bit line, bit line bar, vdd and ground to be inputs. And p and q to be outputs.

Fig 2: Transient Analysis of 6T SRAM

From here we can find the Propagation delay and the average power. Fig -3 and 4 shows that respectively.

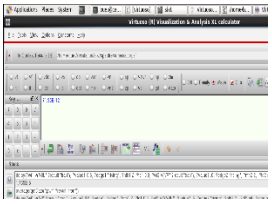

Fig 3: Propagation Delay

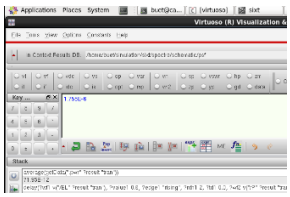

Fig 4: Average Power

Propagation Delay= 7.95×10^{-12}
Average Power =$1 \cdot 755 \times 10^{-6}$

From here we can also calculate the power delay product.
Power propagation delay= Propagation delay x Avg Power

$=7.95 \times 10^{-12}$ x $1 \cdot 755 \times 10^{-6}$
$= 1 \cdot 395 \times 10^{-17}$ Joules

C. *Layout of 6t SRAM*

The layout of a 6T SRAM is given below in figure 5. And the DRC and LVS check is also done for this particular 6T SRAM

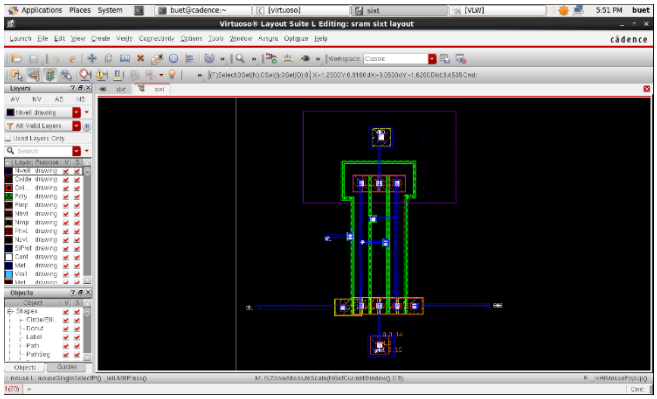

Fig 5: layout of 6T SRAM

The DRC and LVS check of the layout is given in figure 6 and 7 respectively.

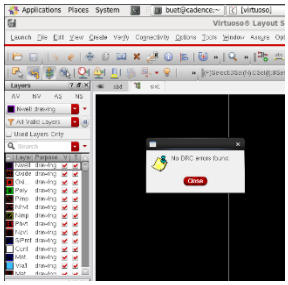

Fig 6: DRC check

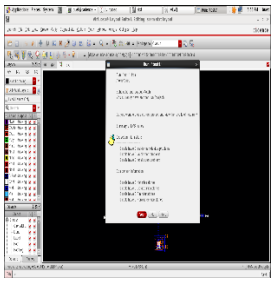

Fig 7: LVS check

We can see that there is no LVS and DRC error in the layout that we designed.

III. 7T SRAM

A. *Operation of 7T SRAM*

The schematic of 8T SRAM The 7T SRAM operates by using seven transistors to store a single bit of data. Six of the transistors form a pair of cross-coupled inverters that hold the data, while the seventh transistor is used to decouple the read and write operations. This extra transistor enhances read stability, ensuring data integrity during high-speed operations by isolating the read path, preventing accidental data flips during reads.

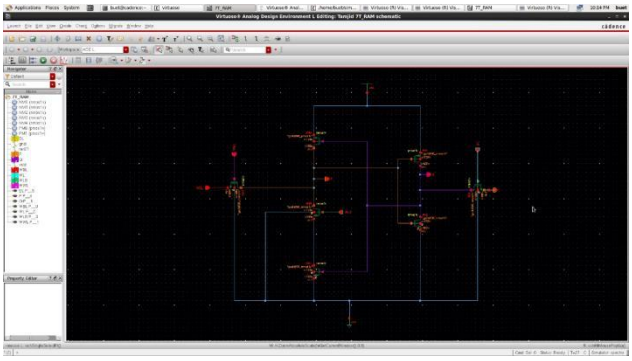

Fig 8: layout of 7T SRAM

B. *Transient Analysis of 7T SRAM*

During the transient analysis of the 7T SRAM we considered the world line, bit line, bit line bar, vdd and ground to be inputs. And P and Q to be outputs.

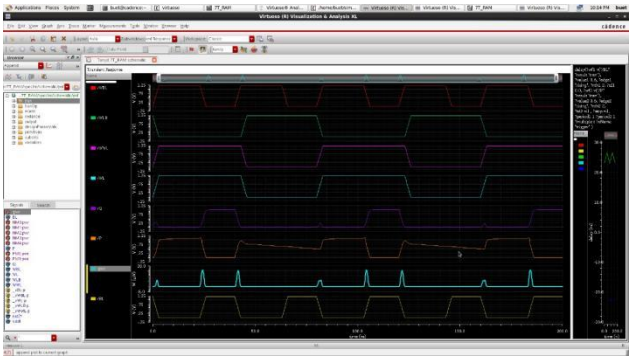

Fig 9: Transient Analysis of 7T SRAM

Here from the graph we calculated the propagation delay and average power

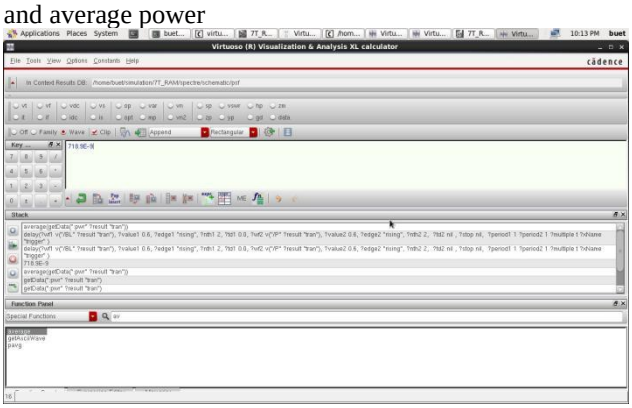

Fig 10: Average Power

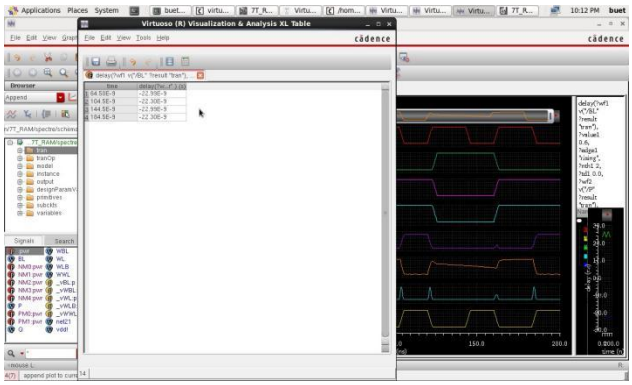

Fig 11: Propagation Delay

Propagation Delay = 22.99×10^{-9}
Average Power = 7.189×10^{-7}

From here we can also calculate the power delay product.
Power propagation delay= Propagation delay x Avg Power

$$= 22.99 \times 10^{-9} \times 7.189 \times 10^{-7}$$
$$= 1.65 \times 10^{-14} \text{ Joules}$$

C. *Layout of 7T SRAM*

The layout of a 7T SRAM is given below in figure 12 And the DRC and LVS check is also done for this particular 7T SRAM

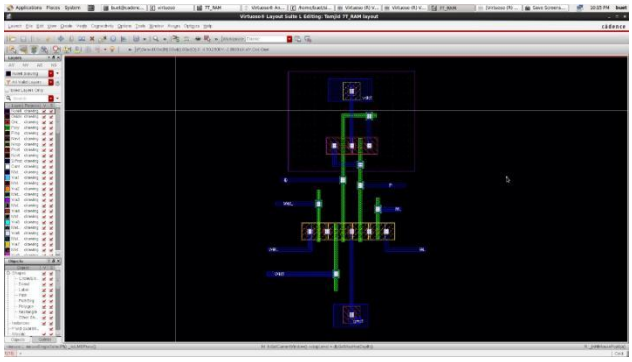

Fig 12: layout of 7T SRAM

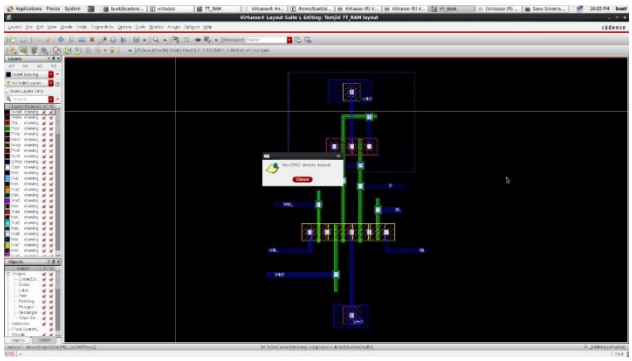

Fig 13: DRC check

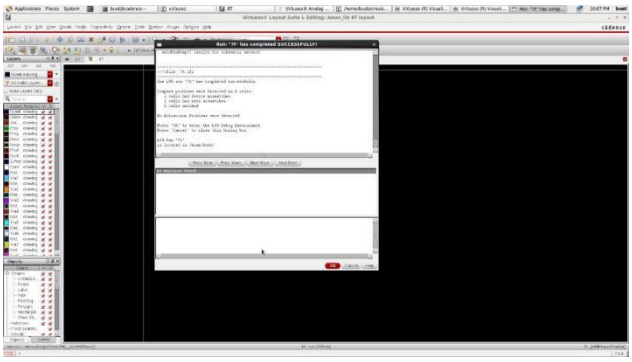

Fig 14: LVS check

We can see that there is no LVS and DRC error in the layout that we designed.

IV. 8T SRAM

A. *Operation of 8T SRAM*

The schematic of 8T SRAM memory cell, shown in Fig. 15, consists of two inverters connected back-to-back, two access transistors (NM2 & NM3) and a read buffer, that consists of two transistors (NM4 & NM5). During write operation word line WWL, bit line WBL and WBLB are used and RWL & RBL are used during read operation.

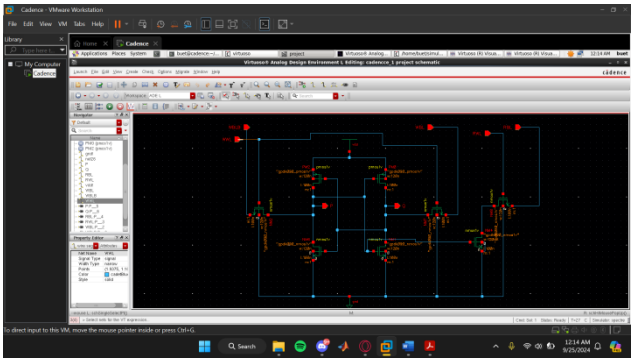

Fig 15: Schematic view of 8T SRAM

The RBL p recharged to VDD and the current flows through the transistor of read buffer, not through the internal nodes. So, the internal nodes remain at the same status as they are. The output waveform in Fig.7 depicts the transient and DC simulation for 8T SRAM cell along with dissipated power at room temperature. The result shows that it dissipates 10.55 µW dynamic power and 18.15 pW static power at the supply voltage of 1.8 V.

B. *Transient Analysis of 8T SRAM*

During the transient analysis of the 8T SRAM we considered the world line, bit line, bit line bar, vdd and ground to be inputs. And p and q to be outputs.

Fig 16: Transient Analysis of 8T SRAM

From here we can find the Propagation delay and the average power. Fig -3 and 4 shows that respectively.

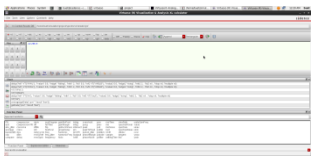

Fig 17: Propagation Delay

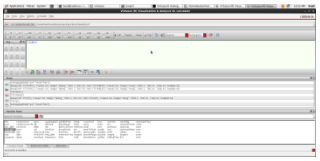

Fig 18: Average Power

Propagation Delay = -32.25×10^{-12}
Average Power = 2.325×10^{-6}

From here we can also calculate the power delay product.
Power propagation delay= Propagation delay x Avg Power

$=-32.25 \times 10^{-12}$ x 2.325×10^{-6}
$= 74.98 \times 10^{-17}$ Joules

C. Layout of 8T SRAM

The layout of a 8T SRAM is given below in figure 19. And the DRC and LVS check is also done for this particular 8T SRAM

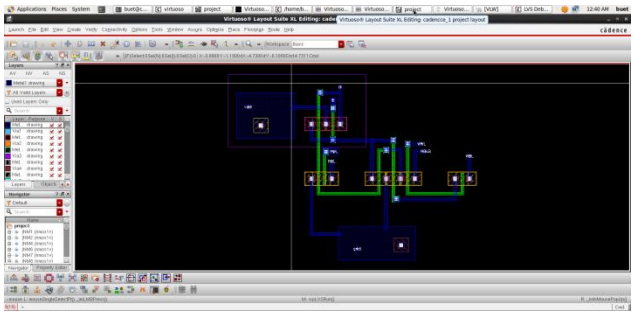

Fig 19: layout of 8T SRAM

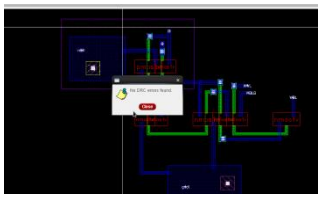

Fig 20: DRC check

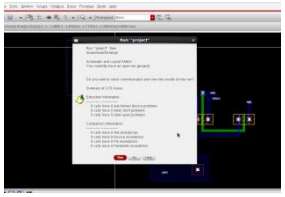

Fig 21: LVS check

We can see that there is no LVS and DRC error in the layout that we designed.

V. Comparison between different SRAMs

The comparison between 6T, 7T, and 8T SRAM shows that the 6T SRAM has the smallest area and is commonly used for basic memory designs. 7T SRAM offers improved dynamic power efficiency, with the least dynamic power consumption among the three, making it ideal for low-power applications. 8T SRAM provides better read stability but consumes the most dynamic power and occupies the largest area

VI. Conclusion

This paper highlights that schematic and layout designs of 6T, 7T, and 8T SRAM cells were created and analyzed. The 6T SRAM occupies the least area, while the 8T SRAM takes up the most space. Variations in power dissipation and delay were also observed as a function of supply voltage.