KWAME NKRUMAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONIC/ELECTRICAL ENGINEERING



MICROPROCESSOR DESIGN PROJECT

MICROPROCESSORS (COE 381)

GROUP 13

1. Emmanuel Kyeremeh - 8240519
2. Richard Ampofo - 8228919
3. Benecentia Mafo-Kwofie - 8241419
4. Brandon Idun-Tawiah - 8238419
5. Michael Acquah - 8225819
6. Rina Kusi Gyan - 8240119
7. Kwesi Asiedu Sarpong - 8246419
8. Paul Amoah - 8228719

ACKNOWLEDGEMENT

We would first of all like to thank the almighty God for taking us through this project. We would also like to thank ***Chris Nutsukpui*** and ***Dr. Jephthah Yankey*** for their very much appreciated assistance in the undertaking of this project.

TABLE OF CONTENTS

[1. SPECIFICATIONS 5](#_Toc103663996)

[1.1. COMPONENTS USED 5](#_Toc103663997)

[1.2. MEMORY AND ALU BUS SPECIFICATIONS 5](#_Toc103663998)

[2. THE ARCHITECTURE AND THE MICROARCHITECTURE 6](#_Toc103663999)

[2.1. INSTRUCTION CATEGORIES 6](#_Toc103664000)

[2.2. INSTRUCTION TYPES 6](#_Toc103664002)

[2.4. MEMORY LABELS 6](#_Toc103664003)

[2.5. A TYPE INSTRUCTIONS 7](#_Toc103664004)

[2.5.1. INSTRUCTION FORMAT 7](#_Toc103664005)

[2.5.2. DATAPATHS 7](#_Toc103664006)

[2.5.3. TRUTH TABLE 8](#_Toc103664007)

[2.6. B TYPE INSTRUCTIONS 8](#_Toc103664008)

[2.6.1. INSTRUCTION FORMAT 8](#_Toc103664009)

[2.6.2. DATAPATHS 9](#_Toc103664010)

[2.6.3. TRUTH TABLE 11](#_Toc103664011)

[2.7. C TYPE INSTRUCTIONS 11](#_Toc103664012)

[2.7.1. INSTRUCTION FORMAT 11](#_Toc103664013)

[2.7.2. DATAPATHS 12](#_Toc103664014)

[2.7.3. TRUTH TABLE 15](#_Toc103664016)

[2.8. COMBINED DATAPATHS 15](#_Toc103664017)

[2.9. COMPONENTS BUILT IN LOGISIM 16](#_Toc103664018)

[2.7.1. REGISTERFILE 16](#_Toc103664019)

[2.7.2. ALU 17](#_Toc103664020)

[2.7.3. A TYPE CONTROL UNIT 18](#_Toc103664021)

[2.7.4. B TYPE CONTROL UNIT 18](#_Toc103664022)

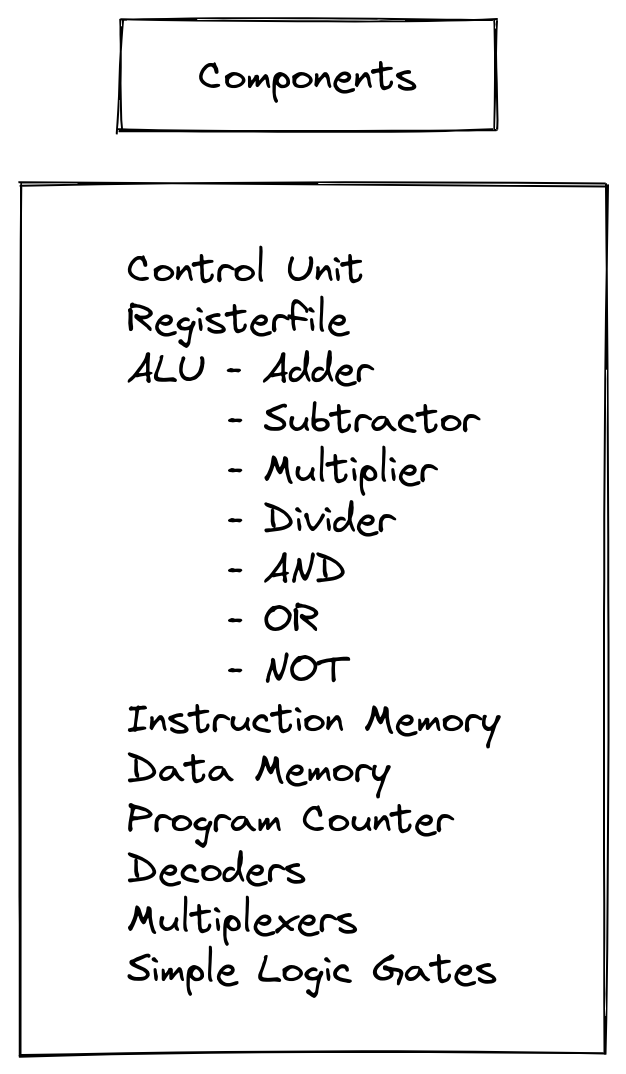
[2.7.5. C TYPE CONTROL UNIT 19](#_Toc103664023)

[2.7.6. COMBINED CONTROL UNIT 19](#_Toc103664024)

[2.7.7. COMPLETE MICROPROCESSOR CIRCUIT 20](#_Toc103664025)

# SPECIFICATIONS

## . COMPONENTS USED



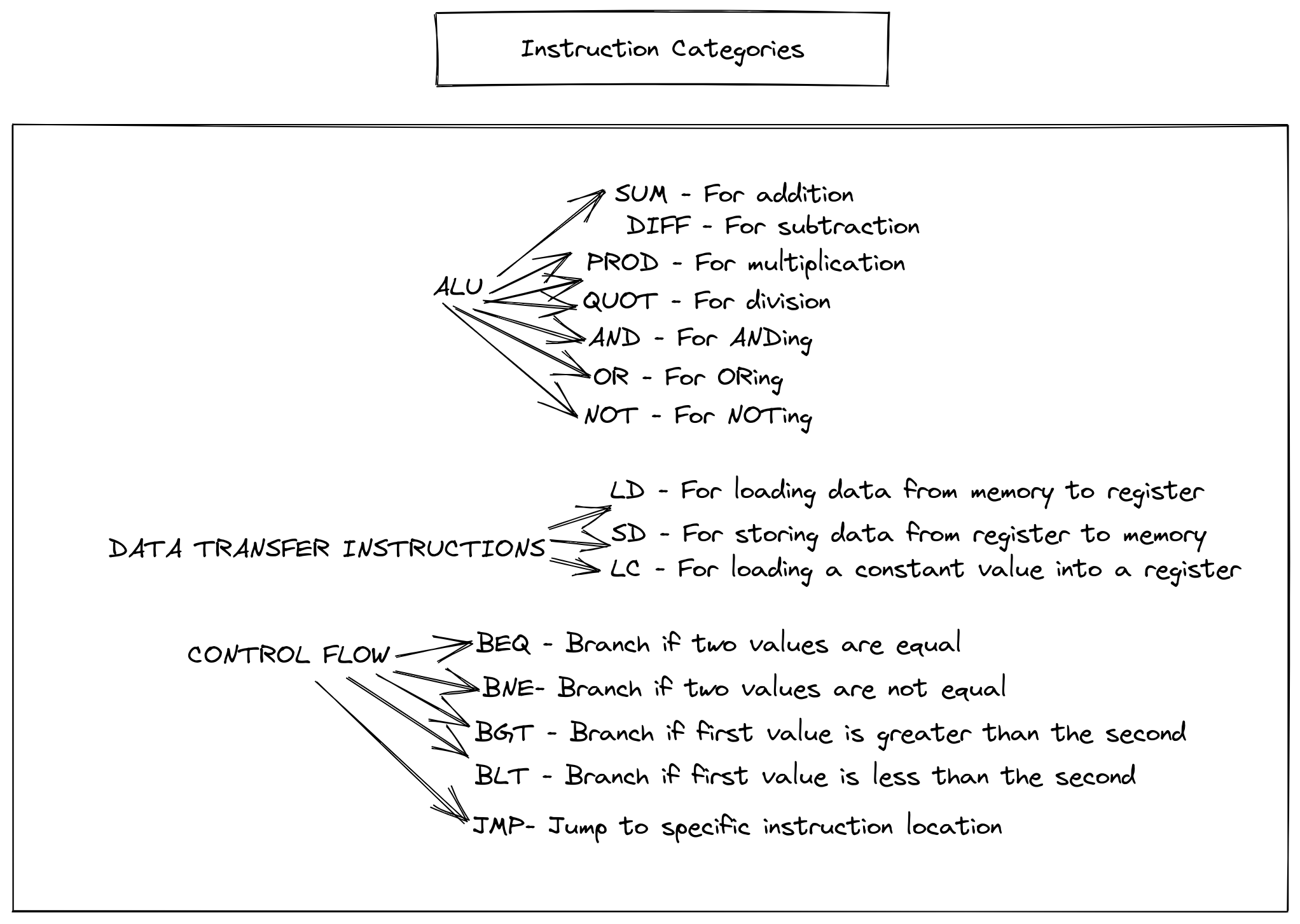
## 1.2. MEMORY AND ALU BUS SPECIFICATIONS



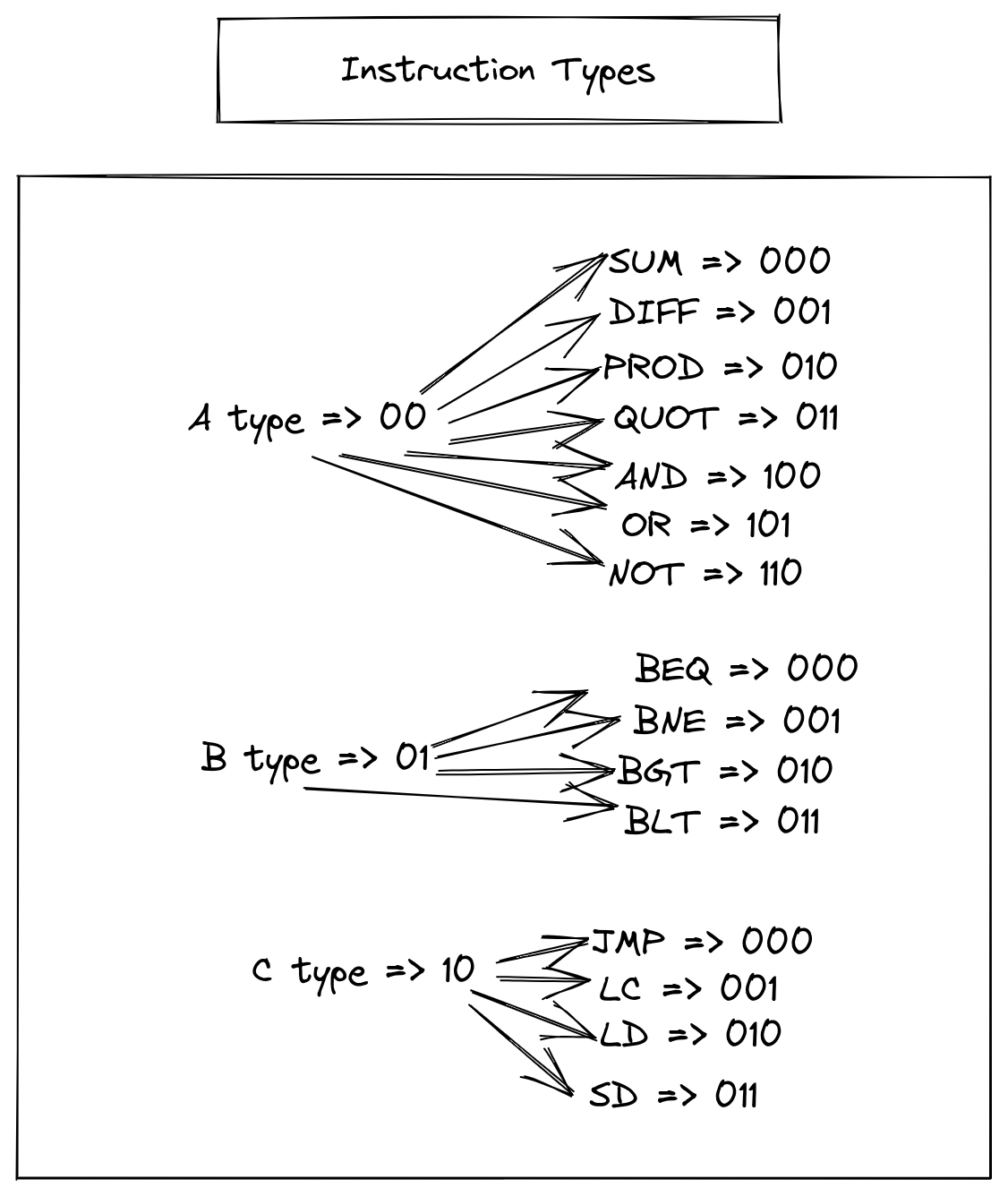
# THE ARCHITECTURE AND THE MICROARCHITECTURE

## 2.1. INSTRUCTION CATEGORIES

## 



## 2.2. INSTRUCTION TYPES

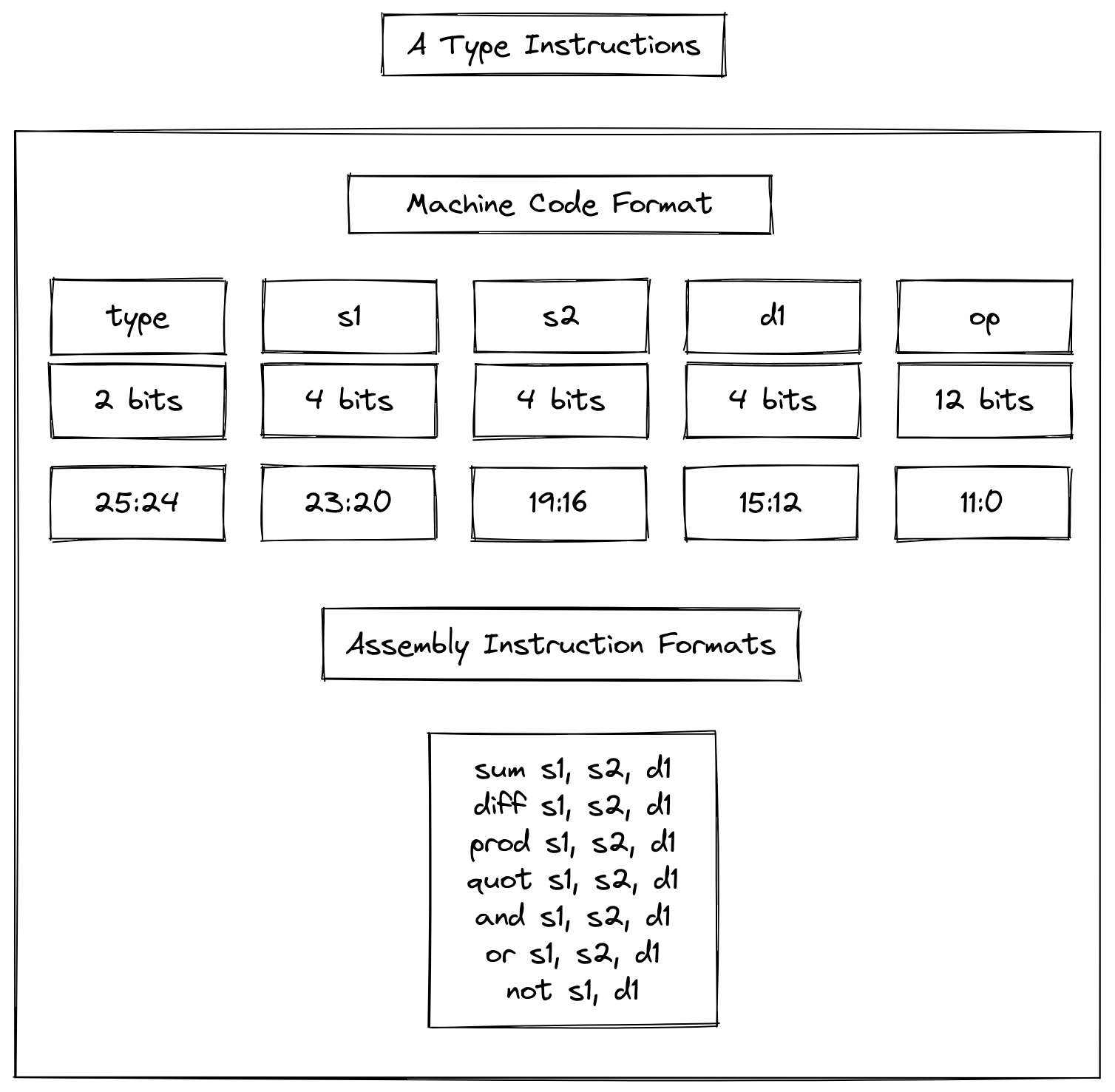


## 2.4. MEMORY LABELS

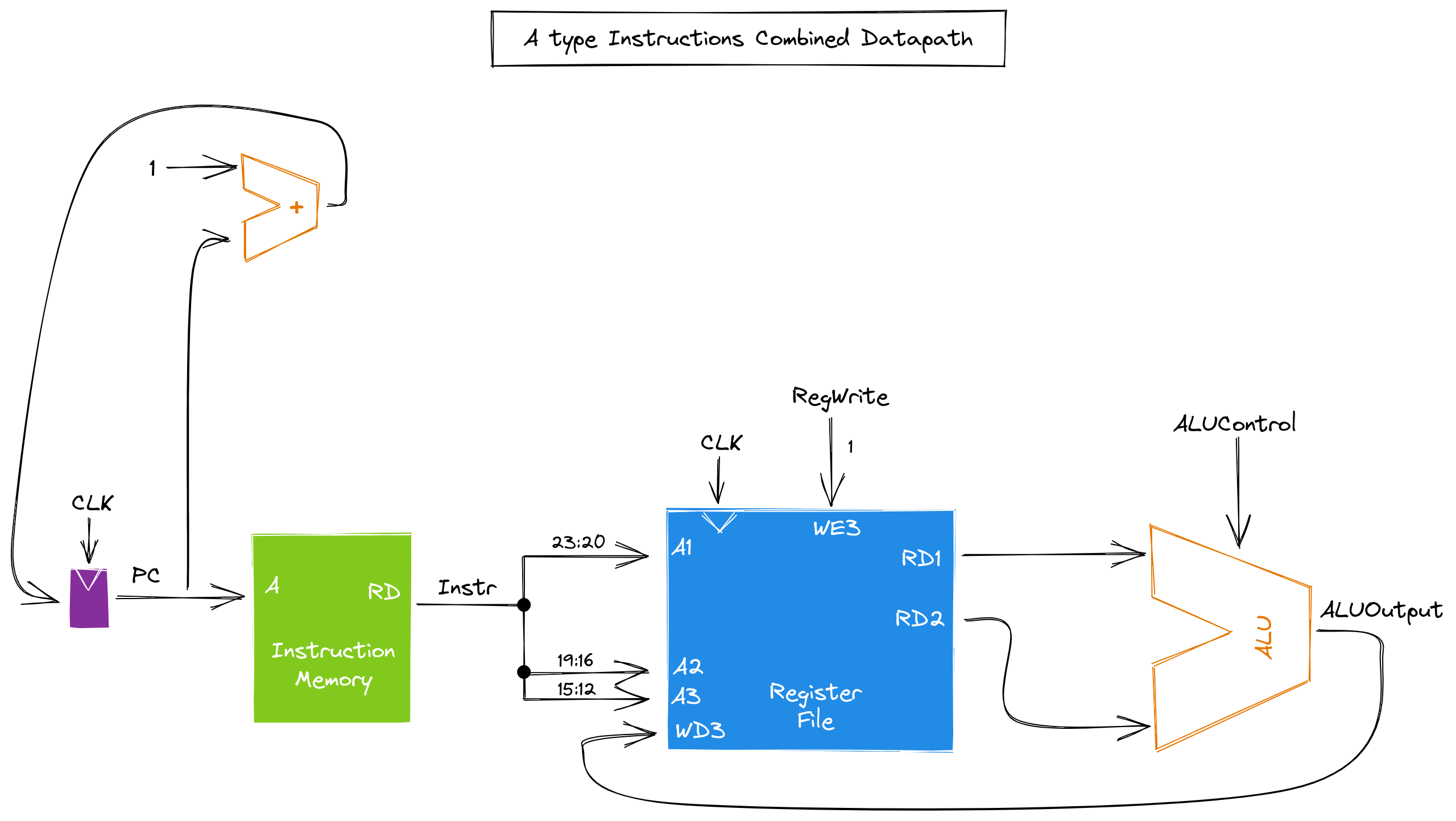


## 2.5. A TYPE INSTRUCTIONS

### 2.5.1. INSTRUCTION FORMAT



### 2.5.2. DATAPATHS

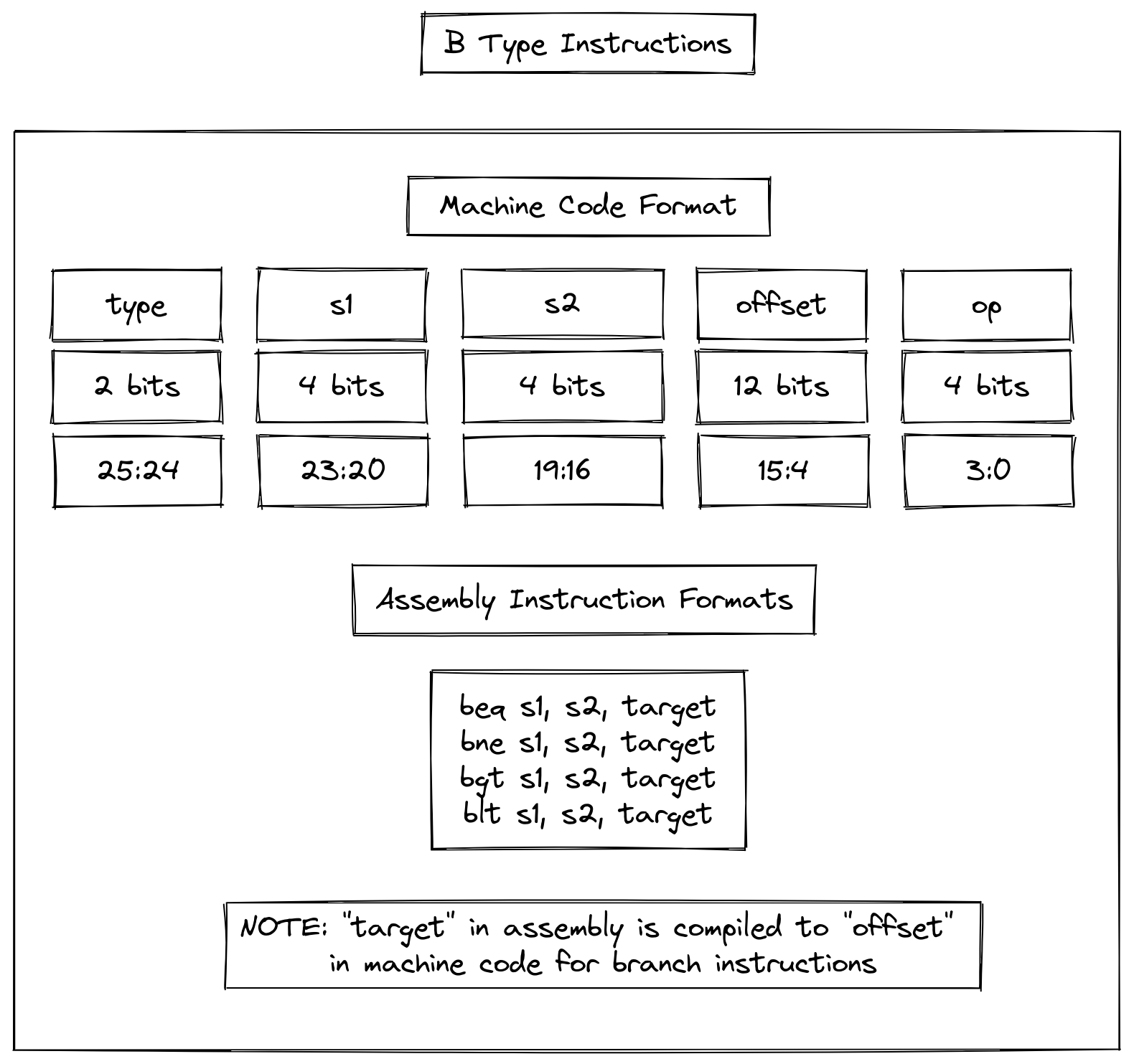


### 2.5.3. TRUTH TABLE

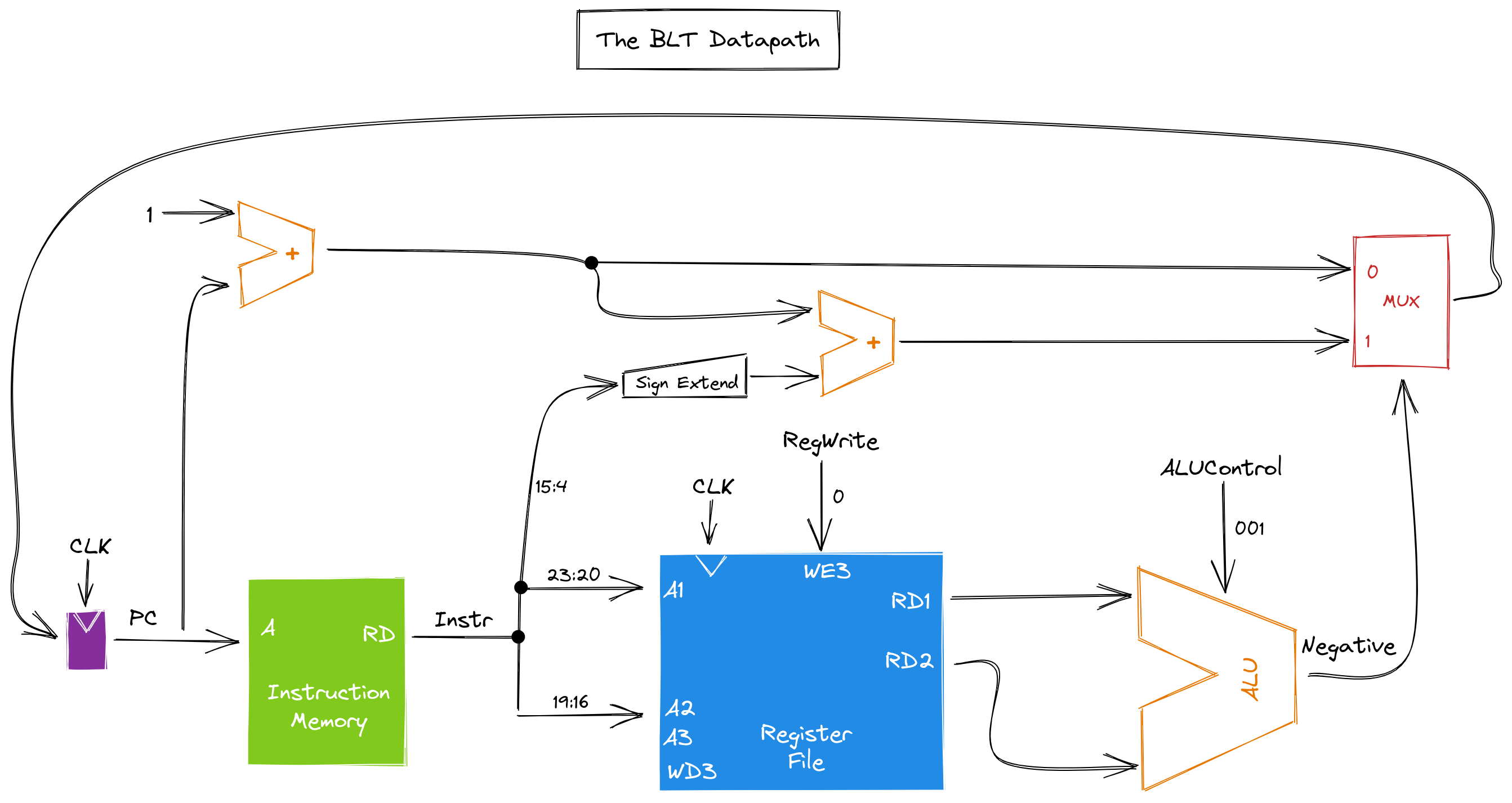
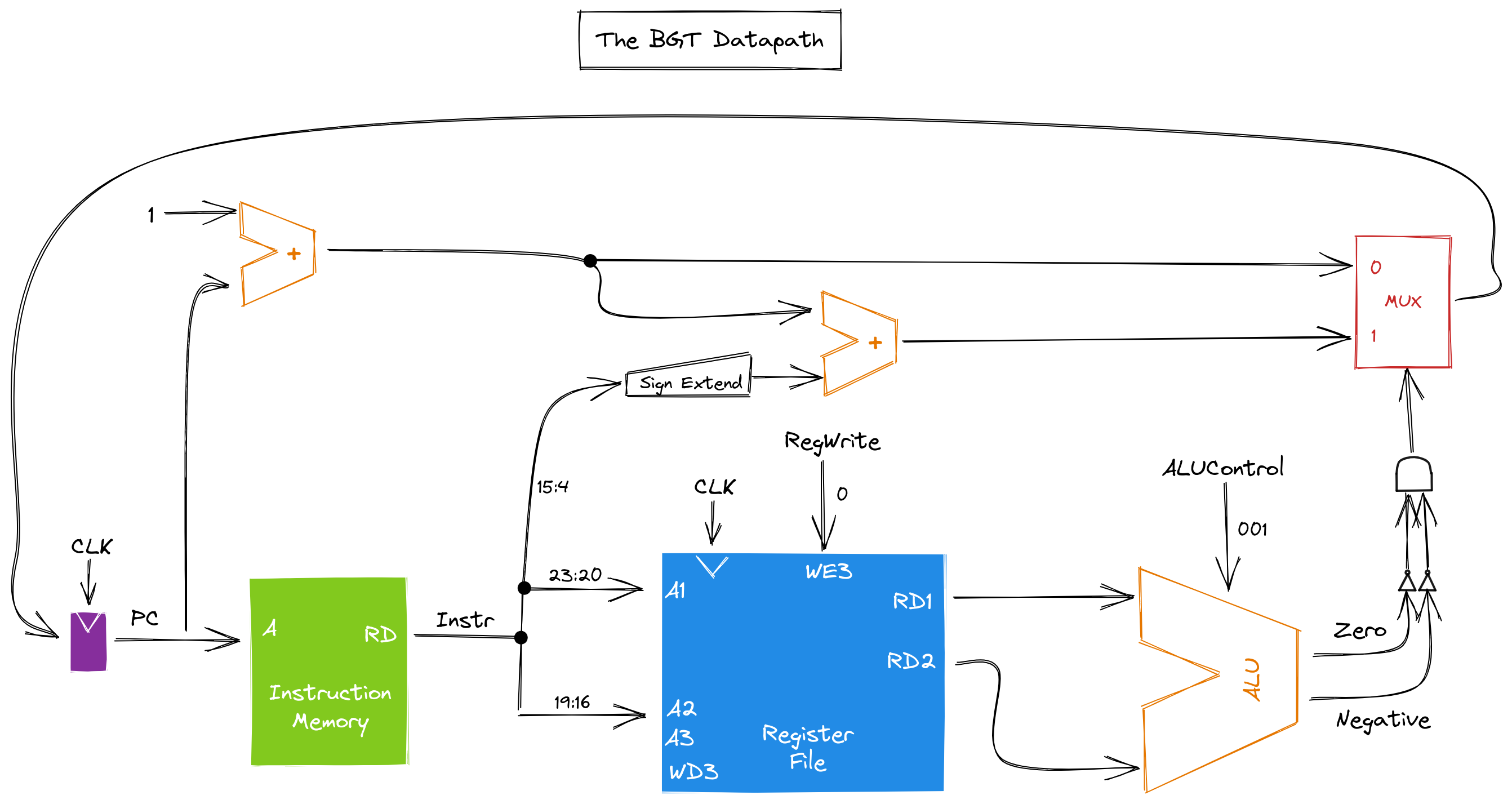
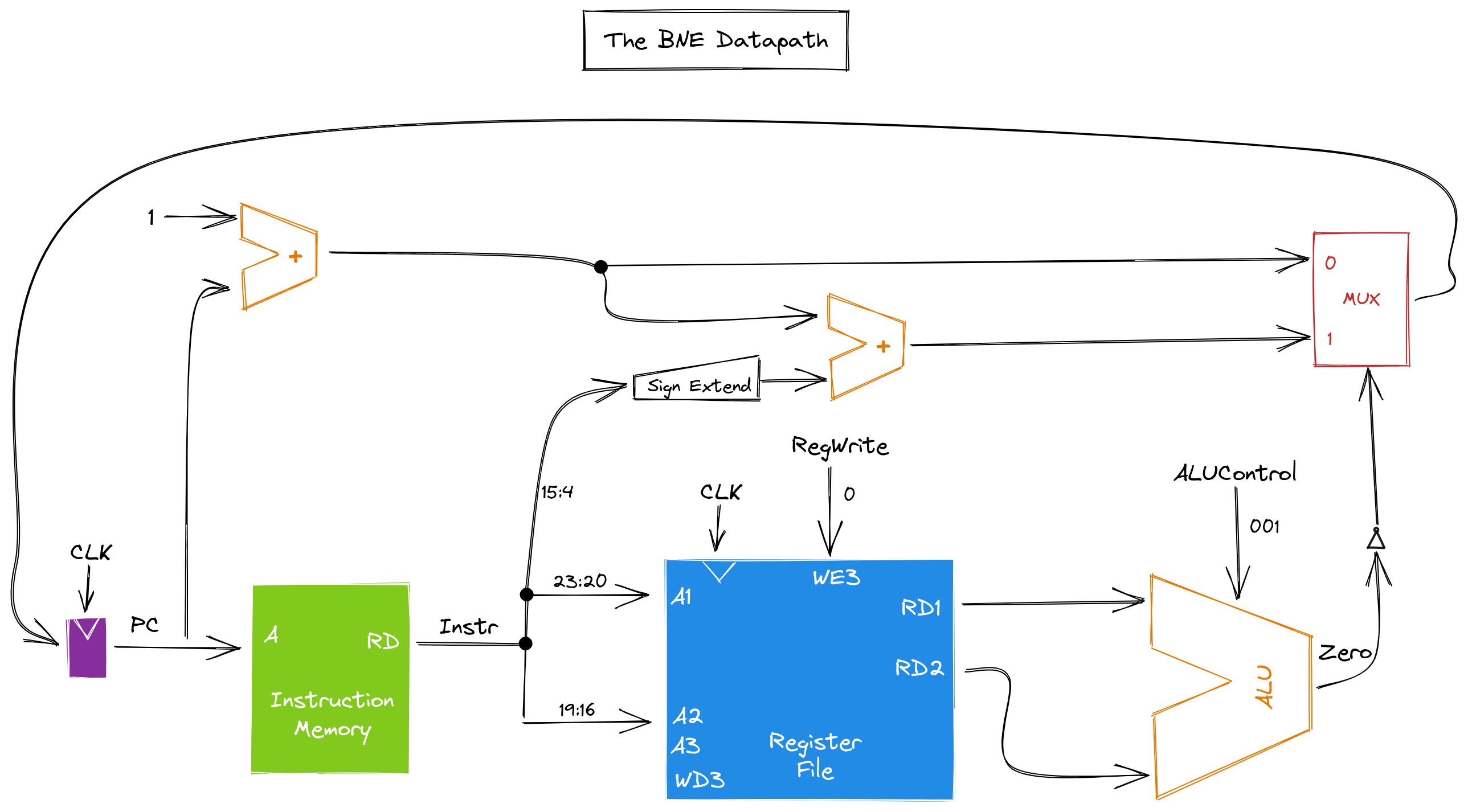


## 2.6. B TYPE INSTRUCTIONS

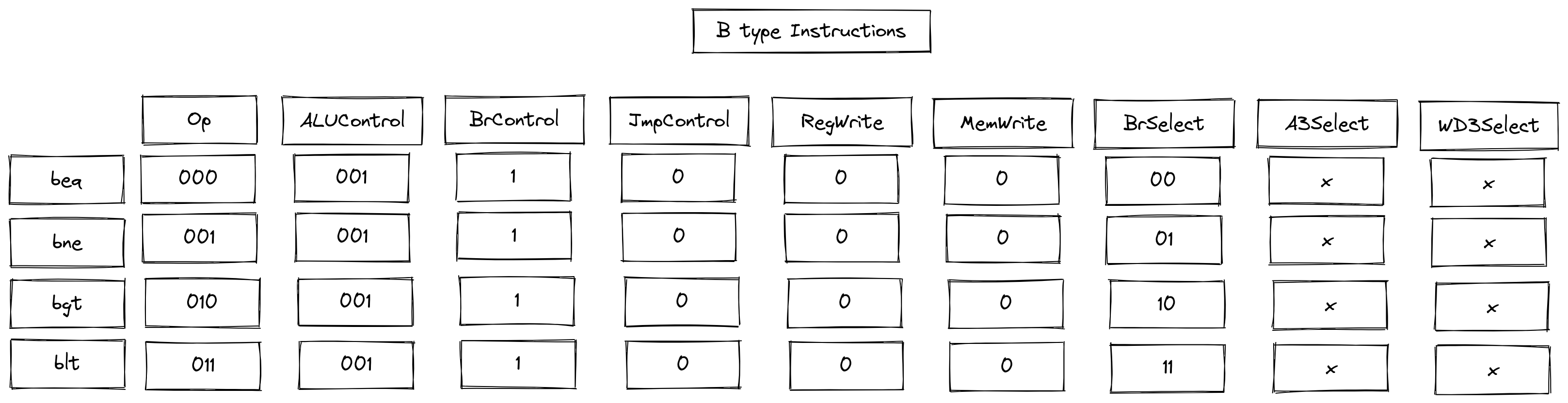
### 2.6.1. INSTRUCTION FORMAT



### 2.6.2. DATAPATHS

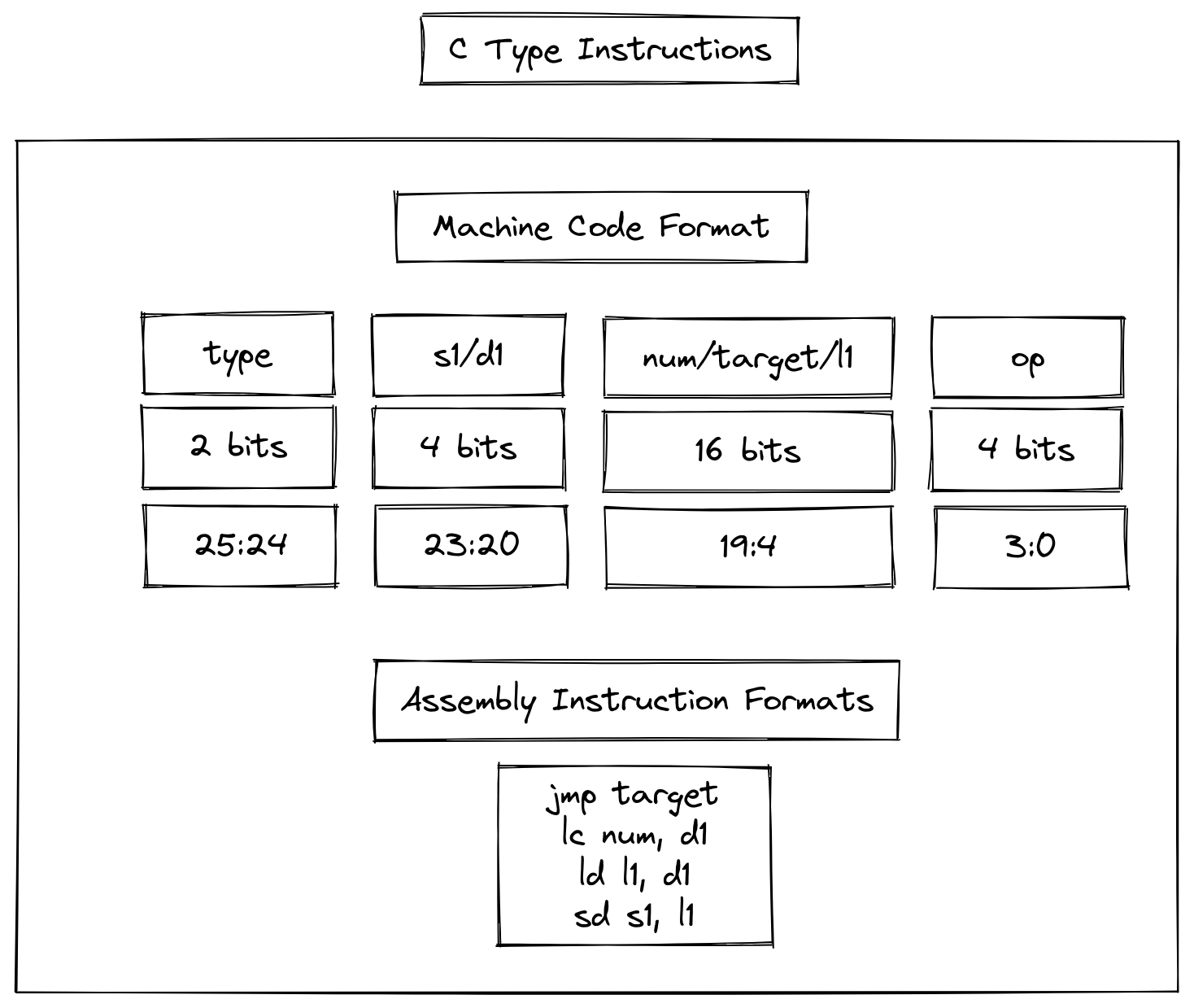


### 2.6.3. TRUTH TABLE

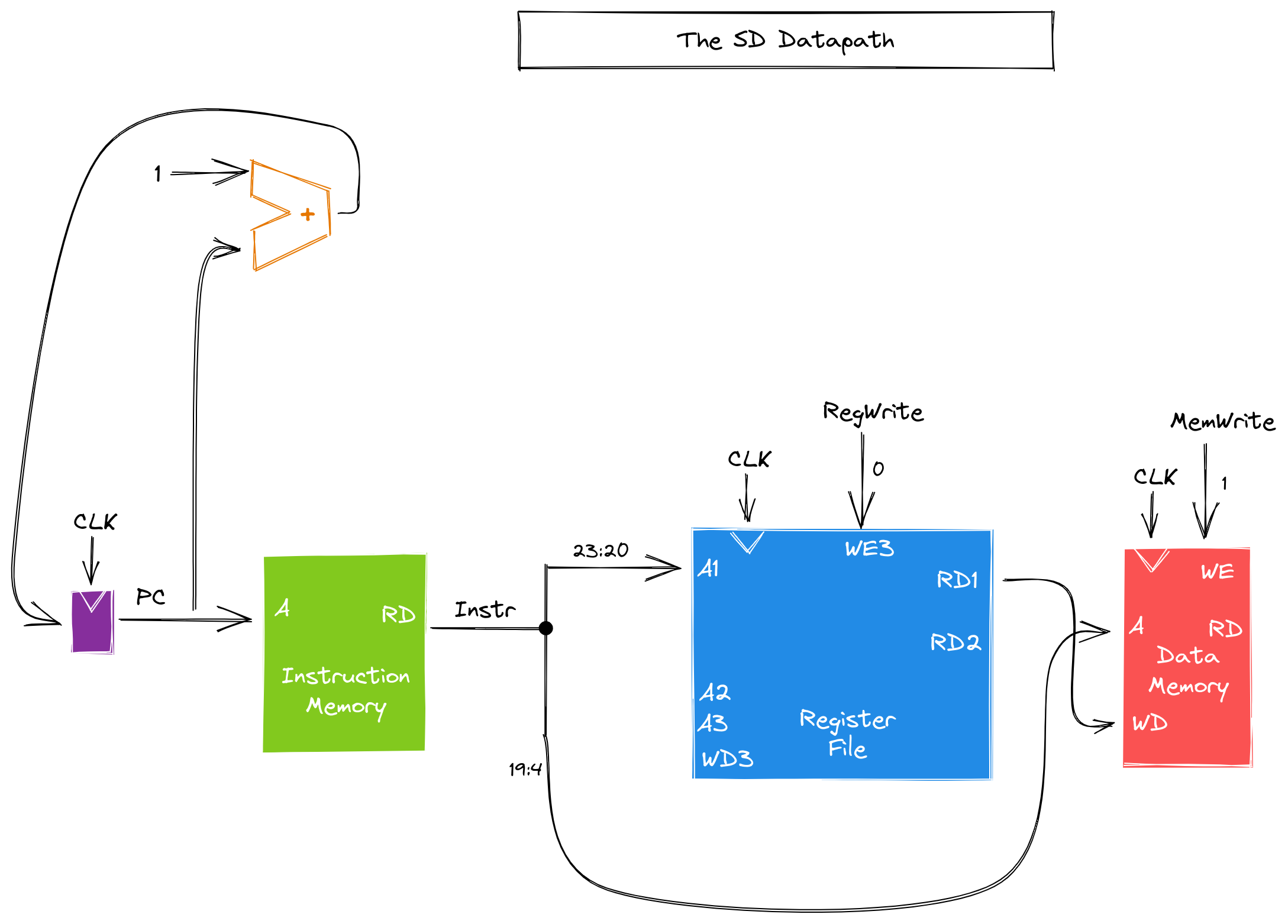
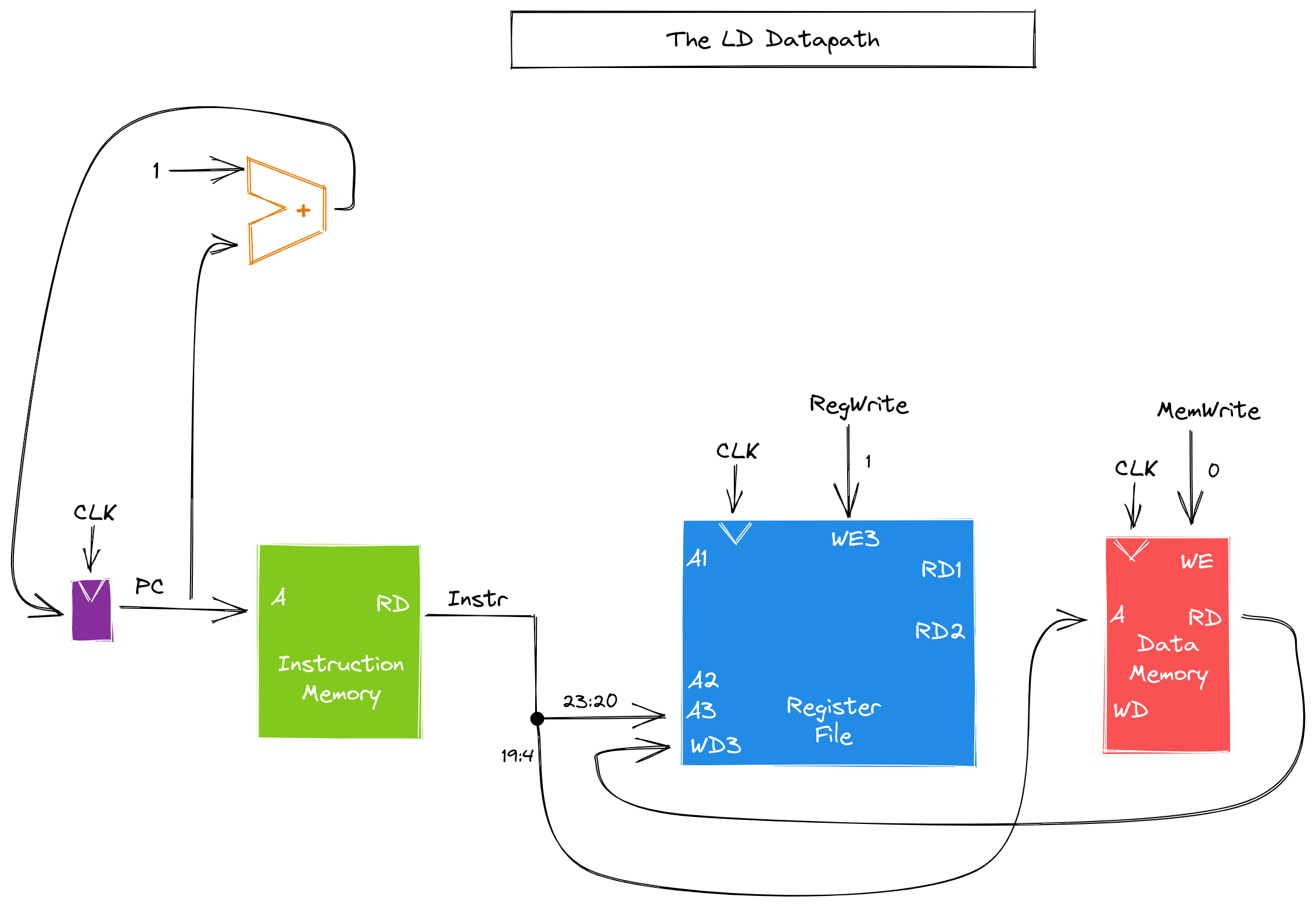
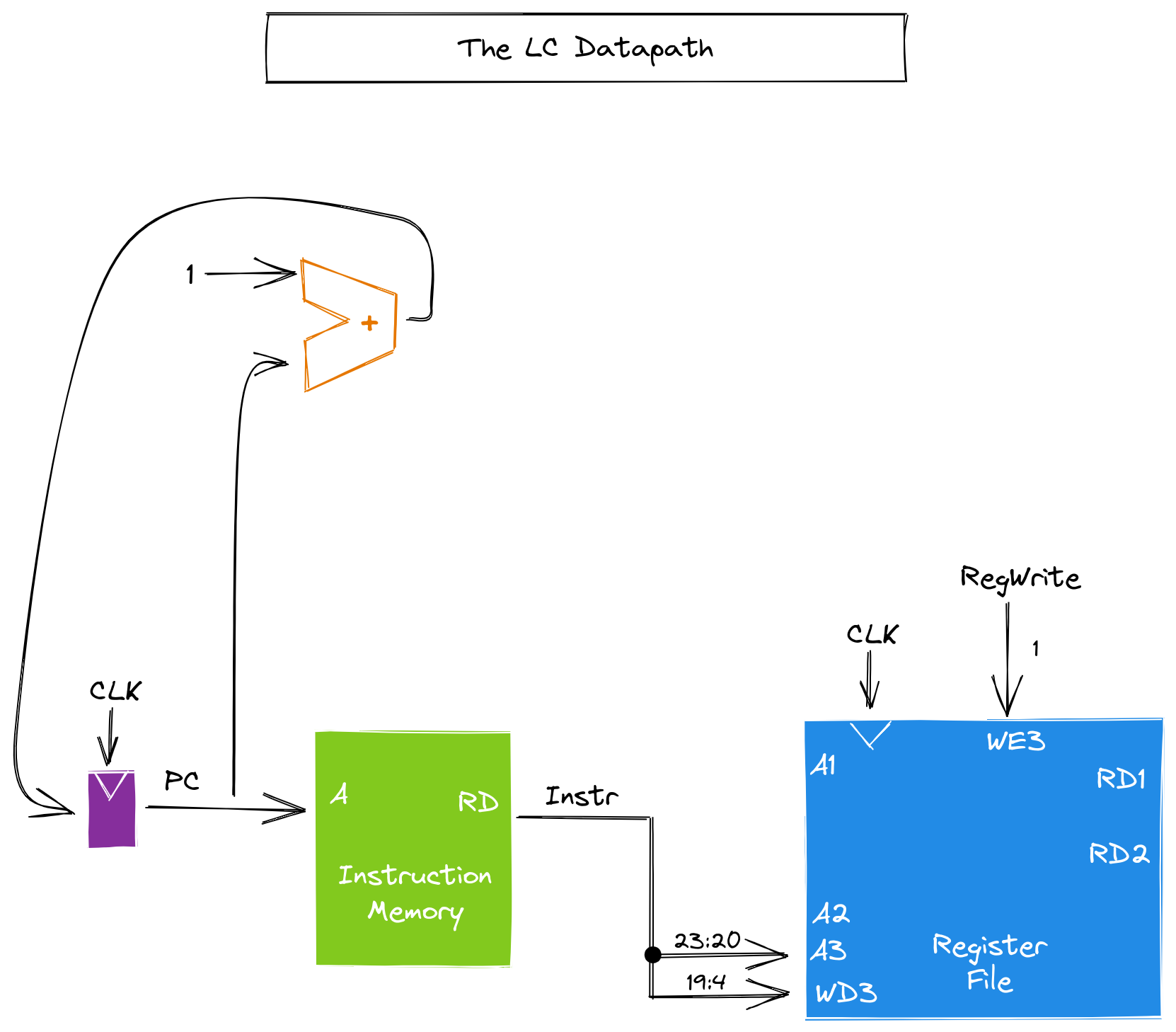
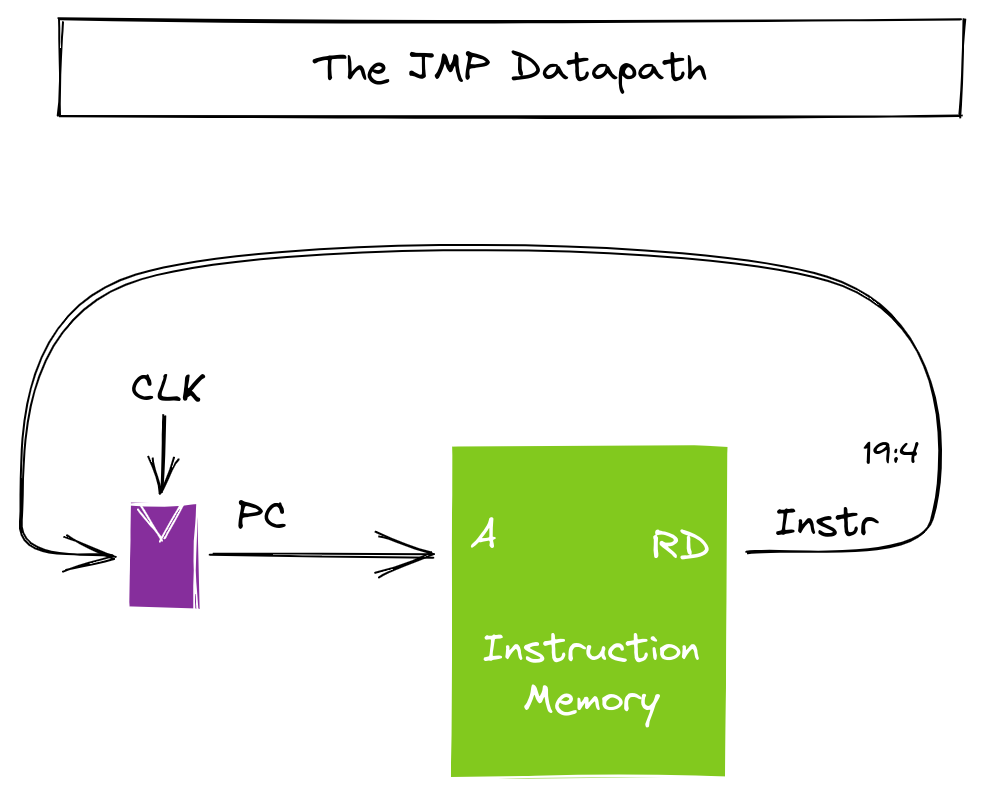


## 2.7. C TYPE INSTRUCTIONS

### 2.7.1. INSTRUCTION FORMAT

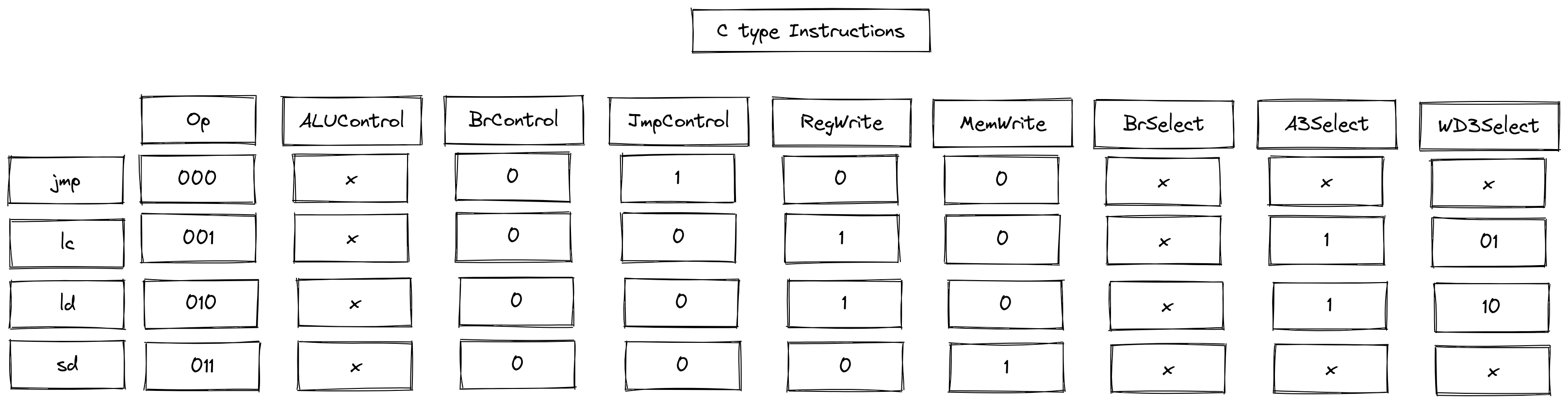


### 2.7.2. DATAPATHS

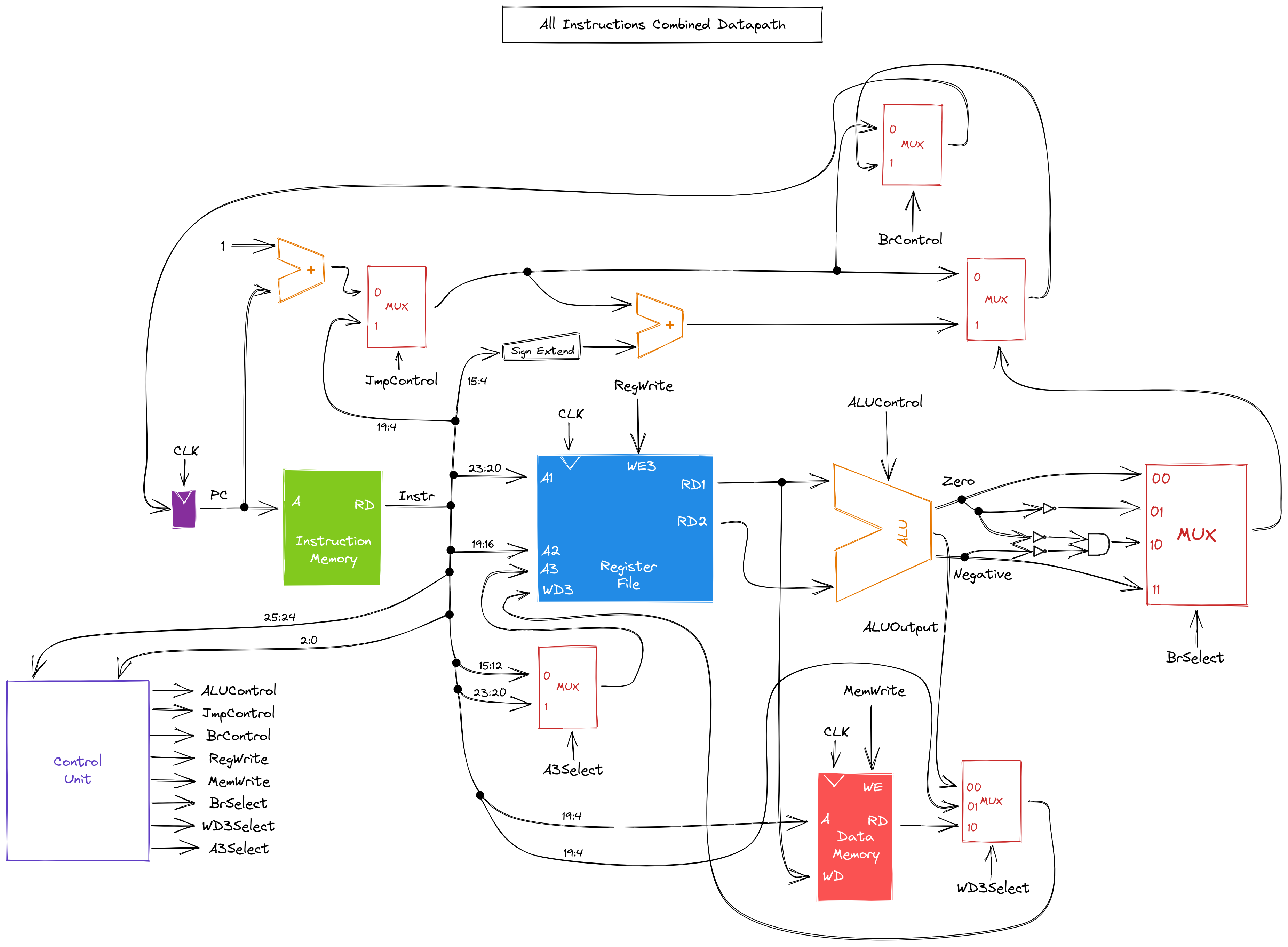


### C:\Users\user\AppData\Local\Microsoft\Windows\INetCache\Content.Word\c-type-combined-datapath.png

### 2.7.3. TRUTH TABLE

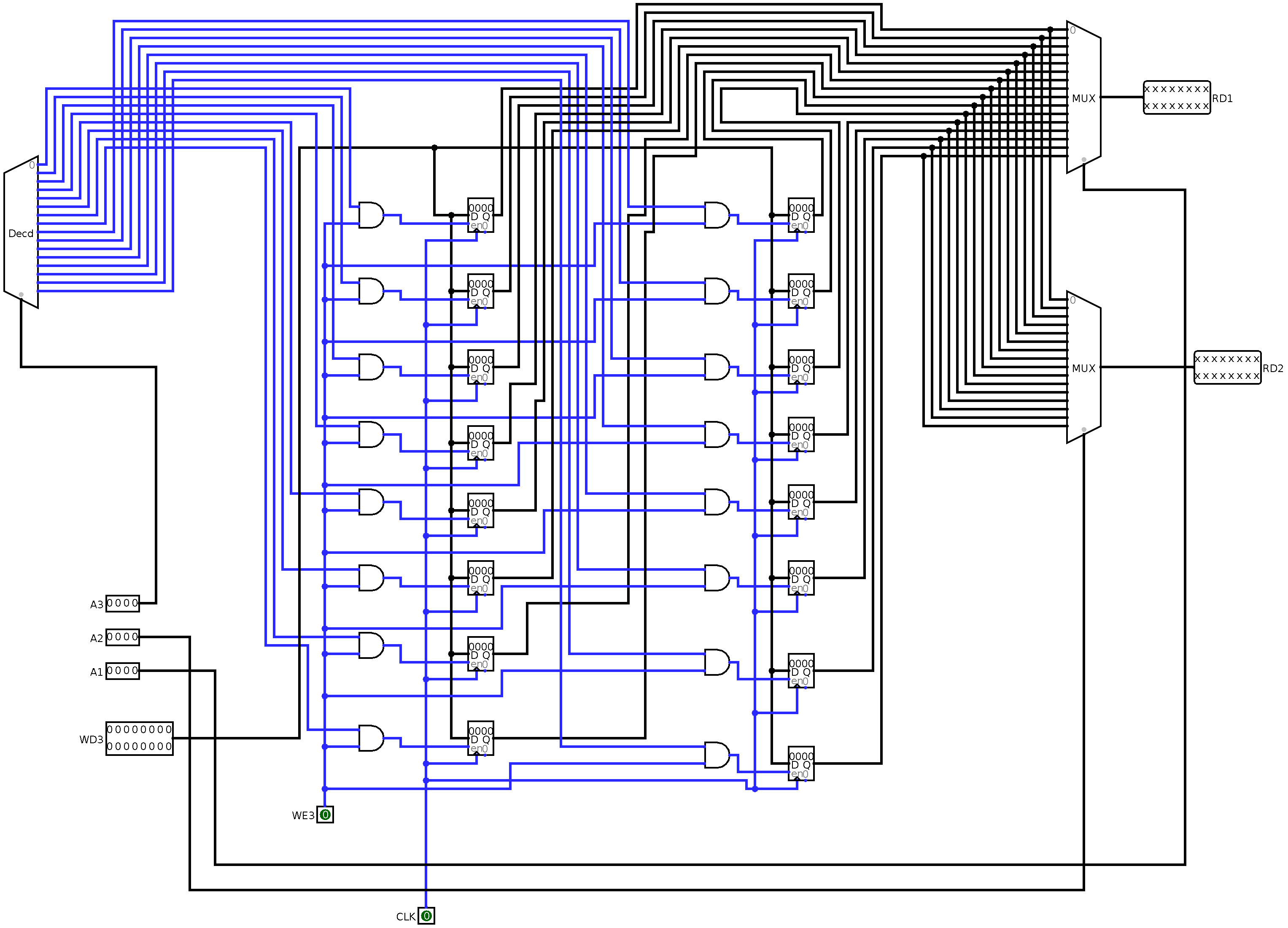


## 2.8. COMBINED DATAPATHS

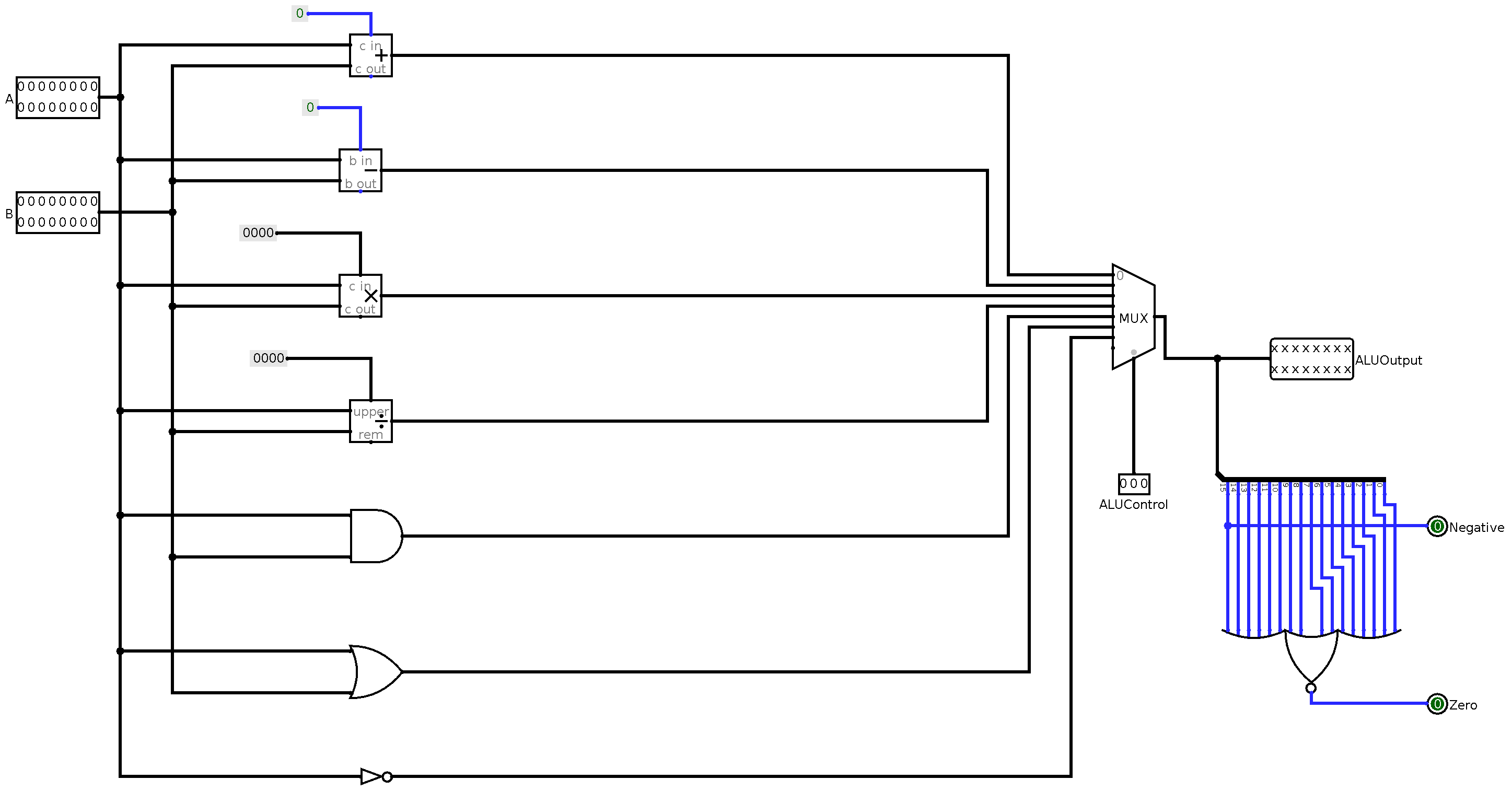


## 2.9. COMPONENTS BUILT IN LOGISIM

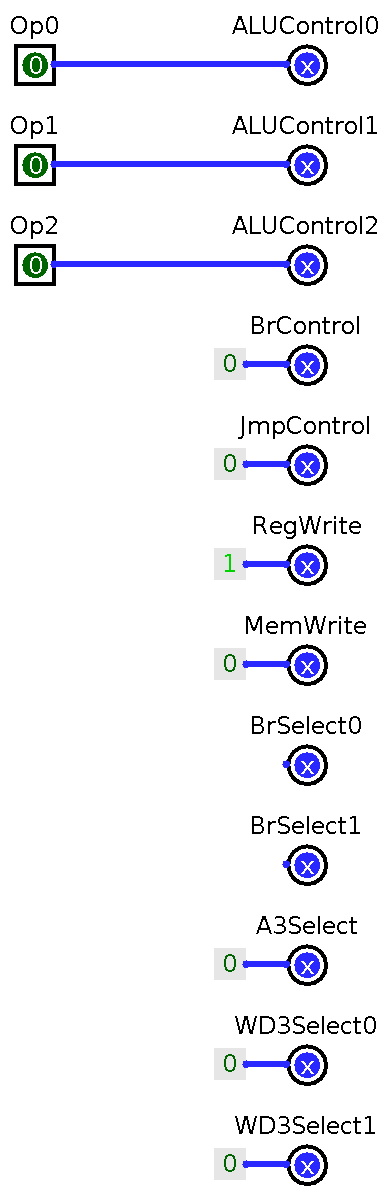
### 2.7.1. REGISTERFILE



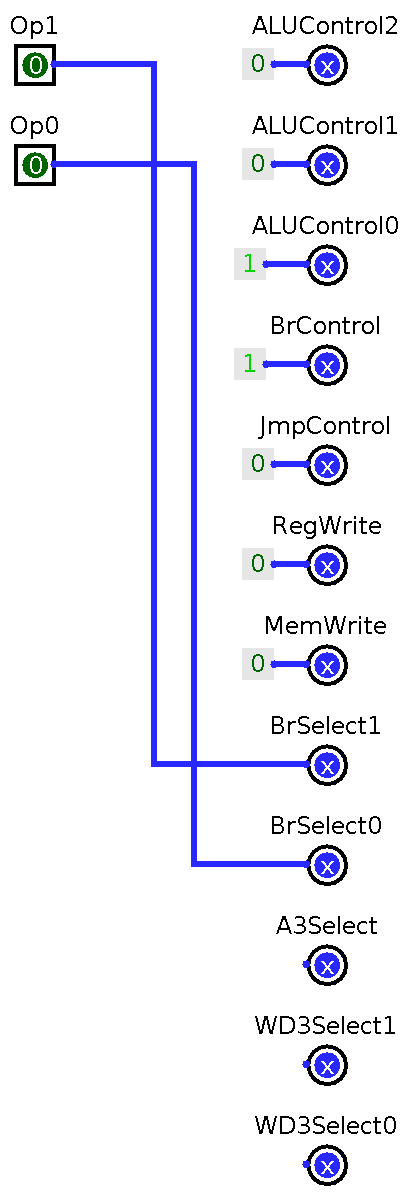
### 2.7.2. ALU



### 2.7.3. A TYPE CONTROL UNIT



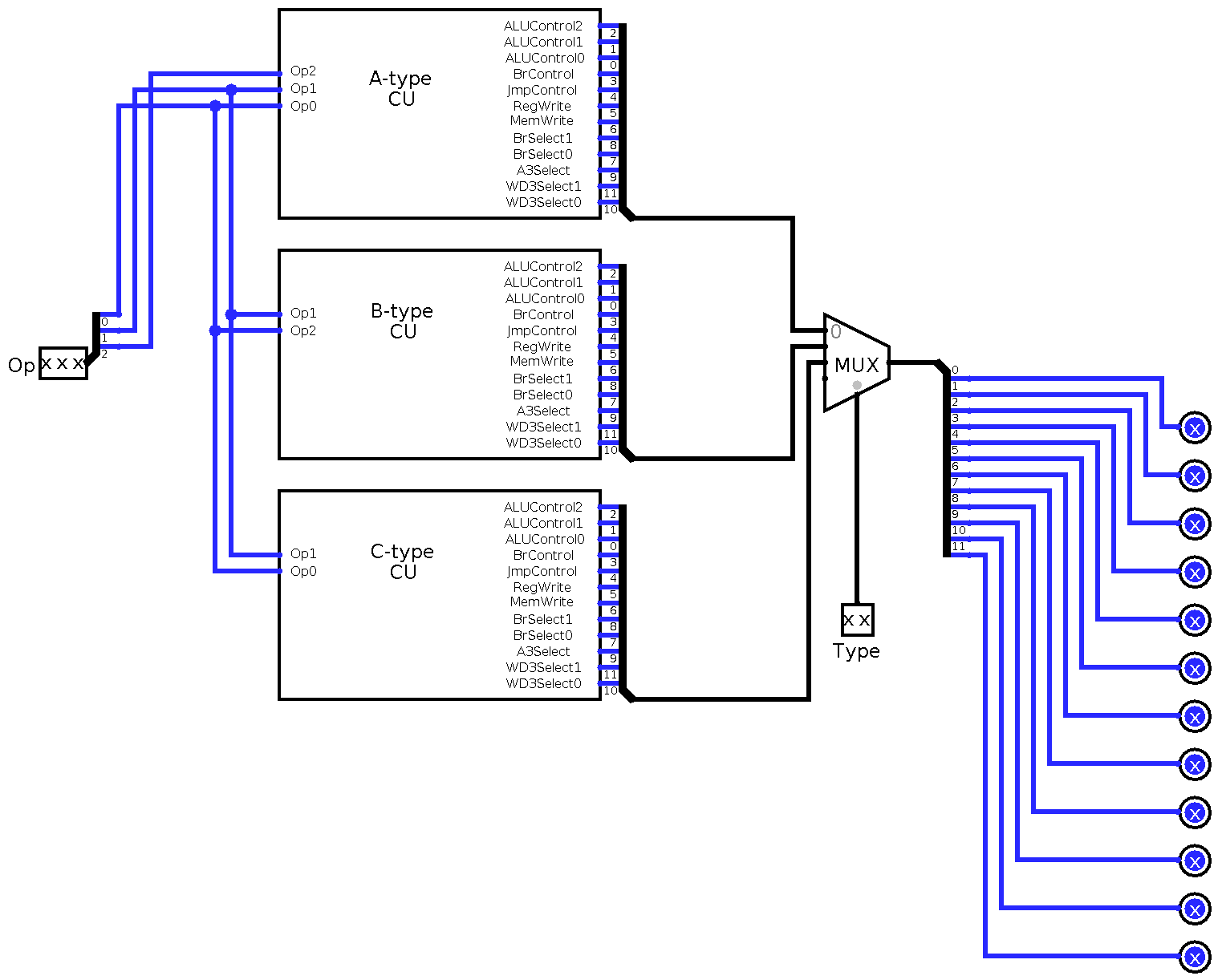
### 2.7.4. B TYPE CONTROL UNIT



### 2.7.5. C TYPE CONTROL UNIT



### 2.7.6. COMBINED CONTROL UNIT



### 2.7.7. COMPLETE MICROPROCESSOR CIRCUIT

