KWAME NKRUMAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

COLLEGE OF ENGINEERING

DEPARTMENT OF ELECTRONIC/ELECTRICAL ENGINEERING

MICROPROCESSOR DESIGN PROJECT

MICROPROCESSORS (COE 381)

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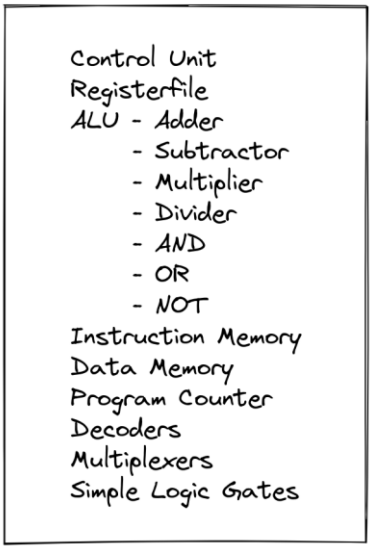
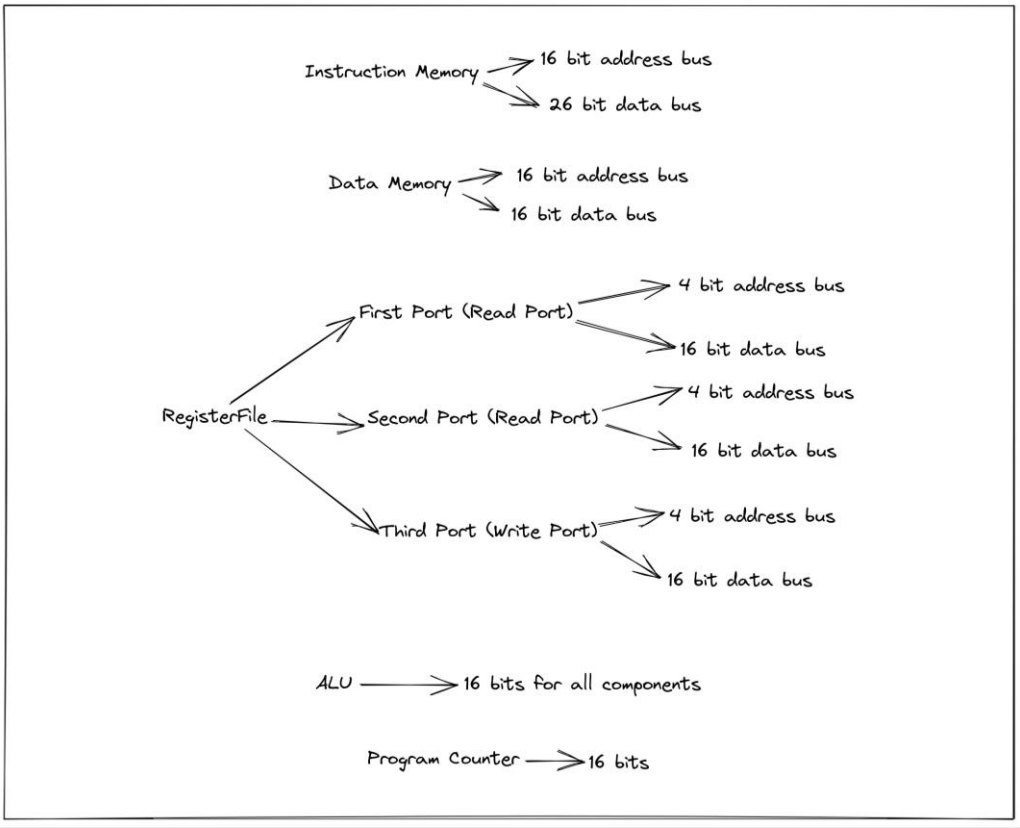


1.2. MEMORY AND ALU BUS SPECIFICATIONS



2. THE ARCHITECTURE AND THE MICROARCHITECTURE

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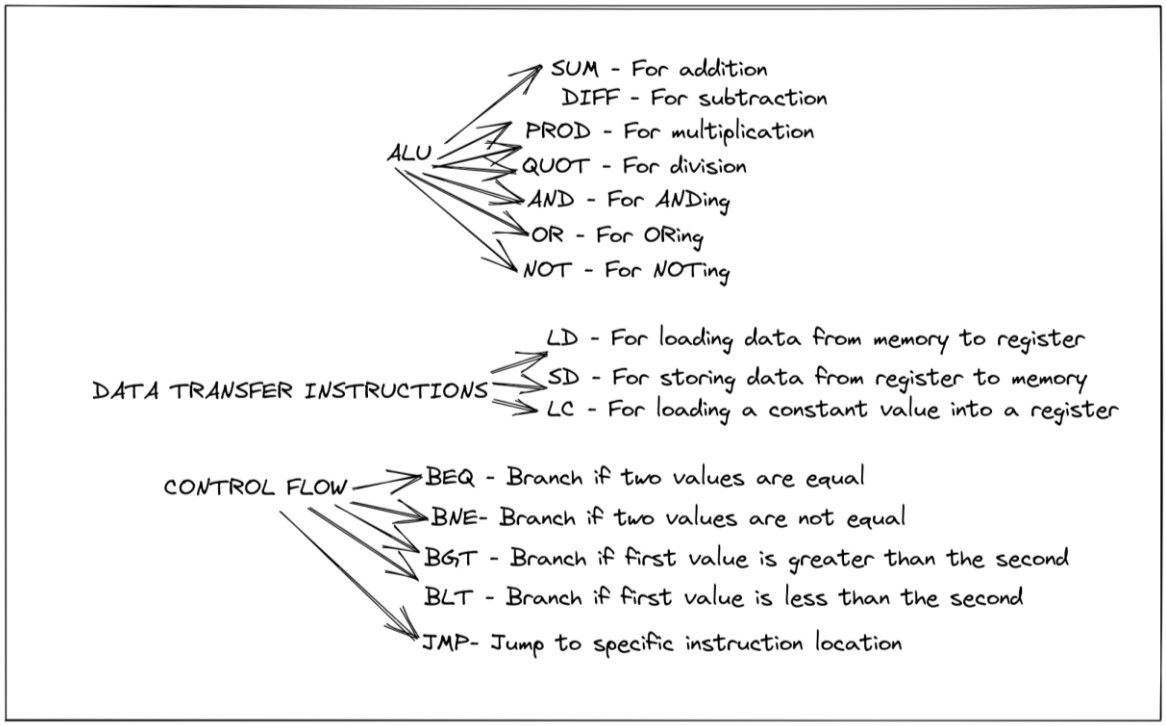

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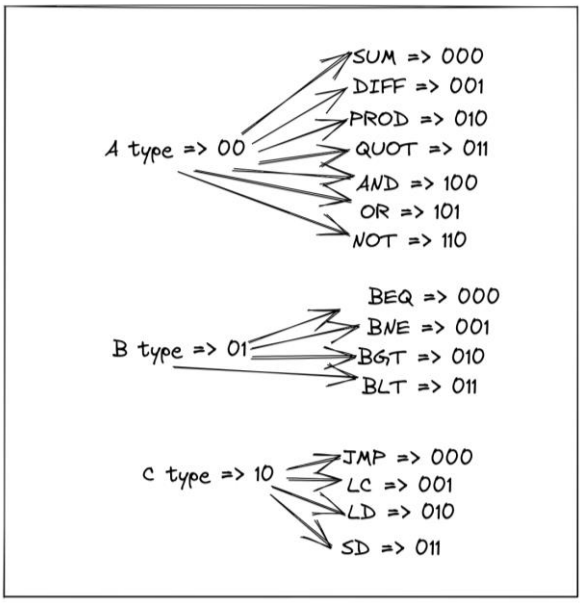

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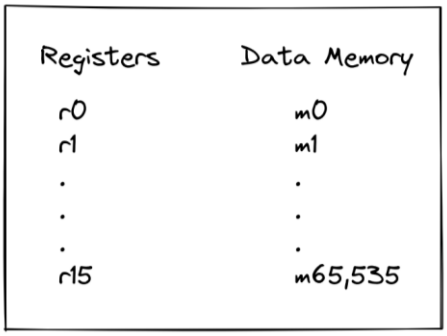
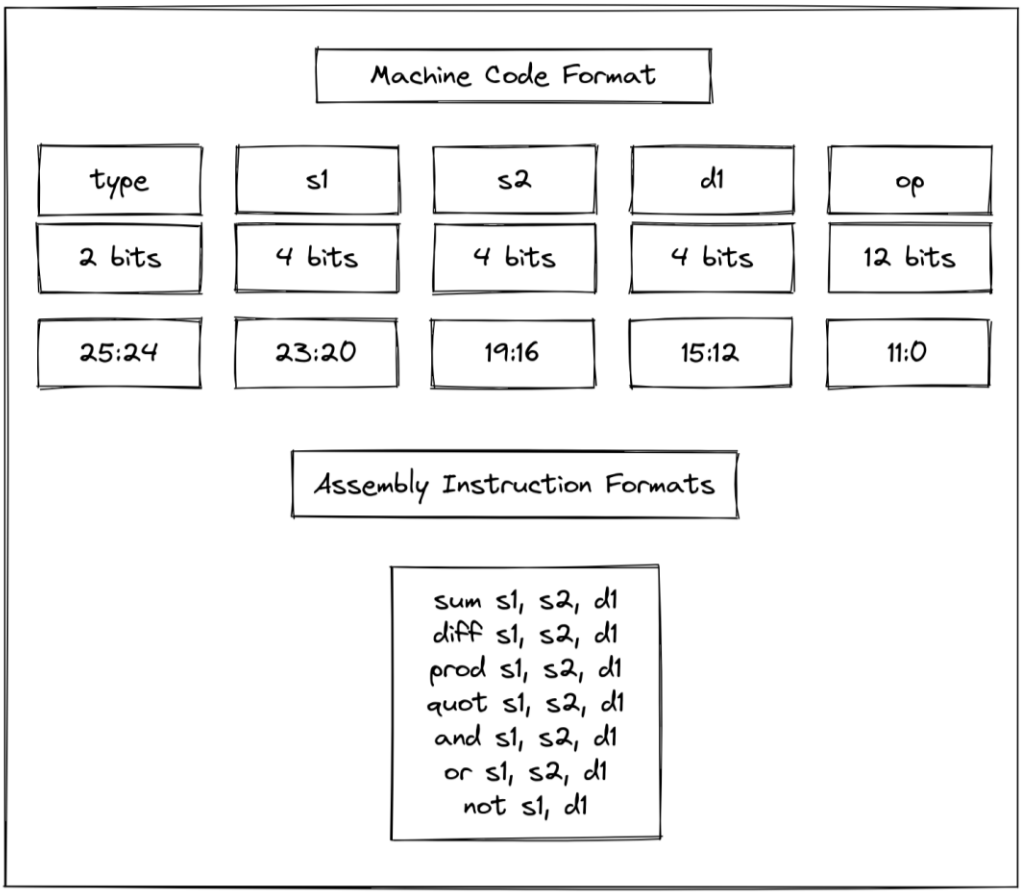
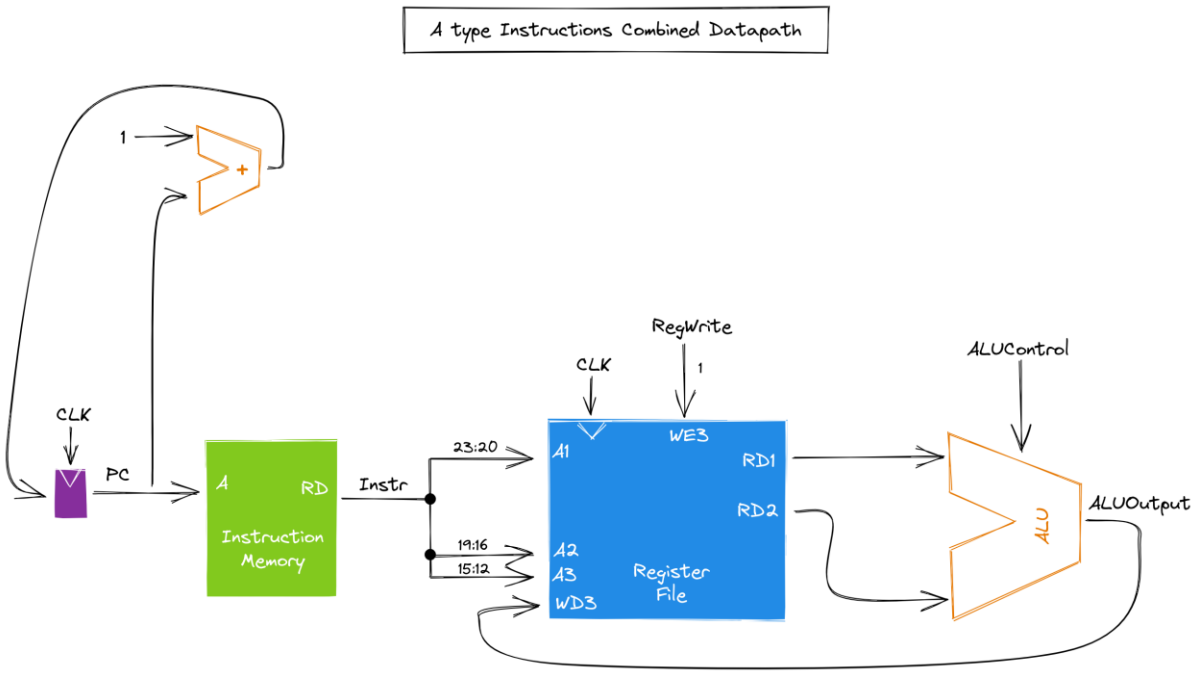


2.5. A TYPE INSTRUCTIONS

2.5.1. INSTRUCTION FORMAT



2.5.2. DATAPATHS



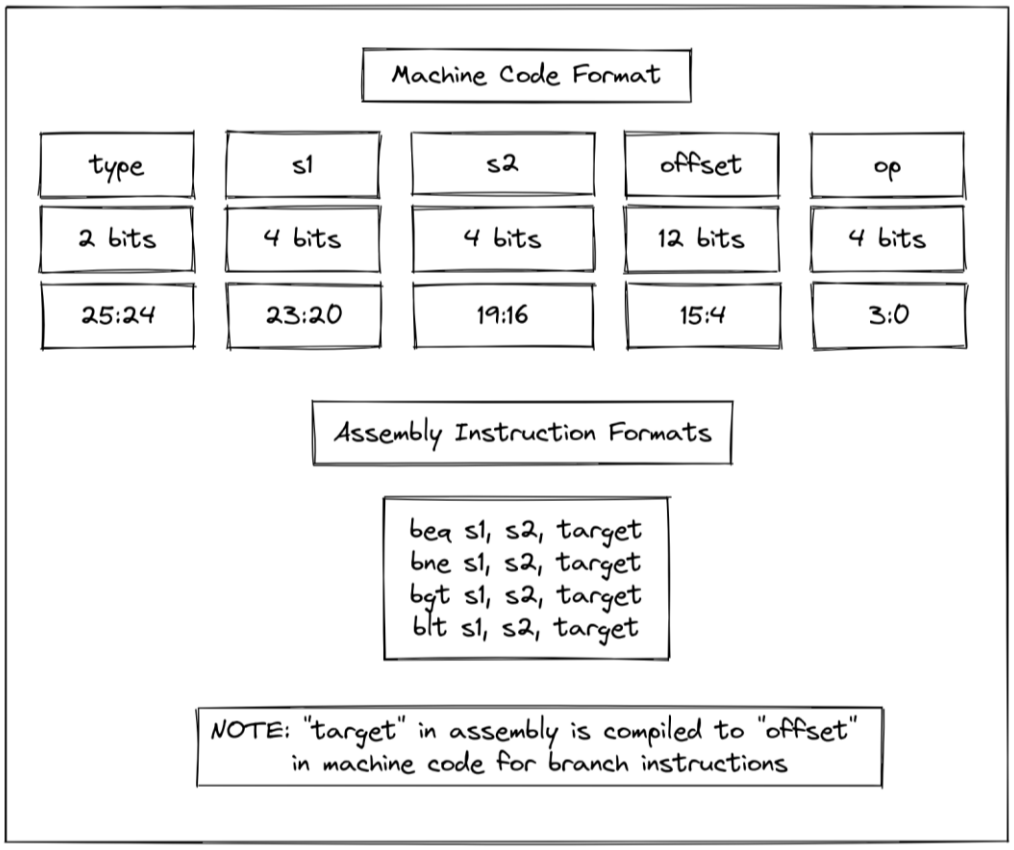
2.5.3. TRUTH TABLE

A type Instructions

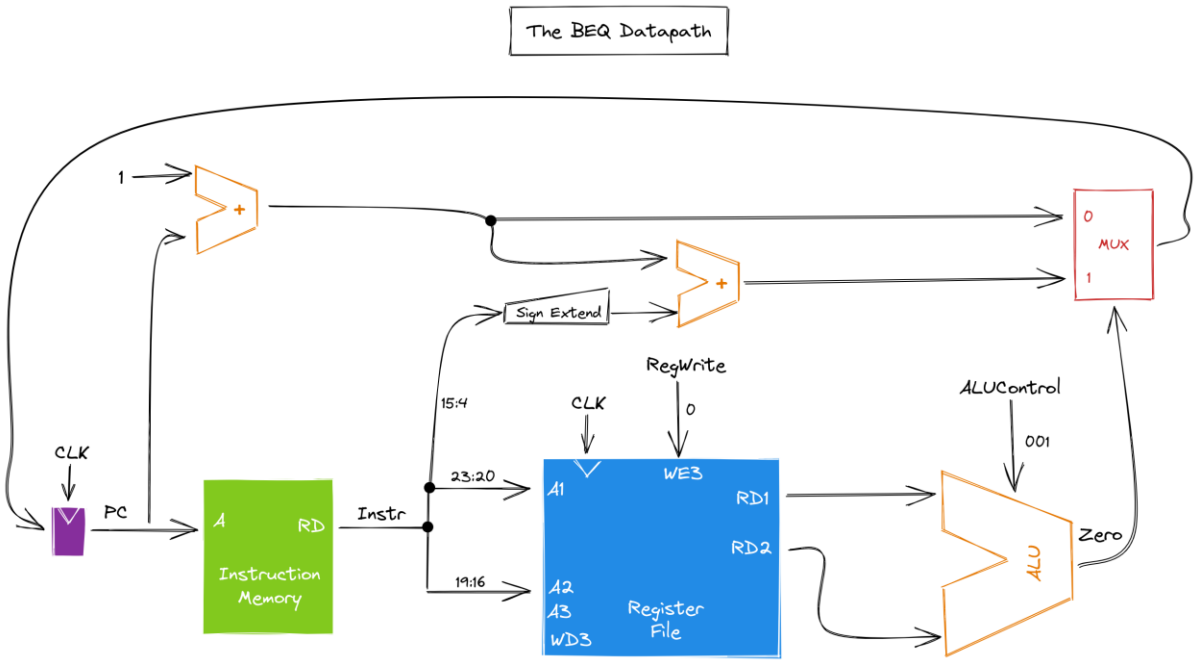
	Op	ALUControl	BrControl	JmpControl	RegWrite	MemWrite	BrSelect	A3Select	WD3Select
sum	000	000	0	0	1	0	x	0	00
diff	001	001	0	0	1	0	x	0	00
prod	010	010	0	0	1	0	x	0	00
quot	011	011	0	0	1	0	x	0	00
and	100	100	0	0	1	0	x	0	00
or	101	101	0	0	1	0	x	0	00
not	110	110	0	0	1	0	x	0	00

2.6. B TYPE INSTRUCTIONS

2.6.1. INSTRUCTION FORMAT



2.6.2. DATAPATHS



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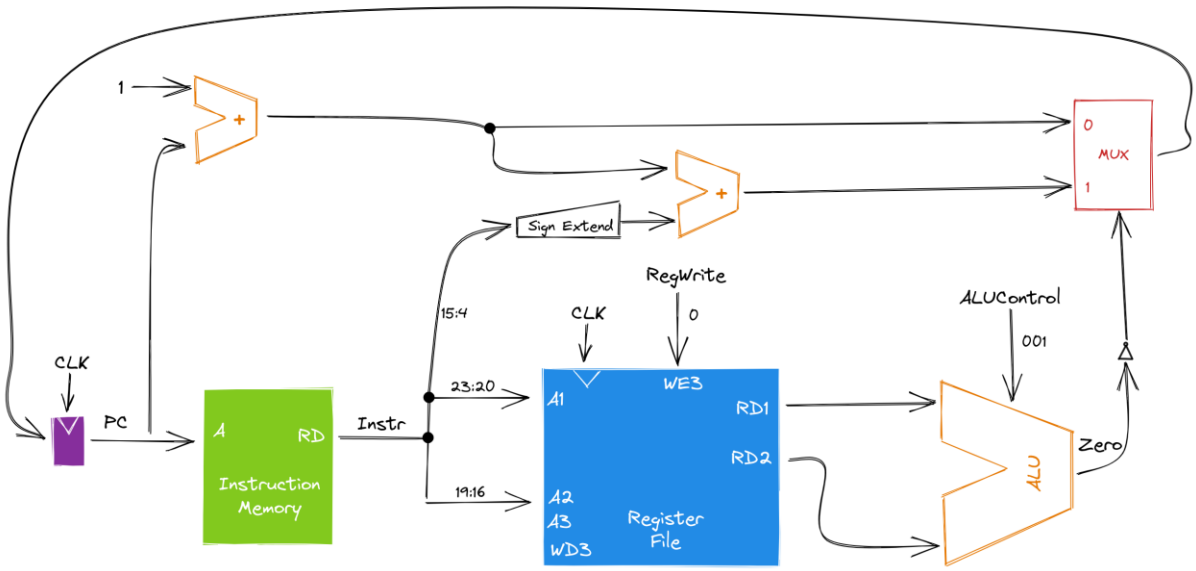
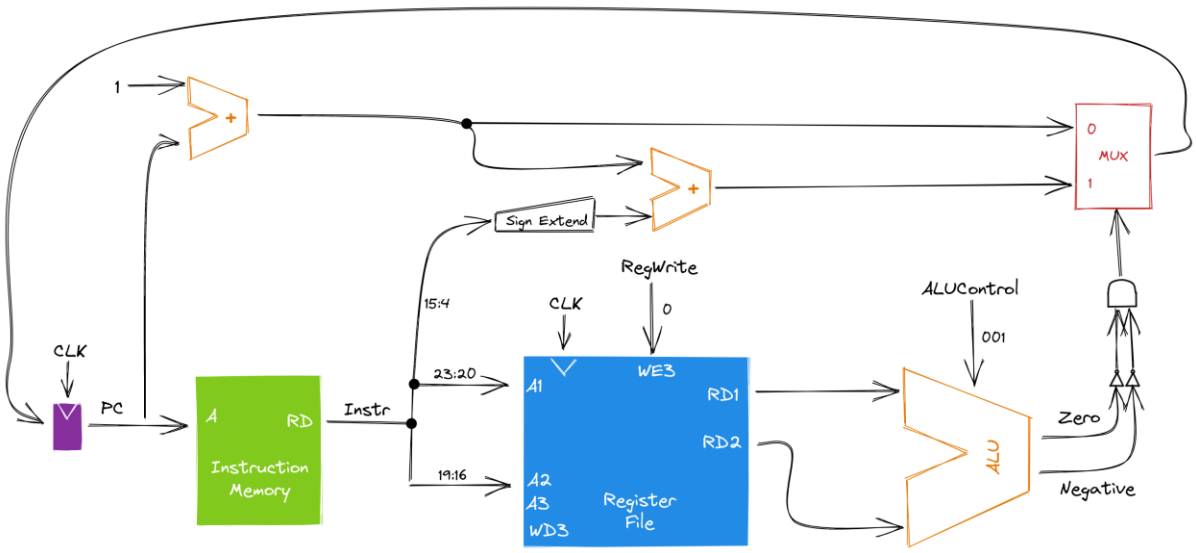
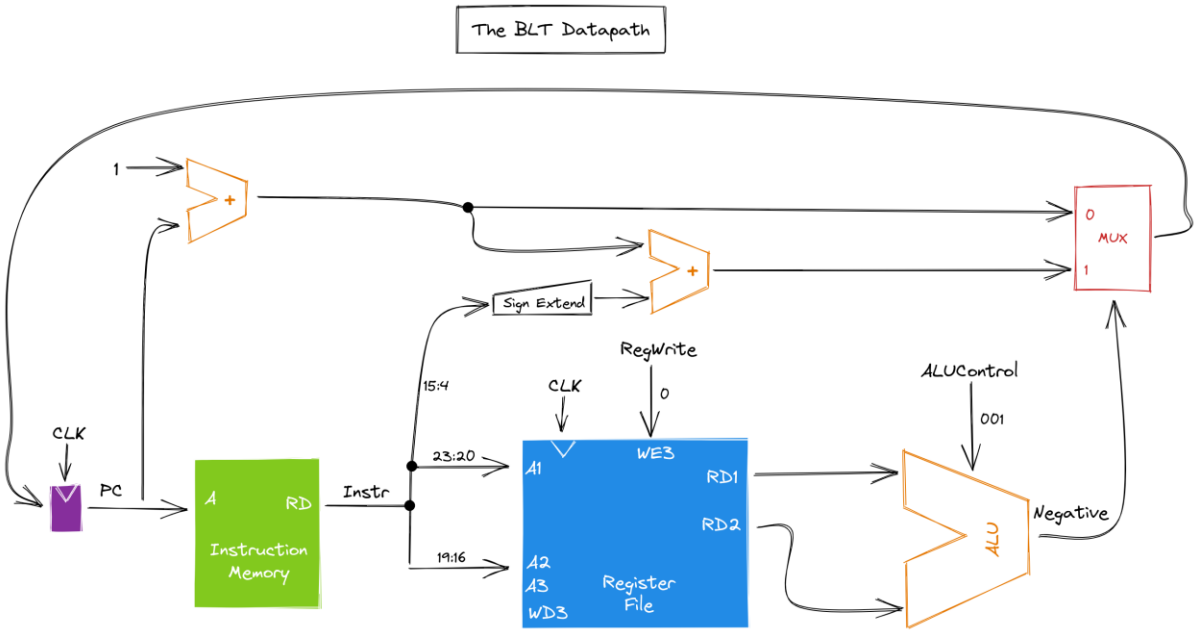


The BGT Datapath





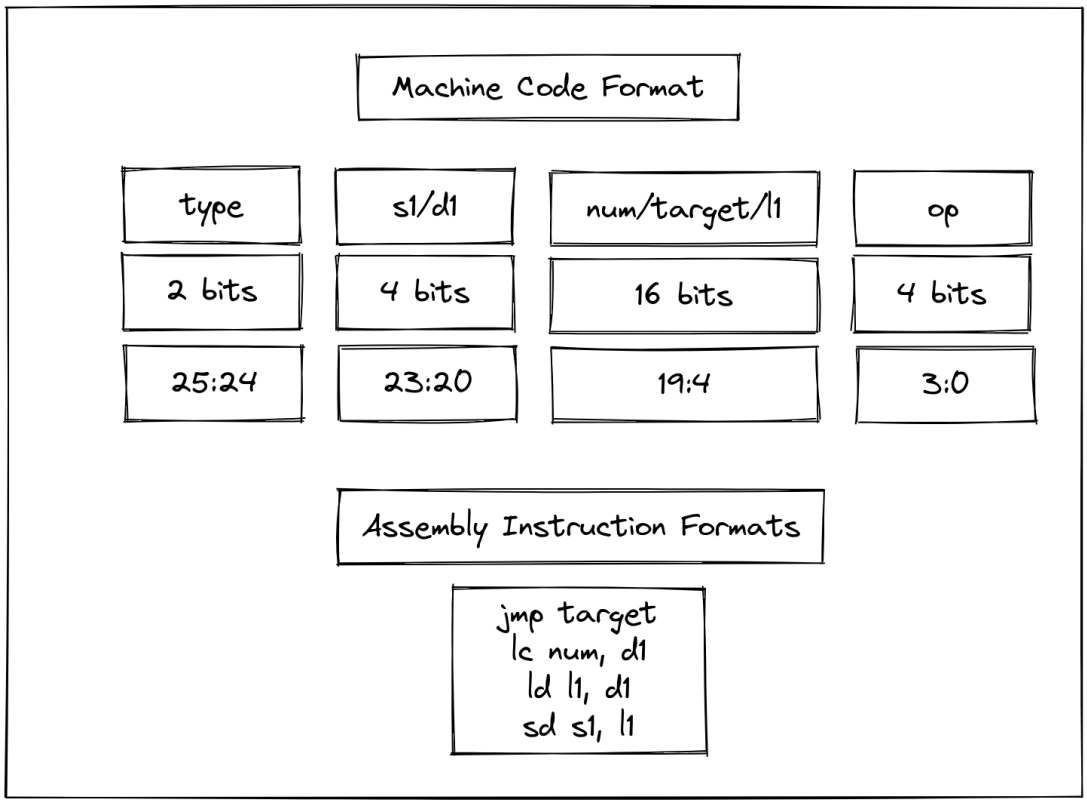
2.6.3. TRUTH TABLE

B type Instructions

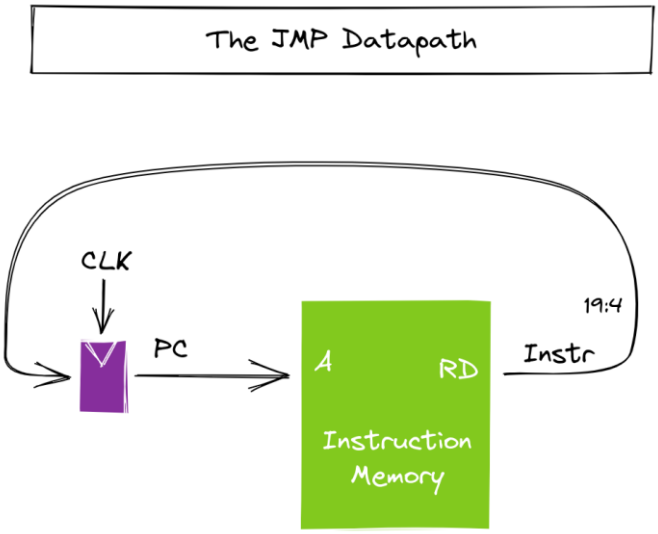
	Op	ALUControl	BrControl	JmpControl	RegWrite	MemWrite	BrSelect	A3Select	WD3Select
beq	000	001	1	0	0	0	00	x	x
bne	001	001	1	0	0	0	01	x	x
bgt	010	001	1	0	0	0	10	x	x
blt	011	001	1	0	0	0	11	x	x

2.7. C TYPE INSTRUCTIONS

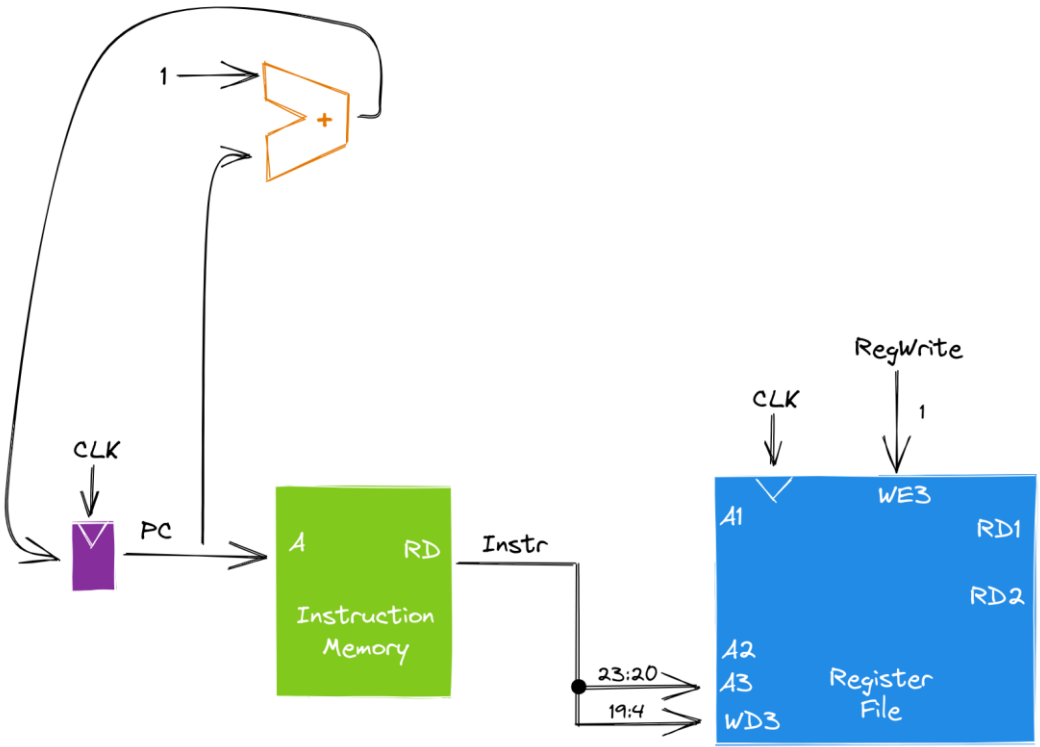
2.7.1. INSTRUCTION FORMAT



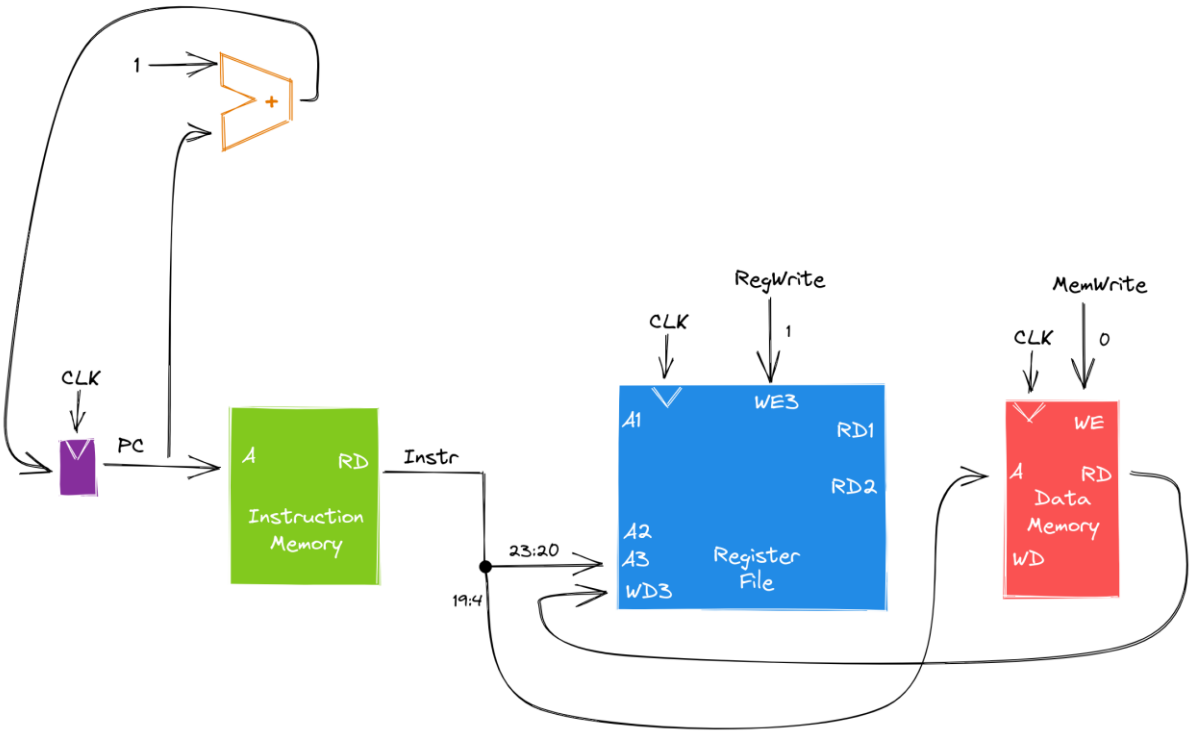
2.7.2. DATAPATHS

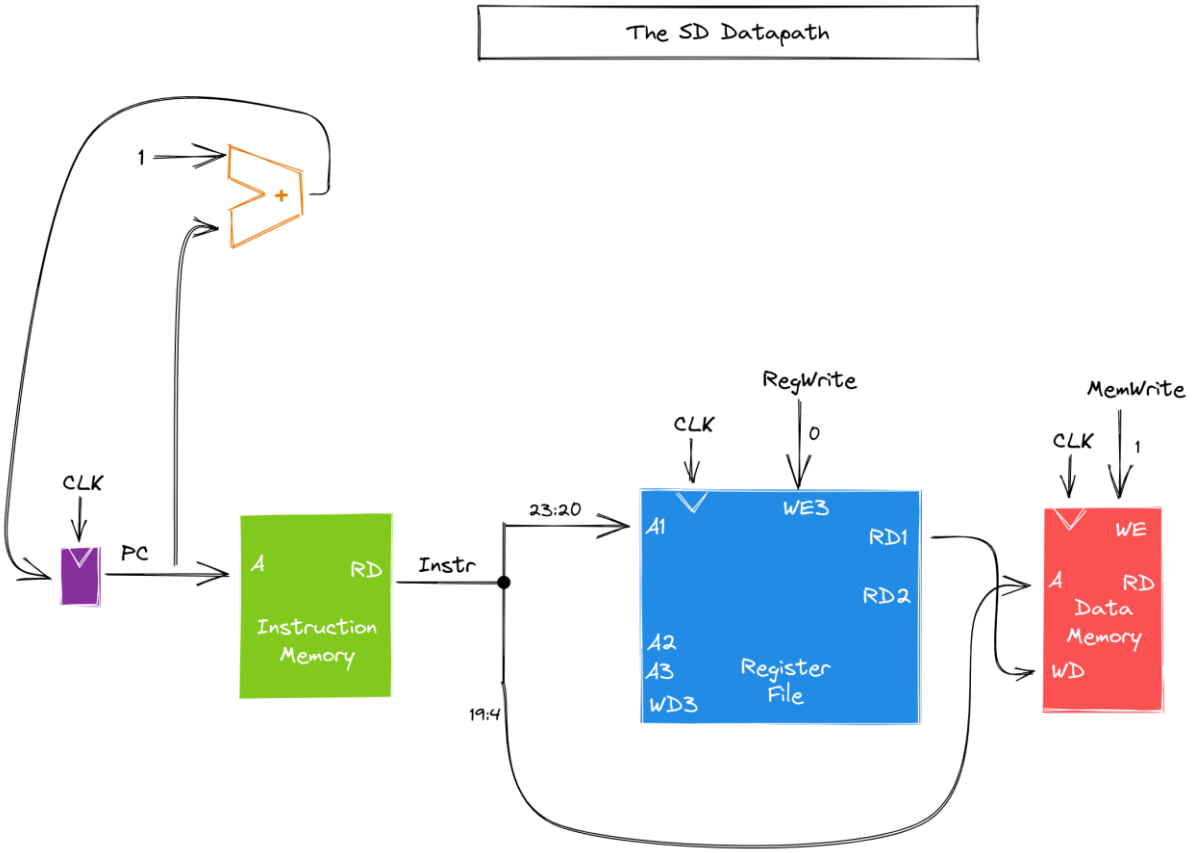


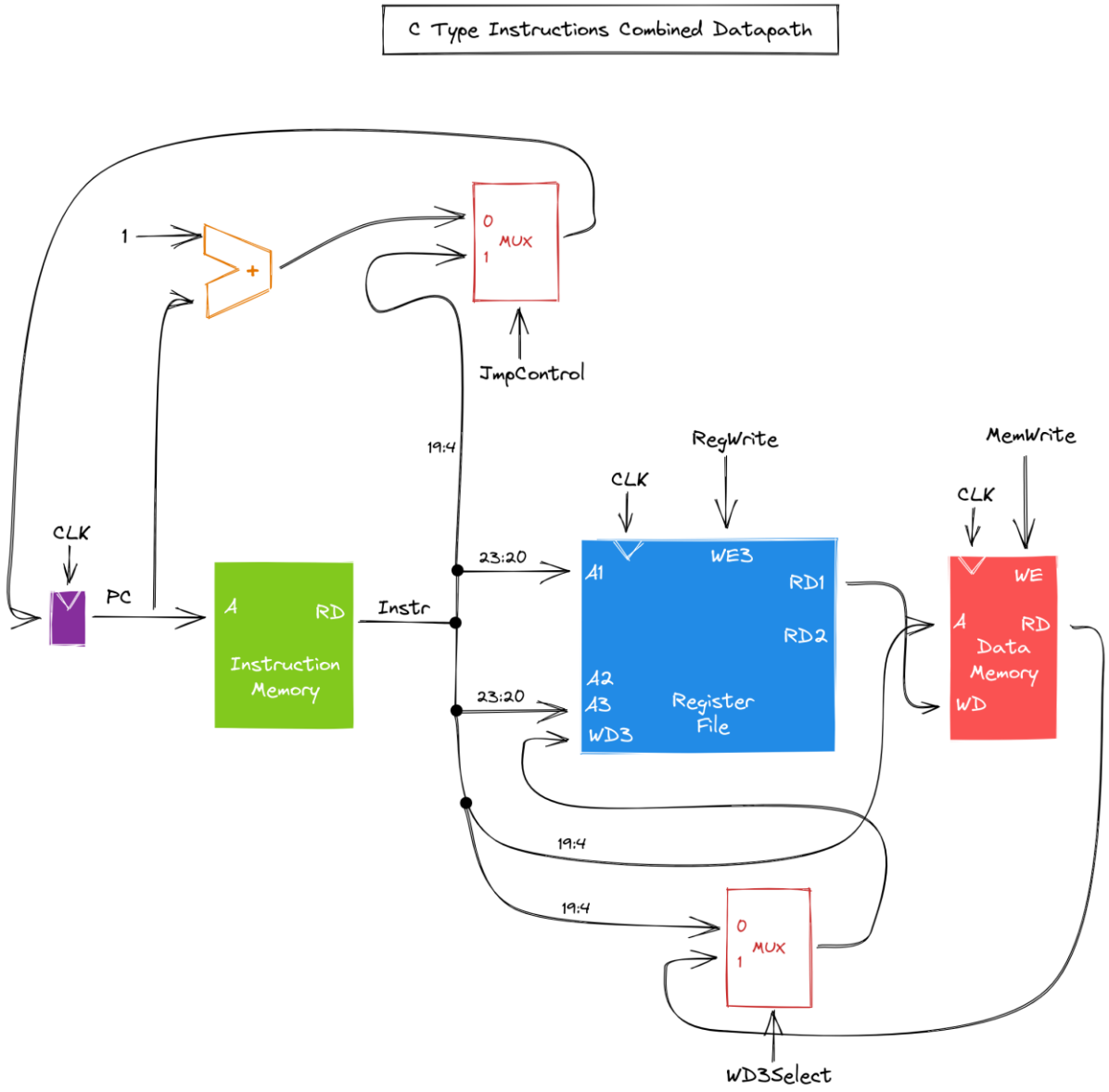
The LC Datapath



The LD Datapath




The SD Datapath
1
+
CLK
PC
A
RD
Instruction Memory
Instr
23:20
19:4
RegWrite
CLK
0
A1
WE3
RD1
RD2
A2
A3
WD3
Register File
MemWrite
CLK
1
WE
A
RD
Data Memory
WD

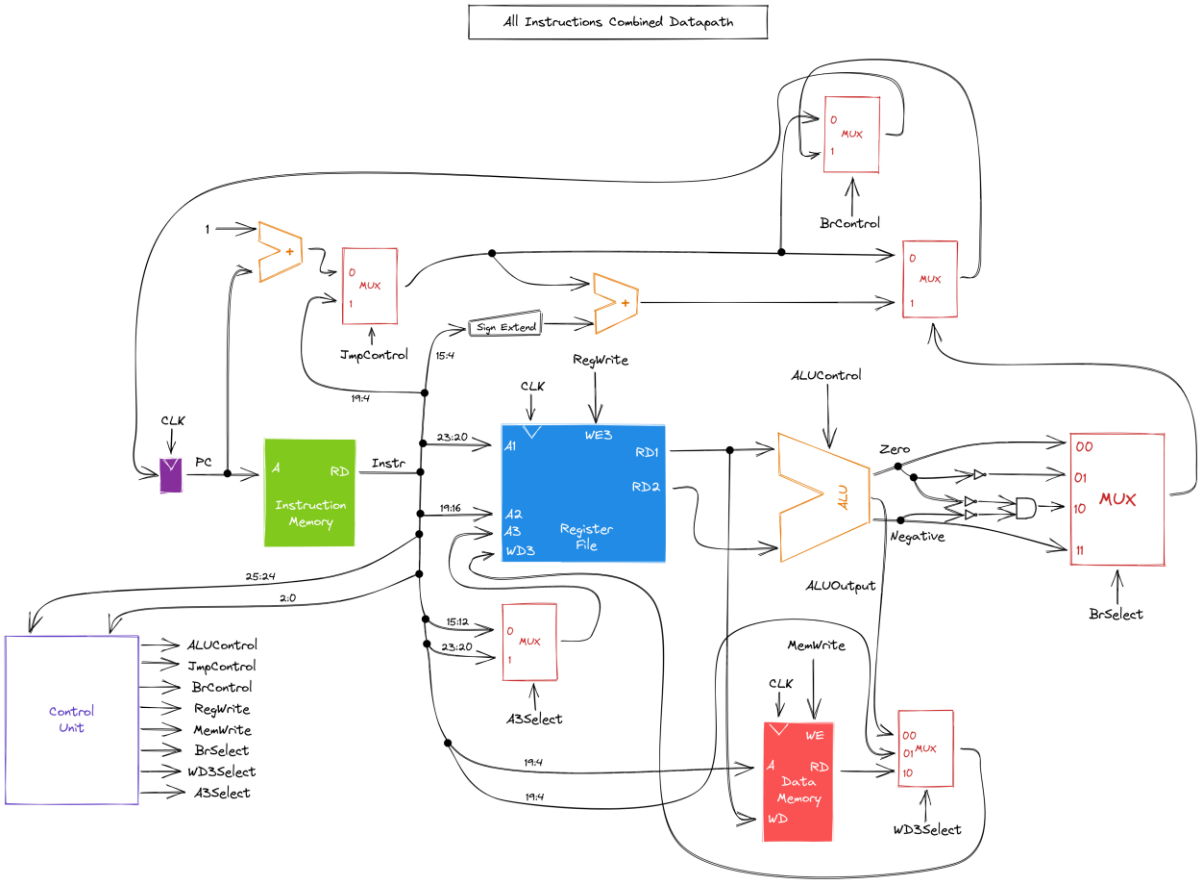


2.7.3. TRUTH TABLE

C type Instructions

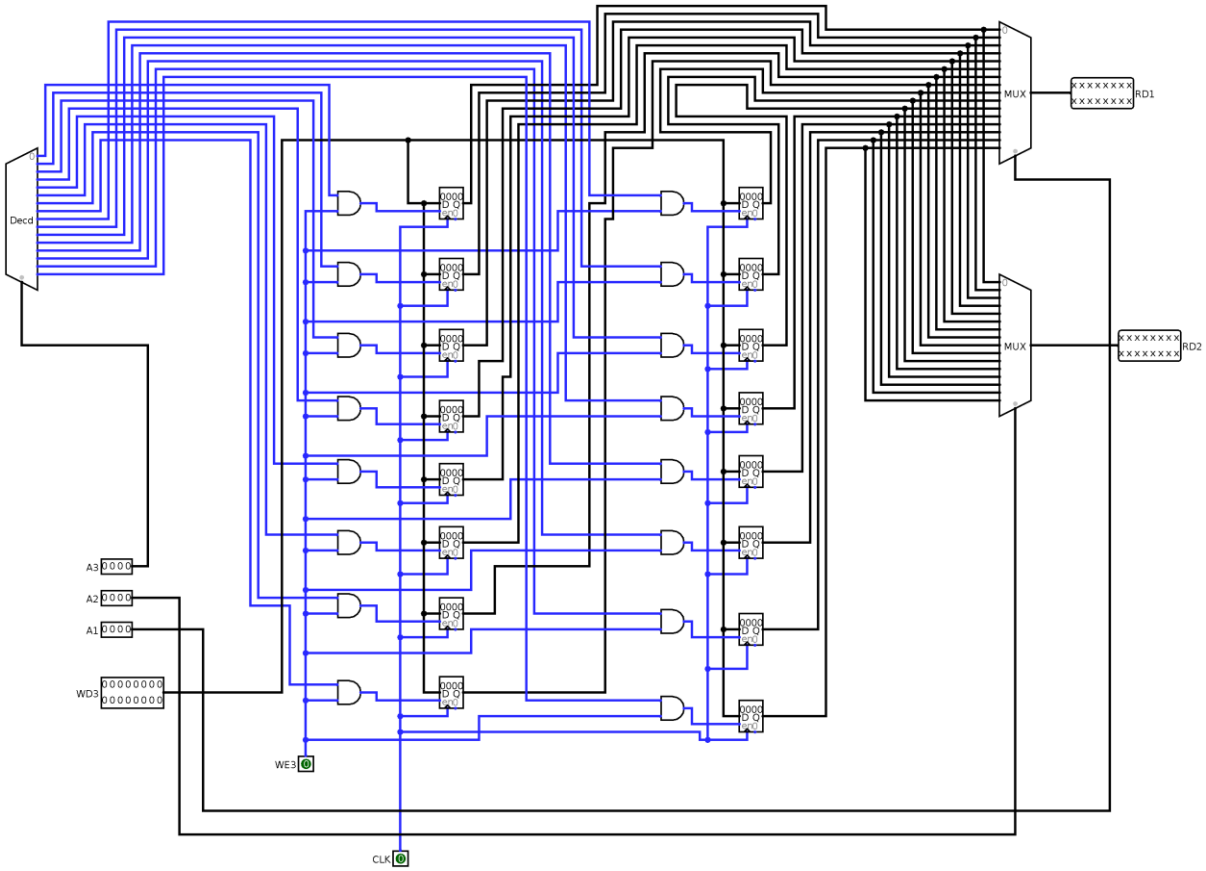
	Op	ALUControl	BrControl	JmpControl	RegWrite	MemWrite	BrSelect	A3Select	WD3Select
jmp	000	x	0	1	0	0	x	x	x
lc	001	x	0	0	1	0	x	1	01
ld	010	x	0	0	1	0	x	1	10
sd	011	x	0	0	0	1	x	x	x

2.8. COMBINED DATAPATHS

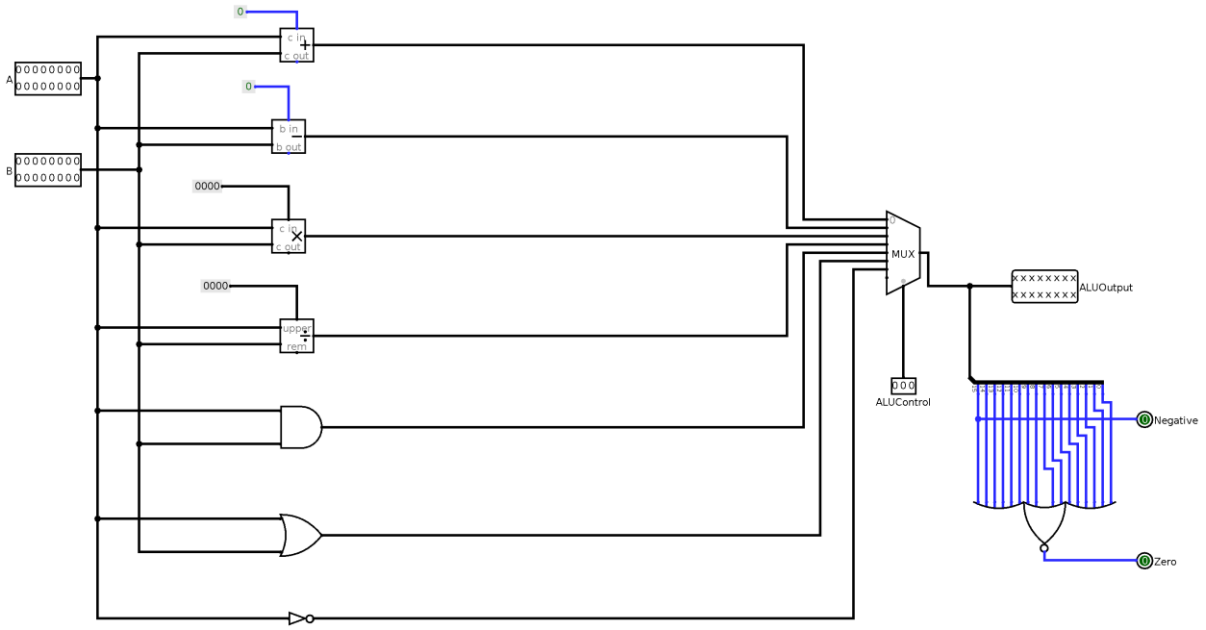


2.9. COMPONENTS BUILT IN LOGISIM

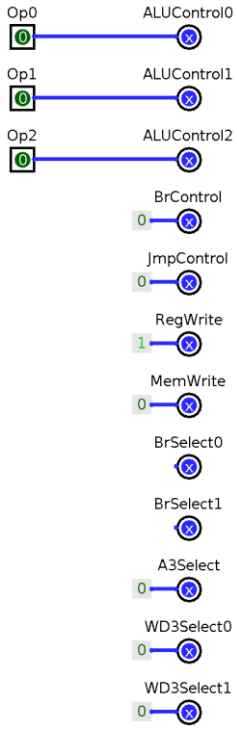
2.7.1. REGISTERFILE


Decd
MUX
RD1
MUX
RD2
A3
A2
A1
WD3
WE3
CLK

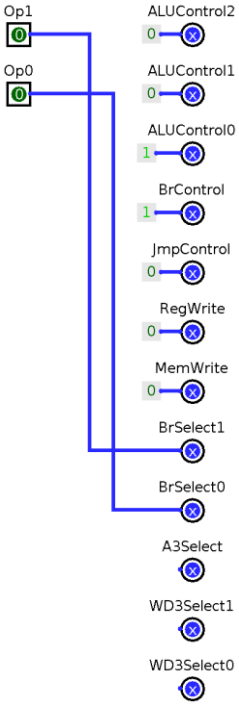
2.7.2. ALU


0
A
0
B
0000
0000
MUX
ALUOutput
ALUControl
Negative
Zero

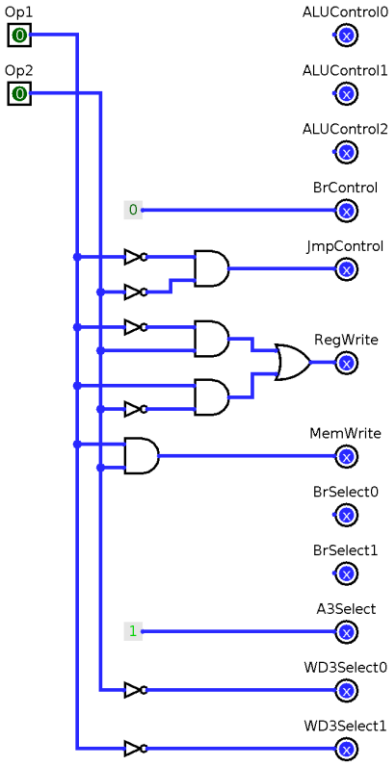
2.7.3. A TYPE CONTROL UNIT



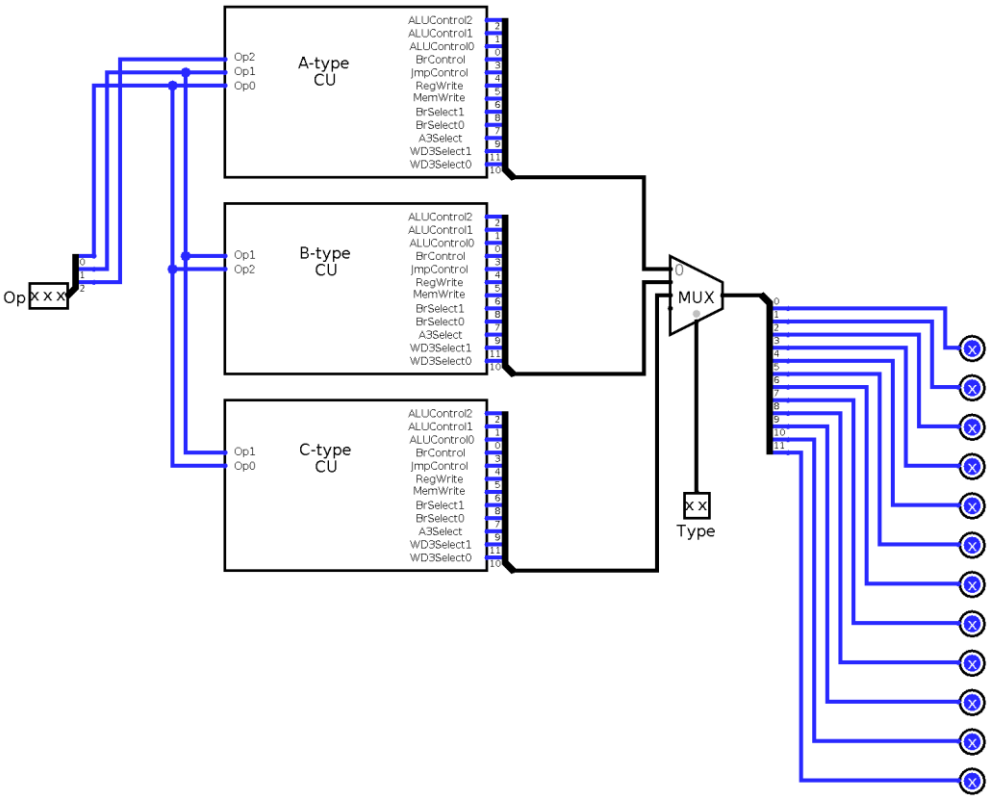
2.7.4. B TYPE CONTROL UNIT



2.7.5. C TYPE CONTROL UNIT



2.7.6. COMBINED CONTROL UNIT



2.7.7. COMPLETE MICROPROCESSOR CIRCUIT