

**CSE 331 COMPUTER
ORGANIZATION**

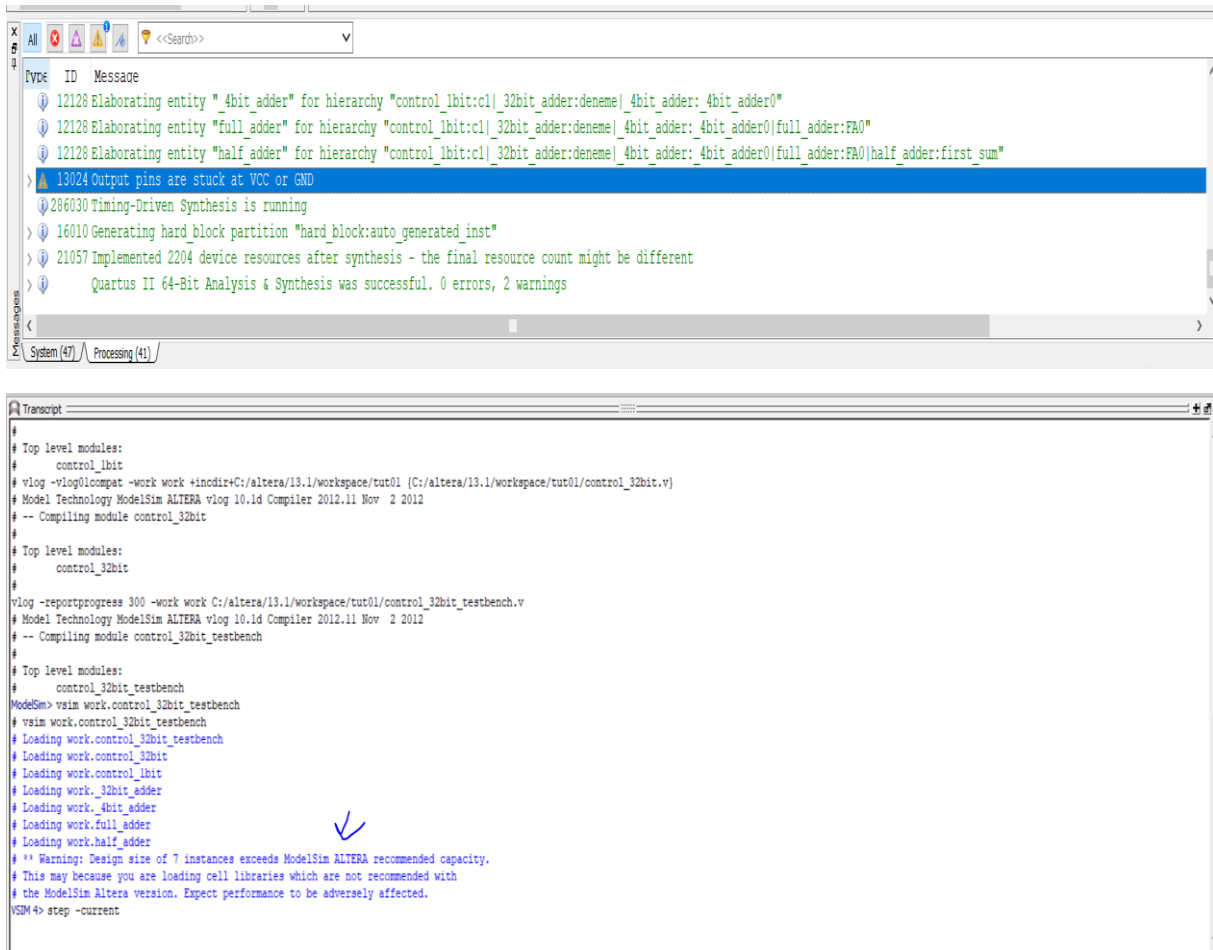
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1901042262

PART1:

Control1bit and control32bit.

Sir, I made part1 over the internet from an online compiler. When I run it on Modelsim, it gave a warning and didn't work. I still uploaded it. It says modelsim is not supported.



The image shows two screenshots from the ModelSim software interface. The top screenshot displays the 'Messages' window, which lists various messages during the compilation and synthesis process. A warning message is highlighted in blue: '13024 Output pins are stuck at VCC or GND'. Other messages include elaborating entities, timing-driven synthesis, and successful synthesis results with 0 errors and 2 warnings.

The bottom screenshot displays the 'Transcript' window, showing the command-line output of the ModelSim compiler. It includes the following text:

```
# Top level modules:
#   control_1bit
# vlog -vlog01compat -work work +inodir=C:/altera/13.1/workspace/tut01 (C:/altera/13.1/workspace/tut01/control_32bit.v)
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module control_32bit
#
# Top level modules:
#   control_32bit
#
vlog -reportprogress 300 -work work C:/altera/13.1/workspace/tut01/control_32bit_testbench.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module control_32bit_testbench
#
# Top level modules:
#   control_32bit_testbench
# ModelSim> vsim work.control_32bit_testbench
# vsim work.control_32bit_testbench
# Loading work.control_32bit_testbench
# Loading work.control_32bit
# Loading work.control_1bit
# Loading work._32bit_adder
# Loading work._4bit_adder
# Loading work.full_adder
# Loading work.half_adder
# ** Warning: Design size of 7 instances exceeds ModelSim ALTERA recommended capacity.
# This may because you are loading cell libraries which are not recommended with
# the ModelSim Altera version. Expect performance to be adversely affected.
VSIOM 4> step -current
```

A blue arrow points to the warning message in the transcript window.

PART2

1-)32 BIT ADDER

First the half adder was designed. then a full adder was made from a half adder. then 4_bit_adder was made using full adder. Then 32_bit_adder was designed using 8 4_bit_adders.

```
Transcript
vlog -reportprogress 300 -work work C:/altera/13.1/workspace/tut01/_32bit_adder_testbench.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module _32bit_adder_testbench
#
# Top level modules:
#   _32bit_adder_testbench
ModelSim> vsim work._32bit_adder_testbench
# vsim work._32bit_adder_testbench
# Loading work._32bit_adder_testbench
# Loading work._32bit_adder
# Loading work._4bit_adder
# Loading work.full_adder
# Loading work.half_adder
VSM> step -current
# time = 0, a =          00000000, b=          ffffffff, answer=          ffffffff
# time = 20, a =          ffffffff, b=          ffffffff, answer=          ffffffff
# time = 40, a =          0003ffff, b=          ffffffff, answer=          0003ffff
# time = 60, a =          0003ffff, b=          00000000, answer=          0003ffff
VSM> step -current
VSM>
```

2-)XOR

32 1-bit xor operations were performed using for.

```
Transcript
#
# Top level modules:
#   _32bit_xor
#
vlog -reportprogress 300 -work work C:/altera/13.1/workspace/tut01/_32bit_xor_testbench.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module _32bit_xor_testbench
#
# Top level modules:
#   _32bit_xor_testbench
ModelSim> vsim work._32bit_xor_testbench
# vsim work._32bit_xor_testbench
# Loading work._32bit_xor_testbench
# Loading work._32bit_xor
VSM> step -current
# time = 0, a =00000000000000000000000000000000, b=11111111111111111111111111111111, answer=11111111111111111111111111111111
# time = 20, a =11111111111111111111111111111111, b=11111111111111111111111111111111, answer=00000000000000000000000000000000
# time = 40, a =00000000000000000000000000000000, b=11111111111111111111111111111111, answer=11111111111111111111111111111111
# time = 60, a =00000000000000000000000000000000, b=00000000000000000000000000000000, answer=00000000000000000000000000000000
```

3-)SUB

After performing the not operation on the 2nd input, addition(32bitadder) the 2nd input with the 1st input was called.

```
Transcript
vlog -reportprogress 300 -work work C:/altera/13.1/_32bit_sub_testbench.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov 2 2012
# -- Compiling module _32bit_sub_testbench
#
# Top level modules:
#   _32bit_sub_testbench
#
# vsim work._32bit_sub_testbench
# Loading work._32bit_sub_testbench
# Loading work._32bit_sub
# Loading work._32bit_adder
# Loading work._4bit_adder
# Loading work.full_adder
# Loading work.half_adder
VSM4> step -current
# time = 0, a = 00000000000000000000000000000000, b=11111111111111111111111111111111, answer=00000000000000000000000000000001
# time = 20, a = 11111111111111111111111111111111, b=11111111111111111111111111111111, answer=00000000000000000000000000000000
# time = 40, a = 00000000000000000000000000000001, b=11111111111111111111111111111111, answer=00000000000000000000000000000000
# time = 60, a = 00000000000000000000000000000001, b=00000000000000000000000000000000, answer=00000000000000000000000000000000
```

4-)SLT

Subtracts 2 numbers and returns the number in bit 32 as the result

```
Transcript
vlog -reportprogress 300 -work work C:/altera/13.1/workspace/tut01/_32bit_slr_testbench.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov 2 2012
# -- Compiling module _32bit_slr_testbench
#
# Top level modules:
#   _32bit_slr_testbench
#
# vsim work._32bit_slr_testbench
# Loading work._32bit_slr_testbench
# Loading work._32bit_slr
# Loading work._32bit_sub
# Loading work._32bit_adder
# Loading work._4bit_adder
# Loading work.full_adder
# Loading work.half_adder
VSM4> step -current
# time = 0, a = 11111111, b= 99999999, result=0
# time = 20, a = 99999999, b= 11111111, result=1
# time = 40, a = 11111111, b= 11111111, result=0
```

5-)NOR

32 1-bit nor operations were performed using for.

```
Transcript
#
# Top level modules:
#   _32bit_nor
#
# vlog -reportprogress 300 -work work C:/altera/13.1/workspace/tut01/_32bit_nor_testbench.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov 2 2012
# -- Compiling module _32bit_nor_testbench
#
# Top level modules:
#   _32bit_nor_testbench
#
# vsim work._32bit_nor_testbench
# Loading work._32bit_nor_testbench
# Loading work._32bit_nor
VSM4> step -current
# time = 0, a = 00000000000000000000000000000000, b=11111111111111111111111111111111, answer=00000000000000000000000000000000
# time = 20, a = 11111111111111111111111111111111, b=11111111111111111111111111111111, answer=00000000000000000000000000000000
# time = 40, a = 00000000000000000000000000000001, b=11111111111111111111111111111111, answer=00000000000000000000000000000000
# time = 60, a = 00000000000000000000000000000001, b=00000000000000000000000000000000, answer=11111111111111111111111111111111
```

6-)AND

32 1-bit and operations were performed using for.

```
Transcript
#
# Top level modules:
#   _32bit_and
#
vlog -reportprogress 300 -work work C:/altera/13.1/workspace/tut01/_32bit_and_testbench.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module _32bit_and_testbench
#
# Top level modules:
#   _32bit_and_testbench
ModelSim> vsim work._32bit_and_testbench
# vsim work._32bit_and_testbench
# Loading work._32bit_and_testbench
# Loading work._32bit_and
VSM4> step -current
# time = 0, a = 00000000000000000000000000000000, b = 11111111111111111111111111111111, answer = 00000000000000000000000000000000
# time = 20, a = 11111111111111111111111111111111, b = 11111111111111111111111111111111, answer = 11111111111111111111111111111111
# time = 40, a = 00000000000000000000000000000000, b = 11111111111111111111111111111111, answer = 00000000000000000000000000000000
# time = 60, a = 00000000000000000000000000000000, b = 00000000000000000000000000000000, answer = 00000000000000000000000000000000
```

7-)OR

32 1-bit or operations were performed using for.

```
Transcript
#
# Top level modules:
#   _32bit_or
#
vlog -reportprogress 300 -work work C:/altera/13.1/workspace/tut01/_32bit_or_testbench.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module _32bit_or_testbench
#
# Top level modules:
#   _32bit_or_testbench
ModelSim> vsim work._32bit_or_testbench
# vsim work._32bit_or_testbench
# Loading work._32bit_or_testbench
# Loading work._32bit_or
VSM4> step -current
# time = 0, a = 00000000000000000000000000000000, b = 11111111111111111111111111111111, answer = 11111111111111111111111111111111
# time = 20, a = 11111111111111111111111111111111, b = 11111111111111111111111111111111, answer = 11111111111111111111111111111111
# time = 40, a = 00000000000000000000000000000000, b = 11111111111111111111111111111111, answer = 11111111111111111111111111111111
# time = 60, a = 00000000000000000000000000000000, b = 00000000000000000000000000000000, answer = 00000000000000000000000000000000
```

8-)MUX32bit

32 1bit 8e3 muxes are used.

```
Transcript
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module mux_32bit
#
# Top level modules:
#   mux_32bit
#
vlog -reportprogress 300 -work work C:/altera/13.1/workspace/tut01/_32bit_mux_testbench.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module _32bit_mux_testbench
#
# Top level modules:
#   _32bit_mux_testbench
ModelSim> vsim work._32bit_mux_testbench
# vsim work._32bit_mux_testbench
# Loading work._32bit_mux_testbench
# Loading work.mux_32bit
# Loading work.mux_1bit
VSM4> step -current
# time = 0, RESULT=11111111111111111111111111111111
```

9-)ALU

[illegible]