

Projektgruppe FastSense

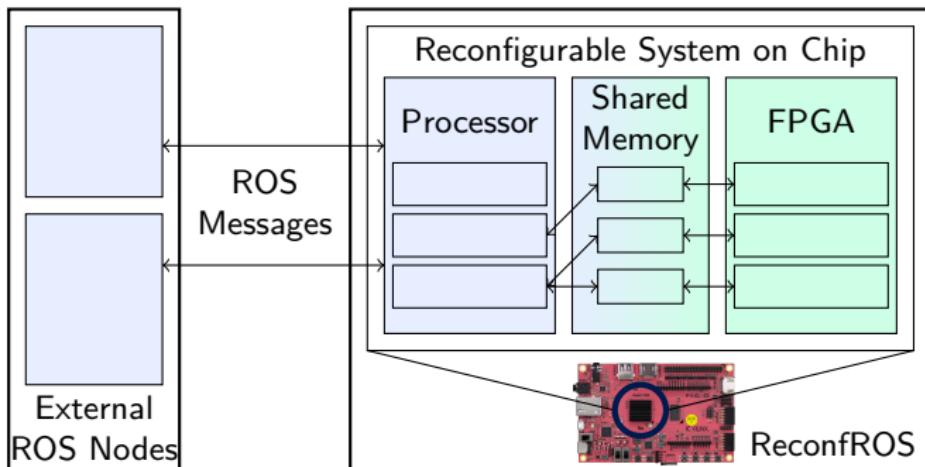
Abschlusspräsentation

11. März 2021

Zielsetzung

- Autonome echtzeitfähige Kartierung
- FPGA-basierte Hardwarebeschleunigung
- Einfaches, handliches System
- Anbindung an bestehende Systeme (LVR2)

MS1: Trail Detection



Camera image



Removing noise



Trail pixel extraction



Thresholding

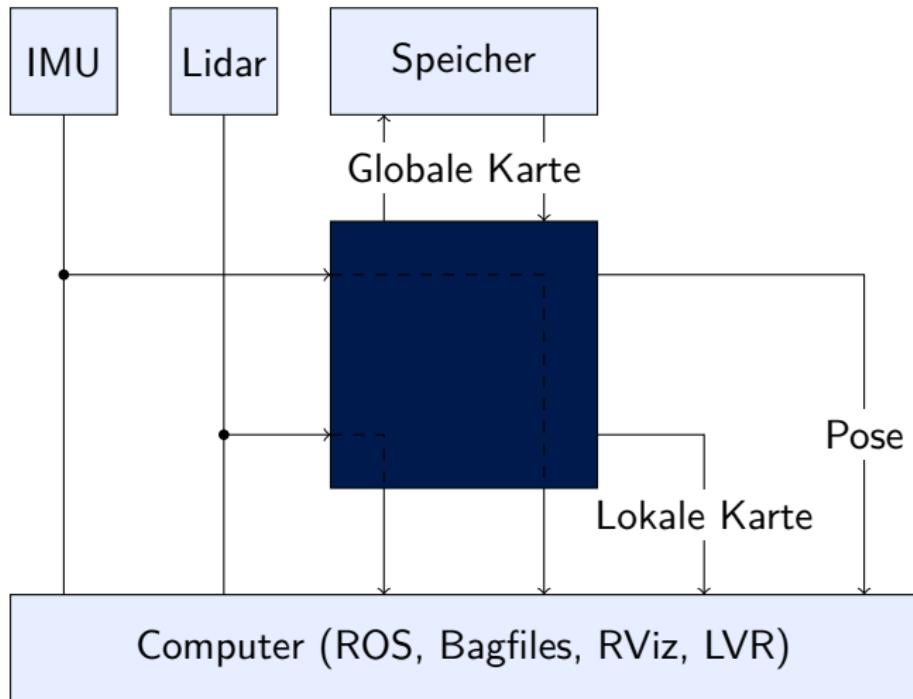


Remove fragments

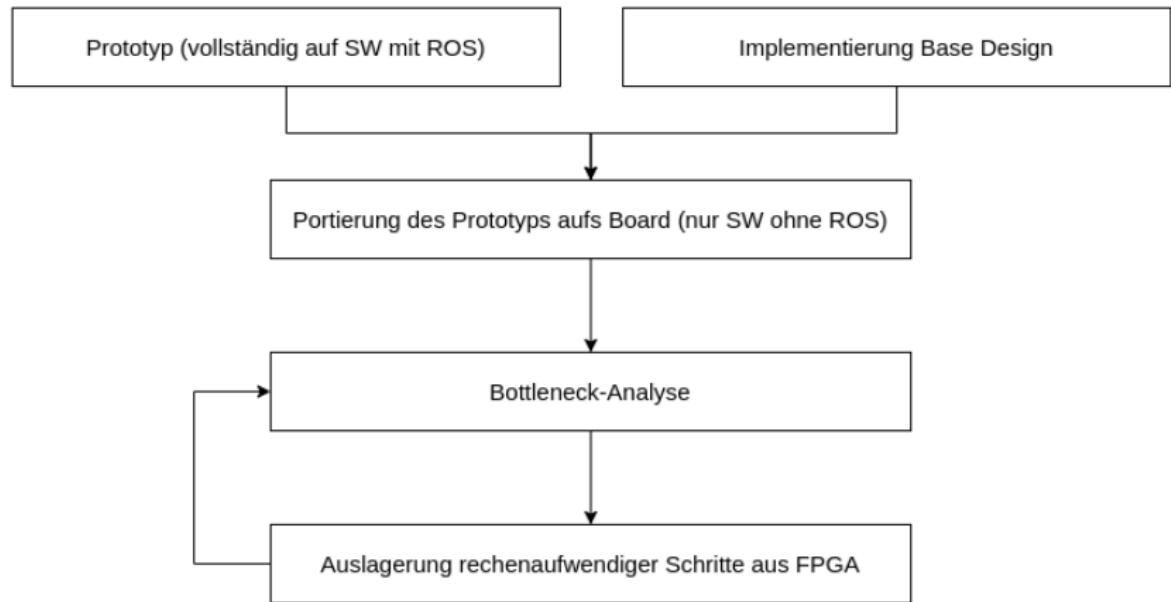


Trail direction

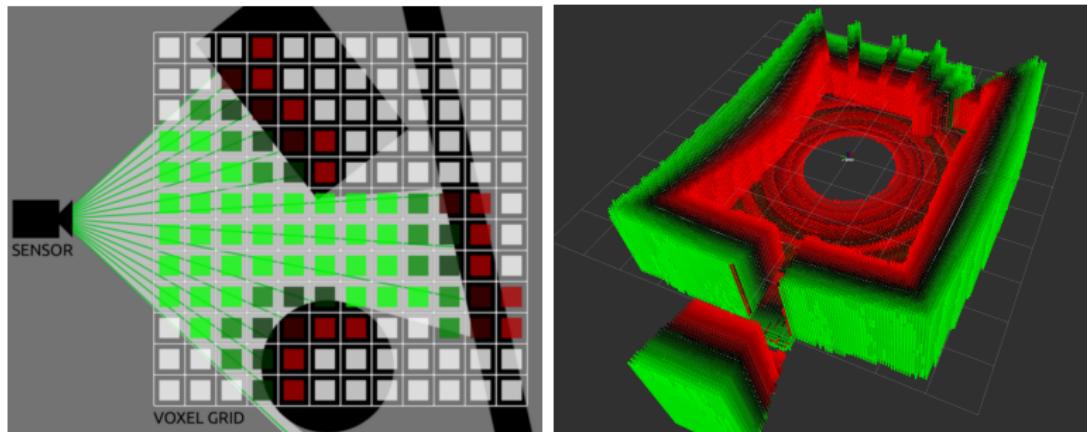
SLAM-Box



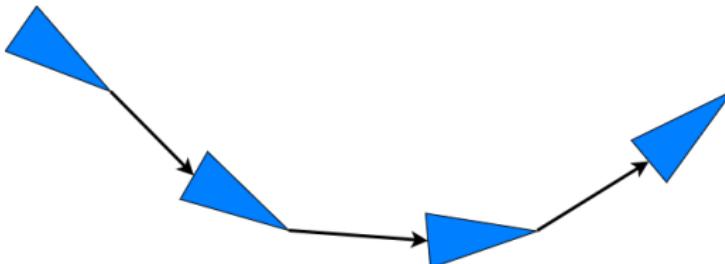
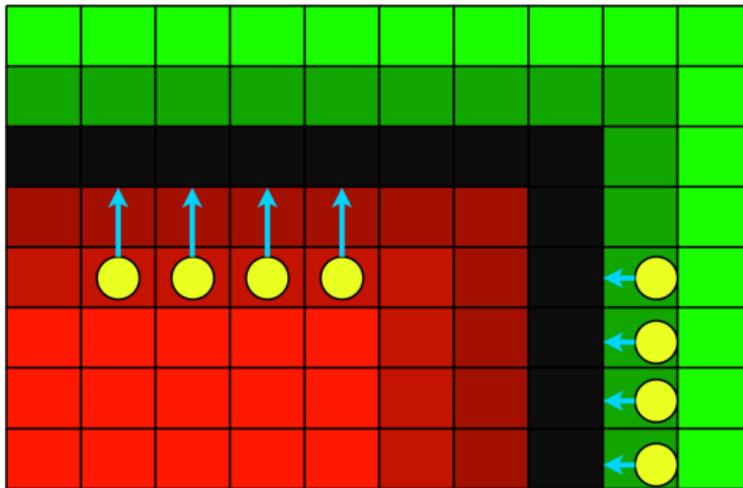
Vorgehen



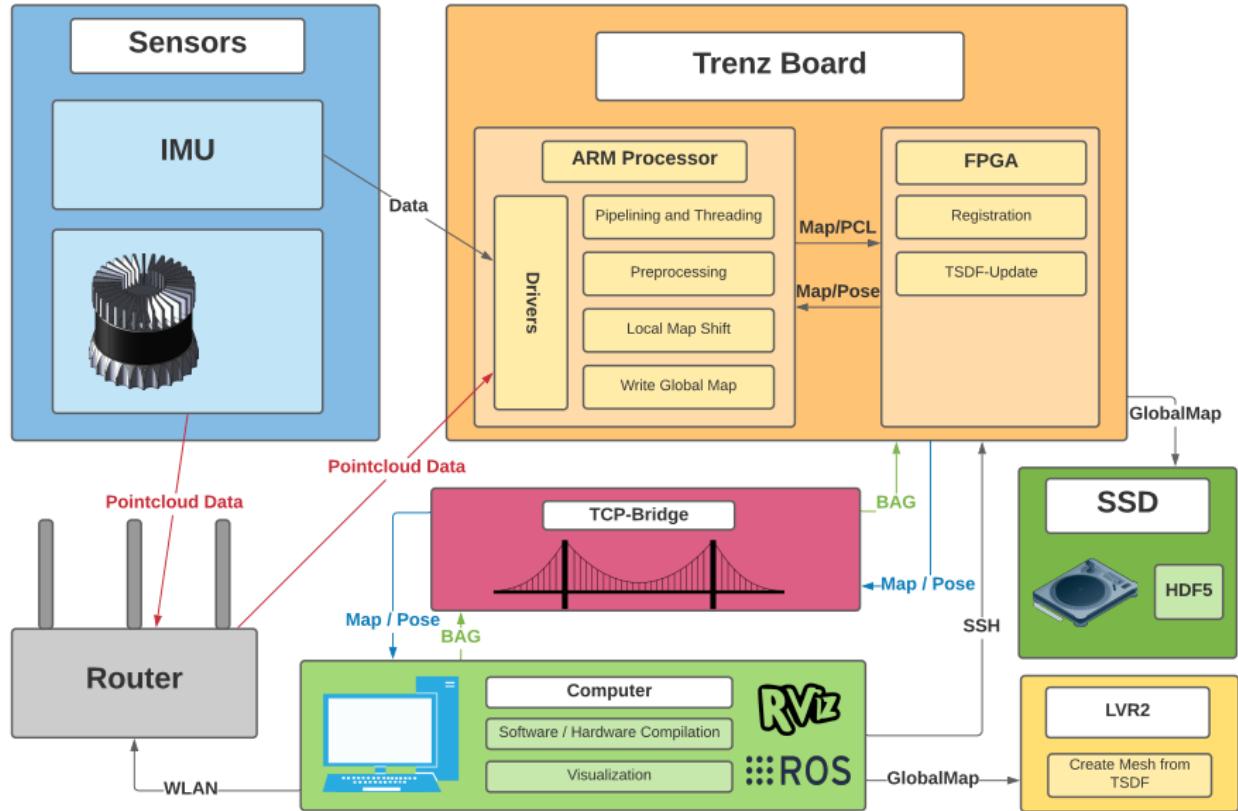
TSDF



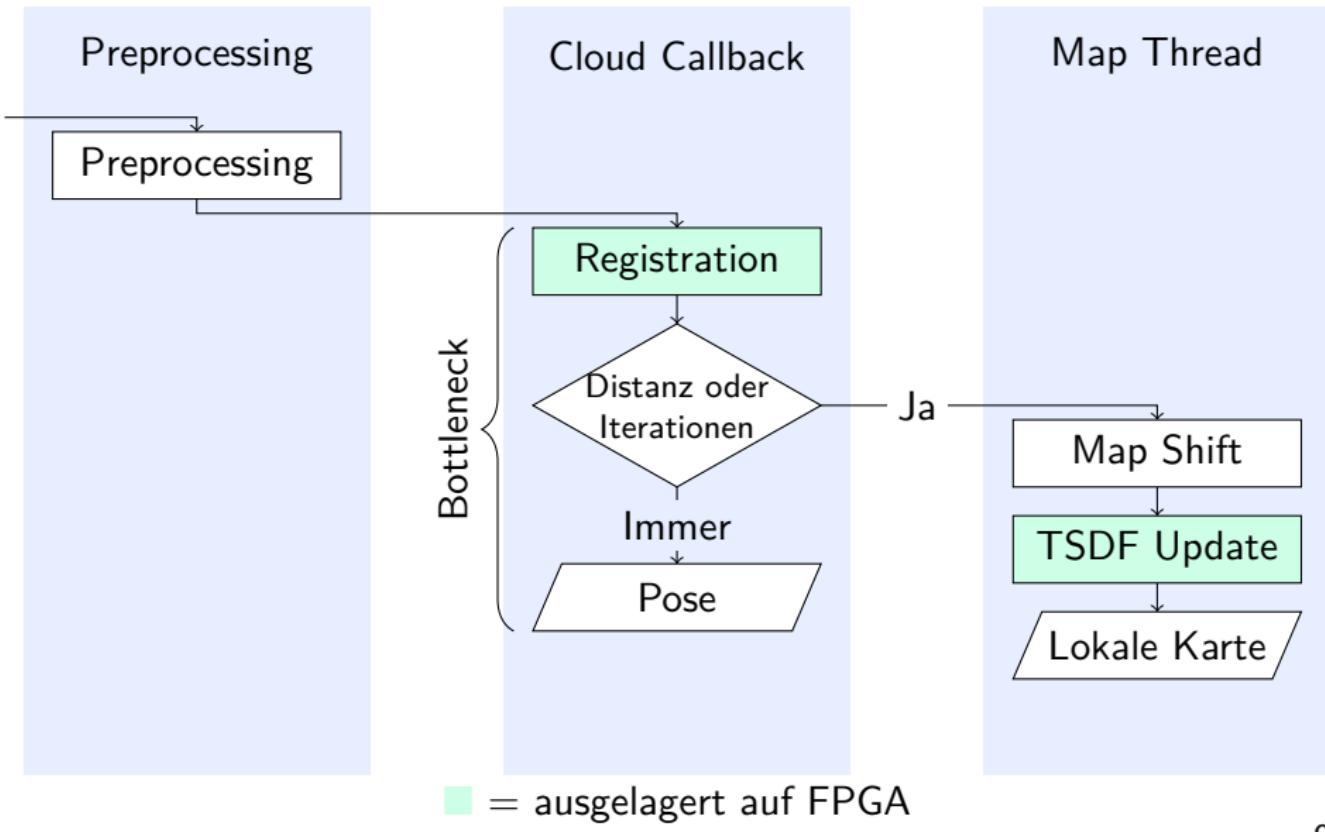
Point-to-TSDF Registrierung



Komponenten

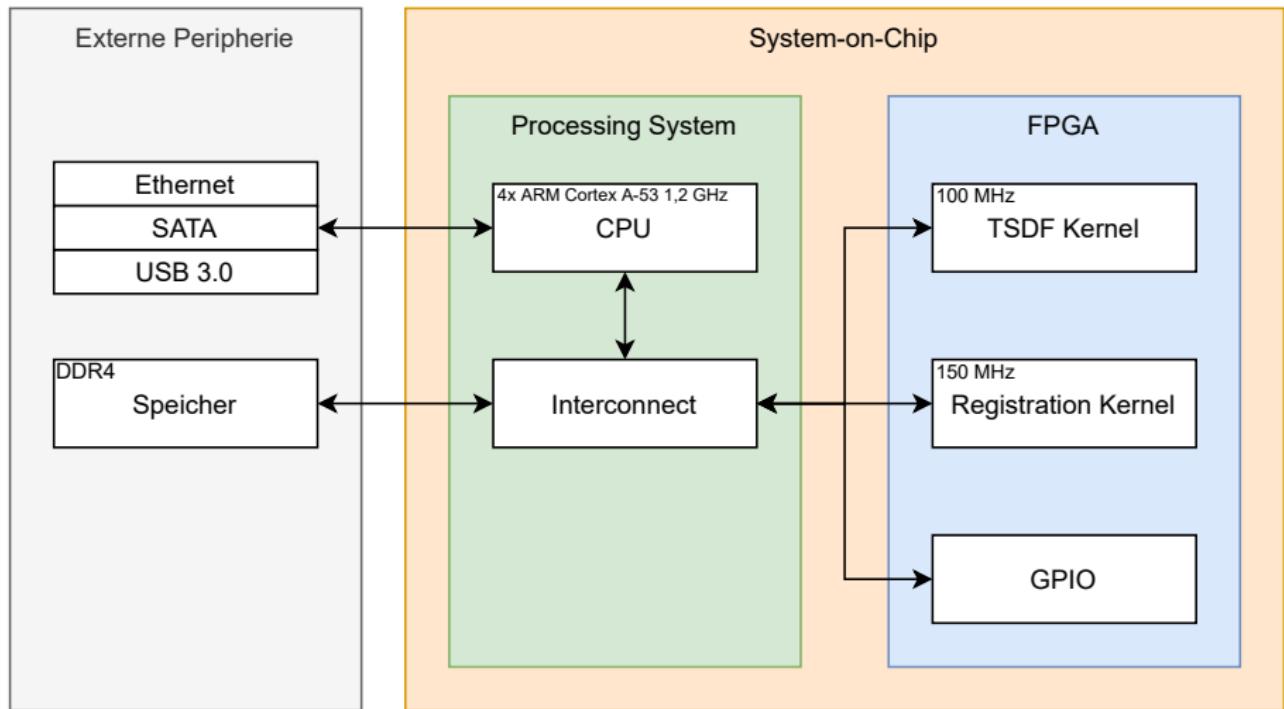


Algorithmus

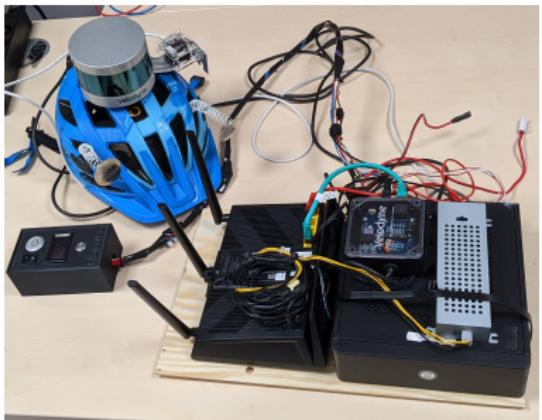
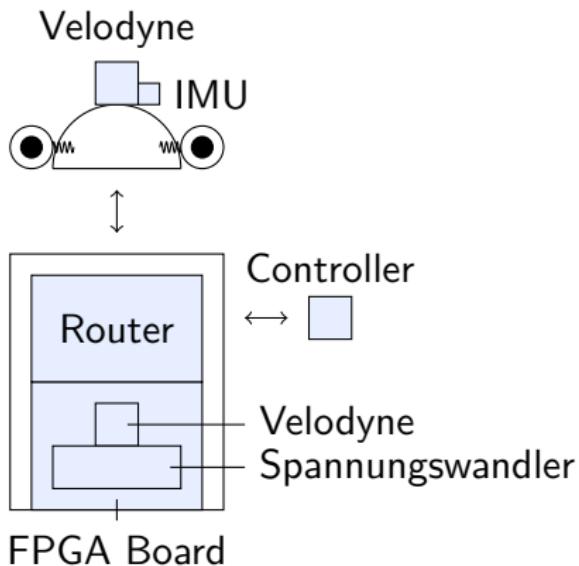


= ausgelagert auf FPGA

Hardware Architektur

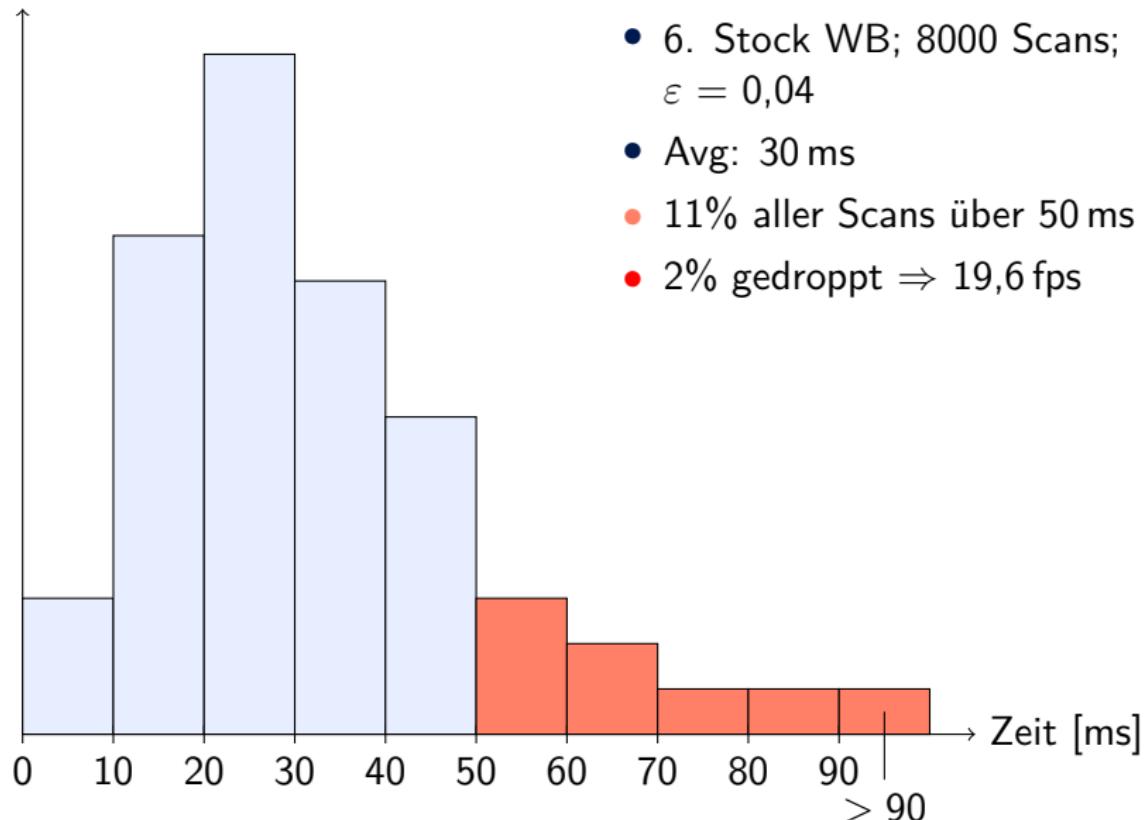


Aufbau



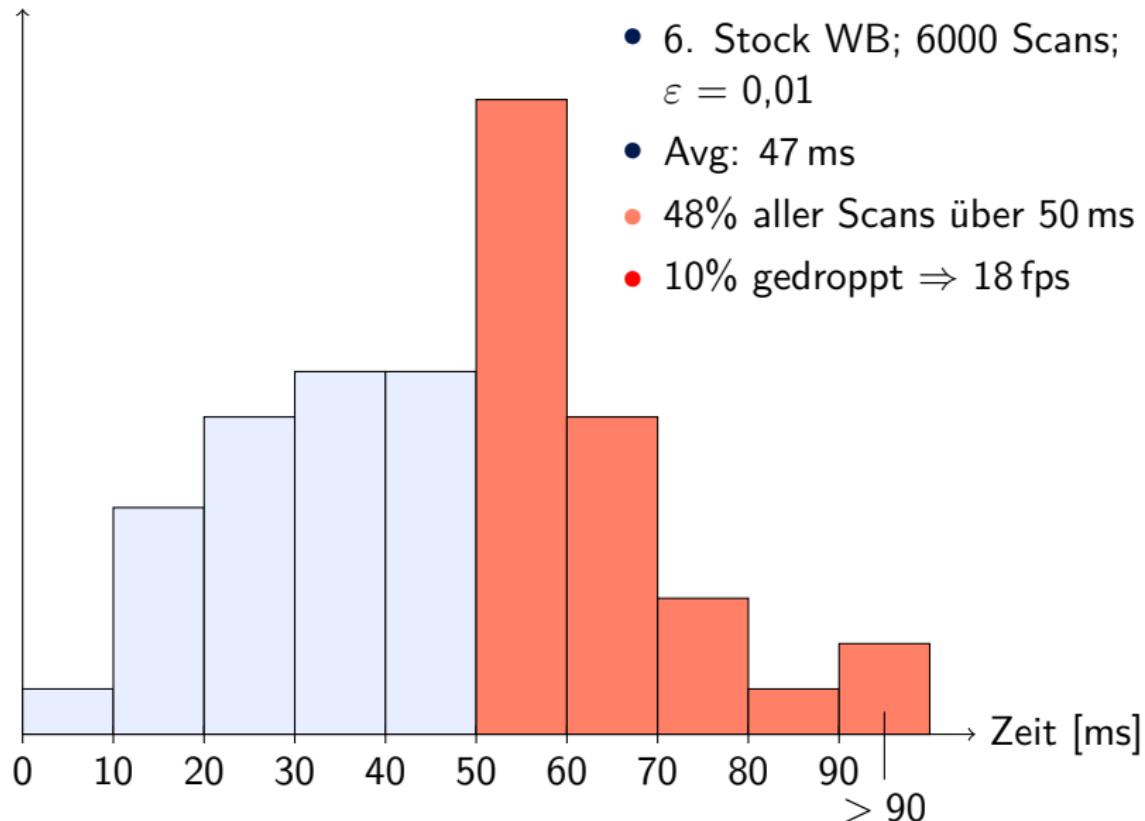
Evaluation: Zeit

Anzahl Scans

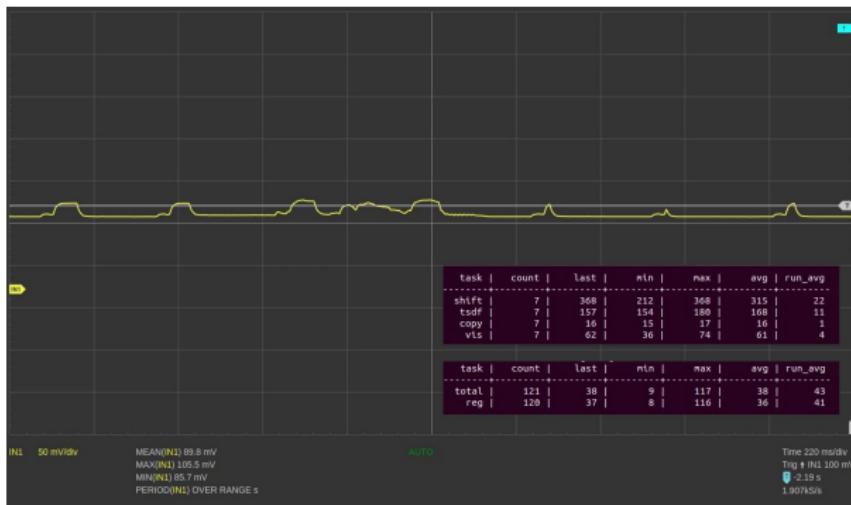


Evaluation: Zeit

Anzahl Scans



Evaluation: Power Consumption



	Idle			Running		
	Mean	Min	Max	Mean	Min	Max
U [mV]	78,7	76	88	89,8	85,7	105,5
I [A]	1,124	1,086	1,257	1,283	1,224	1,507
P [W]	13,488	13,032	15,084	15,396	14,688	18,084

Evaluation: Genauigkeit

- 6. Stockwerk (Distanz in Meter, Auflösung: 6,4cm)

ε	0,01	0,04
	0,0615	0,0505
Geschw.	langsam	schnell
	0,0505	0,0437

- gesamt (langsam, $\varepsilon = 0,04$, Strecke $\approx 270\text{m}$): 0,075349
- 8 Meter Labortest (Distanz in Meter, Auflösung: 6,4cm)

	hin	zurück	gesamt
langsam	0,0548	0,0650	0,0861
schnell	0,1676	0,0459	0,1320

Fazit

- Portables System
- Weiche Echtzeitfähigkeit
- Geringer Stromverbrauch
- Einfache Handhabung
- Einfache Analyse

Ausblick

- Evaluierung mit anderer Sensorik
- Portierung auf Drohne
- Optimierung des Posegraphen (Loop Closing)
- Paper