1. General description

The NJJ29C0B is a joint LF driver and receiver IC with embedded μController. It provides 6 full-bridge LF driver channels and a single receiver to support a shared PKE/immo coil. The device is designed and ideally suited for automotive applications with keyless entry / start functions and can be easily integrated into vehicle electronic control modules.

The device operates at 125 kHz supporting NXP transponders employing amplitude shift keying (ASK) for write and read operation. In order to establish the desired LF field, the needed antenna driver current can be selected separately for each channel.

The differential immobilizer receiver features a high sensitivity and common mode noise immunity to provide a large transponder operating range.

The powerful drivers in combination with the integrated boost converter ensure that the selected current is driven over a wide antenna impedance range, offering high flexibility in the system design.

The NJJ29C0B features a high degree of integration, and hence requires a very low external component count. Integrated voltage regulators generate all required device supplies directly from the vehicles battery.

An integrated 16-bit μController is powered by NXP's 3rd generation low power μController kernel (MRKIIIe). Configuration, settings and data exchange are performed via an SPI slave port with pre-defined command set. A single monitor line is asserted when the NJJ29C0B requires service from the SPI master μC (e.g. in response to an over temperature shutdown).

Wake-up telegram data for each channel can be stored in RAM, transmission of which can be configured to occur autonomously in response to door handle sensor trigger events, thus significantly reducing the system latency time. Stored telegram data can also be used to support autonomous sending of LF telegrams in response to polling timer trigger events for welcome light type applications.

Sophisticated diagnostics functions detect and register either open antennas, antennas shorted to GND or VBAT and inter-antenna shorts. Device overheating is prevented by on-chip temperature monitoring with thermal overload shutdown.

The device comes in a 56 pin HVQFN package with wettable flanks.

2. Features and benefits

2.1 General

- 6 LF full-bridge drivers
- On-chip DC/DC supply boost
- Current regulation to establish constant LF field
- Wide antenna impedance range Z_{ANT} = 10…20 Ohm (higher and lower impedances possible with limited antenna driver current range or accuracy, respectively)
- Class D* implementation for low internal power dissipation
- Differential receiver input for high noise immunity
- High receiver sensitivity for large immobilizer operating range
- Shared coil support for transponder receiver
- Integrated 16-bit µController supporting powerful SPI protocol
- Low number of external components
- Lowest electromagnetic emission (EME) in full bridge mode with midlevel control
- Low power consumption
- Wide supply voltage range from 5 V to 28 V
- Device control via SPI commands
- Small outline package HVQFN56 (wettable flanks)

2.2 Antenna drivers

- 6 LF full-bridge drivers
- Max. LF driver differential peak-peak output voltage 50 V
- Channel driver peak current capability 6*1 A (peak-peak 6*2 A)
- Simultaneous operation of up to 3 channels with peak currents up to 1 A each
- ASK support up to 8 kbit/s
- BPLM support for transponder operation

2.3 Boost converter

- Output voltage
  - up to 25 V for PKE
  - up to 30 V for immo

2.4 Current control

- Sinusoidal antenna currents for low EME (resonant circuit with high Q-factor)
- Class D* antenna drive voltage for low internal power dissipation
- Up to 64 linear current steps (lower steps absent dependent on antenna impedance)
- Absolute accuracy ± 3% ± 20 mA (high current range) to ± 4% ± 20 mA (low current range)
- Current control via PWM duty cycle and boost converter voltage control

2.5 Immobilizer receiver

- Shared coil operation
- Differential input stage
- ASK demodulator

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- Manchester decoder
- Digital baseband signal processing

2.6 Telegram sequencer & data buffer

- Telegram LF transmission sequencer
- Autonomous transmission of pre-defined LF telegrams, triggered by wake-up port events or dedicated timer (e.g. polling for welcome light applications)
- Configurable polling sequence for maximum flexibility
- Data buffers to store wake-up pattern and telegram data

2.7 Protection & shut down

- Battery voltage protection
- Thermal overload protection
- Boost converter protection
- LF driver protection
- RAM parity check
- Indicated to the application by flag

2.8 Diagnostics

- Sophisticated antenna diagnostics (e.g. open/short and inter antenna short detection)
- On-chip temperature monitoring
- Executed on command

2.9 µController (MRKIIIe)

- 16 Bit architecture
- Short instruction execution time
- Handles SPI driven application
- Enables autonomous applications (e.g. polling timer)

2.10 Peripherals

- SPI interface
- 6 wake-up inputs (e.g. for sensor interfaces)
- Timer unit (e.g. for timer triggered polling)
- Status monitor output (e.g. for protection event indication)
- Reset input

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3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
NJJ29C0B	HVQFN56	Plastic thermal enhanced very thin quad flat package, body 8 x 8 x 0.85 mm	SOT684

4. Block diagram

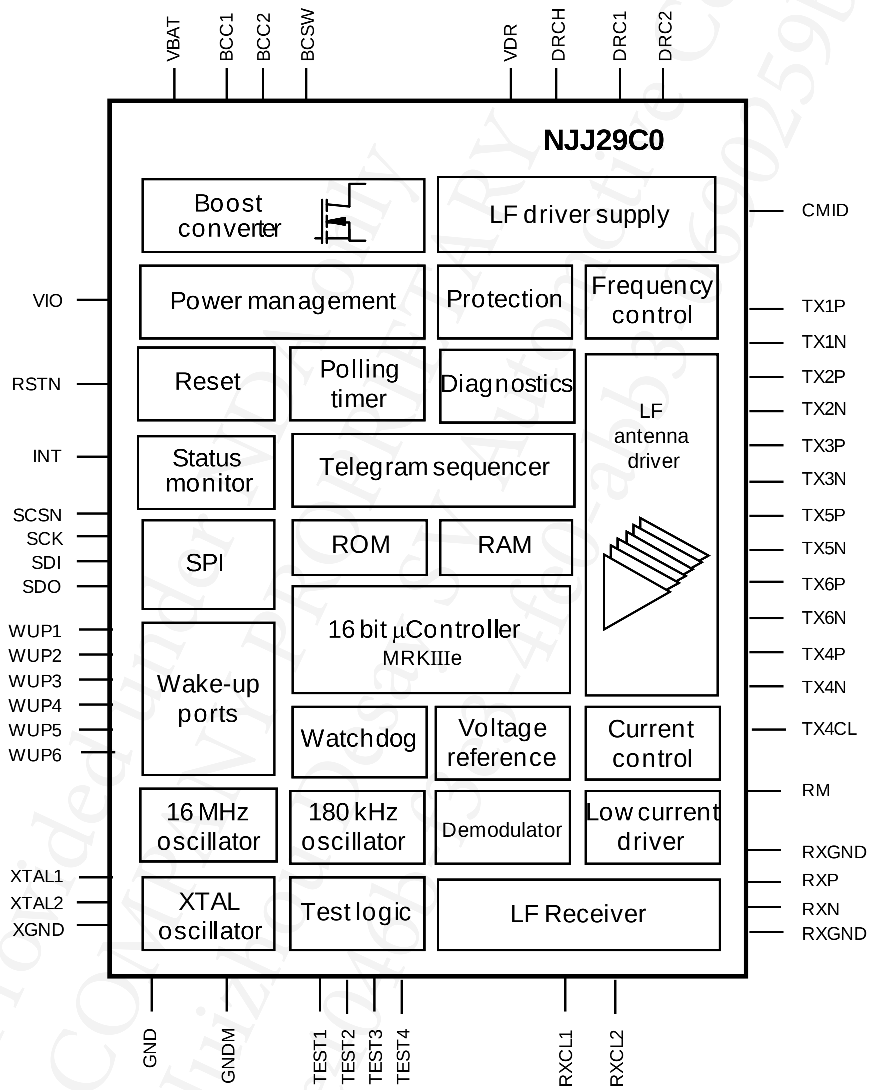

Fig 1. JOKER block diagram

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5. Pinning information

5.1 Pinning

The pin configuration of the NJJ29C0B in HVQFN56 package is shown in Fig 2.

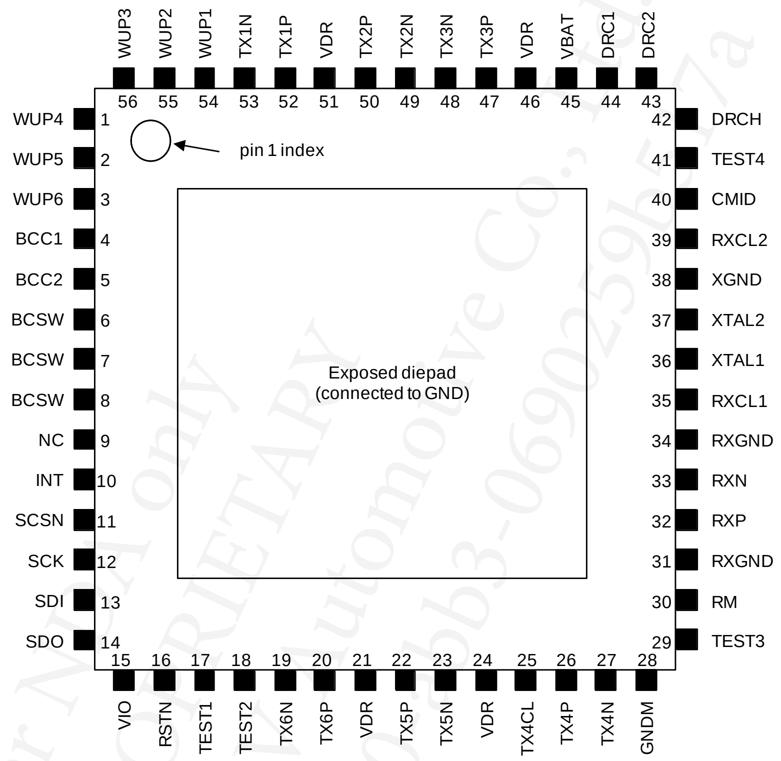

Fig 2. Pin configuration

The exposed die pad of the NJJ29C0B is internally connected to the GND pin and used as common ground for the device.

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
WUP4	1	Wake input	Input with wake-up sense 4, connect to GND if unused
WUP5	2	Wake input	Input with wake-up sense 5, connect to GND if unused
WUP6	3	Wake input	Input with wake-up sense 6, connect to GND if unused
BCC1	4	N.A.	Boost converter, connect to capacitor
BCC2	5	N.A.	Boost converter GND, connect to GND and capacitor
BCSW	6,7,8	N.A.	Boost converter switch, connect to coil and diode
NC	9	N.A.	Not connected
INT	10	Digital output	Interrupt output
SCSN	11	Digital input	SPI chip select not

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Symbol	Pin	Type	Description
SCK	12	Digital input	SPI serial clock
SDI	13	Digital input	SPI data in
SDO	14	Digital output	SPI data out
VIO	15	Supply input	Supply voltage for I/O interface
RSTN	16	Digital input	Reset input active low
TEST1	17	Digital input	Test terminal, unconnected in the application
TEST2	18	Digital output	Test terminal, unconnected in the application
TX6N	19	Analog output	Transmitter 6 negative output (LF antenna driver 6)
TX6P	20	Analog output	Transmitter 6 positive output (LF antenna driver 6)
VDR	21,24,46,51	Supply input	Supply voltage for LF driver
TX5P	22	Analog output	Transmitter 5 positive output (LF antenna driver 5)
TX5N	23	Analog output	Transmitter 5 negative output (LF antenna driver 5)
TX4CL	25	N.A.	Transmitter 4, connect to capacitor
TX4P	26	Analog output	Transmitter 4 positive output (LF antenna driver 4), shared with immo
TX4N	27	Analog output	Transmitter 4 negative output (LF antenna driver 4), shared with immo
GNDM[1]	28	Supply input	Ground potential sense (common ground)
TEST3	29	Digital input	Test terminal, connect to GND
RM	30	N.A.	LF current measurement, connect to resistor
RXGND	31,34	Supply input	Receiver shielding, connect to ground potential
RXP	32	Analog input	Receiver positive input
RXN	33	Analog input	Receiver negative input
RXCL1	35	N.A.	Receiver, connect to capacitor
XTAL1	36	N.A.	XTAL oscillator, connect to XTAL
XTAL2	37	N.A.	XTAL oscillator, connect to XTAL
XGND[1]	38	N.A.	XTAL GND, connect to XTAL load capacitors
RXCL2	39	N.A.	Receiver, connect to capacitor
CMID	40	N.A.	Bridge mid level, connect to capacitors
TEST4[2]	41	Analog input	Test terminal, unconnected in the application
DRCH	42	N.A.	LF driver, connect to capacitor
DRC2	43	N.A.	LF driver, connect to capacitor
DRC1	44	N.A.	LF driver, connect to capacitor
VBAT	45	Supply input	Battery supply voltage for device
TX3P	47	Analog output	Transmitter 3 positive output (LF antenna driver 3)
TX3N	48	Analog output	Transmitter 3 negative output (LF antenna driver 3)
TX2N	49	Analog output	Transmitter 2 negative output (LF antenna driver 2)
TX2P	50	Analog output	Transmitter 2 positive output (LF antenna driver 2)
TX1P	52	Analog output	Transmitter 1 positive output (LF antenna driver 1)
TX1N	53	Analog output	Transmitter 1 negative output (LF antenna driver 1)
WUP1	54	Wake input	Input with wake-up sense 1, connect to GND if unused
WUP2	55	Wake input	Input with wake-up sense 2, connect to GND if unused

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Symbol	Pin	Type	Description
WUP3	56	Wake input	Input with wake-up sense 3, connect to GND if unused

[1] Not suitable as single ground connection for the device

[2] An internal diode is connected between TEST4 and XGND to enable temperature characterization. Driving an external current (range 1μA to 10μA) through this diode and measuring the voltage drop the die temperature can be monitored.

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6. Functional description

6.1 Power management

6.1.1 Power supply sources

The NJJ29C0B derives its power supply from the following sources

- External battery supply (V_{BAT})
- Externally regulated digital interface supply (V_{IO})

The voltages V_{BAT} and V_{IO} can be applied separately without restrictions for the other.

Once the supply voltage V_{BAT} exceeds the power on reset release voltage threshold $V_{BAT,POR,REL}$ the device reset is released and the µController becomes operational. If V_{BAT} falls below the power on reset detection voltage threshold $V_{BAT,POR}$ (minimum operating voltage for the firmware execution), a device reset is generated (Fig 3). By the hysteresis $V_{BAT,POR,HYS}$ it is guaranteed that $V_{BAT,POR,REL}$ is always at a higher level than $V_{BAT,POR}$.

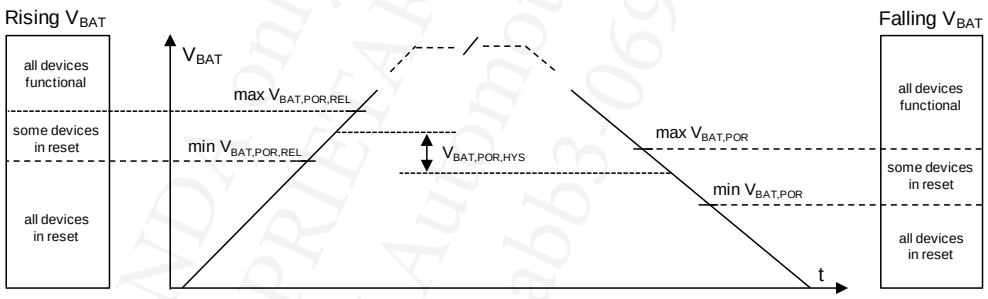

Fig 3. Battery supply reset thresholds

The externally regulated digital interface supply V_{IO} has to exceed its undervoltage detection threshold voltage $V_{IO,UVD}$ for correct I/O pin operation.

In order to reduce the system level current consumption in SLEEP state, the V_{IO} supply can be deactivated (Fig 4).

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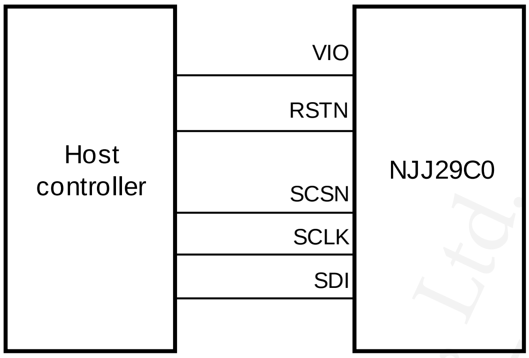

Fig 4. Lines controlled by host controller to switch V_{IO} supply

Before switching off the V_{IO} supply, the host controller outputs RSTN and SCSN have to be set to high impedance (tristate) and the outputs SCLK and SDI have to be set to low level to avoid that the digital I/Os are at a higher supply level than V_{IO}. When switching on the V_{IO} supply, RSTN and SCSN have still to keep their high impedance state until V_{IO} exceeds the undervoltage release threshold ($V_{IO,UVD,REL}$). Afterwards, RSTN and SCSN have to be set to high level before $t_{VIO,UVD}$ is elapsed. This prevents a device power on reset or a device wake-up (Fig 5).

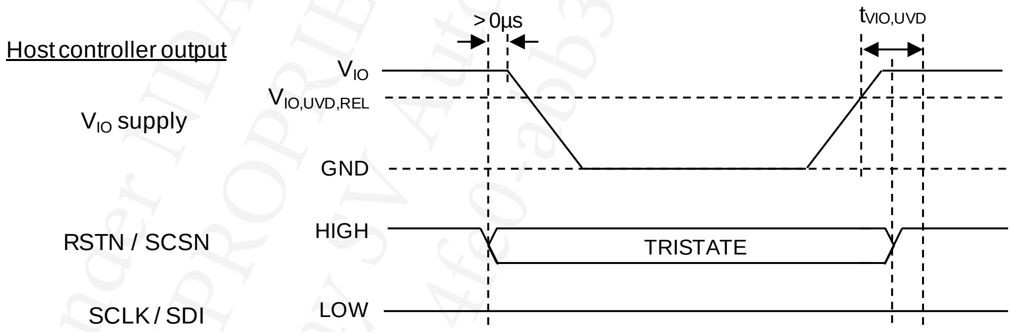

Fig 5. V_{IO} supply switch on/off sequence

6.1.2 Power supply domains

The NJJ29C0B comprises three power supply domains

- permanent power supply domain
- switched regulated power supply domain
- I/O supply domain

Both, the permanent and switched regulated power supply domains are internally derived from V_{BAT}.

The third supply domain, the I/O supply domain, is driven directly from the externally regulated digital interface supply V_{IO}. This supply domain is used to supply the I/O pins RSTN, INT and the SPI interface pins SCSN, SCK, SDI and SDO (Fig 6).

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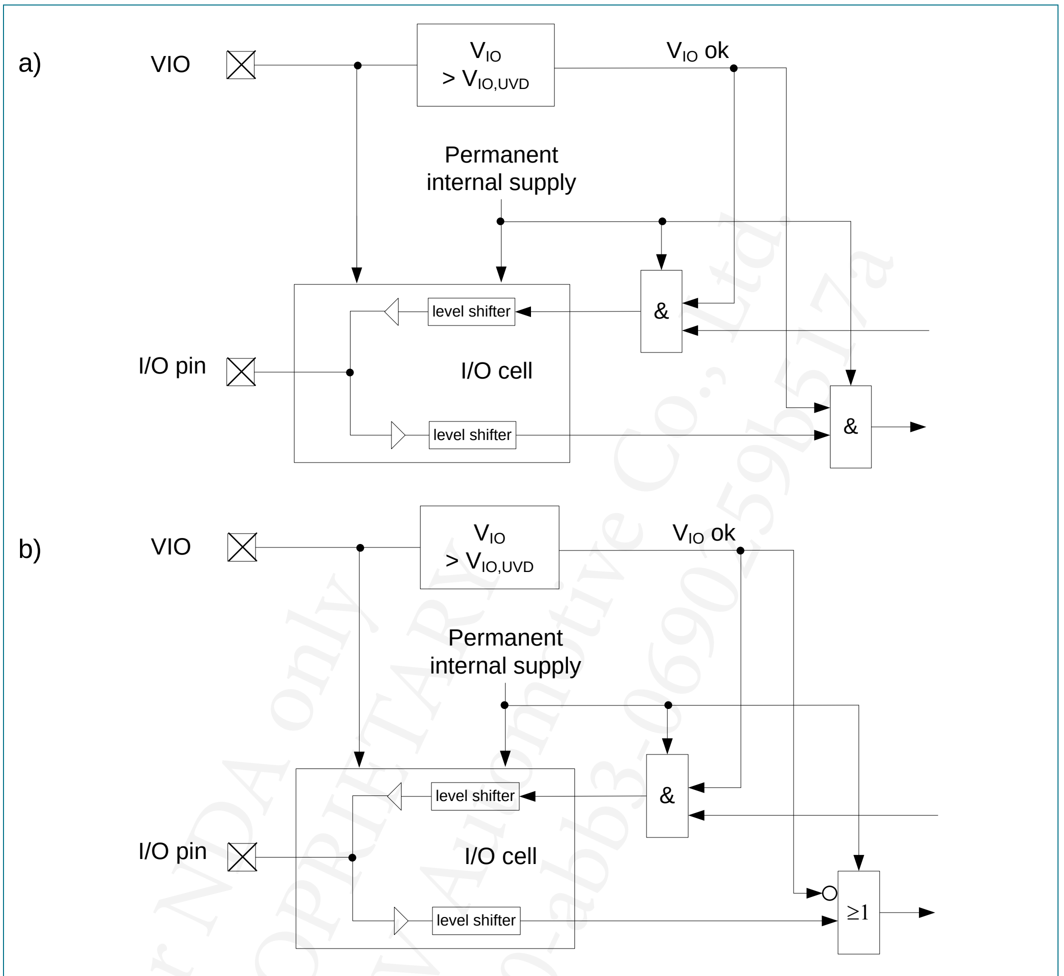

Fig 6. Supply voltage of host controller interface a) INT, SDI, SDO, SCK b) RSTN, SCSN

6.2 Device wake-up

The NJJ29C0B supports four types of wake-up event source (Table 3). In SLEEP or POLLING state, assertion of a wake-up event causes transfer to IDLE state, and the µController to start executing embedded system software. Coming from POLLING state, IDLE state might be an intermediate state, dependent on the configuration.

Table 3. Wake-up sources

Wake-up source	Condition	Comments
Power on reset	See Table 4	µController starts executing cold start sequence
SPI	SPI select (SCSN = 0)	Wake-up to process SPI communication started by the application
WUP1 … WUP6	Edge detection	Enabled by configuration
Polling timer	Timeout value reached	Enabled by configuration and setting the timeout value

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6.3 Device reset

The NJJ29C0B supports six sources for power on reset (POR) operable at device level (Table 4). All resets are unconditional.

Table 4. Power on reset sources

Reset source	Condition	Comments
Reset input pin RSTN	Reset input pin is set to low	Asserted when RSTN is driven low
Low supply voltage	Low V_{BAT}	Asserted when V_{BAT} falls below the minimum threshold $V_{BAT,MIN}$
Software reset	Triggered by SPI command for POR	Asserted when respective SPI command is received
External clock error	Off chip clock stops	Asserted when XTALCLK or PLLCLK stop oscillating. This reset forces the system to restart using the RC oscillator.
Watchdog	Expiration of watchdog timer	Asserted when a watchdog timer overflow error occurs
Memory management	Parity or protection error	Asserted when a RAM parity error occurs or an attempt is made to access an invalid memory address

Assertion of any of the resets causes all device configuration settings to be re-initialized to its factory settings, regardless of the current state of the device, before embedded system software execution restarts.

The contents of RAM are not guaranteed to be preserved over a power on reset. Hence the application shall ensure all data and optionally downloaded embedded software is consistent with the application's expectations and re-downloaded if necessary.

6.4 System clock

The NJJ29C0B contains three oscillators

- 2 internal RC oscillators
- XTAL oscillator

The XTAL oscillator drives a PLL, resulting in four clock sources. Derived from these four clock sources are three clock domains (Fig 7).

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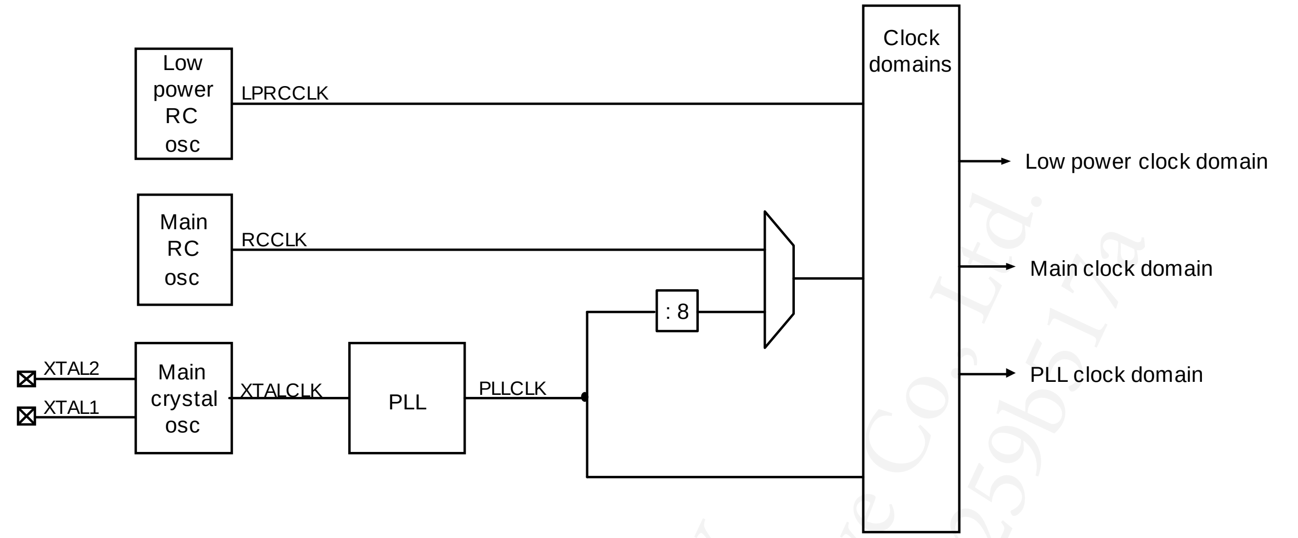

Fig 7. Clock sources and clock domains

6.4.1 Clock sources

The four clock sources of the NJJ29C0B are summarized in Table 5.

Table 5. Clock sources

Symbol	Description
LPRCCLK	Low power RC oscillator clock (for polling timer)
RCCLK	Main RC oscillator clock
XTALCLK	Main crystal oscillator clock
PLLCLK	PLL clock generated by multiplying XTALCLK

LPRCCLK, low power RC oscillator clock:

LPRCCLK is generated by an ultra low power RC oscillator and is activated on demand.

RCCLK, main RC oscillator clock:

RCCLK is the main clock source until the more accurate main crystal oscillator is activated. The main RC oscillator starts up immediately when enabled.

XTALCLK, main crystal oscillator clock:

XTALCLK is generated from a crystal connected to the pins XTAL1 and XTAL2. If XTALCLK stops oscillating, it generates a device reset.

PLLCLK, PLL clock generated by multiplying XTALCLK:

PLLCLK is driven from the main crystal oscillator clock. A PLL is used to multiply the main crystal oscillator clock with a factor of 8. The PLLCLK and the PLLCLK divided by 8 are monitored. If a monitoring failure emerges, a device reset is generated.

6.4.2 Clock domains

The NJJ29C0B provides three clock domains derived from the clock sources (Table 6).

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Table 6. Clock domains

Symbol	Description
Low power clock domain	Polling timer clock
Main clock domain	Main clock for the μController and its peripherals
PLL clock domain	Timing reference for class D* driver control

Low power clock domain, polling timer clock:

The low power clock domain is driven directly from the low power RC clock source LPRCCLK. The domain is used for the polling timer and for monitoring of the PLLCLK divided by 8.

Main clock domain, μController clock:

Dependent on the operating state, the main clock domain is either driven by the internal RCCLK or driven by a clock generated by dividing the PLLCLK by 8. The μController (including timer) is clocked in the main clock domain. During device startup this domain is driven by the RCCLK and switches to the divided PLLCLK under embedded system software control. Internal logic ensures a glitch-free switching from the RCCLK to the divided PLLCLK and vice versa.

Should XTALCLK stop whilst NJJ29C0B is active, e.g. due to a board level fault, a system reset is generated, which forces a cold restart from the internal main RC oscillator.

PLL clock domain, class D* driver clock:

The PLL clock domain is used to generate a high accuracy class D* signal duty cycle for LF transmission.

6.5 Operating states

The operating states of the NJJ29C0B are shown in Fig 8.

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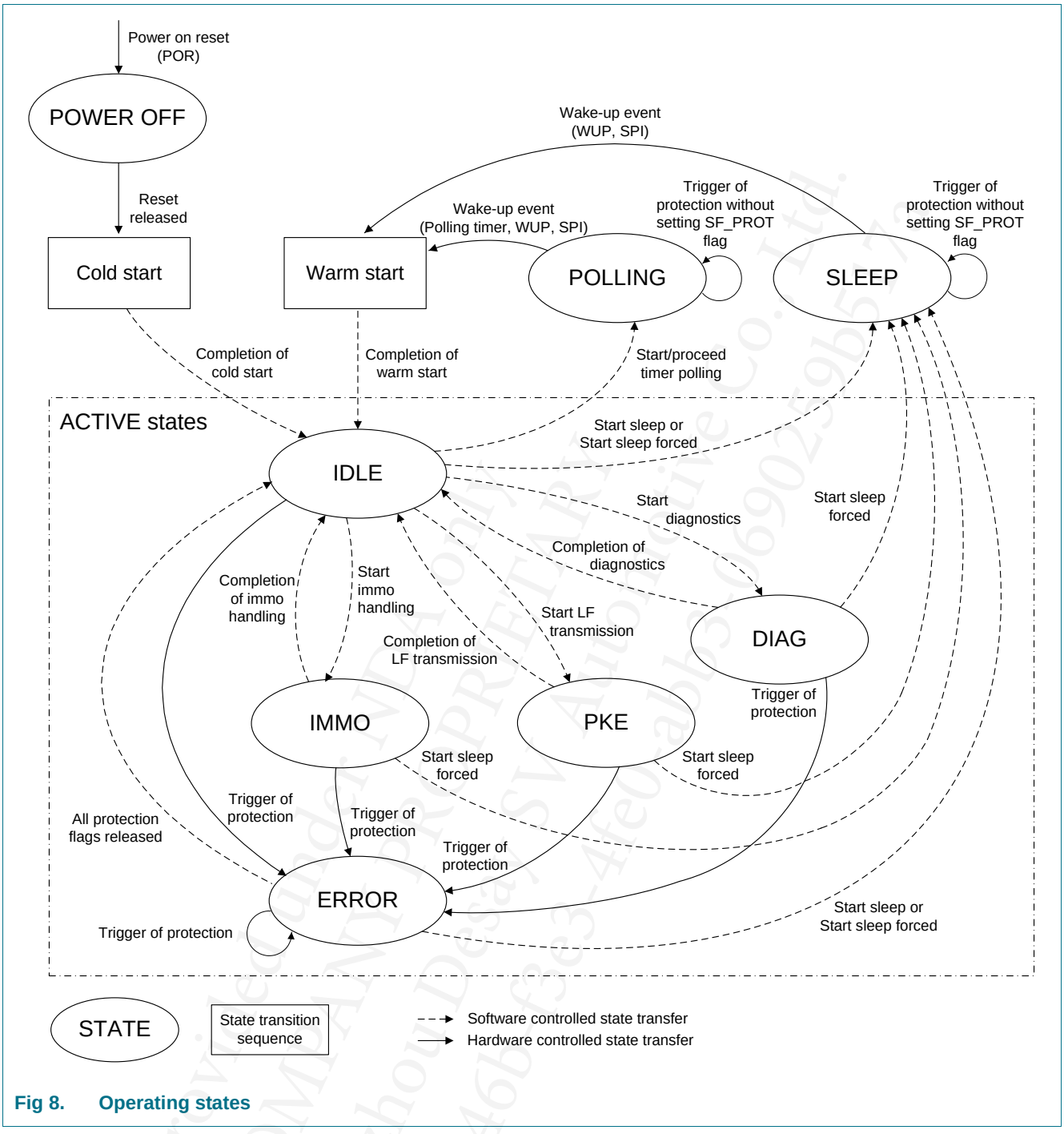

Fig 8. Operating states

In the states POWER OFF, SLEEP and POLLING the μController is inactive. A transfer from these states to other states is initiated in response to a hardware event, like a reset release event or a wake-up event triggered via wake-up port or SPI communication.

In IDLE, PKE, IMMO, DIAG and ERROR state (ACTIVE operation states) the μController is active, while the clock sources XTALCLK and PLLCLK are enabled on demand in PKE, IMMO and DIAG states.

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If active, the boost converter and/or class D* antenna drivers are shut down in response to the assertion of a device protection event (for example an over-temperature event). In order to allow the application to perform diagnostics, the integrated µController and the SPI interface remain active.

Cold Start and Warm Start state transitions include both hardware controlled operations (e.g start-up of internal regulators and oscillators) and embedded system software controlled activities.

According to the operating state, the voltage supplies and functional blocks are enabled (Table 7) and different device clock sources are available (Table 8).

Table 7. Functional blocks dependent on the operating state

State	WUP1 to WUP6	µController	SPI	Boost converter	LF antenna driver TX1, TX2, TX3, TX5, TX6	Immo antenna driver TX4 and receiver RX
POWER OFF	Off	Off	Off	Off	Off	Off
SLEEP	On	Off	Wake-up[1]	Off	Off	Off
POLLING	On	Off	Wake-up[1]	Off	Off	Off
IDLE	On	On	On	Off	Off	Off
IMMO	On	On	On	Config[2]	Off	On
PKE	On	On	On	Config[2]	Config[2]	Config[2]
DIAG	On	On	On	Config[2]	Config[2]	Config[2]
ERROR	On	On	On	Forced off	Forced off	Forced off

[1] SCSN status is monitored to detect wake-up events

[2] Config denotes device behavior dependent on configuration

Table 8. Clock sources dependent on the operating state

State	Low power RC osc	Main RC osc	Main XTAL osc and PLL
POWER OFF	Off	Off	Off
SLEEP	Off	Off	Off
POLLING	On	Off	Off
IDLE	On	On	Off
IMMO	On	On	On
PKE	On	On	On
DIAG	On	On	On/Off[1]
ERROR	On	On	Off

[1] Dependent on diagnostics operation

If the main crystal oscillator and the PLL are active, this oscillator is used as clock source. If only the low power RC oscillator and the main RC oscillator are active at the same time, the main RC oscillator is used as clock source.

6.5.1 POWER OFF state

The POWER OFF state is active as long as the applied battery voltage is lower than the minimum operating voltage. In this state, all blocks of the NJJ29C0B are powered down except for the start-up circuitry.

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If the supply voltages fall below their limit, independent of the actual device state the device enters POWER OFF state and all internal blocks are reset. In POWER OFF state, V_{IO} can be present without damaging the device.

6.5.2 SLEEP state

In SLEEP state, only the permanent supplies are enabled, which drive the power management unit and the wake-up detection circuits. The μController, its peripherals, and other analog / digital circuitry are disabled and the switched regulated power supply domains are switched off.

The contents of the RAM, implemented in the permanent supply domain, are maintained during SLEEP state.

The SLEEP state is exited by the following events

- SPI chip select (SCSN = 0) wake-up initiates transfer to IDLE state
- Valid wake-up condition on one or more wake-up pins (WUP1 to WUP6) initiates transfer to IDLE state, if enabled
- Power on reset triggers transfer to POWER OFF state

6.5.3 POLLING state

POLLING state is similar to SLEEP state. In addition, the low power RC oscillator remains active and the polling timer is activated and initialized according to its configuration.

In POLLING state, each time a polling timer trigger events occurs, the device wakes-up and changes via IDLE state to PKE state in order to send autonomously preconfigured LF frames.

After sending the configured frames, the NJJ29C0B changes from PKE state via IDLE state into POLLING state again, until the next polling timer trigger events occurs.

The POLLING state is exited by the following events

- SPI chip select (SCSN = 0) wake-up initiates transfer to IDLE state
- Valid wake-up condition on one or more wake-up pins (WUP1 to WUP6) initiates transfer to IDLE state, if enabled
- Polling timer expiration initiates transfer to IDLE state
- Power on reset triggers transfer to POWER OFF state

6.5.4 IDLE state

In IDLE state the μController and its peripherals are enabled and the embedded system software is executed. In IDLE state typically SPI communication between the NJJ29C0B and the host controller is performed, allowing configuration of the device and to initiate transfers into other states.

The IDLE state is exited by one of the following events:

- SPI command initiates transfer to IMMO, PKE, DIAG, SLEEP or POLLING state
- Automatic re-entry of POLLING state during timer controlled polling operation after completed PKE operation
- Protection event triggers transfer to ERROR state
- Power on reset triggers transfer to POWER OFF state

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6.5.5 PKE state

In PKE state, LF operations are executed by the µController dependent on the application settings

- Operating the boost converter
- Operating the class D* antenna drivers
- Executing the telegram sequencer

The telegram sequencer implements the required real-time control tasks. SPI communication can be continued in parallel to LF operation.

The PKE state is exited by the following events

- Completion of LF transmission triggers transfer to IDLE state
- Protection event triggers transfer to ERROR state
- Power on reset triggers transfer to POWER OFF state

6.5.6 IMMO state

In IMMO state, immobilizer operations are executed by the µController dependent on the application settings

- Operating the boost converter
- Operating the immobilizer class D* antenna driver
- Operating the immobilizer receiver

While the immobilizer protocol is controlled via SPI commands, the NJJ29C0B handles the required real-time control tasks according to the configuration.

The IMMO state is exited by the following events

- Completion of immobilizer handling triggers transfer to IDLE state
- Protection event triggers transfer to ERROR state
- Power on reset triggers transfer to POWER OFF state

6.5.7 DIAG state

In DIAG state, device diagnostic operations are performed by the µController dependent on the application settings

- Operating the DC current sources
- Operating the boost converter
- Operating the class D* antenna driver

In difference to the protection circuitry, diagnostics is started via SPI command. If a malfunction is detected, the corresponding flag is set and if a continuation of the diagnostics sequence is possible (depends on formerly detected malfunction), it will be continued.The DIAG state is exited by the following events

- Completion of diagnostics triggers transfer to IDLE state
- Protection event triggers transfer to ERROR state
- Power on reset triggers transfer to POWER OFF state

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6.5.8 ERROR state

ERROR state is entered if in any ACTIVE operation state a protection malfunction flag is set. The flag status can be read out by the application via dedicated SPI command.

If the device is in ERROR state and receives a command to transfer to SLEEP state, this state transfer is performed. After exiting SLEEP state, the device enters via IDLE state in ERROR state again, if the malfunction flags have not been cleared (and the root causes have not been removed).

The ERROR state is exited and a transfer to IDLE state takes place if

- All protection flags are cleared

This includes the flag that originally caused the transfer to ERROR state as well as possible other protection flags that have been set afterwards.

On exit, in order to prevent immediate re-entry of the ERROR state, the cause of the protection shall be removed before clearing the flags.

6.5.9 State transitions

6.5.9.1 Cold start sequence

The cold start sequence is executed when the device switches from POWER OFF to IDLE state. The cold start sequence consists of the following activities

1. Enable the internal regulated supply voltages
2. Activate the main RC oscillator
3. Start the execution of the embedded system software and initialize parameters with default values

During step 3, the device switches to IDLE state.

6.5.9.2 Warm start sequence

The warm start sequence is executed when the device is in either SLEEP or POLLING state and a valid wake-up event is detected. The warm start sequence consists of the following activities

1. Enable the internal regulated supply voltages
2. Activate the main RC oscillator
3. Start the execution of the embedded system software by keeping the parameter values

During step 3, the device switches to IDLE state.

6.6 Boost converter

The boost converter provides the supply voltage for the LF driver stages. It embeds the required power switch, thus only an inductor, a schottky diode and an output capacitor are needed as external components. (Fig 9).

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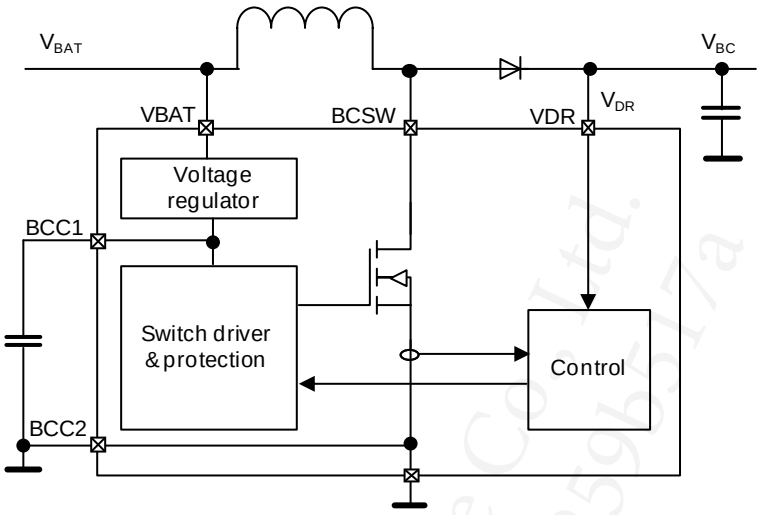

Fig 9. Block diagram of boost converter

The boost converter operates at a nominal switching frequency of four times of the LF driver carrier frequency. The switching frequency is synchronized with the main clock derived from the PLL reference clock.

In the application design it has to be considered that the maximum boost converter output current I_{BC} depends on the battery voltage V_{BAT} and on the boost converter output voltage V_{BC}. Using the recommended external components, the maximum output power of the boost converter is adequate to supply a LF driver at the maximum output voltage V_{BC} while driving an antenna with the maximum output current $I_{DR,BURST}$.

6.6.1 Coil current limitation

The NJJ29C0B contains a boost converter coil current limitation which can be configured by the application. A peak comparator compares the actual boost converter current with the configured maximum coil current. If the configured maximum current is reached, the coil current is limited to the configured value.

The coil current limitation is set by default to 4 A during boost converter ramp-up ($t_{BC,START}$). This ensures that the output capacitor is fully charged before the boost converter coil current limitation is updated to the customer defined level.

6.7 LF antenna driver

The NJJ29C0B provides six full-bridge output drivers for driving high currents through the LF antennas.

In parallel to each power driver, programmable low current (LC) drivers are integrated. Additionally, dedicated DC current sources are provided for driver diagnostics. When activating the low current drivers or the DC current sources, the corresponding power drivers are set to tristate mode.

6.7.1 Bridge operation modes

The LF drivers consist of full-bridge output drivers containing 4 main switches and 2 mid-level switches (Fig 10).

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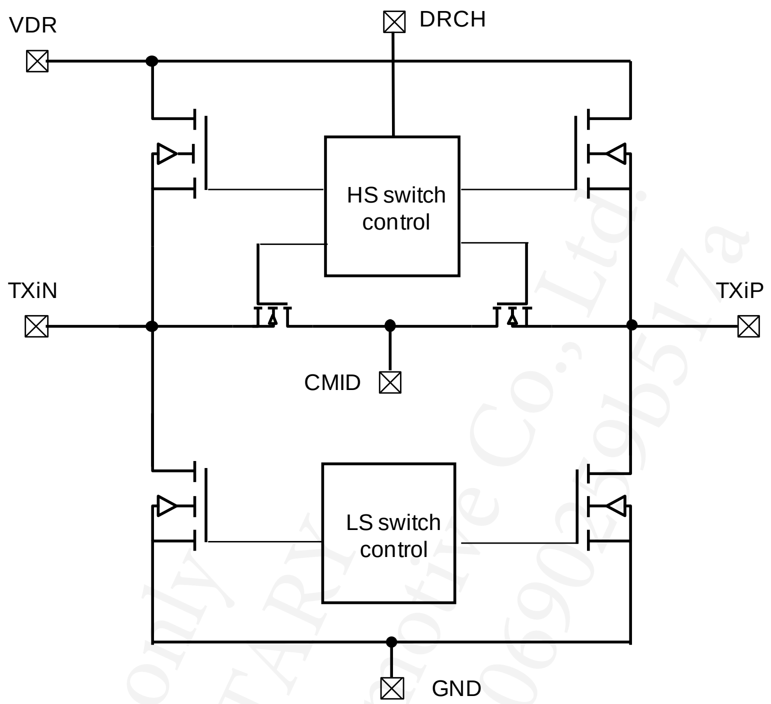

Fig 10. Block diagram of power LF driver

The drivers support the following operation modes, configurable by the application

- Full-bridge operation with mid level control
- Full-bridge operation

In each of these operation modes, the driver output voltage has a rectangular characteristic, while connecting to a series resonant circuit the antenna current will become sinusoidal due the resonant filter characteristic.

6.7.1.1 Full-bridge operation with mid level control

In full-bridge operation with mid level control the antenna is connected differentially between two corresponding driver outputs TXiP and TXiN. The 4 main switches of the driver as well as the mid-level switches are used to generate the class D* antenna driver output signal (Fig 11).

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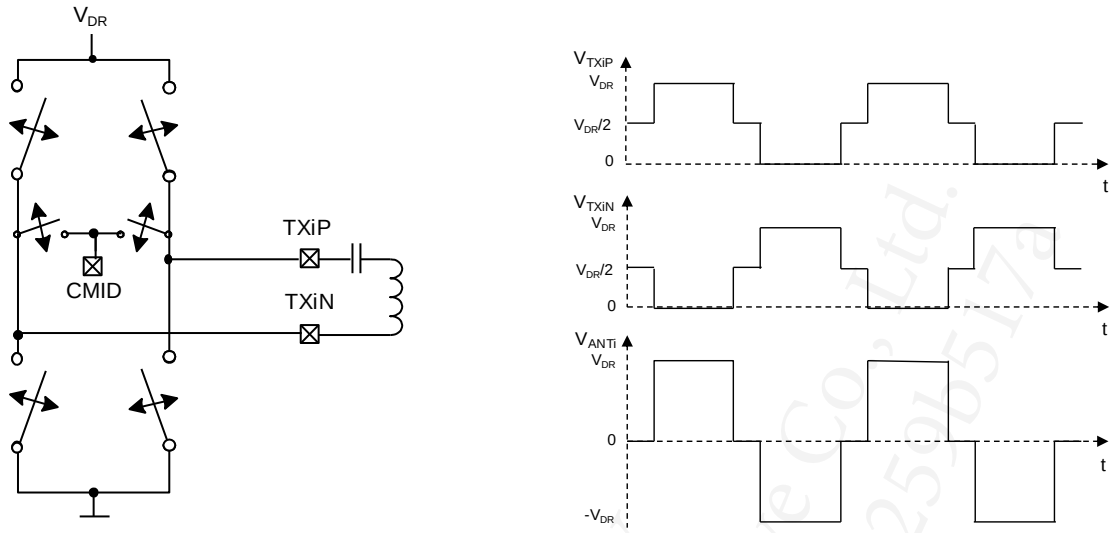

Fig 11. LF driver in full-bridge operation with mid level control

The mid level control circuit keeps the common mode voltage on the antenna lines constant at half of the bridge supply voltage, keeping emission low. Thus, full-bridge operation with mid level control is the recommended device operation mode, since it features low internal power dissipation and low emission.

The antenna peak current is measured in both the positive and negative active driving phase of the full-bridge ($V_{ANT} \neq 0$).

If the antenna peak current cannot be measured (e.g. caused by antenna detuning or for low current values), the device is operated in feed forward mode with deactivated current control loop.

6.7.1.2 Full-bridge operation

In full-bridge operation the antenna is connected differentially between two corresponding driver outputs TXiP and TXiN. The 4 main switches of the class D* driver are used to generate the output signal, while the mid-level switches are de-activated and left open (Fig 12).

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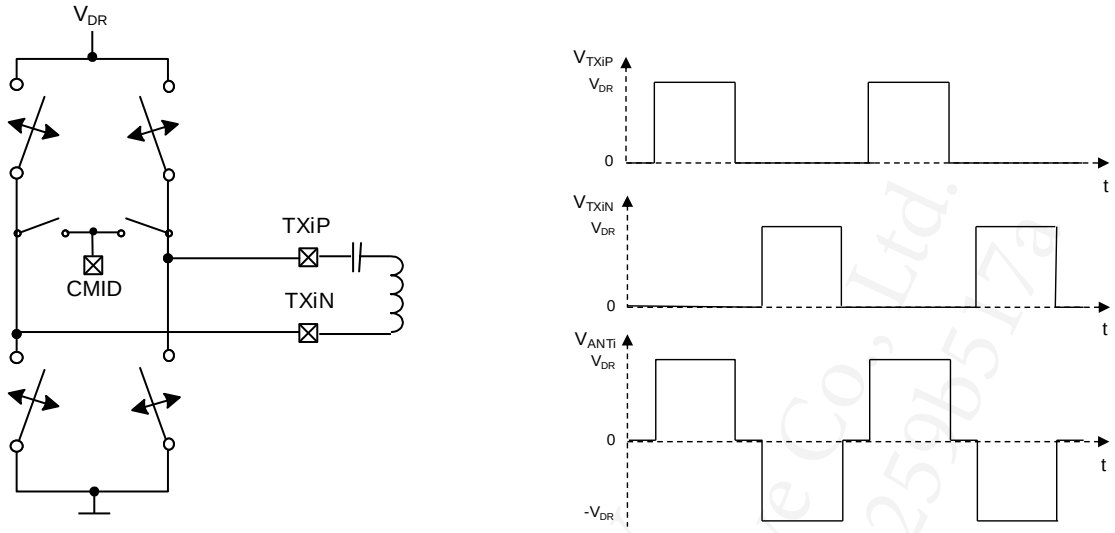

Fig 12. LF driver in full-bridge mode

The common mode voltage on the antenna lines is not constant in a real application, as the driver outputs are not clamped to the mid level via the mid level control switches.

The antenna peak current is measured in both the positive and negative active driving phase of the full-bridge ($V_{ANT} \neq 0$).

If the antenna peak current cannot be measured (e.g. caused by antenna detuning or for low current values), the device is operated in feed forward mode with deactivated current control loop.

6.7.2 Current control

6.7.2.1 Control parameters

The target antenna driver current can be configured in the range between the minimum and maximum value of $I_{DR,RANGE}$ with a step size of $I_{DR,STEP}$.

The device adjusts the peak antenna driver current I_{ANT} for each channel automatically to the target value. For this, the NJJ29C0B embeds an accurate antenna driver current control loop, measuring and correcting the current in each carrier period.

The minimum value of $I_{DR,RANGE}$ depends on the antenna impedance Z_{ANT} which is connected to the LF driver output pins. It is important to notice that the value of Z_{ANT} includes possible antenna detuning with regard to the nominal antenna resonance frequency (which is equal to the carrier frequency f_C). If Z_{ANT} is unknown to the application, the NJJ29C0B provides means to determine the antenna impedance by amplitude and phase measurements. Alternatively, Z_{ANT} (L, Q, antenna detuning) can be set by the application via SPI command.

Based on the antenna impedance, the NJJ29C0B selects the optimum settings for V_{DR} and DCY_{DR} by minimizing harmonic distortions (Fig 13). For this, the NJJ29C0B checks, if the target antenna driver current can be achieved when using the optimum driver duty cycle DCY_{DR}. If this is possible, the boost converter output voltage V_{BC} is selected accordingly.

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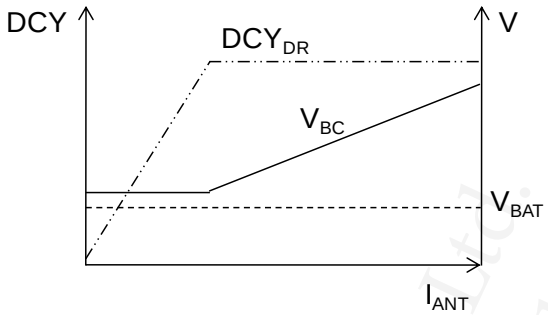

Fig 13. Principle how device selects initial settings for V_{BC} and DCY_{DR}

Otherwise, if the calculated boost converter output voltage is beyond the minimum or maximum value, it is selected to its minimum or maximum value, repectively, and DCY_{DR} is determined to fulfill the target antenna driver current, dependent on the available DCY_{DR} range and Z_{ANT}.

Activating the driver, the boost converter output voltage and the initial class D* duty cycle are set. Driving the antenna, the embedded antenna control loop measures the actual antenna peak current and regulates the driver duty cycle DCY_{DR} (resolution $DCY_{DR,STEP}$) based on the difference between the actual and the target antenna driver current, thus obtaining the specified antenna driver current accuracy.

For optimum performance the antenna impedance magnitude Z_{ANT} shall be within the specified range. However, driving higher and lower impedances is possible with functional degradations. For example, lower Z_{ANT} values will reduce the number of available current steps, while higher Z_{ANT} values do not allow driving the maximum current $I_{DR,BURST}$.

Example: Antenna driver current control, single antenna

The application in full-bridge configuration sets the requested current I_{ANT} for the selected antenna within the range between the minimum to the maximum value of $I_{DR,RANGE}$. The NJJ29C0B computes the initial setting of the boost converter output voltage and of the class D* duty cycle to be used for driving the first carrier cycle.

This computation uses either the results of an antenna impedance measurement started via SPI command before or the values for Li, Qi and Deti that have been transmitted via SPI command before. In both cases the required antenna impedance values are stored in the device.

Next, the device sets the boost converter output voltage and the class D* duty cycle to the initial values. After starting active driving the first carrier cycle, the antenna driver current measurement is started. The measured values are used to determine the deviation to the requested current value and to correct the class D* duty cycle.

The procedure to measure the antenna driver current and to adjust the class D* duty cycle continues, carrier cycle by carrier cycle, until the active antenna driving is switched off.

6.7.2.2 Current ramping

Fast increase and decrease of the antenna driver current facilitates reliable decoding of the ASK modulated signals by the receiver in the car key device.

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Antenna driver current preset values

In order to speed up antenna driver current ramping, preset values calculated internally in the device are set for the two antenna driver current control parameters (boost converter output voltage and duty cycle) before activating the drivers. These preset values are related to the respective antenna impedances and will be used to adjust the initial currents before activating the drivers.

Antenna discharging and current decrease

The antenna current is ramped-down dependent on the bridge operation mode.

In full-bridge operation with mid level control, the main driver switches are opened during the LF carrier off phase. Simultaneously, the antenna is discharged by closing the mid level switches, keeping TXiP and TXiN at V_{MID} level.

In full-bridge operation without mid level control, the high side switches are opened during the LF carrier off phase, while the low side switches are turned on and pull down TXiP and TXiN to GND.

Independent of the bridge operation mode, at the end of an LF transmission sequence both driver outputs TXiP and TXiN are pulled down to GND via $R_{DR,PD}$. These pull down resistors remain enabled until the driver gets activated again (Fig 14).

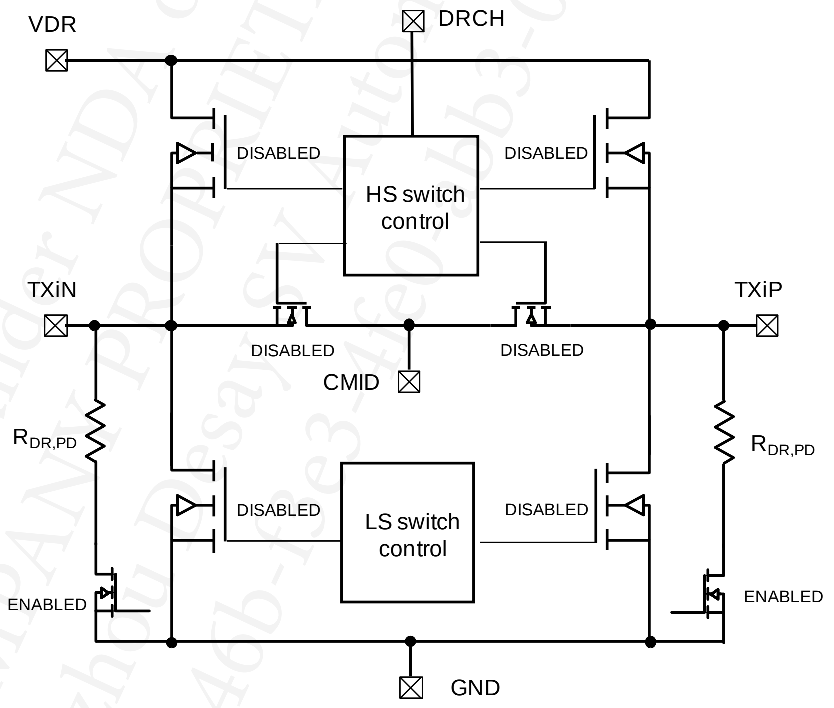

Fig 14. Pull down resistors $R_{DR,PD}$

Antenna current ramp-down by opening the antenna resonance loop

The application can accelerate the antenna driver current ramp-down during LF signal modulation by opening the antenna resonance loop. Due to the capacitor at the driver output the antenna resonance frequency increases (Fig 15), leading to a faster decrease of the antenna driver current (Fig 16).

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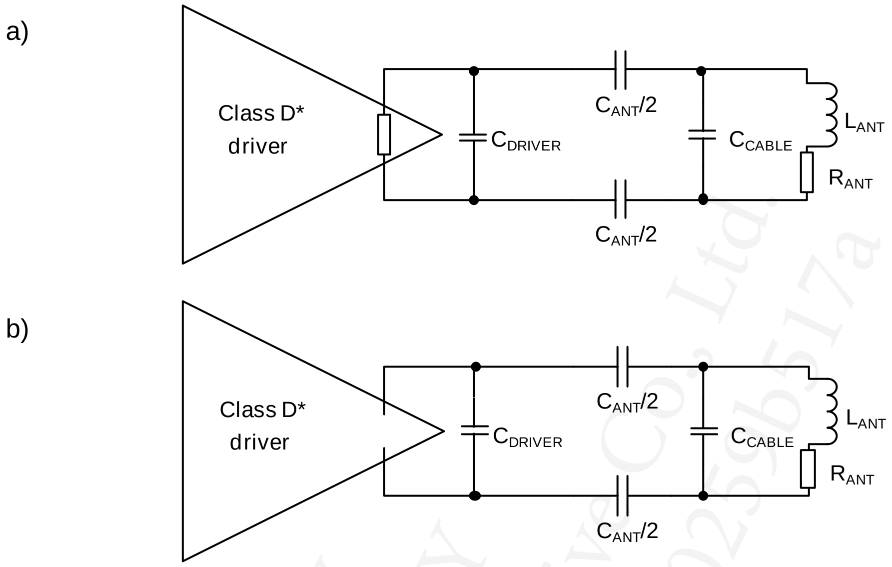

Fig 15. Antenna driver current ramp-down a) Driving the antenna b) Opening the antenna resonance loop

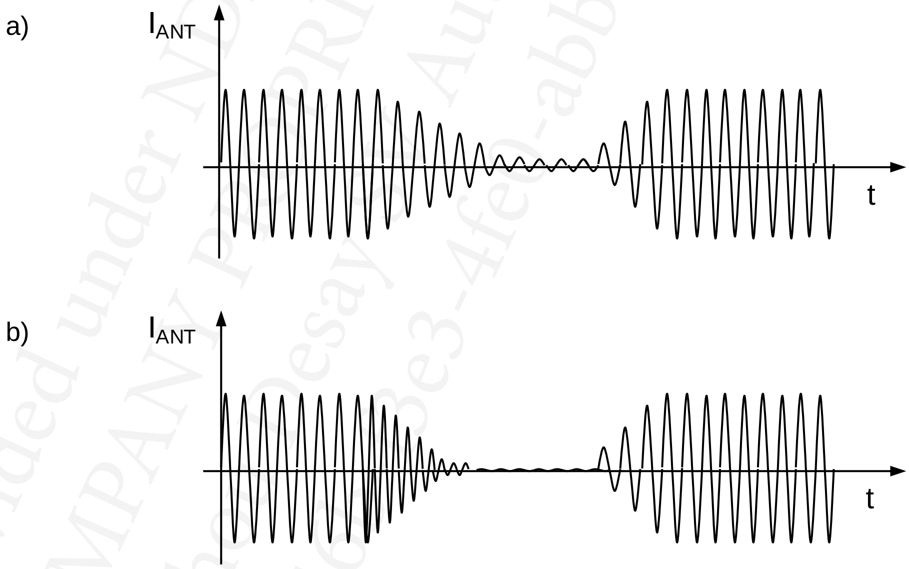

Fig 16. Antenna driver current ramp-down a) Regular procedure b) Opening the antenna resonance loop

Opening the antenna resonance loop in the unmodulated time period, TXiN is connected to GND and all other main driver switches are opened.

Before start of modulation, in full-bridge operation with mid level control, the main driver switches are opened and the mid level switches are closed again. In full-bridge operation

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without mid level control, TXiP is connected to GND having all low side main driver switches turned on.

It is important to notice that opening the antenna resonance loop is not provided at the end of an LF transmission sequence.

6.7.2.3 Dithering

Harmonics at the driver output are reduced by applying symmetrical pulse dithering. With activated dithering the edges of the driver output signals do not occur periodically with fixed timing but with random time shifts centered around the nominal (periodic) time of occurrence (Fig 17). The randomly calculated time shifts change with each carrier cycle.

The dithering can be enabled and configured by the application. The application can reduce the maximum dithering range to values smaller than half the carrier cycle. This might be advantageous especially in applications where small duty cycles are applied.

If activated by the application, dithering will be applied during the complete LF transmission using the pre-set dithering parameters.

Note: Dithering in combination with a detuned antenna can prevent cycle by cycle measurement of the actual antenna peak current.

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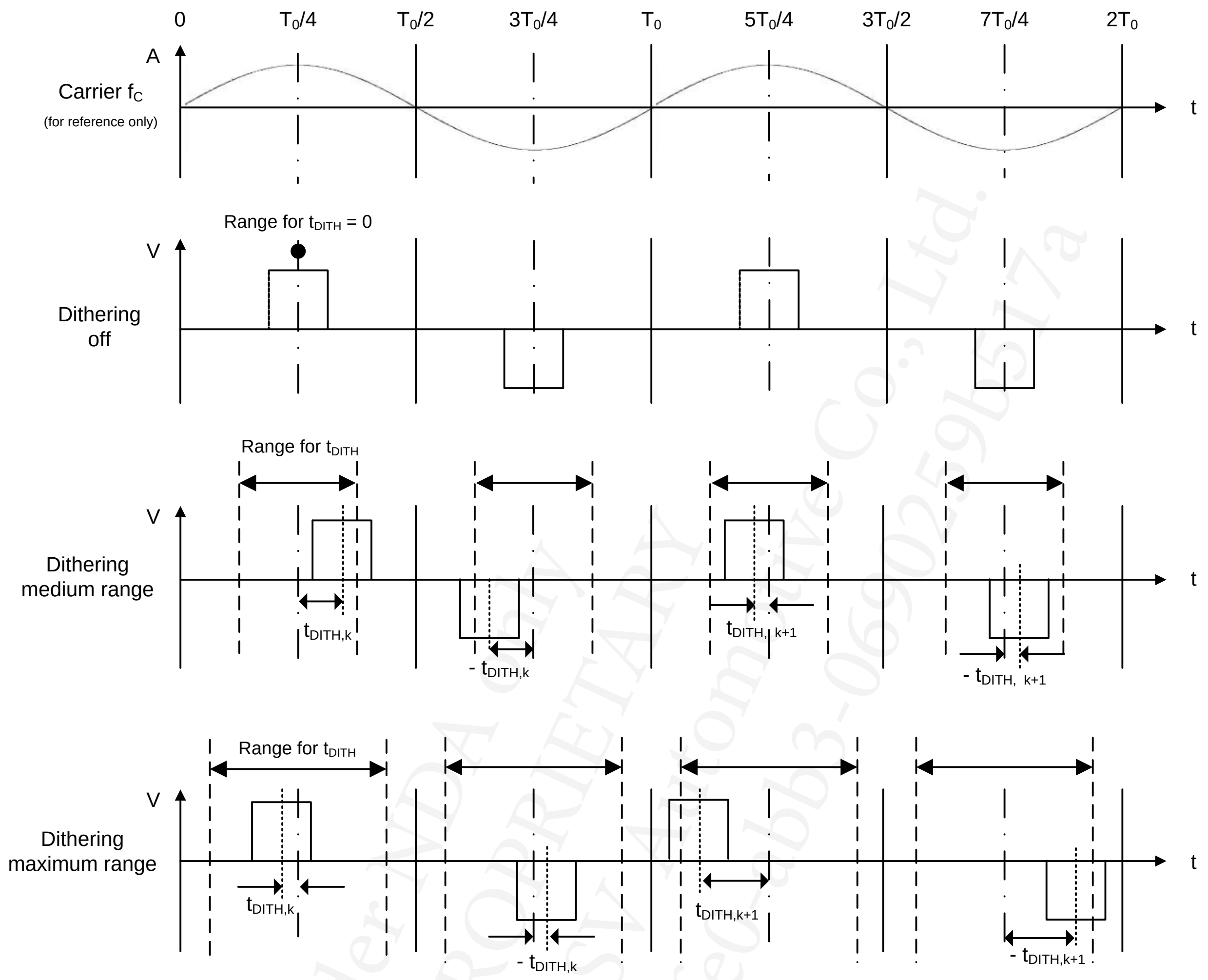

Fig 17. Symmetrical pulse dithering (examples)

Table 9. Dithering range settings (f_C = 125 kHz)

Dithering range	Maximum phase shift	Maximum time shift t_{DITH}
Off	0	0
Minimum	± 22.5 °	± 500 ns
Medium	± 45.0 °	± 1.0 µs
Maximum	± 67.5 °	± 1.5 µs

The randomly calculated time shifts t_{DITH} are limited automatically, when the dithering pulse would exceed the carrier cycle range. The maximum possible time shifts t_{DITH} depend on the duty cycle.

It is important to notice that dithering cannot be applied during immobilizer operation.

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6.7.3 Channel switching

Changing the driven LF channel can be done without restarting the boost converter and class D* supply. The boost converter output voltage is updated by the µController according to the requested settings while considering the actual battery voltage level V_{BAT}. A change of the LF channel is done within the time $t_{CH,CHG}$.

6.7.4 Simultaneous channel operation

The NJJ29C0B allows driving of up to three antennas simultaneously. As for single channel operation, all simultaneously driven channels use their individual current control settings. The boost converter output voltage is adjusted to the channel with the highest power demand and the individual channel currents are controlled via duty cycle adjustment.

If the channel settings differ significantly from each other, it is possible that the individual channel currents cannot be reached. For example, if a large current is selected for one channel and a small current is selected for another channel, the boost converter output voltage is adjusted to the channel with the large current. In this case the smallest duty cycle might not be small enough to adjust the small current for the other channel.

If the baud rate for the simultaneously operated antennas differ, the respective value of the selected driver with the lowest number is used for all antennas.

6.7.4.1 Antenna driver current limitation

The antenna driver currents are limited by the total device power dissipation, which causes device heat up dependent on the ambient temperature T_{amb} as well as on the heat sink and application board properties (R_{th}).

The total device power dissipation P_{TOT} consists mainly of the power dissipation in the

- Boost converter (P_{BC})
- LF drivers (P_{DR})

The junction temperature increase is strongly dependent on the number of simultaneously driven antennas, their parameters, battery voltage and protocol burst length.

6.7.4.2 Current measurement

When driving multiple antennas simultaneously, the currents of the simultaneously activated channels are measured sequentially. In each second carrier cycle the antenna driver current of one channel is measured. When using 2 channels simultaneously the current for each antenna is measured alternated in each fourth carrier cycle, when using 3 channels simultaneously each channel is measured alternated every sixth carrier cycle. Consequently, when using multiple antennas, the current adjustment takes place in every fourth or sixth carrier cycle for each channel (Fig 18).

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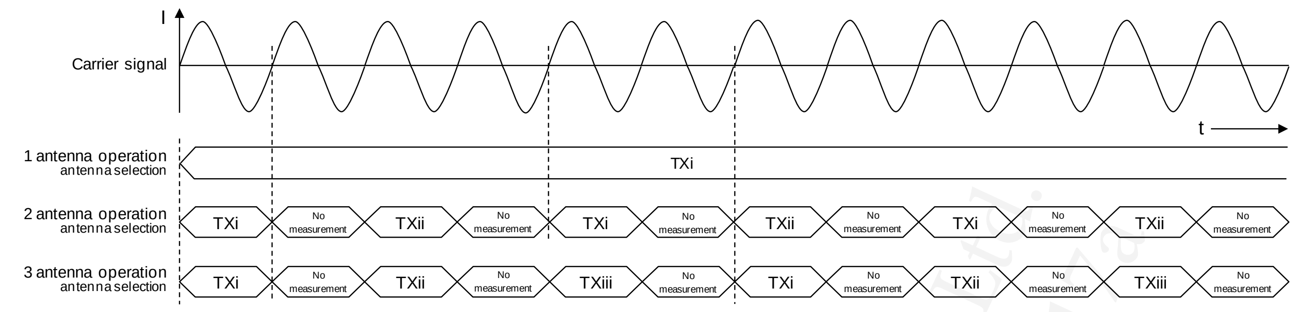

Fig 18. LF driver selection for current measurement

6.8 Parallel low current driver

Each class D* driver channel has both a high (LF) and low current (LC) driver in parallel, though decoding logic ensures only one, or neither of these two drivers can be active. The LC drivers have a fixed internal low voltage supply and are not powered via the boost converter. The LC drivers can be selected by the application on LF channels not configured for main LF telegram transmission.

After selection, the LC drivers are becoming active automatically when transmitting data via the main LF drivers. Dependent on the configuration done by the application, the LC drivers send the inverted main data or dedicated configured data is sent. During carrier off times and when sending constant carrier signals via the main driver, no low current signals are sent.

The user can adjust the low current value I_{DRLC} by setting the LC driver duty cycle. Once configured by the application, the duty cycle values are stored to be used when the LC driver is activated. The LC drivers have no current control mechanism, thus the antenna driver current depends on the antenna impedance.

Fig 19 shows the low current (LC) driver and the generated output signals.

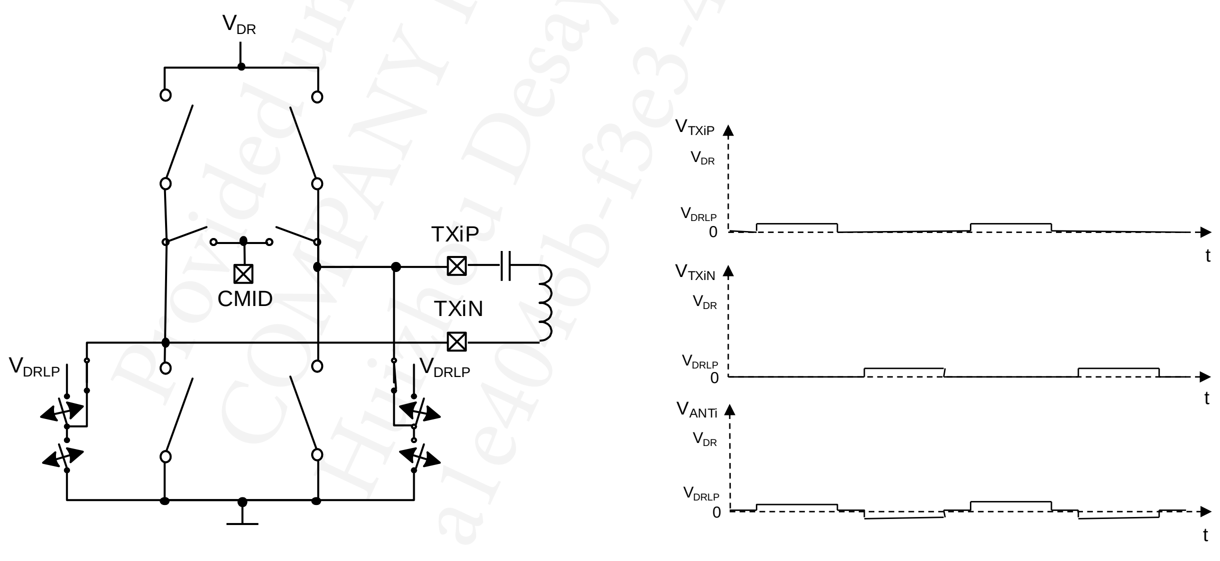

Fig 19. Low current driver

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6.9 Telegram sequencer

The telegram sequencer manages the sending of telegram data through the LF antennas. The data to be transmitted is stored in buffers, located in RAM, which are configured by the application after connecting the NJJ29C0B to the battery. The data is separated in segments. Each segment represents in general one LF protocol part like preamble, code violation, Manchester encoded data etc.

Each buffer has an identifier allowing the telegram sequencer to compose an LF telegram by assembling the corresponding data segments (Fig 20). Thus, common segments like preamble or code violation can be re-used by all channels, while dependent on the channel different data can be sent.

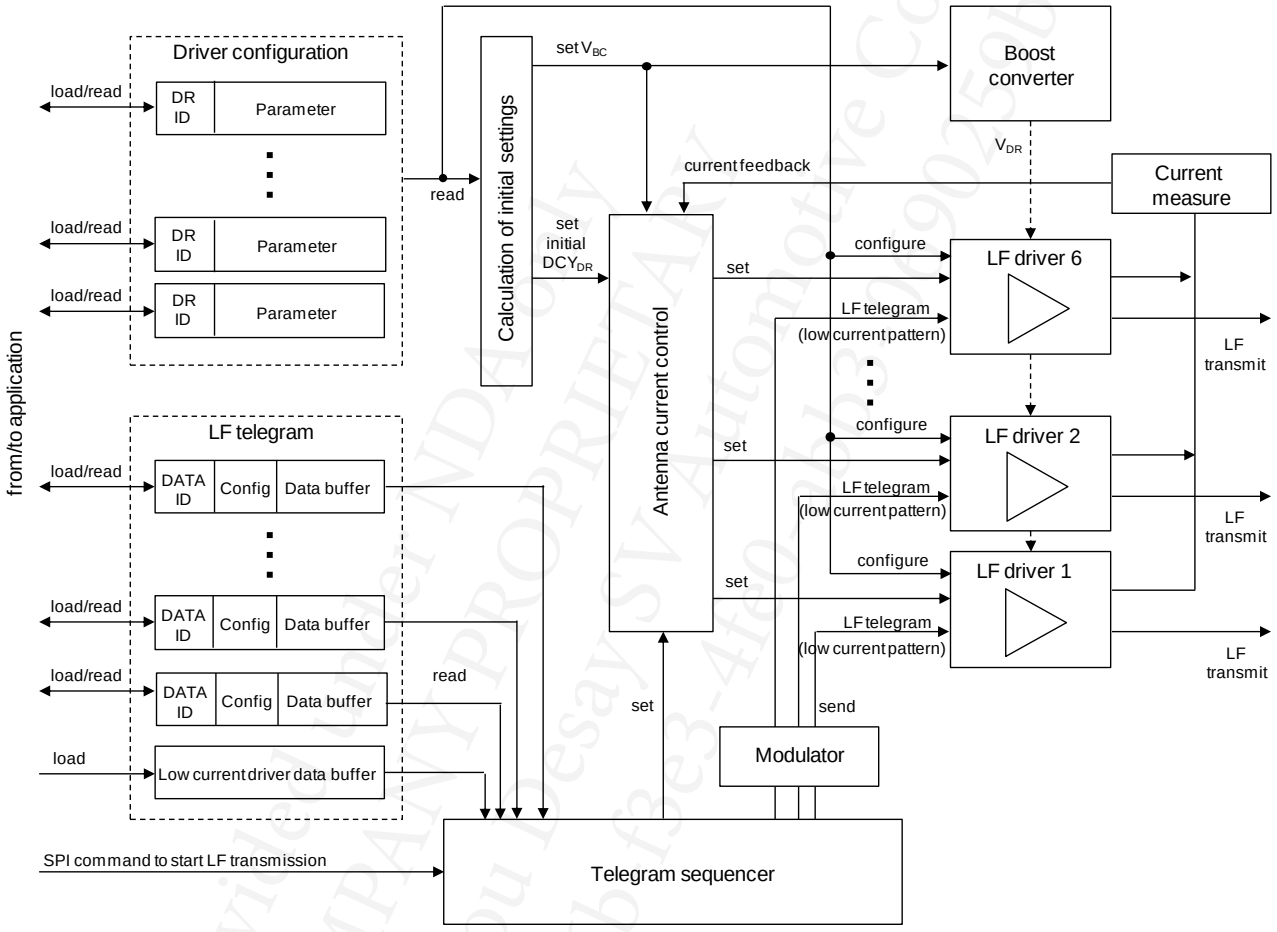

Fig 20. Telegram sequencer

In parallel to the main telegram data transmission on the selected antenna channels, the telegram sequencer also enables a low current pattern to be transmitted on the drivers configured in low current operation. The low current pattern is loaded from the low current driver data buffer in RAM. For each main telegram data segment (DATA ID) the low current pattern is loaded from its beginning and sent in parallel with the main telegram data to its selected antennas. If the low current driver data buffer is shorter than

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the transmitted main telegram data segment, the low current pattern is loaded from its beginning again (ring buffer concept).

6.9.1 Typical LF telegram

Fig 21 shows a typical LF telegram used with NXP keyless entry devices.

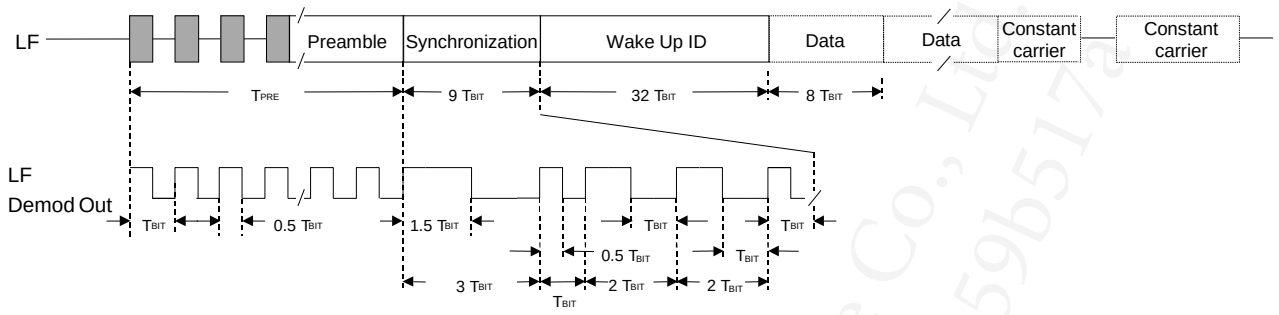

Fig 21. Typical LF telegram

The LF telegram stored in the LF telegram buffer comprises

- Preamble
- Code violation pattern (synchronization)
- Wake-up ID
- Data (optional)
- Constant carrier (optional)

All bit timings are measured between two consecutive rising edges of the coded protocol.

Preamble:

The preamble is a sequence of Manchester coded “zeros” which allow the car key LF interface analog circuitry to settle. The preamble shall feature a minimum length as specified for the car key device.

Synchronization pattern:

During the wake-up sequence first a synchronization pattern is sent, which is a pre-defined startup pattern transmitted at the beginning of the data telegram. This synchronization pattern consists of a code violation pattern, followed by a Manchester coded zero bit.

The "code violation" is a sequence intended to violate the rules of the Manchester code.

Wake-up ID:

Following the synchronization pattern, a Manchester coded user programmed wake-up ID pattern is sent.

Data:

After sending the wake-up ID, the device can continue sending data.

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Constant carrier:

A constant carrier signal may be transmitted for a specified time after sending the wake-up ID or after sending data. This may be used for RSSI measurements. The carrier signal can be switched off for a dedicated time before switching on.

6.9.2 Data coding

In order to allow the application to adapt the LF signals to the system requirements, several data codings are supported.

Manchester coding

The output data of the NJJ29C0B is typically Manchester coded and characterized by the time durations between two consecutive rising edges in the transmitted signal.

Using a carrier frequency of 125 kHz, the Manchester coded data has a bit length T of 128 µs (8 kbit/s), 256 µs (4 kbit/s) or 512 µs (2 kbit/s) and a pulse width of 50% of the overall bit length.

A zero of a Manchester coded bit at the output is coded as a transition from high to low state, a one is coded as a transition from low to high state.

The Manchester coded bits and the referring LF patterns are shown in Fig 22. During the high state of the coded bit the LF signal is on, during the low state the LF signal is off.

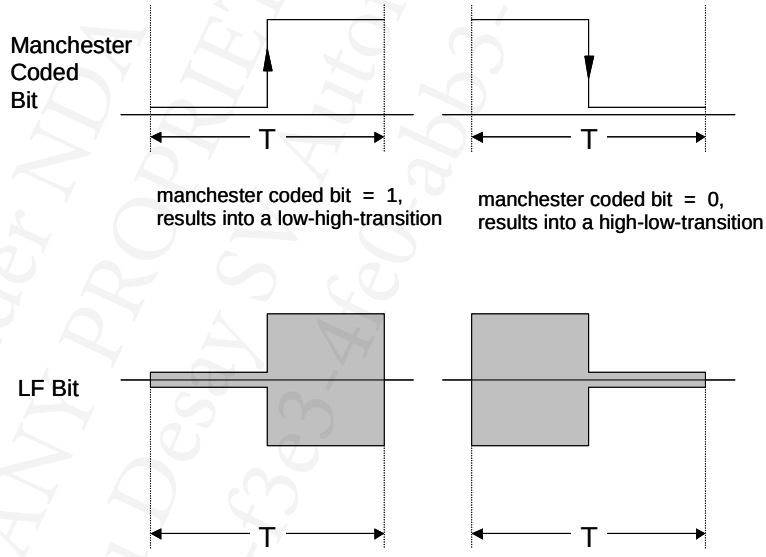

Fig 22. Manchester code

NRZ coding

A zero of a NRZ coded bit at the output is coded as a low state, a one is coded as a high state.

Half bit coding

Half bit coding corresponds to NRZ coding, whereby each transmitted bit is composed by two adjacent data bits (Fig 23).

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Half bit coding allows the composing of e.g. Manchester signals (sending a 1 followed by a 0 or vice versa), NRZ signals (sending two times a 1 or two times a 0) or the composing of code violations (e.g. sending 3 times a 1, followed by a 0).

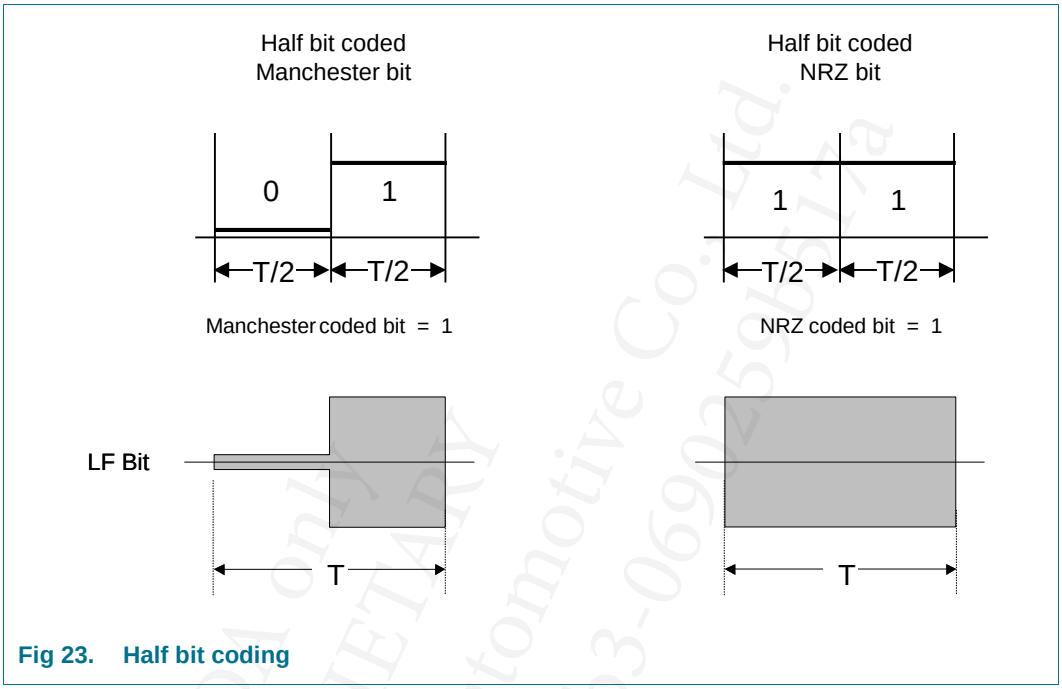

Fig 23. Half bit coding

6.10 Immo transceiver

The NJJ29C0B provides an integrated immo transceiver containing a dedicated LF driver that can be used as shared Immo/PKE driver and a LF receiver function for transponder communication. The immo transceiver drives an external antenna in resonance to establish an LF field that can be modulated by on-off-keying (OOK) of the transceiver and by load modulation from the transponder (Fig 24).

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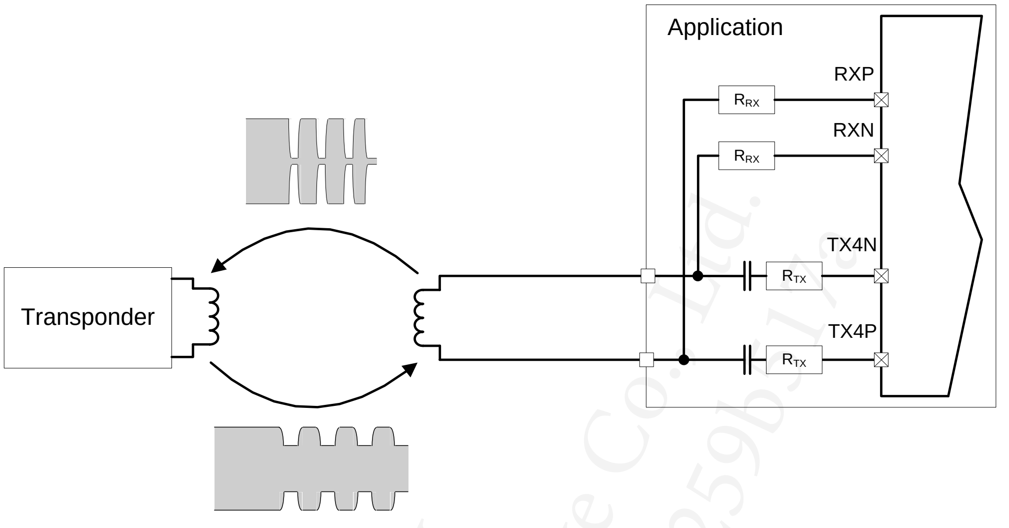

Fig 24. Immo transceiver and transponder

The carrier clock period (T_0) and the LF receiver clock reference are derived from the on-chip XTAL oscillator. The system is designed to operate at the fixed typical carrier frequency of f_C.

The LF receiver provides a differential input architecture to demodulate the load modulation employed by the transponder.

6.10.1 Immo antenna driver

Immo operation is only supported on the dedicated LF driver 4 that provides low output ripple and high antenna drive current capabilities $I_{DR,BURST}$ in order to achieve high immo operating range. The low output ripple is achived by a series low drop-out voltage regulator (LDO) in the LF driver supply path (Fig 25).

When the driver is used for immo receive operation, the regulation loop of the LDO is active and the boost converter output voltage is increased to compensate the LDO voltage drop. Pin TX4CL is used for decoupling of the LDO. For LF driver and for immo transmit operation the power switch of the LDO is permanently closed to provide the maximum LF driver supply voltage.

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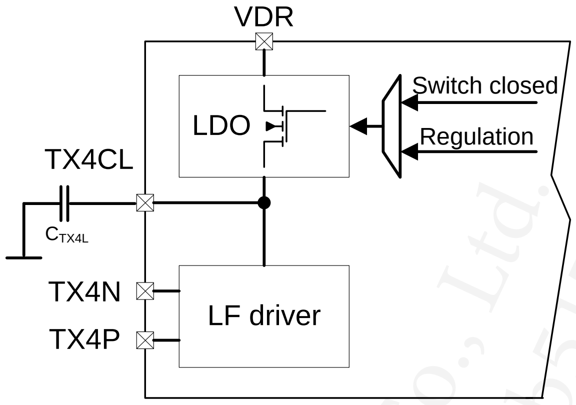

Fig 25. Immo antenna driver

It is possible to configure different values for the immo transmit and receive current. The current control loop is active during immo transmit operation only, hence during immo receive operation the current accuracy may deviate from the specified values.

It is important to notice that dithering and frequency shifting of the LF driver output signal is not supported during immo operation.

6.10.1.1 On off keying modulator

The on off keying (OOK) modulator is used to generate the binary pulse length modulation (BPLM) required for transponder communication. The BPLM pulse times for logic 0 (t_{LOG_0}), logic 1 (t_{LOG_1}), stop pulse (t_{STP}), the write pulse low duration (t_{WRP}) and the receiver wait time for the transponder response (t_{RWT}, determined by the transponder) can be configured (Fig 26).

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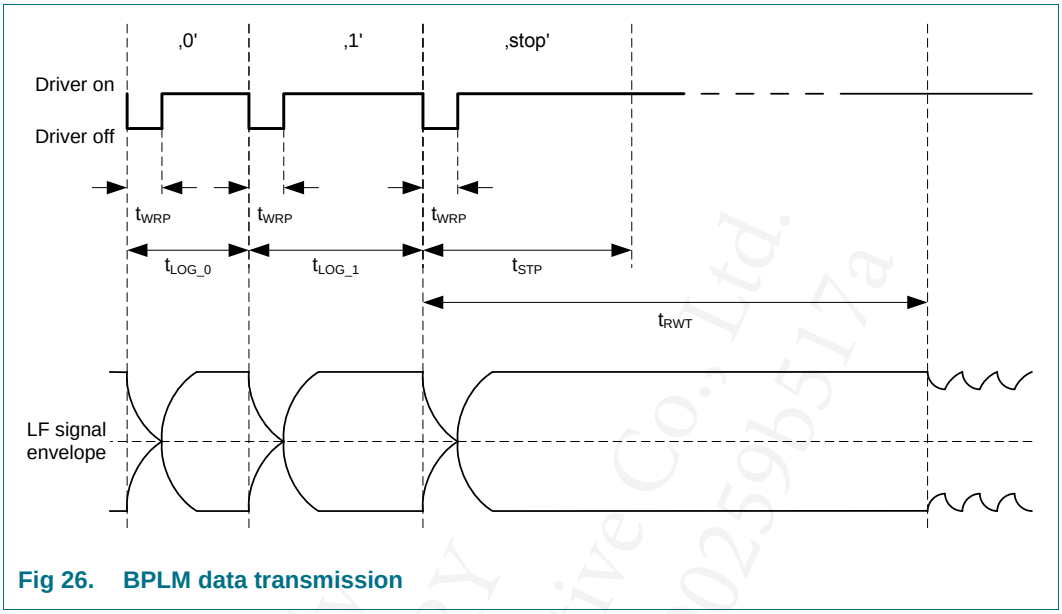

Fig 26. BPLM data transmission

6.10.2 Immo receiver

The architecture of the LF receiver is based on a direct conversion concept of the analog input signal by an ADC (Fig 27). The integrated sigma-delta ADC supports a high dynamic input range. The signal processing is done in the digital domain by decimation chains and baseband signal processing. The baseband signal processing contains the I/Q demodulator that detects the modulation even in case of detuning.

The LF receiver has its own on chip supply to prevent noise crosscoupling from the boost converter or LF drivers. The ADC and the internal supply provide dedicated decoupling pins (RXCL1 and RXCL2).

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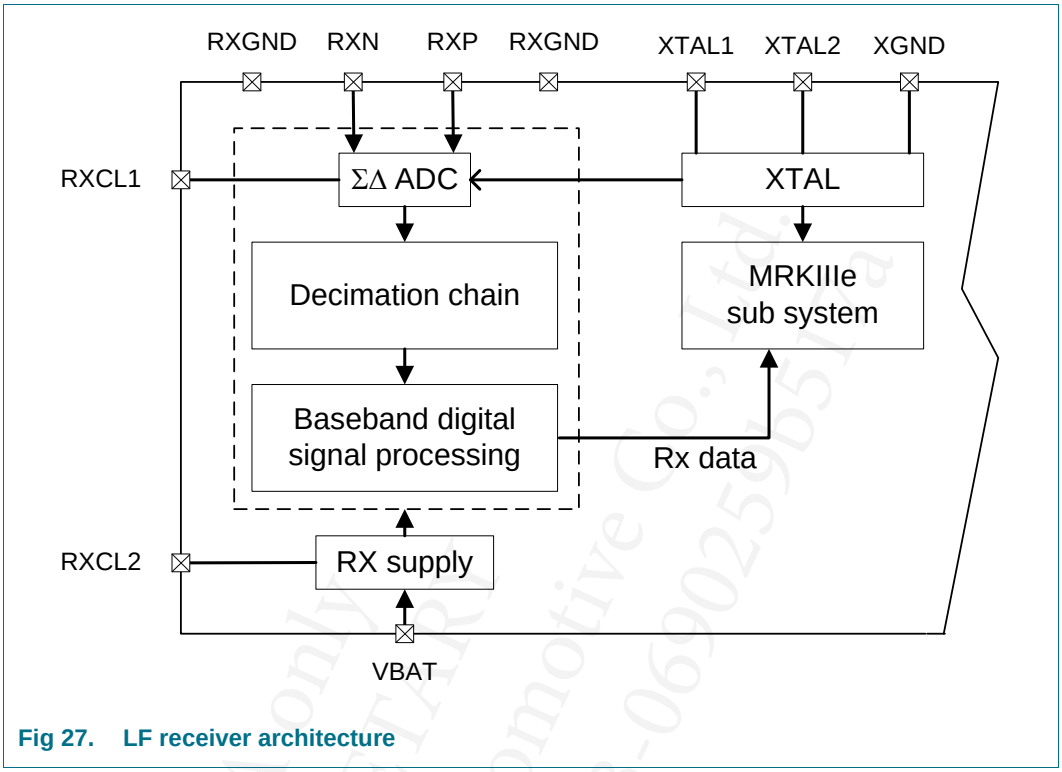

Fig 27. LF receiver architecture

6.10.2.1 Receiver input stage

The NJJ29C0B provides a differential receiver input that is connected to the tap points TAP1 and TAP2 of the immo transceiver antenna (Fig 28).

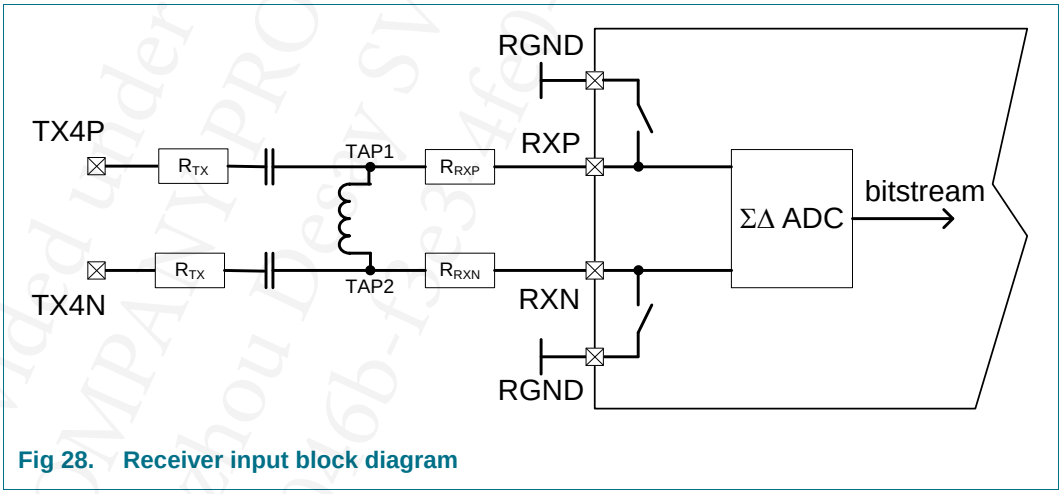

Fig 28. Receiver input block diagram

The series resistors R_{RX} between the tap points and inputs of the device shall be chosen with respect to the maximum tap peak voltages during reception of the transponder load modulation.

$$R_{RX} = \frac{V_{TAP1} - V_{TAP2}}{500\mu A} \quad (1)$$

The LF receiver sensitivity related to the LF signal envelope is shown in Fig 29.

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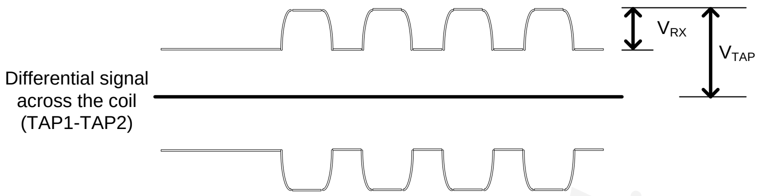

Fig 29. LF receiver sensitivity based on LF signal envelope

The LF receiver sensitivity V_{RX} scales linear with the external R_{RX} resistors. During LF signal transmission or non-operation of the receiver block the inputs of the receiver are protected against high tap voltages by switching to GND.

6.10.2.2 Digital baseband processing

The digital baseband signal processing is done on the signal that is provided by the decimation chain. A high pass filtering is applied to remove all frequencies below the band of interest. After that the Manchester decoding of the baseband signal is performed and feed to the preamble detector.

Dependent on the application configuration, the preamble detector is either looking for the equalizer (EQ 5 x “1”) or the modified equalizer (EQM 6 x “1” + 1x “0”) pattern in the transponder protocol and synchronizes the demodulator to the optimal phase and position of the Rx data in the baseband signal (Fig 30).

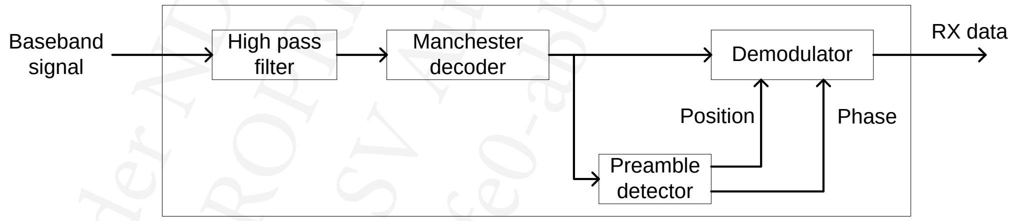

Fig 30. Digital baseband processing block diagram

6.11 Device protection

The protection circuitry monitors several functions during device operation in ACTIVE state. Should a malfunction be detected, the device enters ERROR state, hence the boost converter (if activated) immediately shuts down, the class D* drivers are deactivated and their outputs are set via pull-down resistor R_{PD} to GND.

Any detected malfunction is reported through detailed status bits. If configured, an interrupt signal is asserted for the application via the status monitoring line INT (Fig 31).

Normal operation can be resumed only after removal of the cause for the malfunction and after clearing all associated status bits. The device protection circuitry cannot be disabled.

In SLEEP and POLLING state, in case of a protection event (e.g. battery overvoltage error) the device does not wake-up and no malfunction flag is set.

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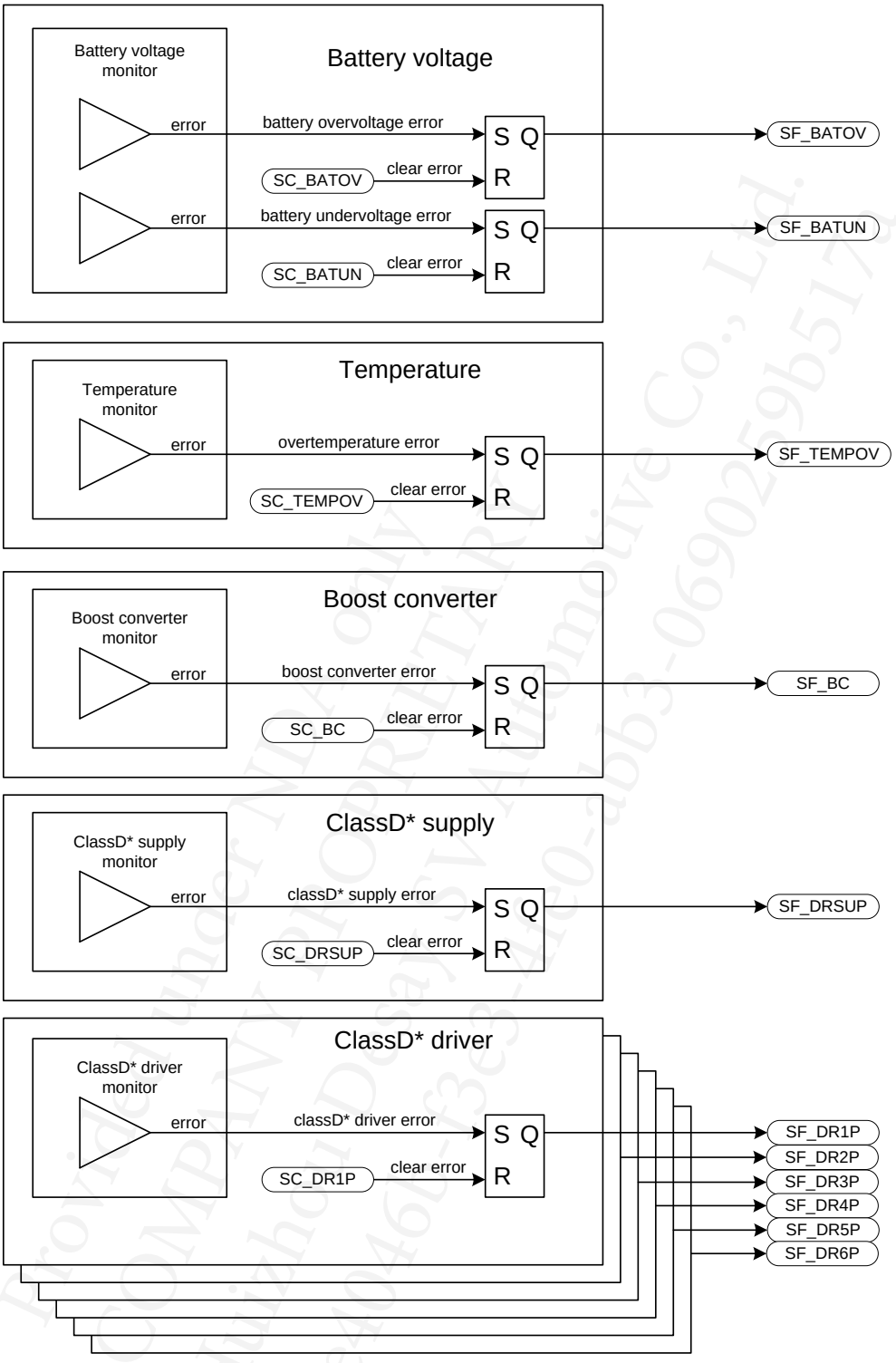

Fig 31. Device protection block diagram

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6.11.1 Battery voltage protection

The battery voltage is monitored at the device pin VBAT and compared to the permitted minimum and maximum values.

Should the maximum V_{BAT} value $V_{BAT,OVS}$ be exceeded, the protective device shut-down is immediately activated and the associated battery error flag is set.

Should V_{BAT} fall below the undervoltage shutdown detection threshold voltage $V_{BAT,UVS}$ the protective device shut-down is immediately activated and the associated battery error flag is set (Fig 32). A hysteresis guarantees that $V_{BAT,UVS,REL}$ is always at a higher level than $V_{BAT,UVS}$.

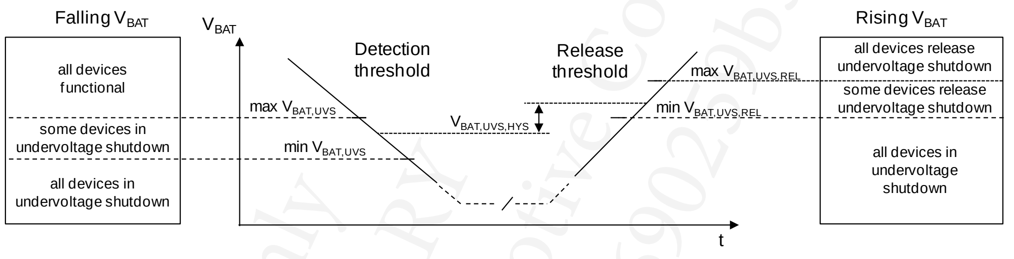

Fig 32. Undervoltage shutdown detection threshold

Should V_{BAT} fall below its minimum value $V_{BAT,MIN}$, the device enters POWER OFF state.

6.11.2 Temperature protection

The device junction temperature is monitored and compared to the maximum allowed value T_{SD}. Should this limit be exceeded, the central thermal shutdown is immediately activated and the over temperature flag is set. The thermal shutdown detection threshold does not have a hysteresis.

6.11.3 Boost converter protection

The boost converter is protected by a voltage ramp-up time control and an overvoltage detector. If a violation is recognized, the protective device shut-down is immediately activated and the boost converter error flag is set.

6.11.4 LF driver supply protection

The proper ramp-up of the common class D* supply block is monitored for short circuit and overload detection. If a violation is recognized, the protective device shut-down is immediately activated and the class D* supply error flag is set.

6.11.5 LF driver protection

Each class D* driver has a dedicated overcurrent and overvoltage detector. If an output current or output voltage failure is detected in one of the class D* drivers, the protective device shut-down is immediately activated and the respective class D* driver error flag is set.

If one or more dedicated class D* drivers cause malfunction, after clearing the respective driver status bits, normal operation with the other class D* drivers can be resumed when the harmed class D* drivers are not switched on again.

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6.12 Device diagnostics

In addition to the chip protection circuits, the device provides sophisticated diagnostics functions. Unlike the chip protection functions which are always active, diagnostics are carried out on request of the application via SPI command.

Device diagnostics are provided to identify malfunction of components in the NJJ29C0B integrated high power peripherals or to detect bad connections to external power path components without straining the device protection circuitry. The diagnostic functions can be triggered by the application for example prior to the activation of the high power peripherals or after a protection event to diagnose the system.

If a malfunction is detected, the diagnostics sets the respective failure indicator and, if configured, provides an interrupt to the application. The following failures in the power stage can be detected:

- Boost converter malfunction
- Class D* supply malfunction
- LF driver output short to ground
- LF driver output short to V_{BAT}
- Short between LF driver outputs
- Open antenna connections

The failure indicator status provides detailed information about which drivers are affected. The status can be read by the application via SPI commands (Fig 33).

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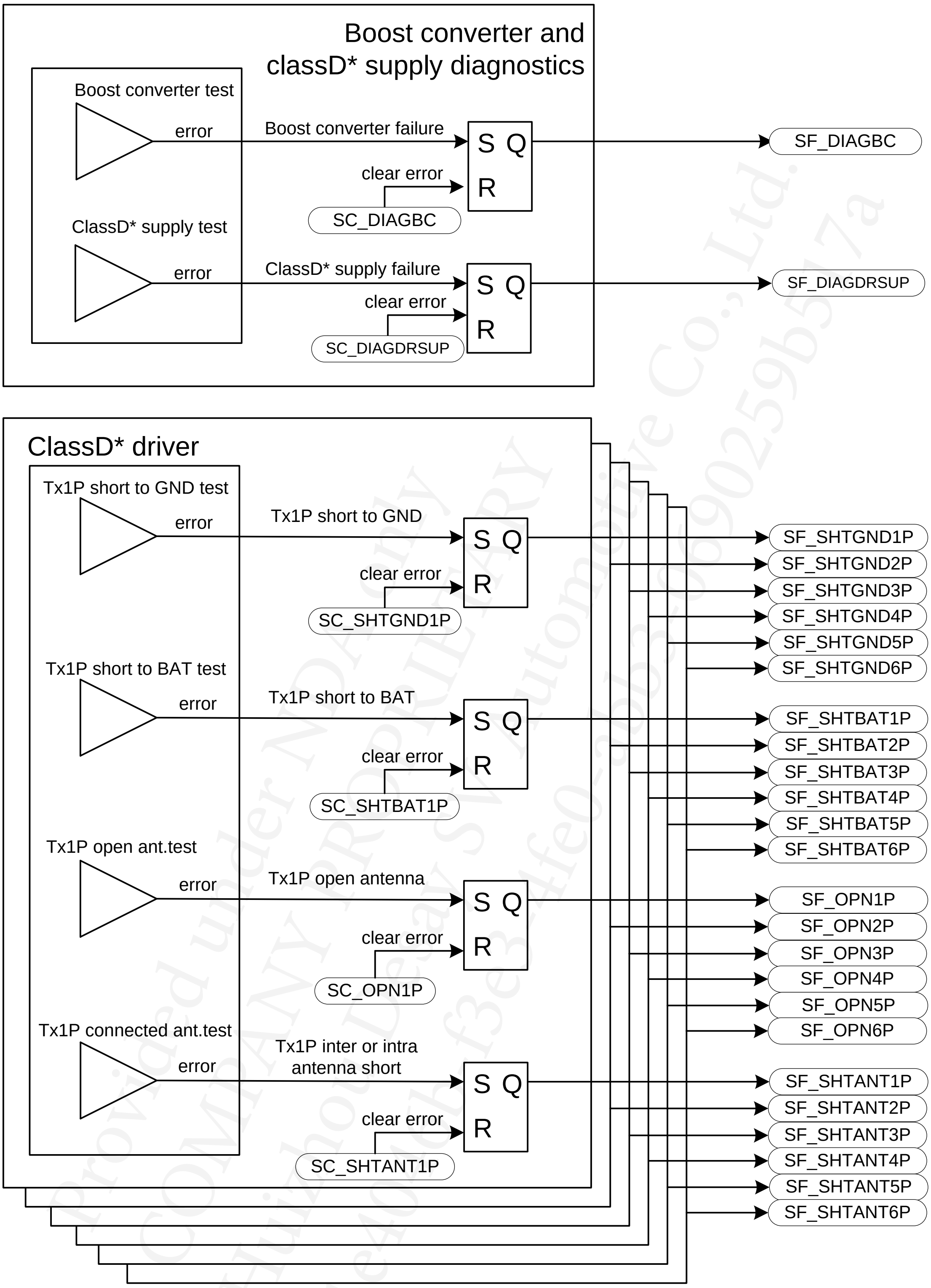

Fig 33. Device diagnostics block diagram

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6.12.1 Diagnostics sequence

The diagnostics sequence is configurable and consists of several parts. Diagnostics of the boost converter and class D* supply as well as checking each LF driver can be separately selected. The overall order of the diagnostics sequence is described in the following, assuming all diagnostics parts are activated.

First, the low dropout voltage regulator in the supply path for LF driver 4 is checked for an output DC short to ground. For this, a DC current source integrated in the regulator is used in a dedicated diagnostic mode with limited current.

Second, the external connections of the driver outputs are checked for shorts to battery, ground and to other driver outputs. This check is performed using dedicated DC current sources integrated in the class D* drivers. Boost converter, class D* supply and class D* power drivers are thus not activated in order to prevent damage at the power stages in failure case (Fig 34).

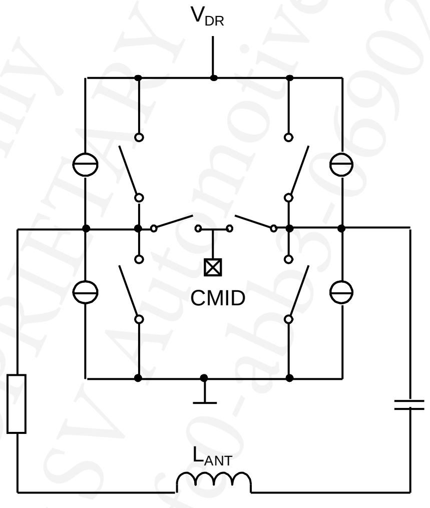

Fig 34. Class D* driver diagnostics with DC current sources

Next, the boost converter and class D* supply are enabled to check their external connections. During this test, the boost converter is activated in a special mode with limited current and the class D* driver stages are not enabled to limit the maximum output power.

Finally, the driver outputs are tested to detect any open antenna connections. For this check, the boost converter and class D* drivers are activated.

6.13 SPI interface

The NJJ29C0B provides an SPI slave interface, supplied by V_{IO}. The input pin SCSN has a pull-up configuration (Fig 35).

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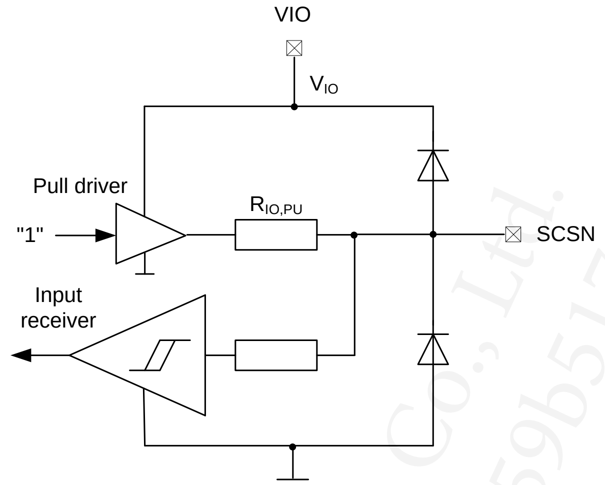

Fig 35. Input with pull-up (SCSN)

The pins SCK and SDI have an input with repeater mode (Fig 36). If an external low level is detected (voltage at pin falls below the low level threshold), the driver pulls down the pin and actively drives the low level even if the external signal is removed (e.g. because the host controller IO has changed to high impedance). If an external high level is detected (voltage at pin increases the high level threshold), the driver pulls up the pin and actively drives high level even if the external signal is removed. The pull driver is active only if V_{IO} is applied.

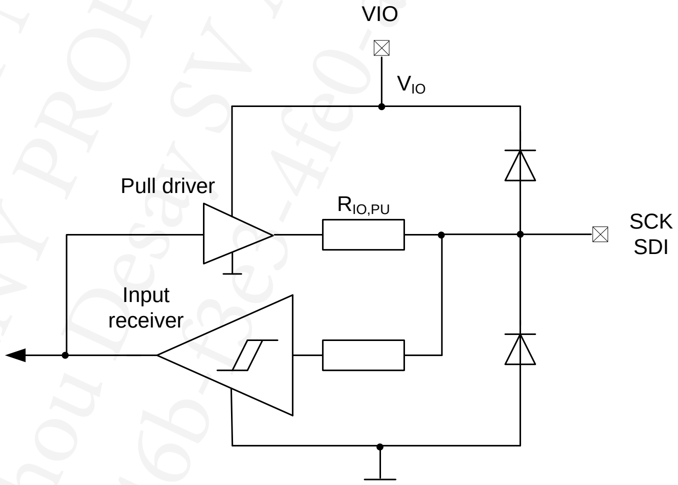

Fig 36. Input with repeater mode (SCK, SDI)

The pin SDO is a push/pull output, supplied by V_{IO} (Fig 37). The input receiver signal is not processed.

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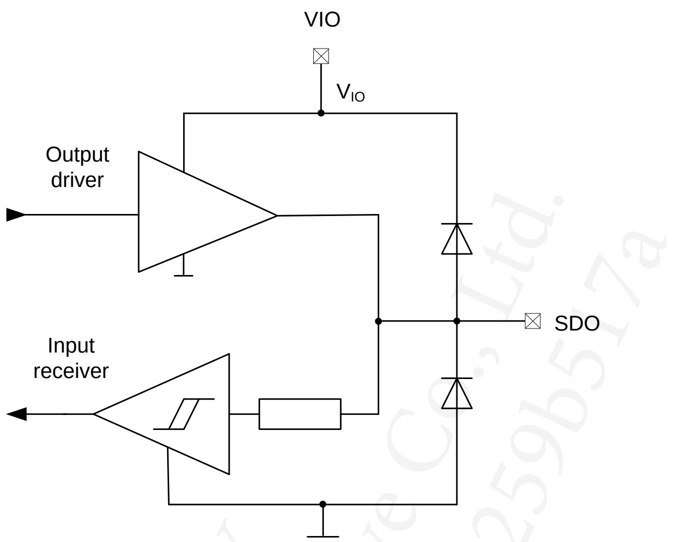

Fig 37. Push/pull output (SDO)

The host controller determines with the SPI clock signal SCLK when data is being transmitted (Fig 38).

The clock polarity is idle low (clock polarity CPOL = 0), thus the first valid edge of SCLK is a rising edge.

The SPI data coming from the host controller (SDI) is sampled after the falling edge of the SPI clock (clock phase CPHA=1). The data outgoing to the host controller (SDO) is changed after the rising edge of the SPI clock.

The SPI data transfer is byte-oriented. Each byte transfer begins with the LSBit and ends with the MSBit.

If SCSN becomes temporarily high after reception of a complete byte, the reception of the following bytes will be continued after SCSN becomes low again, provided that the expected data reception time has not been exceeded.

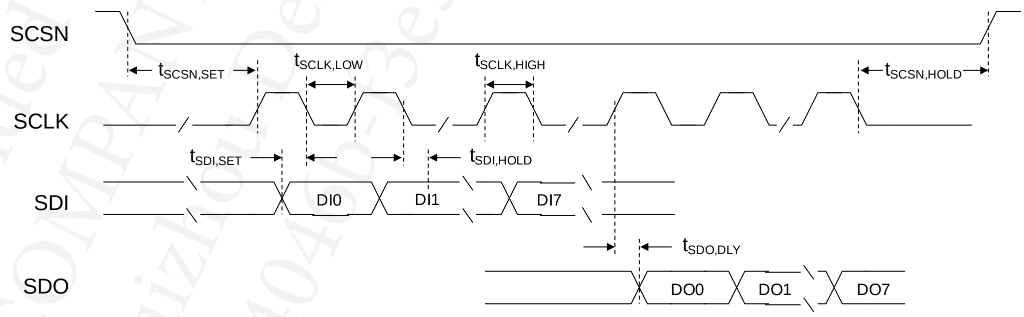

Fig 38. SPI communication (ACTIVE state)

6.14 Status monitor

The interrupt pin INT is a push/pull output, supplied by V_{IO} (Fig 39).

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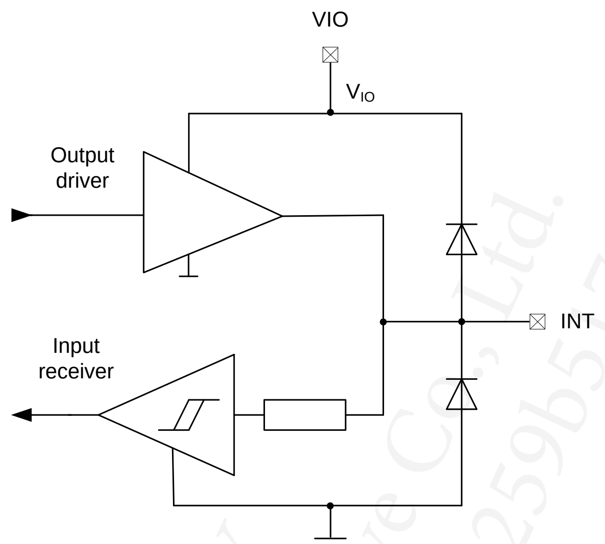

Fig 39. Push/pull output (INT)

The INT pin is used as status monitor line asserted to signal the application that an unexpected notable event within the NJJ29C0B has occurred, and that attention is required from the application. The input receiver signal is not processed in the device.

If a power on reset occurs, after completing the cold start sequence the INT pin is always set. In difference, the following events can be assigned by the application to trigger the INT line (Table 10).

Table 10. INT monitor line assignment

Event group	Event description	Status flag
Immobilizer	Immo ADC overdrive	SF_OVRDRV
Protection	Boost converter voltage error	SF_BC
	Driver supply voltage error	SF_DRSUP
	LF driver i current or voltage error	SF_DRiP
	Battery overvoltage	SF_BATOV
	Battery undervoltage	SF_BATUN
	Over temperature	SF_TEMPOV
Wake-up ports	Port i wake-up	SF_WUPi
Temperature indication	Temperature warning	SF_TWARN
Operation status	LF transmission ready	SF_TXREADY
	Immo receiver ready	SF_RXREADY
	Impedance measurement ready	SF_IMPMEAS
	Diagnostics ready	SF_DIAG

The INT monitor line functionality is enabled by setting the appropriate configuration in the corresponding mask bit (SM_xx) (Fig 40). The INT line is reset by clearing the respective SC_xx bit (provided no other event masked to set the INT line is triggered).

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Independent of enabling or disabling the INT monitor line functionality, the application can read the device status by polling the associated status flags SF_xx.

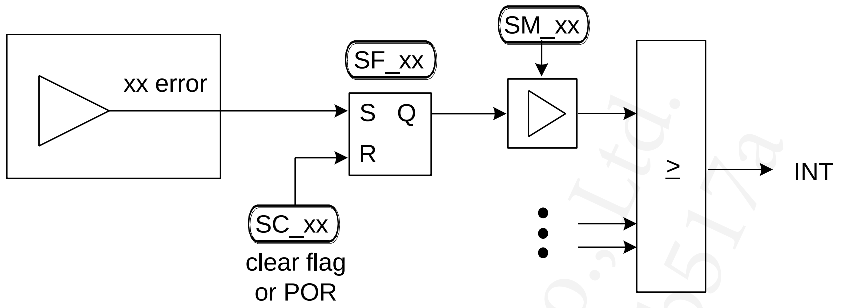

Fig 40. Status flag handling and INT output (realized in software)

Setting of the INT line is associated with the respective status flag SF_xx and not with the causing event. For example, as the flag SF_TXREADY is not set after finishing LF transmission in timer triggered polling mode, also the INT pin is not set in this case.

The INT pin is never set in SLEEP and POLLING state.

6.15 Reset input

The reset input RSTN is an active low digital input with permanent pull-up, supplied by V_{IO} (Fig 41).

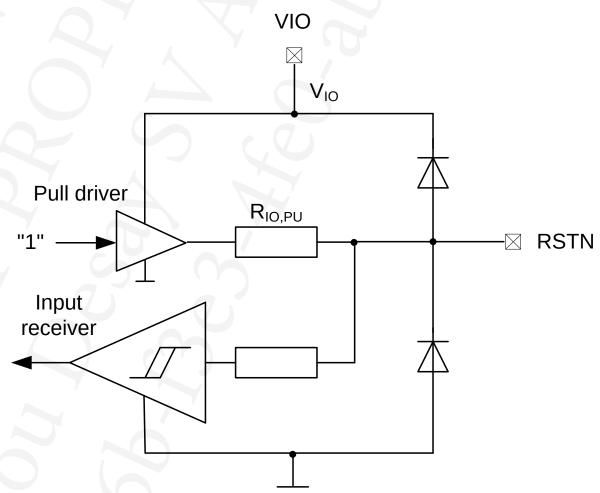

Fig 41. Input with pull-up (RSTN)

Setting RSTN to "low" causes all NJJ29C0B blocks to reset. After releasing the RSTN pin the device starts up with a power on reset.

6.16 Wake-up ports

The device provides six inputs with wake-up logic (e.g. for sensor interfaces) (Fig 42).

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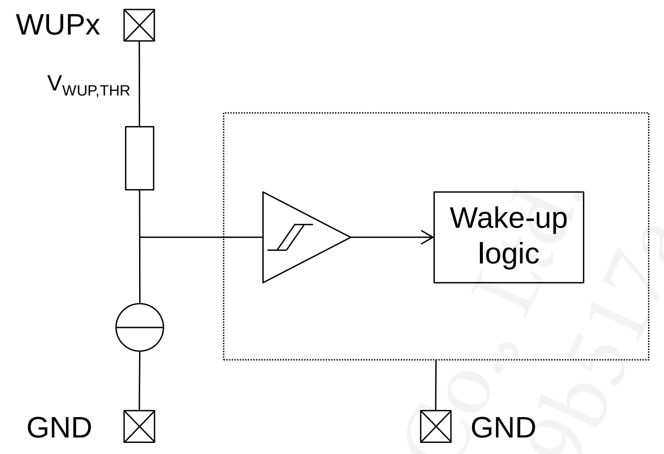

Fig 42. Input with wake-up logic

After enabling, all wake-up ports (WUP1 to WUP6) are able to cause wake-up events. The signal edge is configurable. A wake-up event is recognized after a filter time $t_{WUP,WAKE}$, which helps to prevent triggering on disturbance pulses. All device specific timings start after internal detection of the wake-up event.

If the device is in SLEEP or POLLING state, first the embedded μController wakes up within the time $t_{MRK3,WAKE}$ and transfers into IDLE state.

In IDLE state, the embedded μController debounces and validates the wake-up signal, dependent on the configuration. Each wake-up signal classified as valid sets a port related internal flag, which has to be cleared by the application. Additionally, the INT pin is set, if configured.

If the wake-up signal is classified as invalid and the wake-up event was triggered in SLEEP or POLLING state before, the device re-enters SLEEP or POLLING state again, respectively.

The polling sequence timing diagram (transfer from IDLE to PKE state) is shown in Fig 43, assuming that additional wake-up signal debouncing and validation is switched off.

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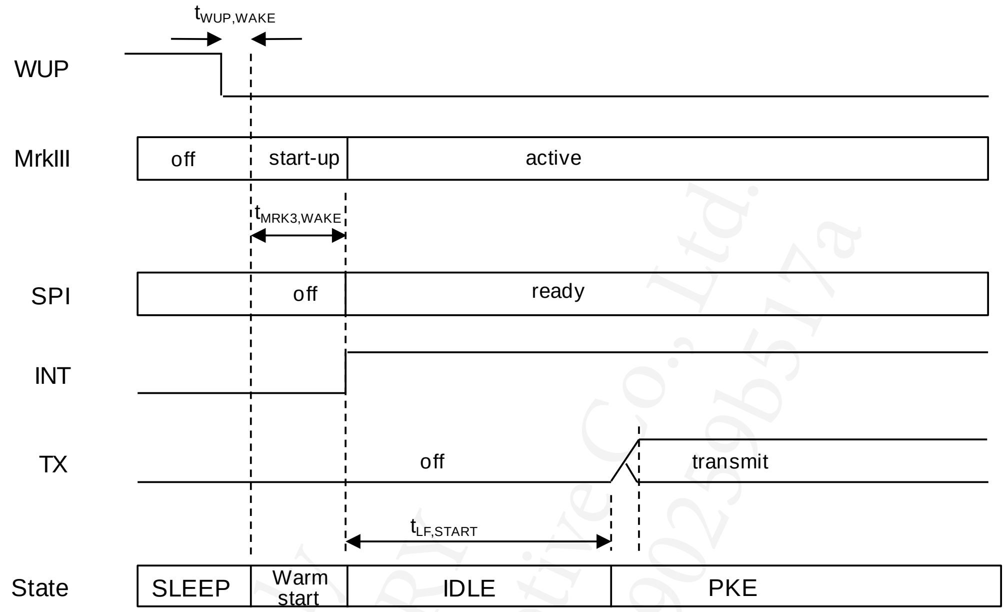

Fig 43. Start-up und LF timing (shown for wake-up event triggered polling operation)

6.17 Polling timer

The polling timer clock is generated with the help of the integrated low power RC oscillator. The polling timer is used in POLLING state to wake-up the device periodically after pre-configurable timing intervals and to send autonomously LF telegrams with flexible length via the telegram sequencer without support from the application. The polling sequence can be configured by the application.

Fig 44 shows an example for a timer triggered polling sequence. After starting the pre-configured polling sequence via SPI command, the device switches to POLLING state until the configured polling time 1 exceeds. The NJJ29C0B transfers to PKE state and starts sending the pre-configured data1 in parallel on TXi and TXiii. The data have to be identical for simultaneously used channels and can contain all data codings supported by the telegram sequences including constant carrier signals and carrier off phases. An example for two data patterns interrupted by a carrier off phase is shown after exceeding of polling time 2.

The whole polling sequence is repeated continuously until a wake-up event occurs. Afterwards, the NJJ29C0B transfers to IDLE state, sets the INT pin (if configured for the wake-up event) and waits for further instructions from the application.

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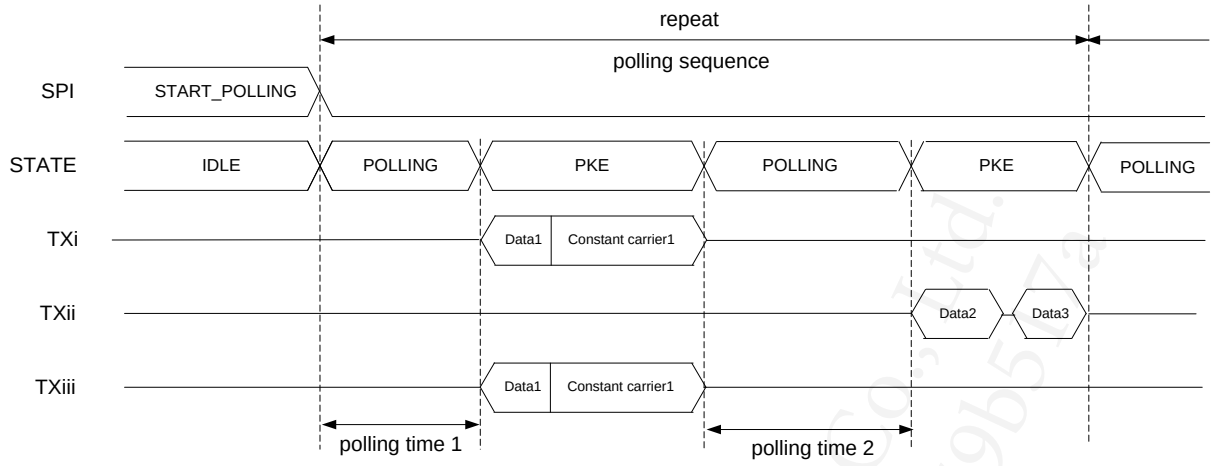

Fig 44. Timer triggered LF polling (example polling sequence)

6.18 Watchdog timer

The device incorporates a watchdog timer. The watchdog timer is active in all ACTIVE states and is inactive otherwise. If the watchdog timer is active and not periodically restarted by the embedded system software of the µController, it generates a device reset. Consequently, the device passes through a power on reset cycle and continues program execution, starting with the cold start sequence.

6.19 Temperature indication

The NJJ29C0B contains a build-in temperature indication unit that checks the device junction temperature. The temperature indicator is used both for device over temperature protection and for comparing the junction temperature with a temperature threshold programmable in the range between the minimum and maximum value of T_{IND} in steps of $T_{IND,STEP}$.

Setting the pre-programmed temperature warning to a value below the device over temperature protection threshold allows the application to take corrective measures if the threshold temperature is reached. For example, one measure might be to discard sending the next LF telegram, or to decrease the number of simultaneously driven channels, or the power level at which LF transmissions are made.

The temperature threshold measurement function can be configured to trigger the application via the INT pin.

6.20 Antenna impedance measurement

In order to allow making pre-settings for the boost converter, LF driver supply and classD* duty cycle even if the application did not pre-configure antenna parameters, the NJJ29C0B provides facilities to measure the antenna impedance.

The application selects the antennas to be measured and starts the antenna impedance measurements. The NJJ29C0B determines the magnitude and phase of the antenna impedance for each of the selected connected antennas. The determined values are stored and used to calculate the respective boost converter settings and initial class D* driver duty cycle for antenna driver operation.

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6.21 μController

The NJJ29C0B contains an integrated 16-bit μController powered by NXP's 3rd generation low power μController kernel with enhanced instruction set (MRKIIIe), which controls device operation.

The μController utilizes a Harvard architecture featuring a 16 bit ALU.

The μController is ready for operation within the start-up time $t_{MRK3,WAKE}$ after recognizing a wake-up event in SLEEP state.

6.22 Memory modules

The device contains two different types of memories

- ROM
- RAM

6.22.1 ROM

The ROM contains the NXP implemented embedded system software including the SPI command handler. The system code memory is not visible for the application.

6.22.2 RAM

The battery backed RAM is used by the μController core during system code execution. The RAM is also used for data storage and embedded system software extensions downloaded via SPI commands. Before starting a download, a POR shall be asserted to clear the RAM history and to ensure a safe setup.

The RAM contents are preserved in SLEEP, POLLING and ACTIVE states, but are lost in POWER OFF state.

6.22.3 Memory and application program protection

The integrity of the memory content is checked by the measures

- Watchdog timeout
- RAM parity checks
- Access permission checks

Should one of the integrity checks indicate a problem, the device performs a power on reset.

6.23 SPI controlled operation

The device is supervised by the application via SPI commands. The NJJ29C0B reads and acts on data received via SPI according to the specified protocol and timing. The SPI handling is performed by the μController.

The SPI command set gives access and control to all device functions including diagnostics and telegram sequencer. A dedicated SPI command with flexible parameter setting enables the NJJ29C0B to autonomously send LF data without further SPI interaction of the application. The autonomous transmission of the data buffer content via the telegram sequencer is triggered by the polling timer or by a wake-up event recognized at the wake-up ports.

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7. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{amb}	Operating temperature		-40	+105	°C
T_{sto}	Storage temperature		-40	+105	°C
T_{vj}	Virtual junction temperature		-40	+175	°C
$V_{max,BAT}$	Voltage at pin VBAT		[1] -0.3	+40	V
$V_{max,BCSW}$	Voltage at pin BCSW		[1] -0.3	+40	V
$V_{max,DR}$	Voltage at pin VDR		[1] -0.3	+40	V
$V_{max,TX}$	Voltage at any TX pin		[1] -0.3	+40	V
$V_{max,WUP}$	Voltage at any WUP pin		[1] -0.3	V_{BAT}+0.3	V
$I_{max,WUP}$	Current at any WUP pin		-5	+5	mA
$V_{max,VIO}$	Voltage at pin VIO		[1] -0.3	+6.0	V
$V_{max,IO}$	Voltage at any V_{IO} related pin (INT, RSTN, SCSN, SCK, SDI, SDO, TEST1, TEST2)		[1] -0.3	V_{IO}+0.3	V
$V_{max,TEST3}$	Voltage at pin TEST3		-3.6	+0.3	V
$V_{max,TEST4}$	Voltage at pin TEST4		-0.3	+3.6	V
$I_{max,TEST4}$	Current at pin TEST4			100	µA
$V_{max,XTAL}$	Voltage at any XTAL pin		[1] -0.3	+1.95	V
$I_{max,RX}$	Current at any RX pin		[1] -2	+2	mA
$I_{latch-up}$	Latch-up current		[2] -100	+100	mA
$V_{ESD,HBM}$	ESD, human body model	local pins	[3] 2		kV
		global pins	[3] 4		kV
$V_{ESD,CDM}$	ESD, charged device model		[4] 500		V

Notes

[1] With respect to GND

[2] According to AEC-Q100-004

[3] According to AEC-Q100-002

[4] According to AEC-Q100-011

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8. Thermal characteristics

Table 12. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{TH,JC}$	Thermal resistance from junction to case	[1]	8	K/W

Notes

[1] Dependent of the thermal coupling between package and PCB. Simulated value for junction to case, if case is connected to an infinite heat sink PCB area @ 0 m/s air flow.

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9. Static characteristics

Table 13. Static characteristics

T_{amb} = -40 to +105 °C, GND = 0 V, V_{BAT} = 8 V to 18 V, V_{IO} = 2.9 V to 5.5 V, f_C = 125 kHz, T_0 = 1/f_C, C connected between pins VBAT and GND, Z_{ANT} = 10 to 20 Ω, Q ≤ 25, external components according to Table 14, full-bridge mode with midlevel control.

Unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Battery supply							
$V_{BAT,POR}$	Power on reset detection threshold voltage			3.5		4.0	V
$V_{BAT,POR,REL}$	Power on reset release threshold voltage			5.0		5.5	V
$V_{BAT,POR,HYS}$	Power on reset hysteresis		[1]	0.7	1.6	2.0	V
$V_{BAT,UVS}$	Undervoltage shutdown detection threshold voltage			4.5		5.0	V
$V_{BAT,UVS,REL}$	Undervoltage shutdown release threshold voltage			5.0		5.5	V
$V_{BAT,UVS,HYS}$	Undervoltage shutdown hysteresis		[1]	0.3	0.6	1.0	V
$V_{BAT,OVS}$	Overvoltage shutdown detection threshold voltage			28		30	V
$V_{BAT,OVS,REL}$	Overvoltage shutdown release threshold voltage			26.5		28.5	V
$V_{BAT,OVS,HYS}$	Overvoltage shutdown hysteresis		[1]	1.0	1.7	2.5	V
$I_{BAT,SLEEP}$	Battery supply current in SLEEP state	T_{VJ} @ 30 °C	[2] [3]		15	25	µA
		T_{VJ} @ 55 °C	[2] [3]		16	35	µA
		T_{VJ} @ 85 °C	[2] [3]		25	65	µA
		T_{VJ} @ 105 °C	[2] [3]		65	200	µA
$\Delta I_{BAT,POLL}$	Additional battery supply current in POLLING state with respect to $I_{BAT,SLEEP}$		[2]			20	µA
$I_{BAT,IDLE}$	Battery supply current in IDLE state	V_{RSTN} = V_{SCSN} = V_{IO}, V_{SCK} = GND, V_{WUP1-6} = GND	[2]		2.1	4.5	mA
$I_{BAT,XTAL}$	Battery supply current in IDLE state with XTAL running		[2]		2.3	5	mA
$I_{BAT,CLK}$	Battery supply current in IDLE state with XTAL and PLL running		[2]		9.5	12	mA
$I_{BAT,BC}$	Battery supply current in IDLE state with XTAL, PLL and boost converter running (boost converter enabled without load)	V_{DR} = 15 V	[2]		17	23	mA
		V_{DR} = 25 V	[2]		18	27	mA
$I_{BAT,DR,SUPPLY}$	Battery supply current in IDLE state	V_{DR} = 15 V	[2]		22	32	mA

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
	with XTAL, PLL, boost converter and LF driver supply running	V_{DR} = 25 V	[2]		24	35	mA
$I_{BAT,DR,NOLOAD}$	Additional battery supply current for each LF driver channel enabled, without antenna connected to the driver output		[2]		5	9	mA
$I_{BAT,RX}$	Additional battery supply current during immo receive operation		[2] [4]		22	28	mA
XTAL oscillator							
$R_{XTAL,MARGIN}$	Oscillation start-up margin		[5]		1		kΩ
$C_{XTAL,1}$	Pin capacitance		[5]	0.5	1	2	pF
$C_{XTAL,2}$	Pin capacitance		[5]	1	1.6	2.5	pF
Boost converter							
V_{BC}	Typical output voltage	5 V < V_{BAT} ≤ 11.5 V Single channel IMMO state	[6] [7]	13.5		30	V
		V_{BAT} > 11.5 V Single channel IMMO state	[6] [7]	V_{BAT} + 2		30	V
		5 V < V_{BAT} ≤ 8 V Single channel PKE state	[7]	13.5		25	V
		8 V < V_{BAT} ≤ 11.5 V Up to 3 channels simultaneously PKE state	[7]	13.5		25	V
		V_{BAT} > 11.5 V Up to 3 channels simultaneously PKE state	[7]	V_{BAT} + 2		25	V
$I_{BC,DR,SUPPLY}$	Boost converter load current for internal LF driver supply	V_{DR} = 15 V	[2]		16	27	mA
		V_{DR} = 25 V	[2]		22	35	mA
$I_{BC,DR,NOLOAD}$	Boost converter load current per LF antenna driver channel, without antenna load connected to the driver output	V_{DR} = 15 V	[2]	8	13	29	mA
		V_{DR} = 25 V	[2]	8	18	29	mA
$I_{BC,STEP,NUM}$	Coil current limitation step number		[8]		13		-
$I_{BC,STEP,SIZE}$	Coil current limitation step size			0.4	1	1.5	A
$I_{BC,STEP,ACC}$	Coil current limitation accuracy	CUR_MAX[3:0]=0x0Fh		-15		+15	%
LF antenna driver							
$I_{DR,BURST}$	Output peak current driver capability per channel in burst mode	Single channel	[9] [10] [11]	1 - $I_{DR,ACC}$			A
		2 channels simultaneously	[9] [10] [12]	1 - $I_{DR,ACC}$			A

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		3 channels simultaneously	[9] [10] [12]	1 - $I_{DR,ACC}$			A
$I_{DR,LV}$	Output peak current burst mode for low battery supply voltage	5 V < V_{BAT} < 8 V, Single channel	[10] [11]	0.3			A
$I_{DR,HV}$	Output peak current burst mode for high battery supply voltage	18 V < V_{BAT} < 28 V, Single channel	[10] [11] [13]	0.3			A
$I_{DR,CONT}$	Output peak current continuous wave	Single channel, V_{BAT} = 8 V, 1 min continuous operation	[10]	0.6			A
		Single channel, V_{BAT} = 5 V, 1 min continuous operation	[10]	0.2			A
$I_{DR,RANGE}$	Output peak current range	PKE state All channels	[14] [15] [16]	47		1000	mA
		IMMO state, channel 4 Z_{ANT} = 20 Ω	[14] [15]	220		1000	mA
		IMMO state, channel 4 Z_{ANT} = 10 Ω	[14] [15]	330		1000	mA
$I_{DR,STEP}$	Output peak current step size		[17]		15.625		mA
$I_{DR,ACC}$	Output peak current absolute accuracy	Burst mode without modulation Antenna tuned Dithering off PKE operation and immo transmit operation 0.5 $I_{DR,BURST}$ < I ≤ $I_{DR,BURST}$	[18] [19] [20] [21] [22]	-3% -20mA		+3% +20mA	
		Burst mode without modulation Antenna tuned Dithering off PKE operation and immo transmit operation min $I_{DR,RANGE}$ < I ≤ 0.5 $I_{DR,BURST}$	[18] [19] [20] [21] [22]	-4% -20mA		+4% +20mA	
$I_{DR,SHORT}$	Output current short circuit detection threshold	5 V < V_{BAT} < 28 V	[23]	1.5		3.0	A
N_{DR}	Number of simultaneously driven channels (antennas)			2		3	
Z_{ANT}	Magnitude of complex antenna load impedance	$I_{DR,BURST}$ = 1 A with DCY_{DR} up to 66.6%	[24]	10		20	Ω
$R_{DR,ON}$	Driver main switch on-state resistance		[25]		1.2	3.0	Ω
$R_{DR,PD}$	Driver internal pull-down resistor for non used channels			10	22	50	kΩ
Low current driver							
I_{DRLC}	Maximum output peak-peak current		[26]	16		67	mA

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{DRLC}	Low current outputs driven simultaneously to main LF antenna driver			0		5	
Receiver							
V_{RX}	Differential peak-peak sensitivity between TAP1 and TAP2	5 V < V_{BAT} < 28 V, V_{TAP} = 255 V (peak), R_{RX} = 510 kΩ	[27] [28] [29]	2	10	25	mV
R_{RX}	RX pin resistors			100			kΩ
Protective temperature shut-down							
T_{SD}	Temperature shutdown detection threshold			160	167	174	°C
Diagnostics							
$V_{DIAG,SHTBAT}$	Driver short to battery supply detection threshold voltage			0.5	1	1.6	V
$V_{DIAG,SHTGND}$	Driver short to GND supply detection threshold voltage			V_{DR} – 2.5V	V_{DR} – 1.7V	V_{DR} – 1.3V	V
$I_{DIAG, SHTBAT}$	Driver short to battery supply detection current	1 channel in half bridge configuration		1.1		3.1	mA
$I_{DIAG, SHTGND}$	Driver short to GND supply detection current	1 channel in half bridge configuration		1.1		3.1	mA
IO interface (host controller interface, reference voltage for SCSN, SCK, SDO, SDI, INT, RSTN)							
V_{IO}	Supply voltage range	4 V < V_{BAT} < 28 V		2.9		5.5	V
$V_{IO,UVD}$	Undervoltage detection threshold voltage	5 V interface, 4 V < V_{BAT} < 28 V		4.35	4.5	4.65	V
		3.3 V interface, 4 V < V_{BAT} < 28 V		2.90	3.00	3.10	V
$V_{IO,UVD,REL}$	Undervoltage release threshold voltage	5 V interface, 4 V < V_{BAT} < 28 V		4.45	4.60	4.75	V
		3.3 V interface, 4 V < V_{BAT} < 28 V		3.00	3.10	3.20	V
I_{IO}	Supply current	V_{IO} = 5 V unloaded			6	14	µA
		V_{IO} = 3.3 V unloaded			5	12	µA
$V_{IO,IN,HIGH}$	High level input voltage	2.9 V < V_{IO} < 5.0 V	[30]	0.7*V_{IO}		V_{IO}	V
		5.0 V ≤ V_{IO} < 5.5 V	[30]	0.75*V_{IO}		V_{IO}	V
$V_{IO,IN,LOW}$	Low level input voltage	2.9 V < V_{IO} < 5.0 V	[31]	0		0.3*V_{IO}	V
		5.0 V ≤ V_{IO} < 5.5 V	[31]	0		0.25*V_{IO}	V
$V_{IO,HYS}$	Input hysteresis			0.05*V_{IO}		0.4*V_{IO}	V
$V_{IO,OUT,HIGH}$	High level output voltage	$I_{IO,OUT}$ = 4 mA		V_{IO}-0.4		V_{IO}	V
$V_{IO,OUT,LOW}$	Low level output voltage	$I_{IO,OUT}$ = -4 mA		0		0.4	V
$I_{IO,IN}$	Input current			-1		1	µA
$I_{IO,OUT}$	Output current drive capability	V_{IO}-0.4 V		4		12	mA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{IO,PU}$	Internal pull-up resistor	Pin RSTN, SCSN	40		100	kΩ
Wake-up input						
$I_{WUP,IN}$	Input current for each pin WUPi	V_{WUP} < 28 V	0		1.5	µA
$V_{WUP,THR}$	Wake-up input threshold voltage	5 V < V_{BAT} < 28 V	2		4	V
Temperature indication						
T_{IND}	Temperature indication range	[32]	85		155	°C
$T_{IND,STEP}$	Temperature indication step size	[32]		5		°C

[1] By the hysteresis it is guaranteed for each single device that the release threshold voltage is always at higher level than the detection threshold voltage

[2] See Fig 48

[3] $I_{BAT,SLEEP}$ increases for battery voltages V_{BAT} below 8V

[4] Only receiver without LF driver which needs to be activated for receiving

[5] For characterization, the 16 MHz quartz crystal unit NDK NX3225GB -16.000M was used

[6] The boost converter delivers typical 30 V to compensate the voltage drop of the series LDO in the LF driver supply path during immo operation. The typical maximum output voltage at pin TX4CL is 25V.

[7] The min and max value is a typical value each. The absolute maximum value can become up to 2 V higher. Please note that special external conditions like load dump are not considered.

[8] Lowest coil current limitation setting starts with an offset, thus the maximum value of the coil current limitation exceeds $I_{BC,STEP,NUM}$ * $I_{BC,STEP,SIZE}$

[9] Characterized in continuous mode operation

[10] Dependent of the thermal coupling between package and PCB, simulated value for JEDEC Test Card: 2 - Layer, 50x50mm with 1 ground plane, CU 35 µm; @ 0 m/s air flow.

[11] Single channel burst operation is 1:5 ON/OFF ratio, max burst length < 50 ms constant carrier

[12] Simultaneous channel burst operation is 1:13 ON/OFF ratio, max burst length < 20 ms constant carrier

[13] Minimum LF antenna driver current might be higher for Z_{ANT} < 20 Ω

[14] Value is a (rounded) multiple of $I_{DR,STEP}$

[15] The minimum output peak current is below or equal to the min. value of $I_{DR,RANGE}$ plus the max. value of $I_{DR,ACC}$. The maximum output peak current is above or equal to the max. value of $I_{DR,RANGE}$ minus the min. value of $I_{DR,ACC}$.

[16] For low current values or in case of relevant antenna detuning, the LF antenna is automatically driven in feed-forward (uncontrolled) operation.

[17] Value derived from $I_{DR,BURST}$ / 64, corresponding to 64 current steps

[18] The current is measured inside the device and not in the antenna. Depending on the antenna topology and the antenna cable length the antenna driver current can differ.

[19] In order to comply with the antenna driver current accuracy the device needs the knowledge of the antenna impedance (for example by interrogating the MEAS_ANT_IMP_ADVANCED command).

[20] The specified antenna current accuracy is valid in tuned antenna condition. For detuned antennas please refer to the device application note.

[21] The characterization was performed with current probe and applying a band pass filter.

[22] A peak-to-peak measurement of the time signal gives correct results for a pure sine signal only. As the the antenna current signal is disturbed in general, it is measured by applying a Fourier transformation with Flat Top window to separate the relevant f_c frequency component.

[23] The shut down will not trigger below the min. value of $I_{DR,SHORT}$. The shut down will always trigger above the max. value of $I_{DR,SHORT}$.

[24] Higher and lower values for Z_{ANT} are possible, but with functional limitations (antenna driver current range / antenna driver current accuracy). Lower Z_{ANT} values will reduce the number of available current steps. Higher Z_{ANT} values do not allow $I_{DR,BURST}$ maximum current with a driver duty cycle DCY_{DR} up to 66.6%.

[25] Each LF driver contains 4 main switches, 2 of which are active simultaneously

[26] The current is adjusted via the low current driver duty cycle. The current value depends on the antenna impedance.

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[27] Sensitivity scales linear with V_{TAP} and therefore R_{RX} shall be adjusted accordingly.

[28] R_{RX} shall have 1/f noise below 1.7e-7 V_{RMS}/Hz in the frequency range of 500 Hz – 8 kHz.

[29] Sensitivity is measured differentially across the coil according to Fig 29.

[30] Application has to ensure that the input voltage is above the min valueof High level input voltage

[31] Application has to ensure that the input voltage is below the max value of Low level input voltage

[32] See Fig 49

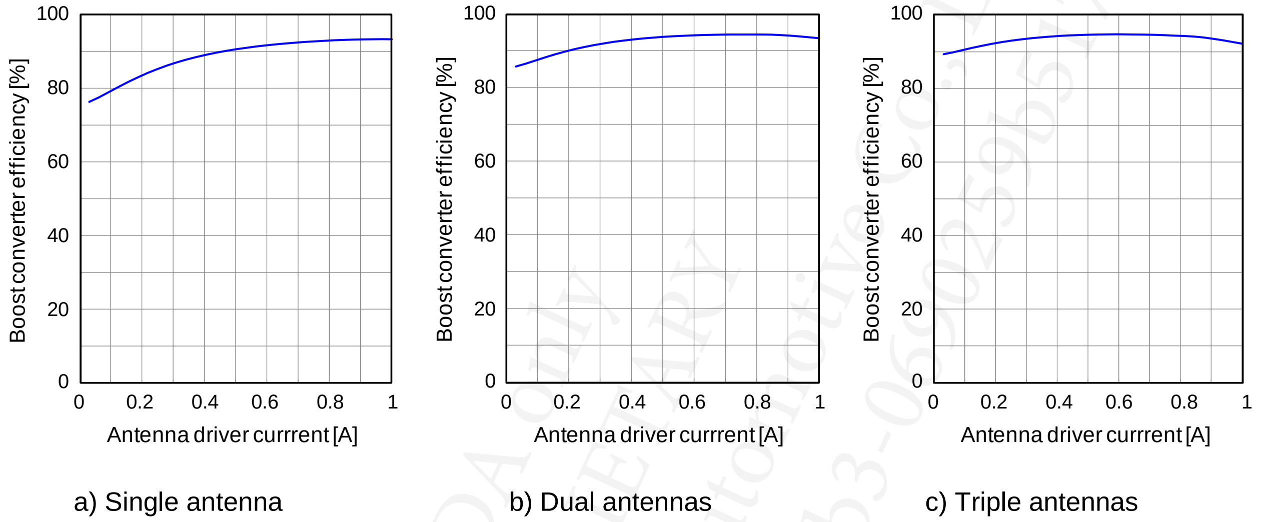

Fig 45. Typical boost converter power efficiency, PKE operation, V_{BAT} = 12 V, Z_{ANT} = 20 Ω

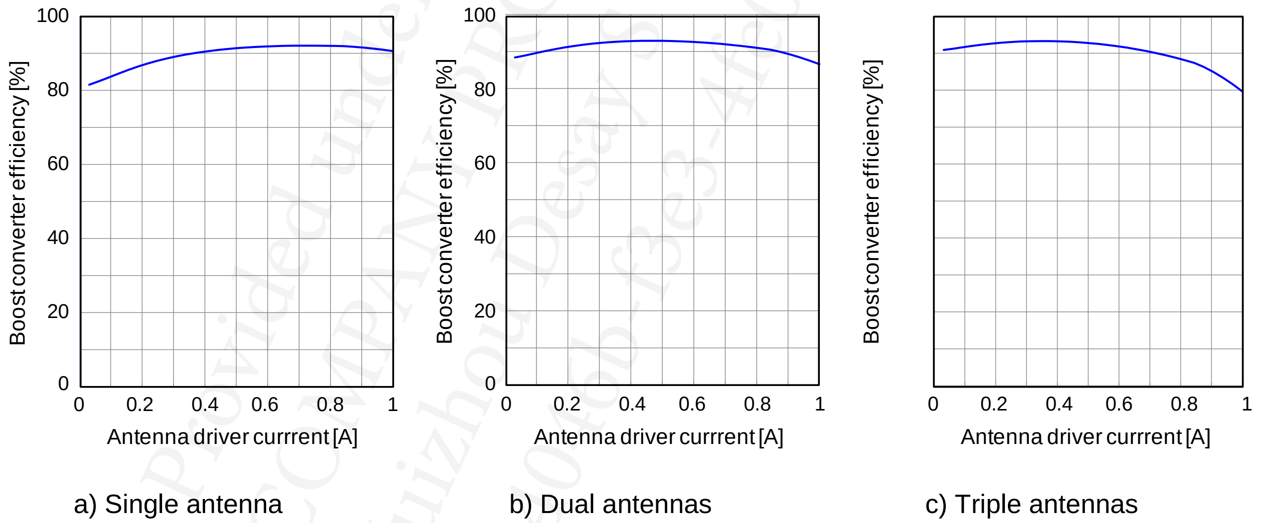

Fig 46. Typical boost converter power efficiency, PKE operation, V_{BAT} = 8 V, Z_{ANT} = 20 Ω

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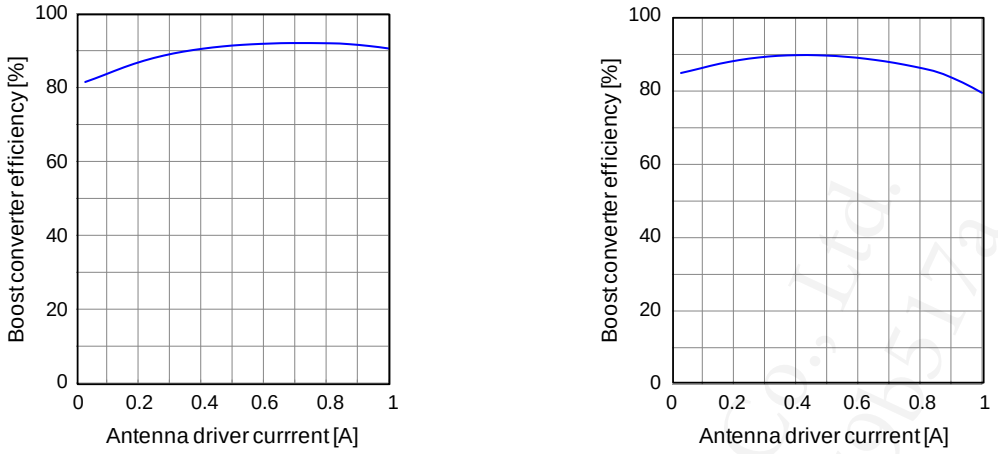

a) V_{BAT} = 8 V

b) V_{BAT} = 5 V

Fig 47. Typical boost converter power efficiency, immo operation, Z_{ANT} = 20 Ω

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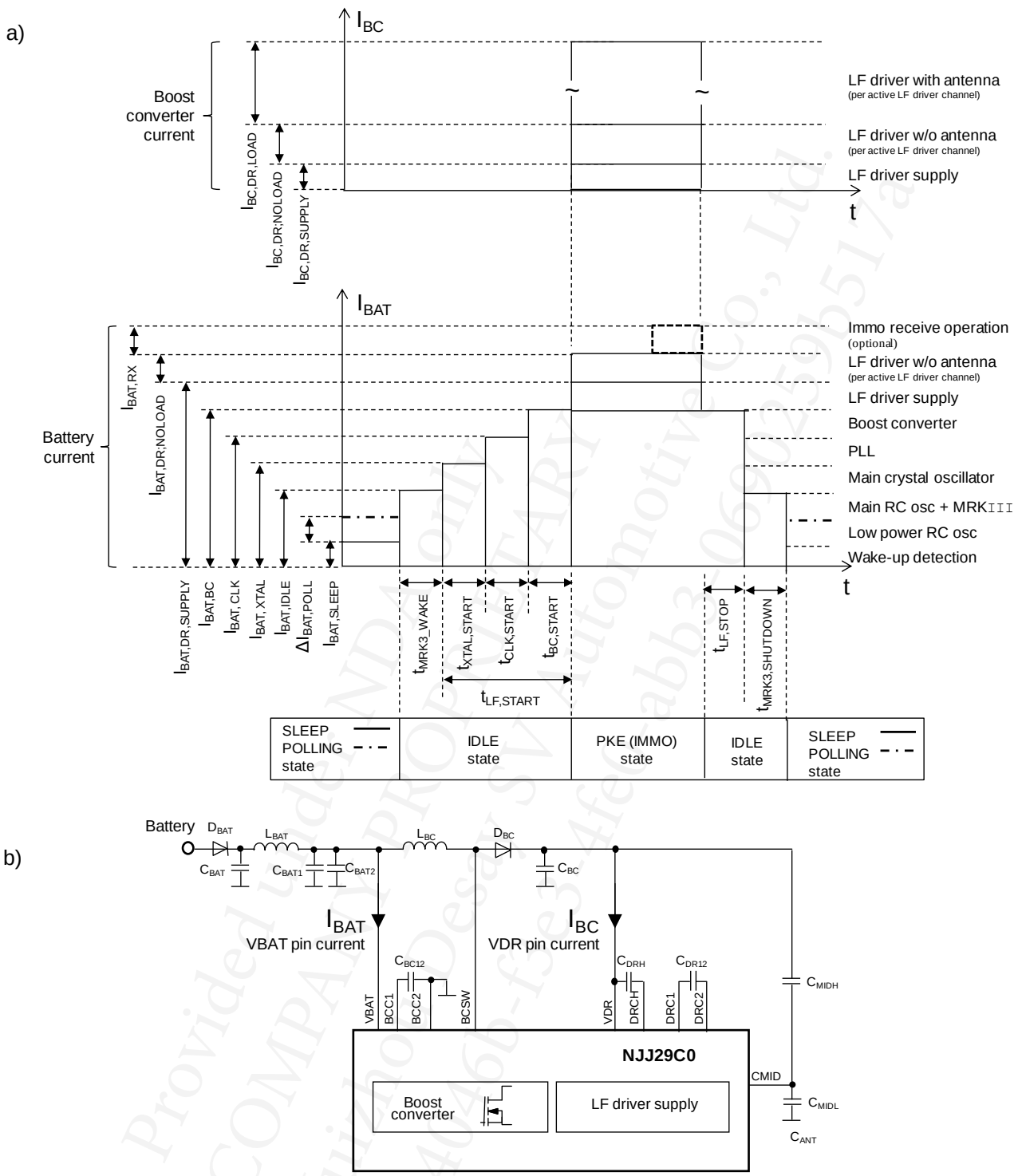

Fig 48. Currents and timings during LF antenna driver operation (a) and current assignment (b)

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Table 14. External components for boost converter

	Purpose	Required Characteristic
L_{BC}	Boost converter charging choke	$L \leq 5.1\mu H$ $L \geq 2.3\mu H$ @ $I_{peak} = 11.6A$ [1] $DCR \leq 15m\Omega$
D_{BC}	Boost converter freewheel diode	$V_f \leq 1V$ [2] $V_r \geq 50V$ $I_{f,peak} \geq 11.6A$ [3]
C_{BC}	Boost converter output capacitor	$C = 10\mu F$ [4][5] $C \geq 5.0\mu F$ @ 30V $V_{max} \geq 50V$ $ESR \leq 15m\Omega$
C_{BC12}	Boost converter driver supply decoupling	$C \geq 1.0\mu F$ @ 6V $C \leq 3.3\mu F$ @ any voltage below 6V $V_{max} \geq 16V$ $ESR \leq 150m\Omega$

[1] In case of a short on an LF driver the maximum peak current will be higher (up to 20 A). In this condition $L_{BC} \geq 1\mu H$.

[2] Higher V_f will reduce boost converter efficiency

[3] Average current is up to 3 A

[4] Represents a nominal capacitor value

[5] Sum value $C_{BC} + C_{TX4L} \leq 15\mu F$ @ 30V

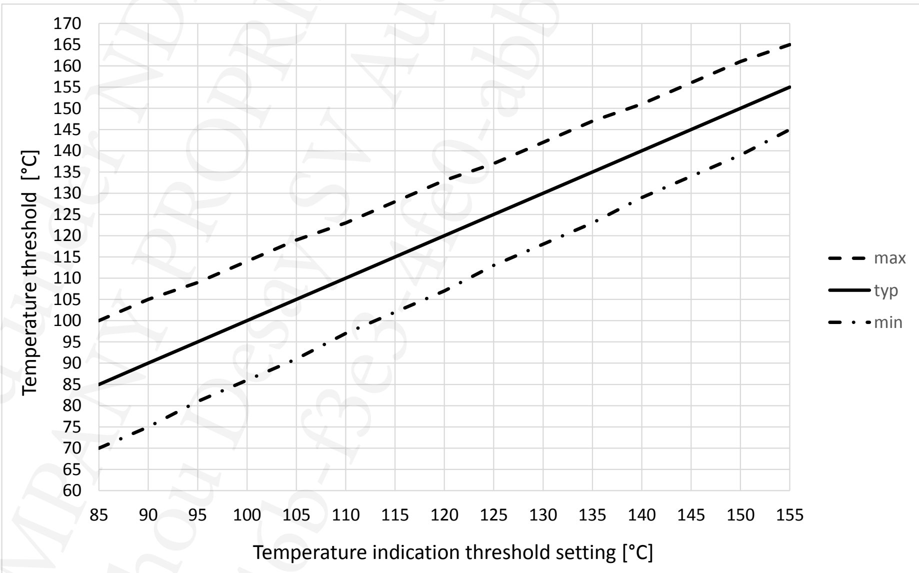

Fig 49. Temperature threshold dependent on temperature indication threshold setting

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10. Dynamic characteristics

Table 15. Dynamic characteristics

T_{amb} = -40 to +105 °C, GND = 0 V, V_{BAT} = 8 V to 18 V, V_{IO} = 2.9 V to 5.5 V, f_C = 125 kHz, T_0 = 1/f_C, C connected between pins VBAT and GND, Z_{ANT} = 10 to 20 Ω, Q ≤ 25, external components according to Table 14, full-bridge mode with midlevel control.
Unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Power management							
t_{POR}	Power on start-up time (time from POWER OFF state to IDLE state, cold start time)	V_{BAT} > $V_{BAT,POR,REL}$		0.8	2.1	4	ms
$t_{MRK3,WAKE}$	Wake-up time after wake-up event detection (time from SLEEP or POLLING state to IDLE state, including µController start, enabling SPI and setting INT pin if applicable, warm start time)	4 V < V_{BAT} < 28 V	[1]	0.3	0.6	1	ms
$t_{MRK3,SHUTDOWN}$	Shut-down time to disable µController and main RC oscillator (time from IDLE state to SLEEP or POLLING state)	4 V < V_{BAT} < 28 V	[1]	50		400	µs
On chip RC oscillator							
$f_{OSC,RC}$	Main RC oscillator clock frequency			14.4	16	17.6	MHz
XTAL oscillator							
$f_{XTAL,OSC}$	Main crystal oscillator frequency		[2]		16		MHz
$\Delta f_{XTAL,OSC}$	Oscillator frequency tolerance		[2] [3]	-1000		1000	ppm
$t_{XTAL,START}$	Oscillator start-up time	Equivalent serial resistance ESR = 120 Ω Voltage on XTAL2 reached 1Vpp	[1] [2] [4]	100		500	µs
PLL clock							
$t_{CLK,START}$	PLL clock start-up time		[1]	10	50	100	µs
Boost converter							
$t_{BC,START}$	Boost converter start-up time		[1]	50	210	650	µs
LF antenna driver							
$t_{LF,START}$	SPI message to LF field enable (time from IDLE state to PKE state,considers start-up of XTAL, boost converter, LF driver power supply and LF driver), see Fig 50	SPI message with min number of byte, $t_{SPI,CLK}$ = 2 µs (500 kbit/s), CUR_MAX = 0x0F (max)	[1]	0.5	1.6	1.7	ms
		SPI message with max number of byte, $t_{SPI,CLK}$ = 2 µs (500 kbit/s), CUR_MAX = 0x0F (max)	[1]	0.1	0.6	0.8	ms

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{IMMO,START}$	SPI message to LF field enable (time from IDLE state to IMMO state,considers start-up of XTAL, boost converter, LF driver power supply, LDO, receiver and LF driver) see Fig 51	CUR_MAX = 0x0F (max)	2.0	2.6	3.0	ms
$t_{LF,STOP}$	LF field disable time (time from PKE state to IDLE state,considers ramp-down of XTAL, boost converter, LF driver power supply and LF driver)			530		µs
$t_{CH,CHG}$	LF channel change (time between LF driver off and LF driver on), see Fig 52	SPI command triggered operation 1 to 1 channel	464	496	552	µs
		SPI command triggered operation 1 to 2 channels	712	776	800	µs
		SPI command triggered operation 1 to 3 channels	752	1024	1088	µs
		Wake-up event triggered polling or timer triggered polling PTIMEi = 0 (0 ms) 1 to 1 channel	472	536	720	µs
		Wake-up event triggered polling or timer triggered polling PTIMEi = 0 (0 ms) 1 to 2 channels	720	812	992	µs
		Wake-up event triggered polling or timer triggered polling PTIMEi = 0 (0 ms) 1 to 3 channels	768	952	1232	µs
Telegram sequencer						
BR_{2k}	Output bit rate 2 kbit/s		1.91	1.95	1.99	kbit/s
BR_{4k}	Output bit rate 4 kbit/s		3.82	3.90	3.98	kbit/s
BR_{8k}	Output bit rate 8 kbit/s	Single channel [5] Q < 16	7.64	7.80	7.96	kbit/s
BPLM timing						
t_{LOG_0}	Pulse time for ‘logic 0’	$T_0 = 1/f_c$ n = 19 .. 34	n * T_0 – 1.5	n * T_0	n * T_0 + 1.5	µs
t_{LOG_1}	Pulse time for ‘logic 1’	$T_0 = 1/f_c$ n = 28 .. 43	n * T_0 – 1.5	n * T_0	n * T_0 + 1.5	µs
t_{STP}	Pulse time for stop pulse	$T_0 = 1/f_c$ n = 36 .. 47	n * T_0 + 40	n * T_0 + 50	n * T_0 + 75	µs
t_{WRP}	Write pulse low duration	$T_0 = 1/f_c$ n = 4 ..15	n * T_0	n * T_0 + 3	n * T_0 +8	µs

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WTP}	Receiver wait time for transponder response		202 * T_0 + t_{SYNC}		32 * 202 * T_0 + t_{SYNC}	µs
t_{SYNC}	Receiver wait time for transponder response synchronization offset		-16 * T_0		15 * T_0	µs
Receiver						
$t_{RX,START}$	Start-up time	5 V < V_{BAT} < 28 V	100	250	500	µs
$t_{HP,SETTLE}$	High pass filter settling time	5 V < V_{BAT} < 28 V			1.6	ms
BR_{RX}	Input bit rate 4 kbit/s			3.9		kbit/s
Protection						
$t_{PROT,SHUTDOWN}$	Protection event shut-down time (hardware controlled operating state transfer)		0.1	1.0	10	µs
SPI interface						
$t_{SPI,CLK}$	SPI clock period	4 V < V_{BAT} < 28 V, C_{SDO} = 50 pF	500			ns
$t_{SCSN,SET}$	Chip select setup time		84			ns
$t_{SCSN,HOLD}$	Chip select hold time		250			ns
$t_{SCLK,LOW}$	Data clock low time		250			ns
$t_{SCLK,HIGH}$	Data clock high time		250			ns
$t_{SDI,SET}$	Data in setup time		167			ns
$t_{SDI,HOLD}$	Data in hold time		167			ns
$t_{SDO,DLY}$	Data out delay	C_{SDO} = 50 pF			240	ns
$t_{RESP,DLY,CMD}$	SPI command response delay time	Depends on SPI command [6]				
$t_{SCSN,FILT}$	Chip select low filter time	Hardware edge detection	0.05		1	µs
IO interface (host controller interface)						
$t_{VIO,UVD}$	Undervoltage detection filter time		5		20	µs
RSTN pin						
$t_{RSTN,FILT}$	Reset low filter time	[7]	0.05		100	µs
Wake-up input						
$t_{WUP,WAKE}$	Wake-up input filter time	5 V < V_{BAT} < 28 V	5		40	µs
Polling timer						
$f_{OSC,RC,POL}$	Polling timer RC oscillator clock frequency		162	180	198	kHz
$t_{POL,INT}$	Typical time interval	$f_{OSC,RC,POL}$ = 180.0 kHz [8]	1		65535	ms
$t_{POL,STEP}$	Typical step size	$f_{OSC,RC,POL}$ = 180.0 kHz		1		ms

[1] See Fig 48

[2] For characterization, the 16 MHz quartz crystal unit NDK NX3225GB-16.000M was used

[3] Crystal resonator required, sensitivity degradation with ceramic resonator

[4] Application has to ensure that XTAL oscillator starts-up with chosen crystal within specified time

[5] Using the high bit rate may impact the system performance

[6] See NJJ29C0B SPI command set specification

[7] Application has to drive the RSTN signal for longer than the maximum reset low filter time

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[8] The time interval is derived from a continuously running timer providing a 1 ms tick. As the timer is not synchronized, setting the minimum value of 2 ms results in an effective pause between 1 ms and 2 ms.

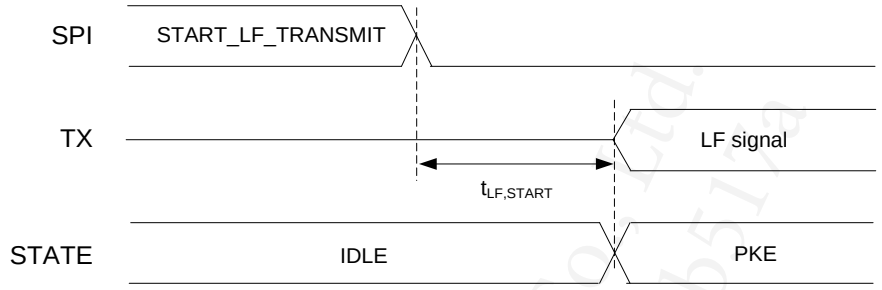

Fig 50. SPI message to LF field enable time $t_{LF,START}$

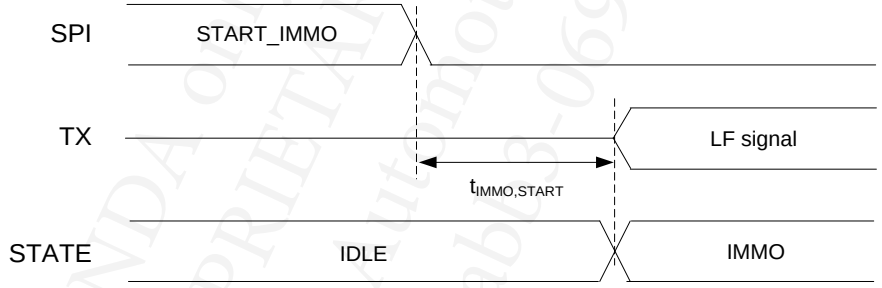

Fig 51. SPI message to LF field enable time $t_{IMMO,START}$

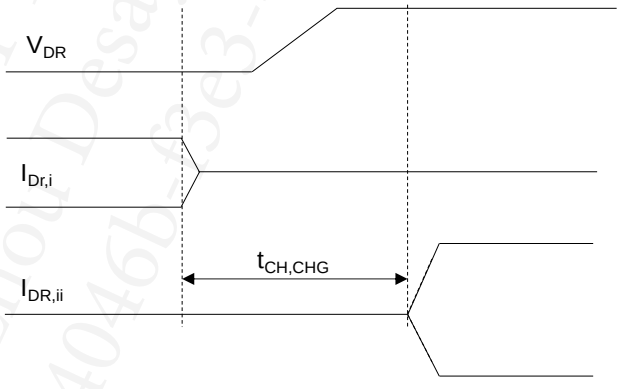

Fig 52. LF channel change time $t_{CH,CHG}$

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11. Application information

11.1 Application diagram

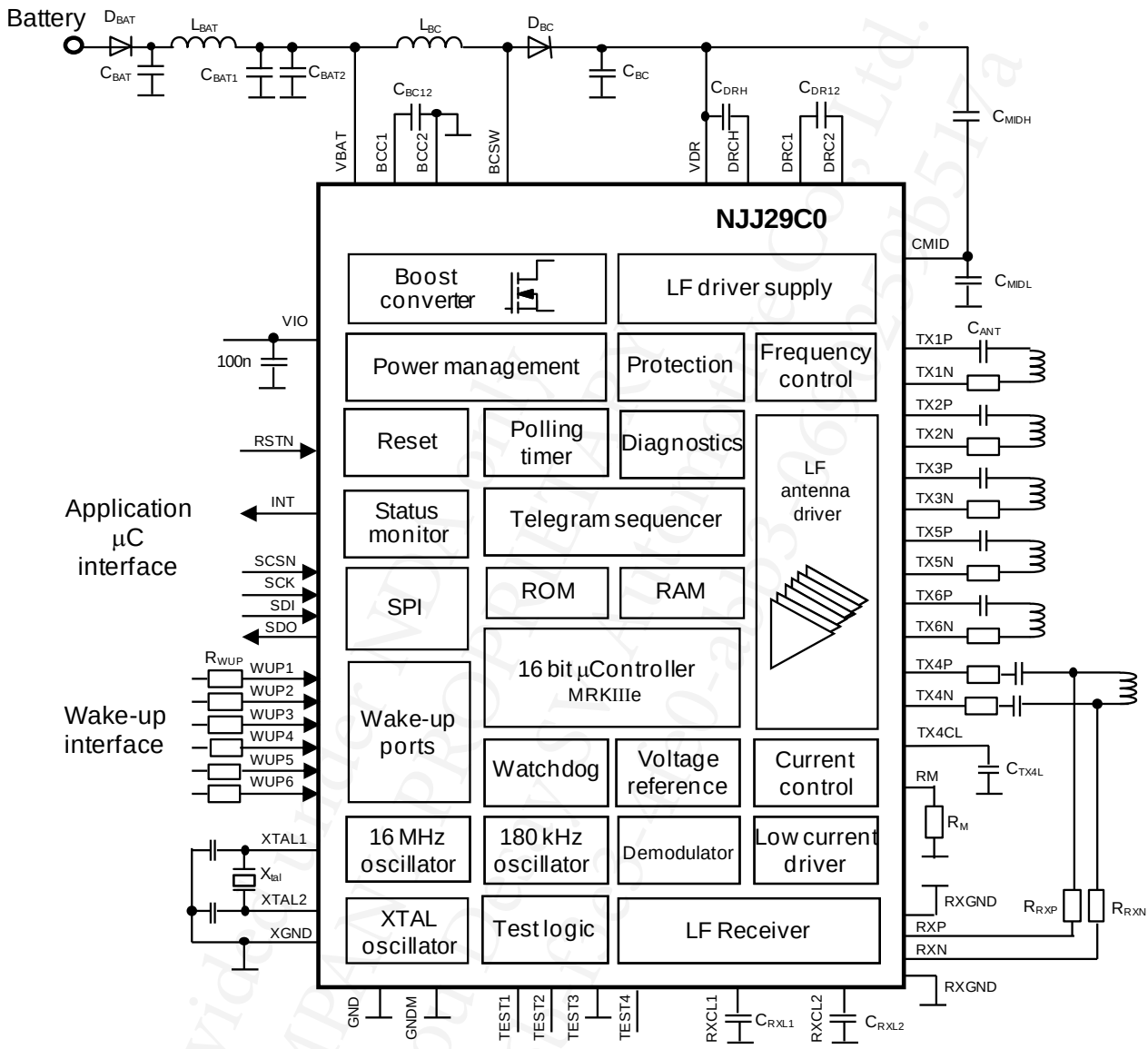

Fig 53. Typical application schematic

11.2 Typical external components

The typical external components are selected for an application based on the following conditions:

- Peak antenna driver current 3x1A in 20Ω @ 8V ≤ V_{BAT} ≤ 18V
- $I_{BAT,AVG}$ = 9.6 A during LF driver on time
- Temperature range is $T_{ambient}$ -40°C to 105°C

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Table 16. External components

	Purpose	Required Characteristic
L_{BAT}	Supply line input filter choke	L ≥ 2.3µH [1] DCR<15mΩ
C_{BAT}	Supply line input filter capacitor, input side	C ≥ 5.0µF @ 30V V_{max} ≥ 50V ESR ≤ 15mΩ
C_{BAT1}	Supply line input filter capacitor, output side	C = 220µF @ 16V [2] V_{max} ≥ 50V ESR ≤ 100mΩ
C_{BAT2}	Supply line input filter capacitor, output side	C ≥ 5.0µF @ 30V V_{max} ≥ 50V ESR ≤ 15mΩ
D_{BAT}	Supply line input diode	V_r ≥ 50V $I_{f,peak}$ ≥ 11.6A [3]
L_{BC}	See Table 14	
D_{BC}	See Table 14	
C_{BC}	See Table 14	
C_{BC12}	See Table 14	
C_{MIDH}	Vmid filter capacitor	C ≥ 100nF @ 25V C ≤ 330nF @ any voltage below 25V V_{max} ≥ 50V ESR ≤ 150mΩ
C_{MIDL}	Vmid filter capacitor	C ≥ 100nF @ 25V C ≤ 330nF @ any voltage below 25V V_{max} ≥ 50V ESR ≤ 150mΩ
C_{DRH}	ClassD* high side	C ≥ 500nF @ 6V[4] C ≤ 3µF @ any voltage below 6V V_{max} ≥ 16V ESR ≤ 150mΩ
C_{DR12}	ClassD* charge pump capacitor	C ≥ 50nF @ 25V[4] C ≤ 330nF @ any voltage below 25V V_{max} ≥ 50V ESR ≤ 150mΩ
C_{TX4L}	IMMO driver supply decoupling	C = 4.7µF[2] [5] V_{max} > 50V ESR ≤ 150mΩ
RM	Antenna driver current sense resistor	R = 1kΩ High accuracy, at least +/- 1% 0.1W
R_{RXP}	Positive RX input series resistor	R = 510kΩ V_{max} ≥ 250V
R_{RXN}	Negative RX input series resistor	R = 510kΩ V_{max} ≥ 250V
C_{RXL2}	RX supply voltage decoupling	C ≥ 1.5µF @ 6V C ≤ 4.7µF @ any voltage below 6V V_{max} ≥ 16V ESR ≤ 150mΩ

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	Purpose	Required Characteristic
C_{RXL1}	RX frontend reference voltage decoupling	C ≥ 230nF @ 3V C ≤ 430nF @ any voltage below 3V V_{max} ≥ 16V ESR ≤ 150mΩ
R_{WUP}	WUP input current limiting resistance	R = 3.3k Ω Accuracy +/- 10% 0.25W
X_{tal}	Xtal	16 MHz
C_{ANT}	Antenna couple capacitors	Depends on antenna inductance, should set antenna resonance frequency to 125 kHz

[1] In case of a short on an LF driver the maximum average current will be higher (up to 18 A)

[2] Represents a nominal capacitor value

[3] In case of a short on an LF driver the maximum peak current will be higher (up to 20 A)

[4] The C_{DRH} / C_{DR12} capacitance ratio shall be kept at 10

[5] Sum value C_{BC} + C_{TX4L} ≤ 15µF @ 30V

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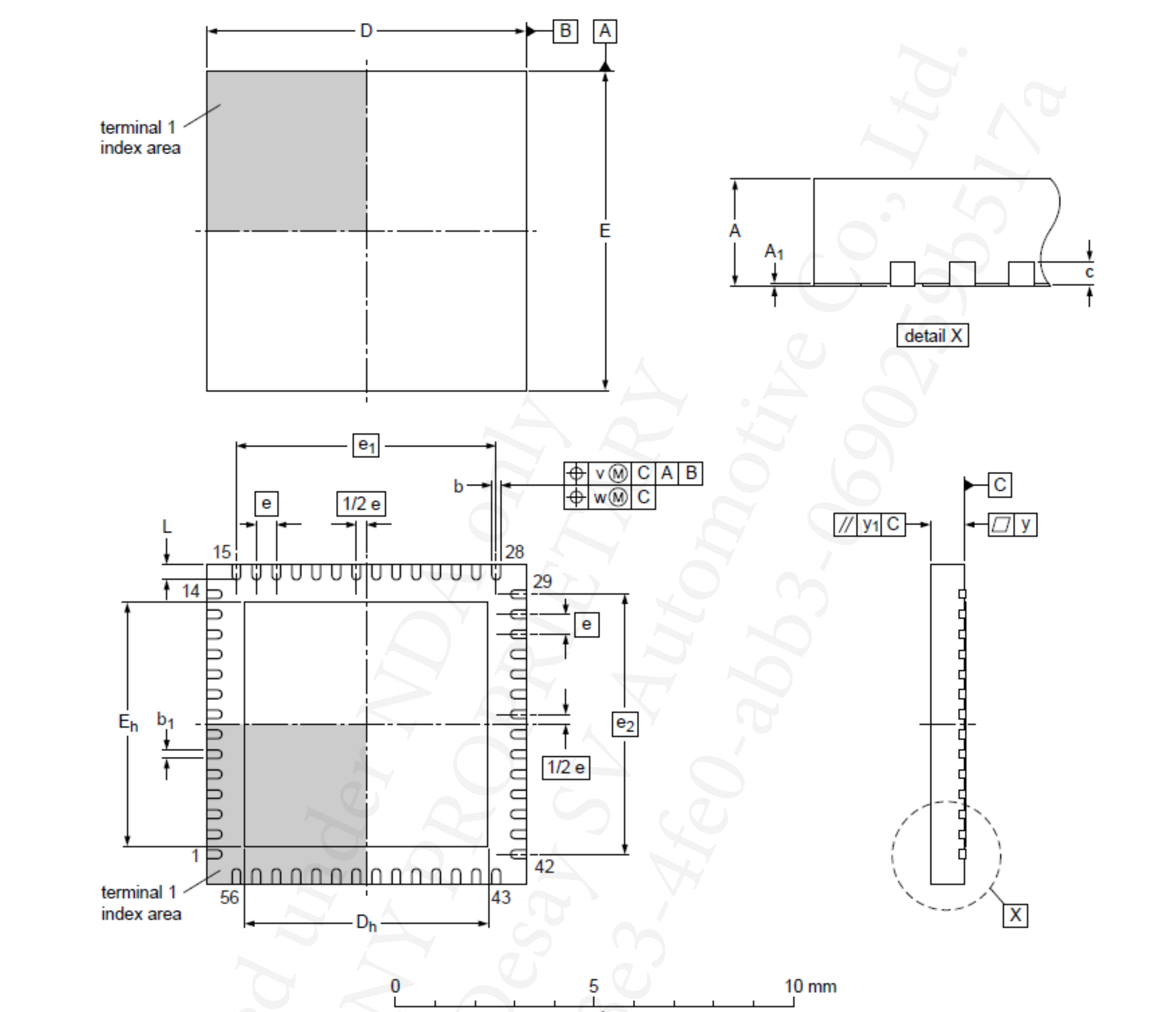
12. Package outline

HVQFN56: plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 x 8 x 0.85 mm **SOT684-14**



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	b_1(2)	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	1.00	0.05	0.30	0.30		8.1	6.25	8.1	6.25				0.5				
	nom	0.85	0.02	0.21	0.26	0.2	8.0	6.10	8.0	6.10	0.5	6.5	6.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18	0.18		7.9	5.95	7.9	5.95				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.
2. Dimension is applicable for lead 6, 7 and 8.

sot684-14_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT684-14		- - -				~~15-11-09~~ 15-11-30

Fig 54. Package outline SOT684 (HVQFN56)

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13. Glossary

13.1 Special word usage

may	In this document this word means that the item is truly optional.
shall	In this document this word denotes that the definition is a mandatory requirement of the specification.
should	In this document this word means that the definition is a desired, but not mandatory requirement of the specification.
application	In this document this word means the application hardware plus the application software.
application software	In this document this means the host controller software including commands and data transferred via SPI to NJJ29C0B.
embedded system software	In this document this means the NXP implemented software for controlling the NJJ29C0B including the SPI command handler.
µController	In this document this word means the NJJ29C0B integrated 16-bit µController MRK III-e

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14. References

[1] **NJJ29C0B - SPI Command Set —** Specification of SPI commands for device control

[2] **AN-SCA 1602 B** — JOKER Application Note

15. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NJJ29C0B_2	20171020	Product data sheet	-	NJJ29C0B_1
Modifications	• Data sheet status changed from Preliminary data sheet to Product data sheet • Revision history reset			
NJJ29C0B_1	20170818	Preliminary data sheet	-	
Modifications	• Initial version			

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16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification or product development
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification
Product [short] data sheet	Production	This document contains the product specification

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices.

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